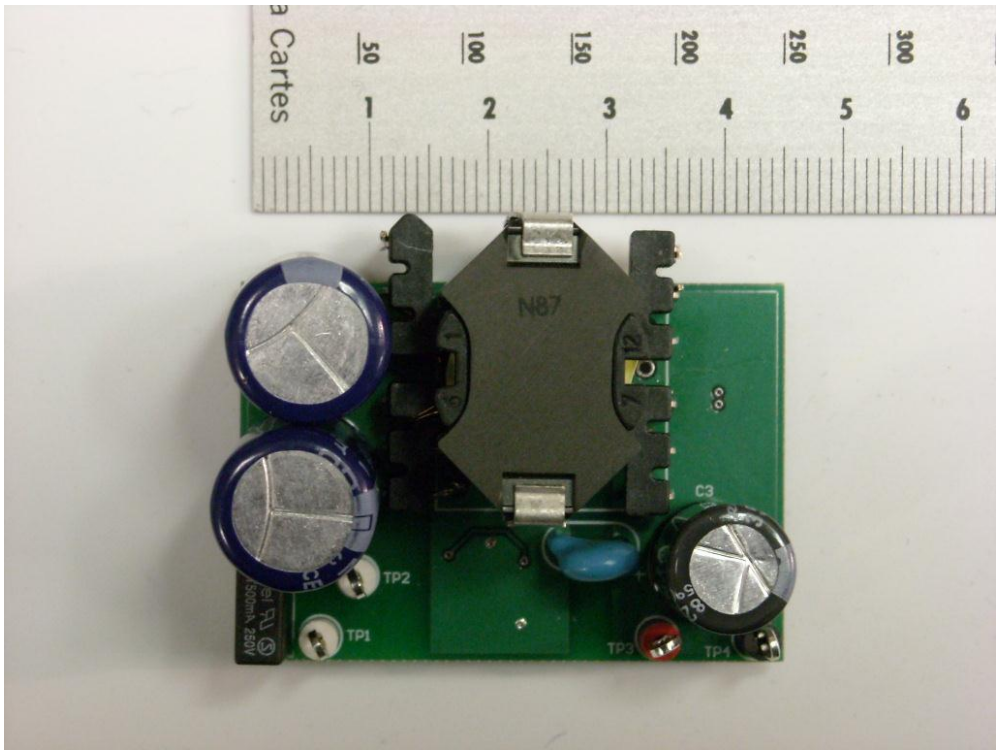
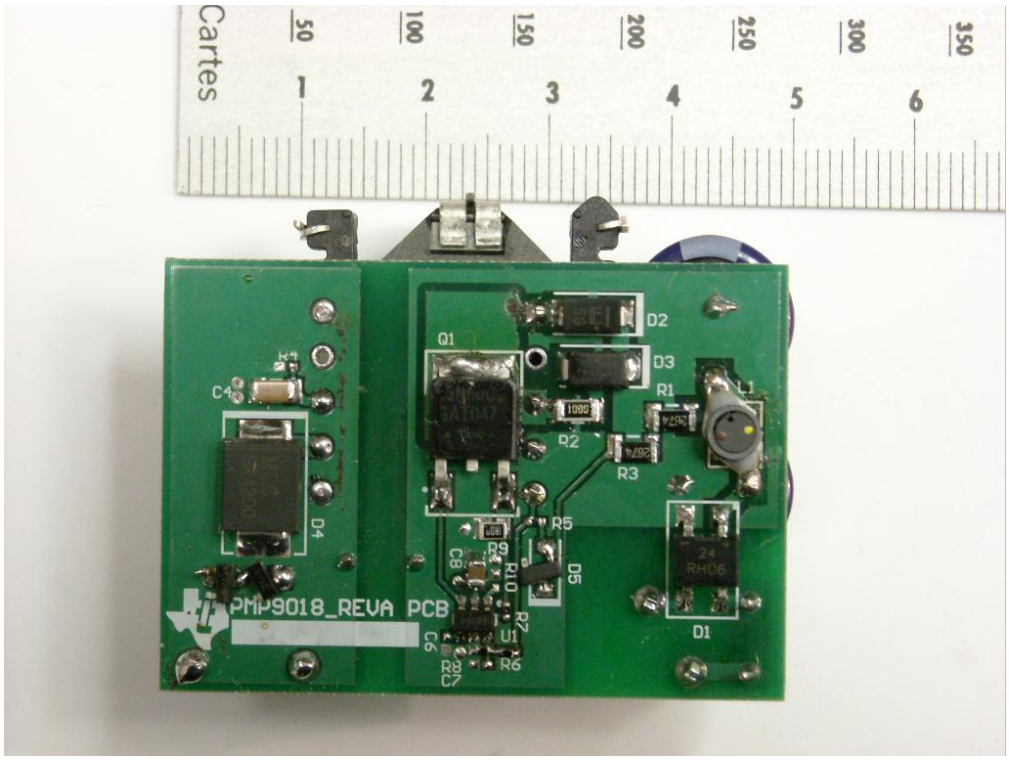
Photos of the prototype:

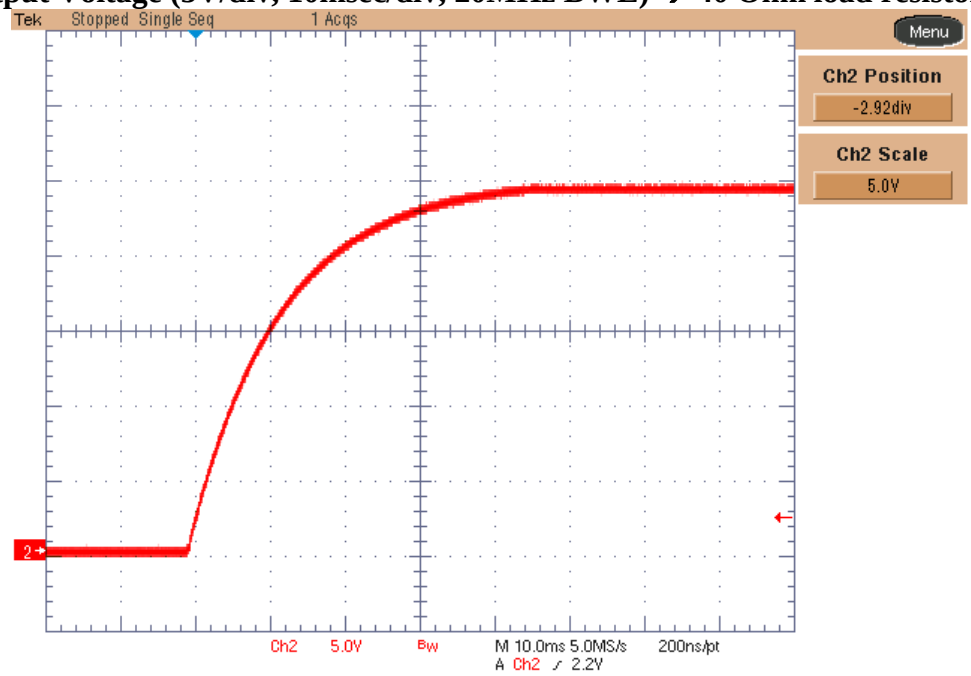




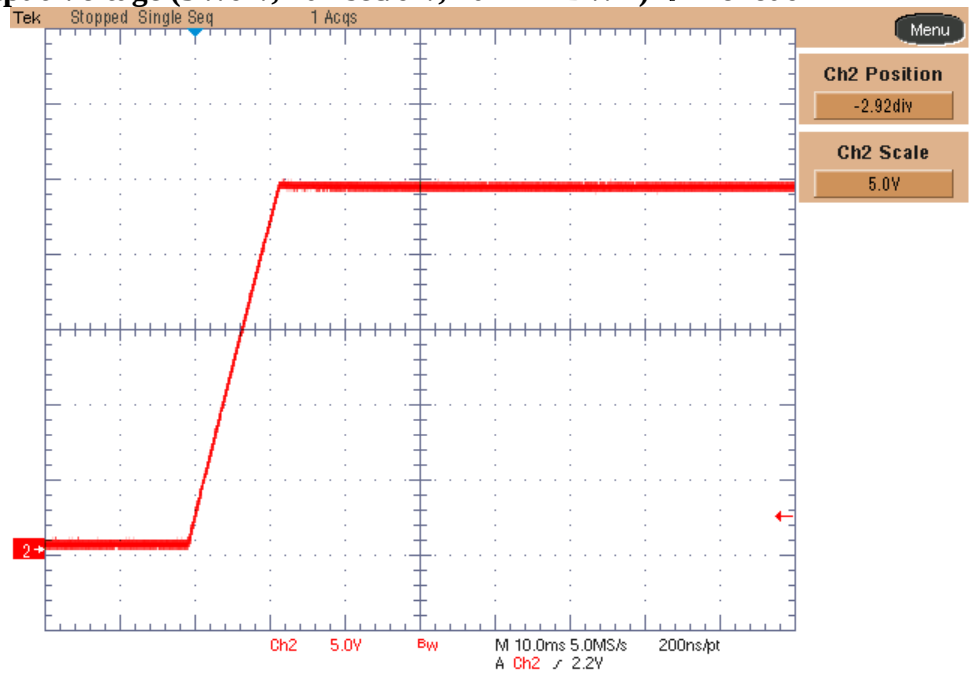
1 Output Voltage at Startup

The output voltage ramp-up behavior at startup is shown in the image below. The input voltage has been set to 320Vdc. The load was a 40 Ohm resistor (top picture) and not connected in the bottom one.

Ch.2: Output Voltage (5V/div, 10msec/div, 20MHz BWL) → 40 Ohm load resistor

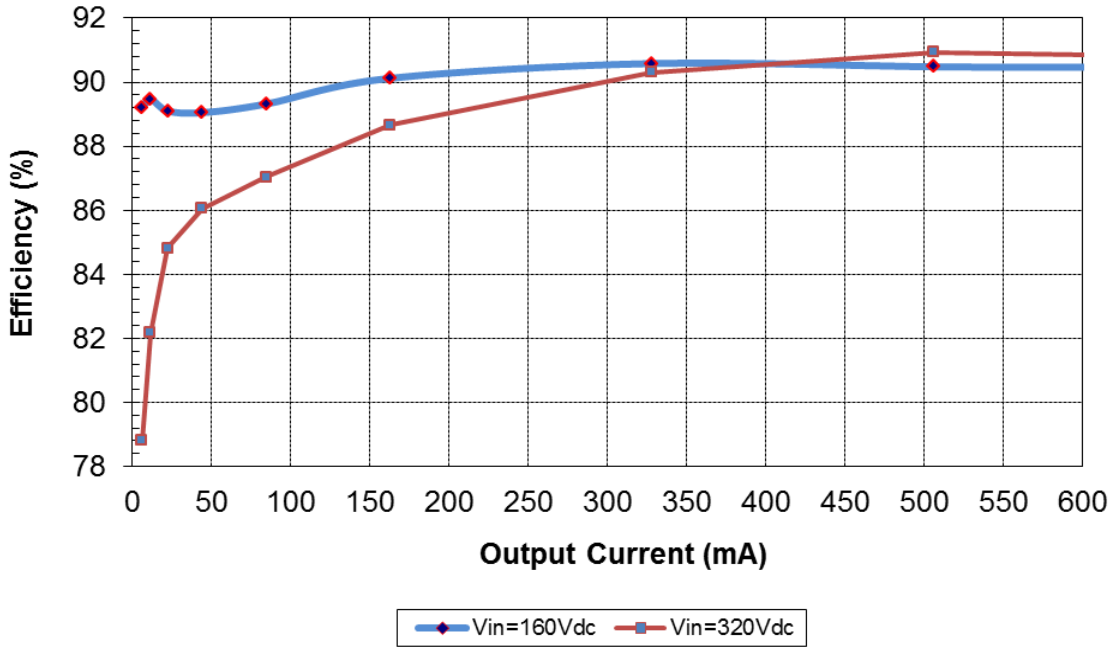


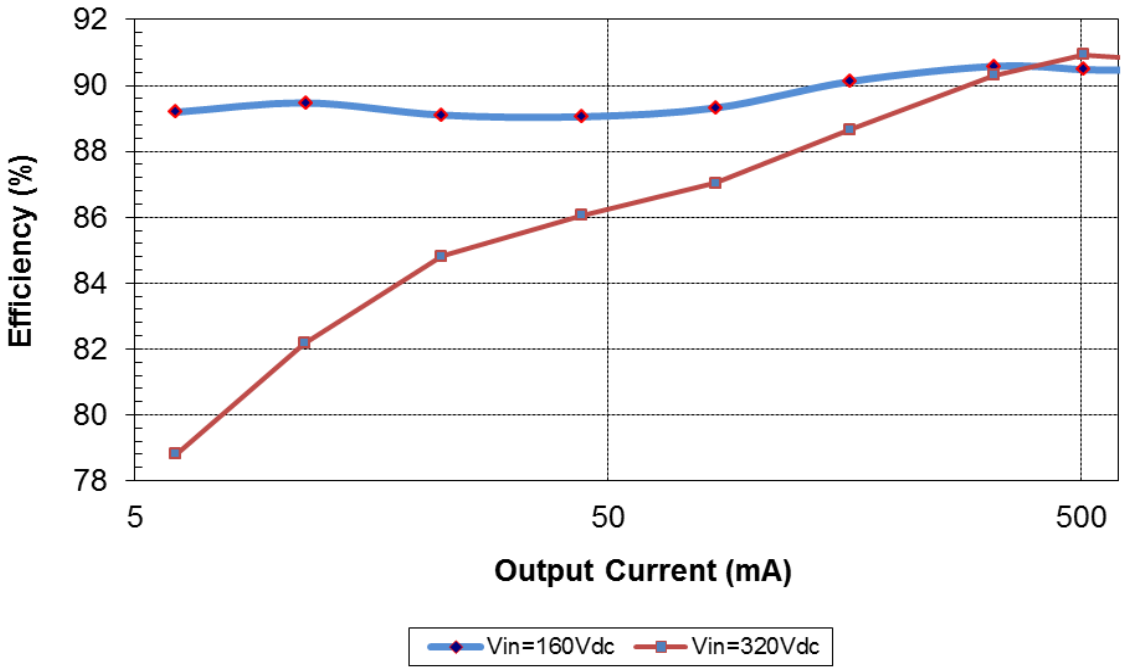
Ch.2: Output Voltage (5V/div, 10msec/div, 20MHz BWL) → No load



2 Efficiency

The efficiency data are shown in the tables and graphs below. The load has been varied between 0 and 600mA. The input voltage has been set to 160Vdc and 320Vdc. The second graph is the same like the first one but with logarithmic x-scale.



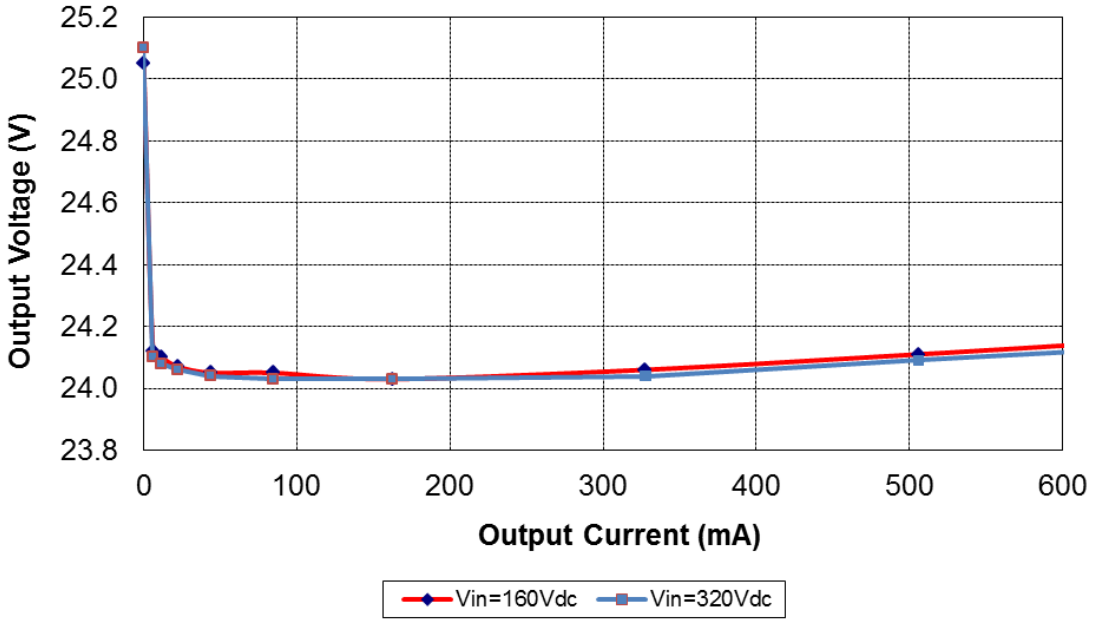


Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff (%)
0.0	25.05	0.000	0.316	160	0.051	0.051	0.0
6.1	24.12	0.147	1.031	160	0.165	0.018	89.2
11.5	24.10	0.277	1.936	160	0.310	0.033	89.5
22.3	24.07	0.537	3.765	160	0.602	0.066	89.1
43.9	24.05	1.06	7.410	160	1.186	0.130	89.1
84.5	24.05	2.03	14.22	160	2.275	0.243	89.3
162.8	24.03	3.91	27.13	160	4.341	0.429	90.1
327.7	24.06	7.88	54.4	160	8.704	0.820	90.6
506.2	24.11	12.20	84.3	160	13.488	1.284	90.5
606.2	24.14	14.63	101.1	160	16.176	1.542	90.5

Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff (%)
0.0	25.10	0.000	0.237	320	0.076	0.076	0.0
6.1	24.10	0.147	0.583	320	0.187	0.040	78.8
11.4	24.08	0.275	1.044	320	0.334	0.060	82.2
22.3	24.06	0.537	1.977	320	0.633	0.096	84.8
44.0	24.04	1.06	3.841	320	1.229	0.171	86.1
84.5	24.03	2.03	7.29	320	2.333	0.302	87.0
162.8	24.03	3.91	13.79	320	4.413	0.501	88.7
327.7	24.04	7.88	27.26	320	8.723	0.845	90.3
506.1	24.09	12.19	41.9	320	13.408	1.216	90.9
606.3	24.12	14.62	50.3	320	16.096	1.472	90.9

3 Output Voltage Regulation vs. Load

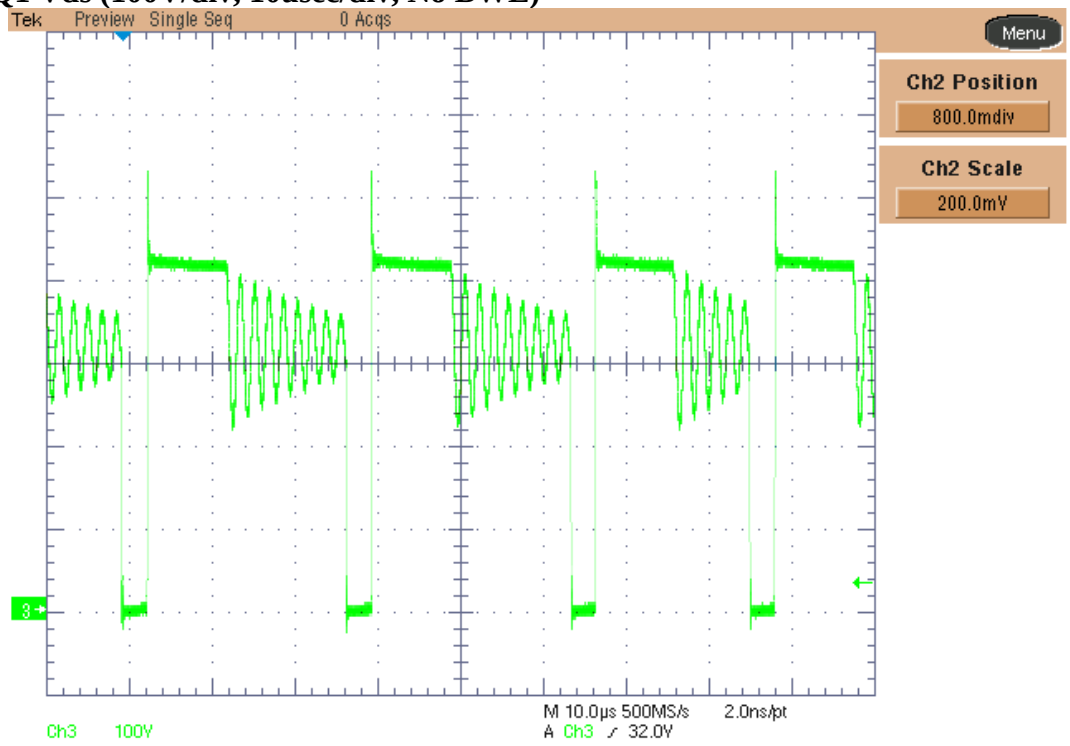
The output voltage variation as function of output current is shown below.



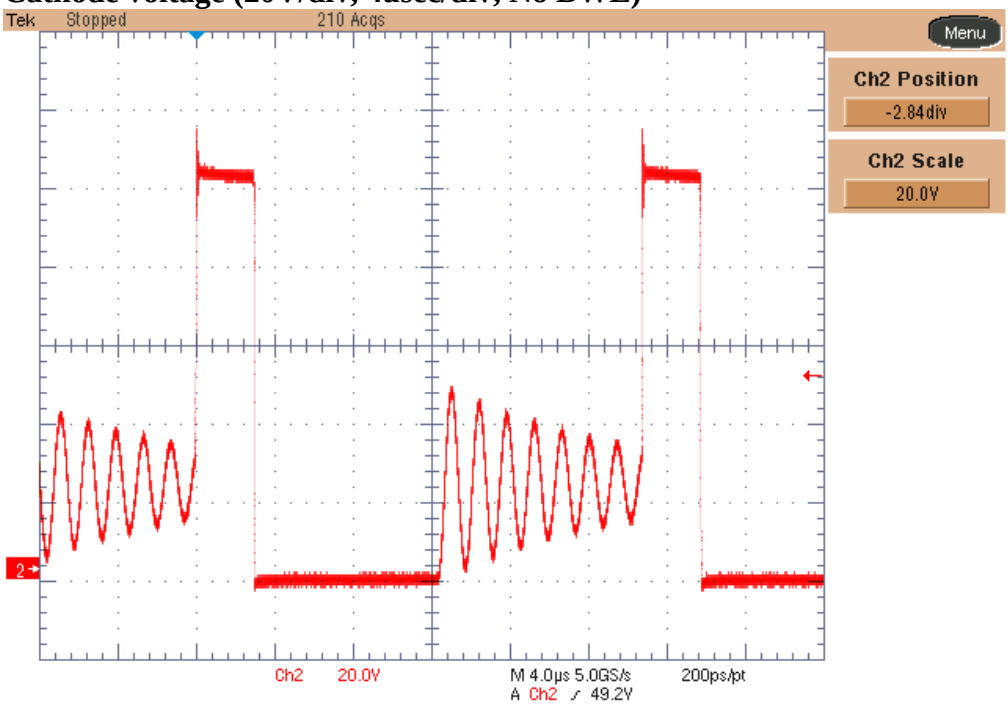
4 Switching Node Waveforms

The image below shows the voltage on drain of Q1 and cathode of D4 at 320Vdc input voltage and full load conditions.

Ch3: Q1 Vds (100V/div, 10usec/div, No BWL)



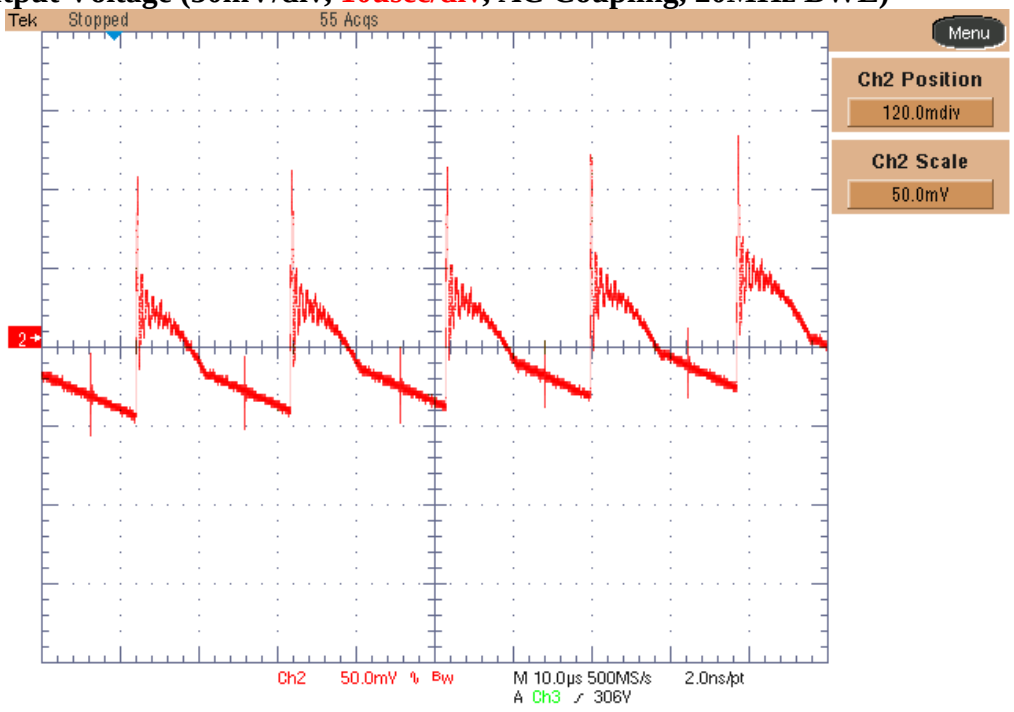
Ch2: D4 Cathode voltage (20V/div, 4usec/div, No BWL)



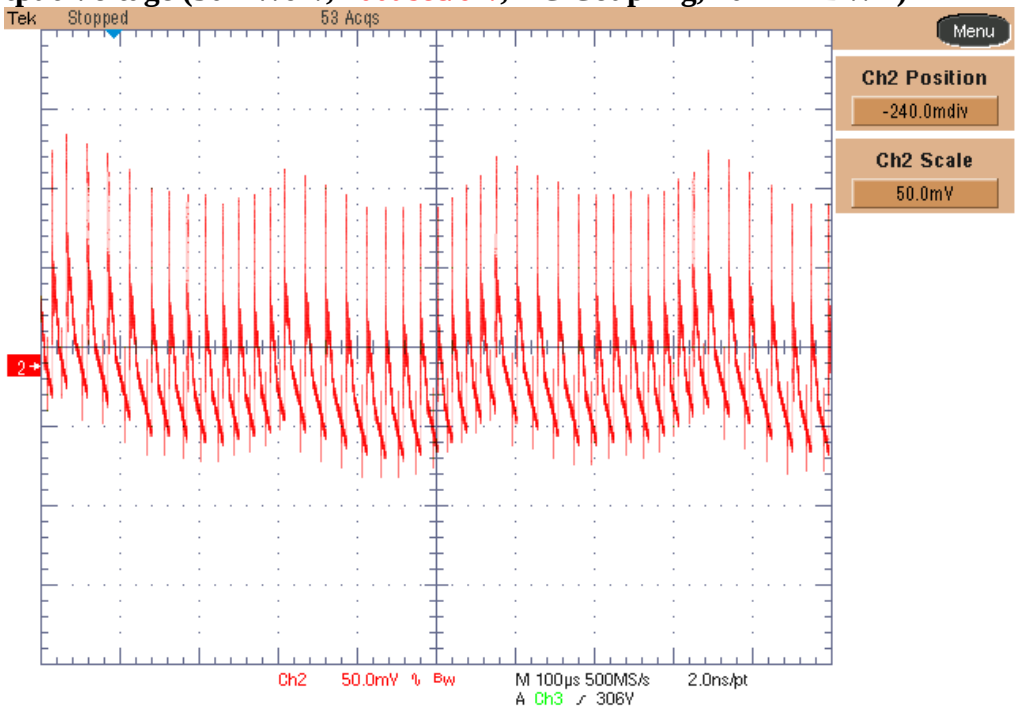
5 Output Ripple Voltage

The output ripple voltage is shown in the pictures below. The difference between the upper and the bottom one is the time scale, enlarged in order to show the effect of frequency dithering.

Ch2: Output Voltage (50mV/div, 10usec/div, AC Coupling, 20MHz BWL)



Ch2: Output Voltage (50mV/div, 100usec/div, AC Coupling, 20MHz BWL)



6 Thermal Analysis

The thermal analysis of the converter shows the temperatures for each component, in the pictures below. The converter has been placed horizontally on the bench without any forced convection. The input voltage was 320V and the output fully loaded. The ambient temperature was 23C.

Thermal picture of the bottom side of the board:

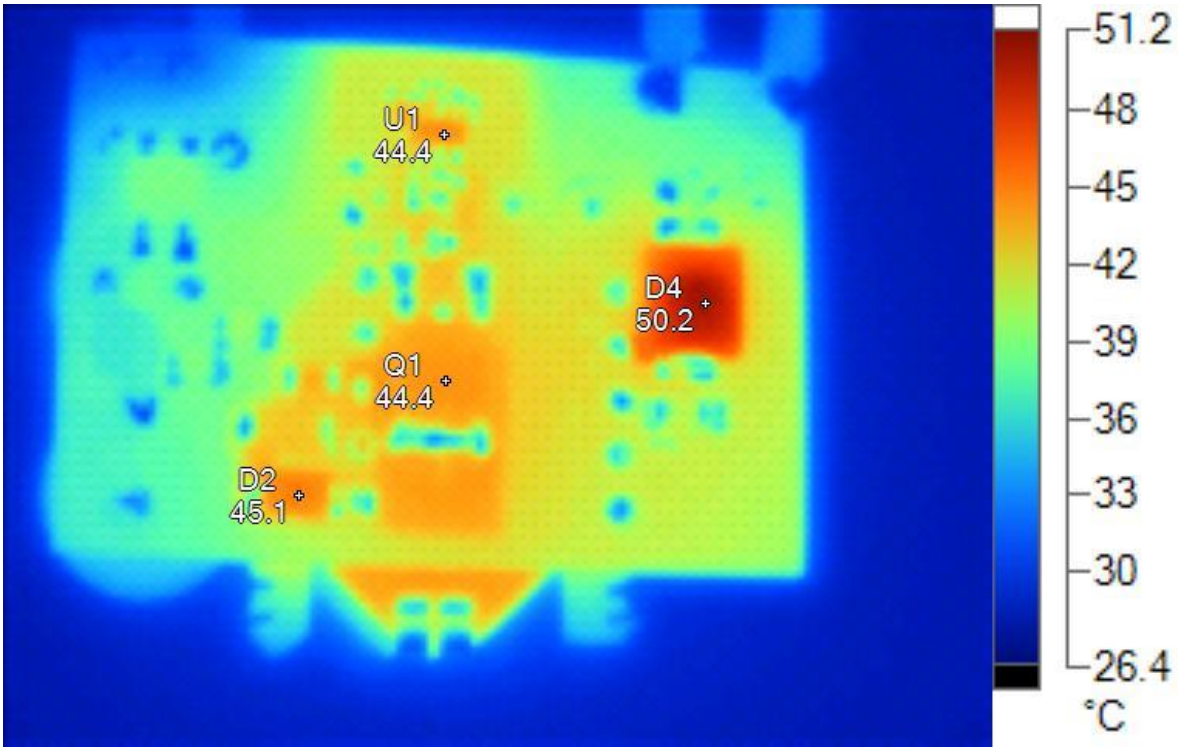


Image Info

Background temperature	23.0°C
Average Temperature	34.9°C
Image Range	27.4°C to 50.2°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	10/16/2013 5:37:57 PM

Main Image Markers

Name	Temperature
D4	50.2°C
D2	45.1°C
Q1	44.4°C
U1	44.4°C

Thermal picture of the top side of the board:

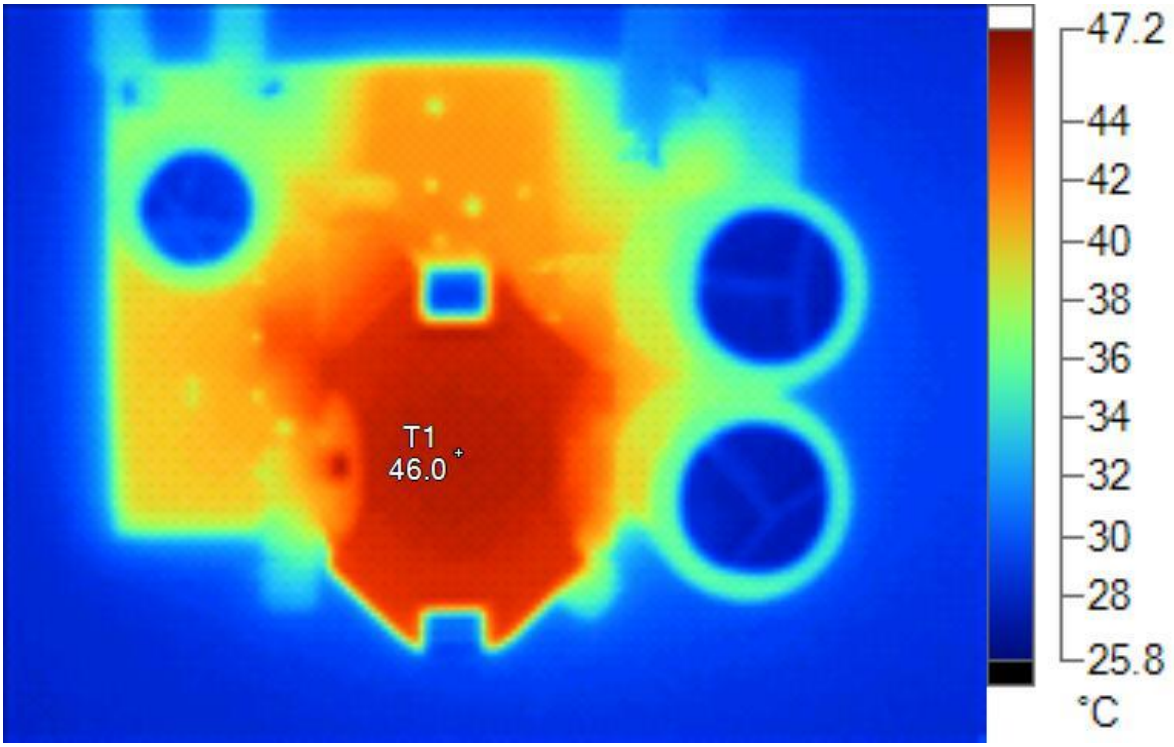


Image Info

Background temperature	23.0°C
Average Temperature	34.0°C
Image Range	26.8°C to 46.3°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	10/16/2013 5:44:28 PM

Main Image Markers

Name	Temperature
T1	46.0°C

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