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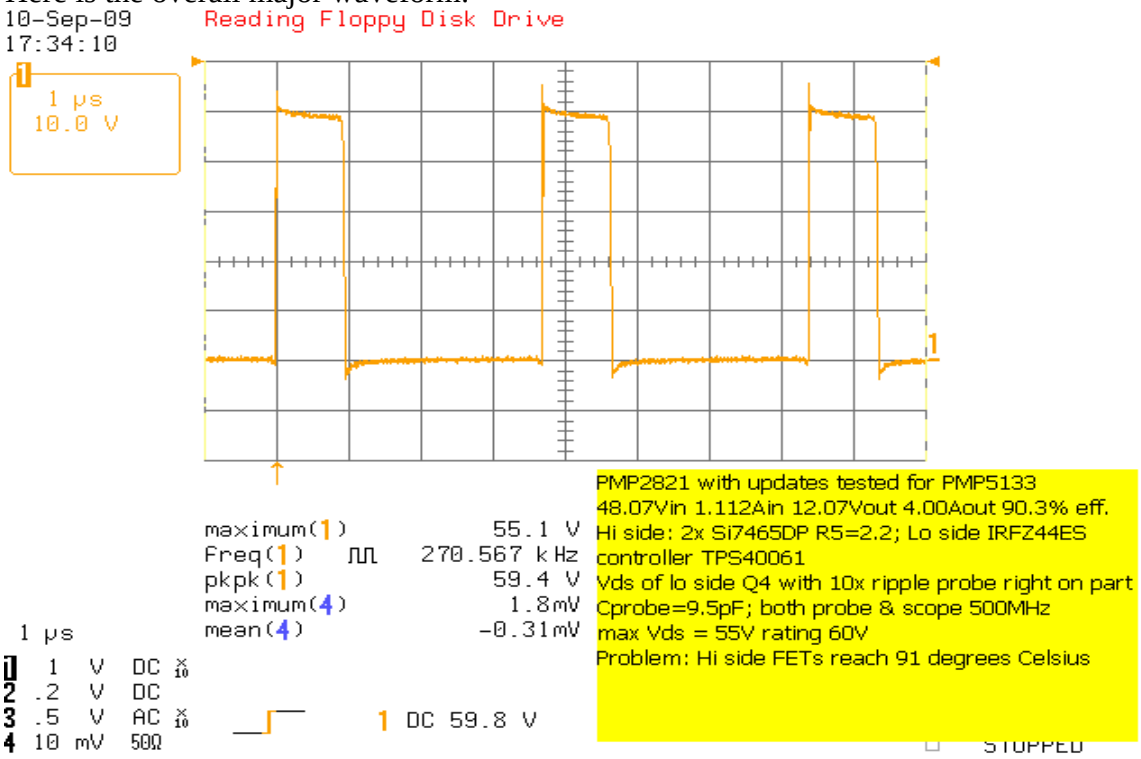
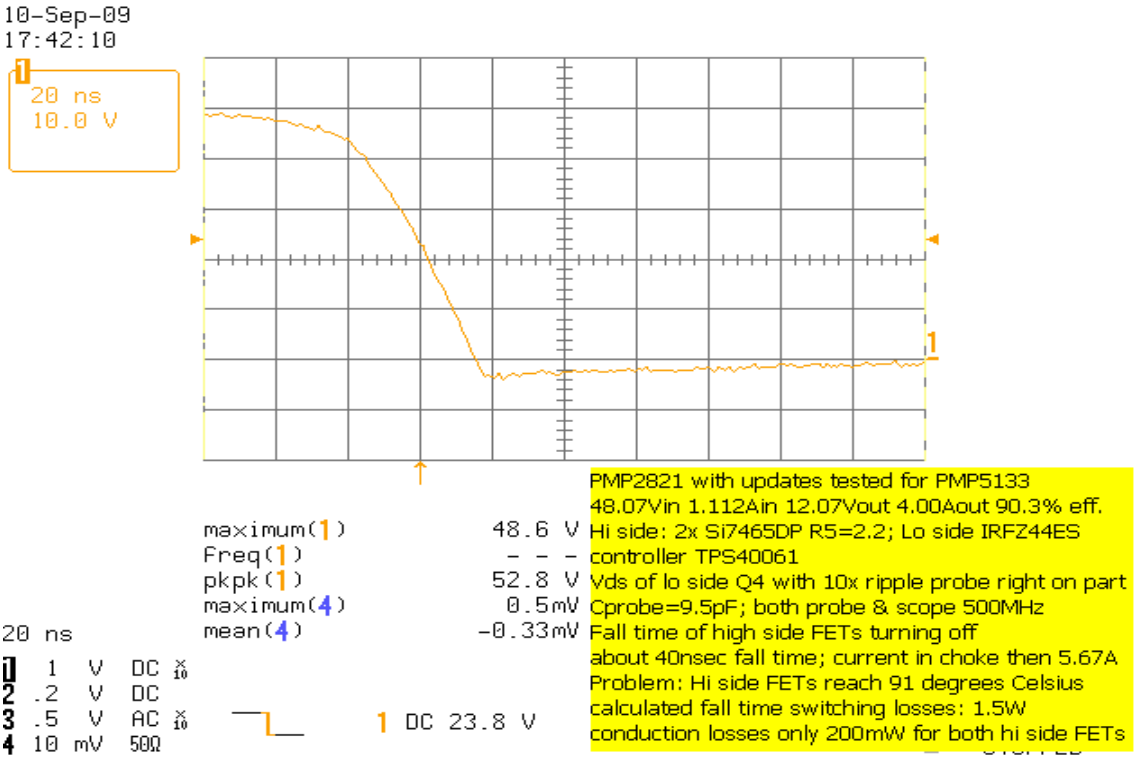
Initial testing with PMP2821 with all its updates, but Vin set to 48V and output 12V at 4.0A:
Vin = 48.07V Iin = 1.112A Vout = 12.07V Iout = 4.00A eff. = 90.3%; Losses = 5.17W
One hi side FET getting to 91 degrees Celsius from room ambient:
Major cause of loss and heating: slow turn off: For hi side using two P-FETs Si7465DP which have slow turn off. See waveforms next page.
Turn on much faster at under 10nsec, and not too fast to overvoltage low side FET rated at 60Vds.
Need faster high side FETs: Candidate FDMC5614P from Fairchild in power pad 3x3
Published on resistance is about 50% higher increasing conduction losses from 200mW for both to 300mW.
But published turn off time 11nsec vs. 30msec.
Even if actual speed only doubled, turn off losses will drop from 1.5W to 750mW.

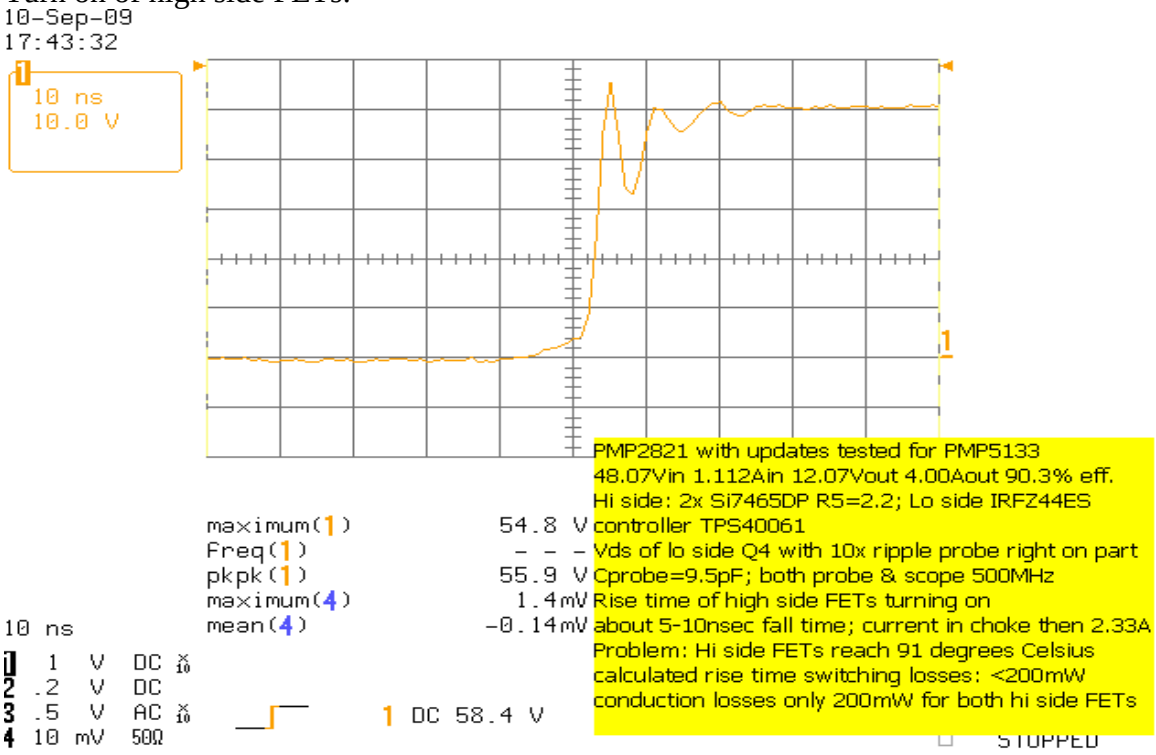
Here is the overall major waveform:



Turn off of hi side FETs:

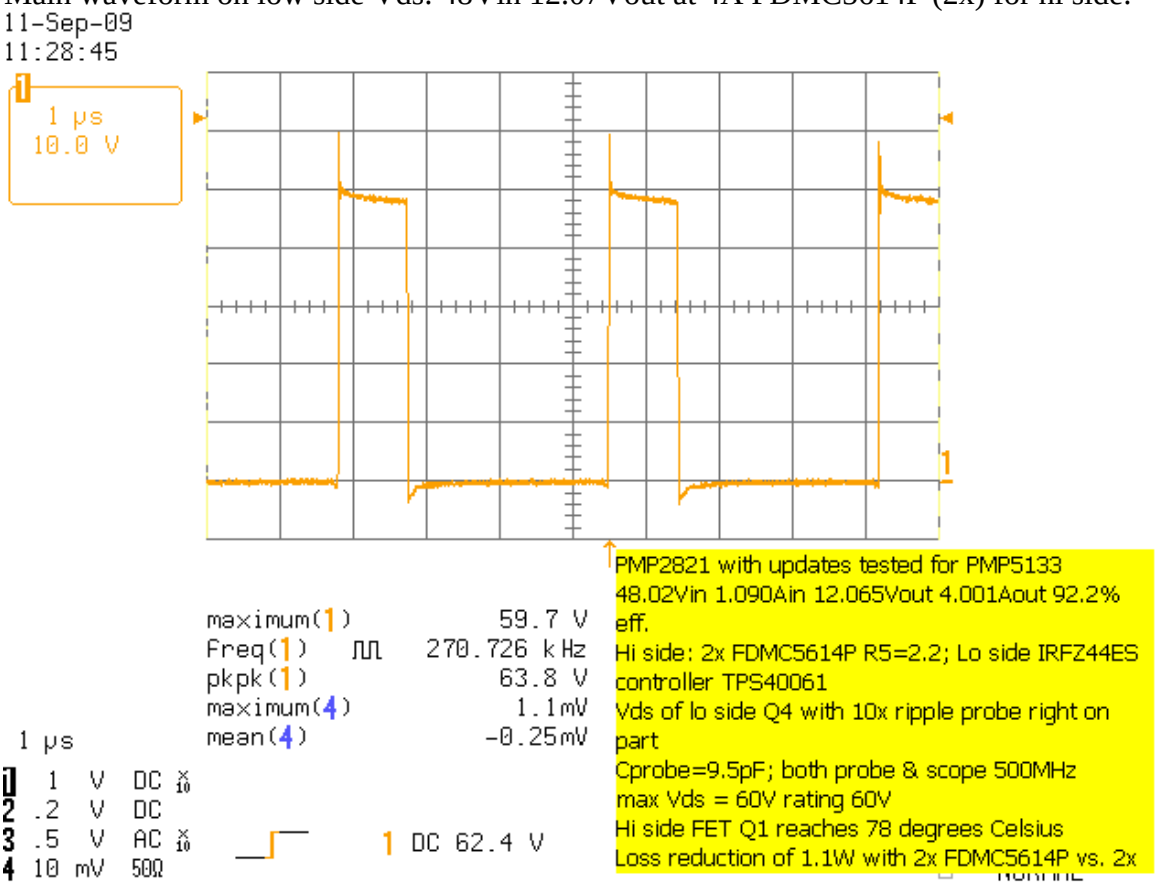


Turn on of high side FETs:



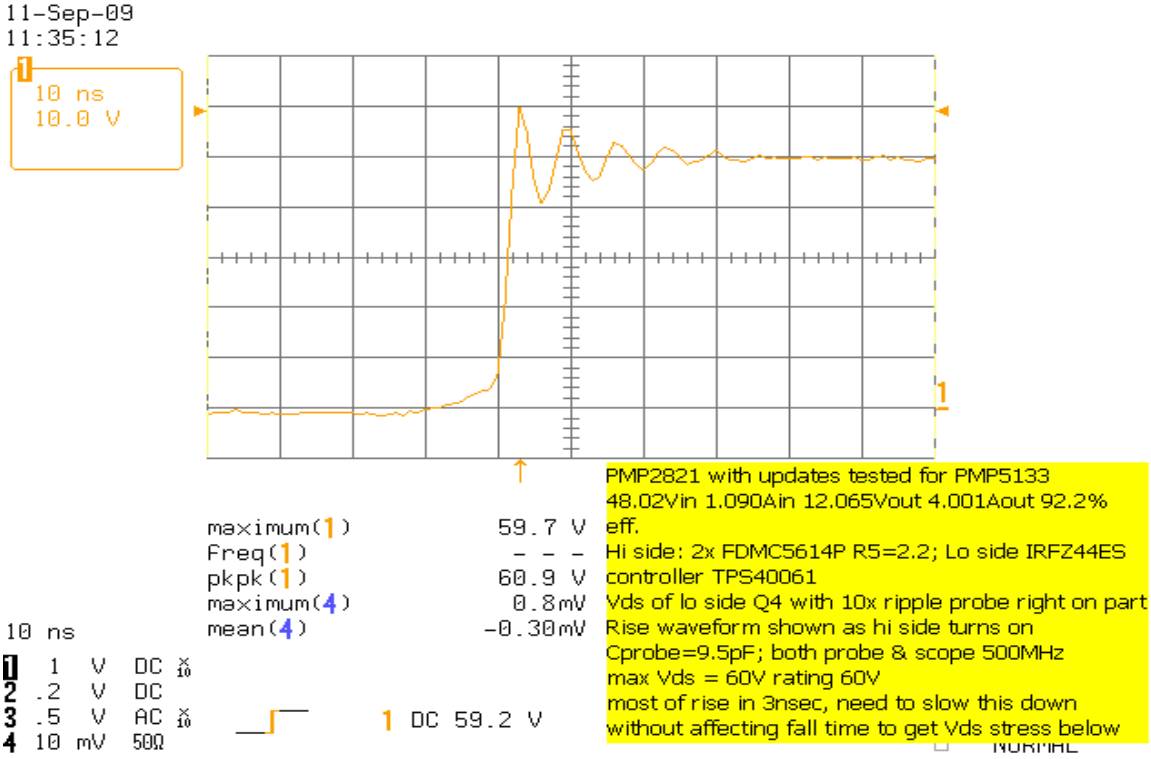
Now the high side MOSFETs were changed from Vishay Si7465DP (2x) to Fairchild FDMC5614P (2x). Then run at same conditions:
48Vin 12Vout at 4A room ambient:
Efficiency now 92.2% vs. 90.3% with loss reduction of 1.1W
Hottest FET Q1 (hi side) now 78 degrees C vs. 91 degrees C
Max Vds stress on low side FET now 60V vs. 55 V before
Main waveform fall time 20 nsec vs. 40nsec before
Main waveform rise time from about 10%: 3nsec vs. 5nsec

Main waveform on low side Vds: 48Vin 12.07Vout at 4A FDMC5614P (2x) for hi side:



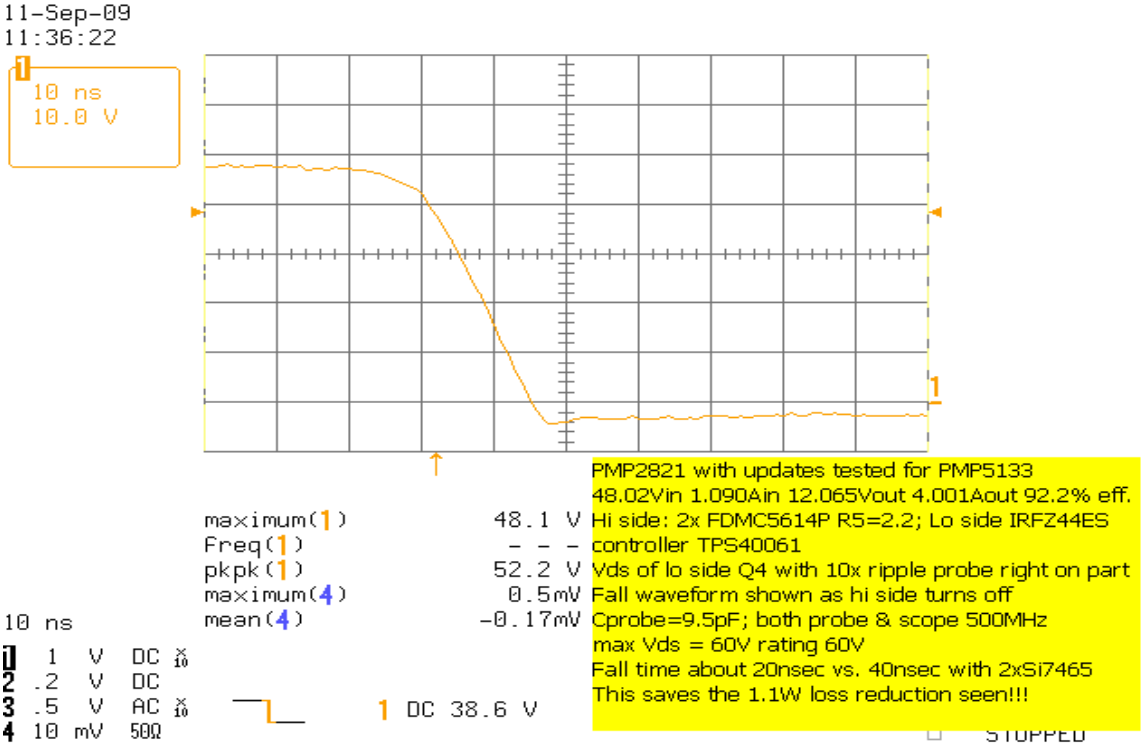
Qq

Details of rise and then fall waveform with FDMC5614Ps: 48Vin 12.07Vout at 4A



Qq

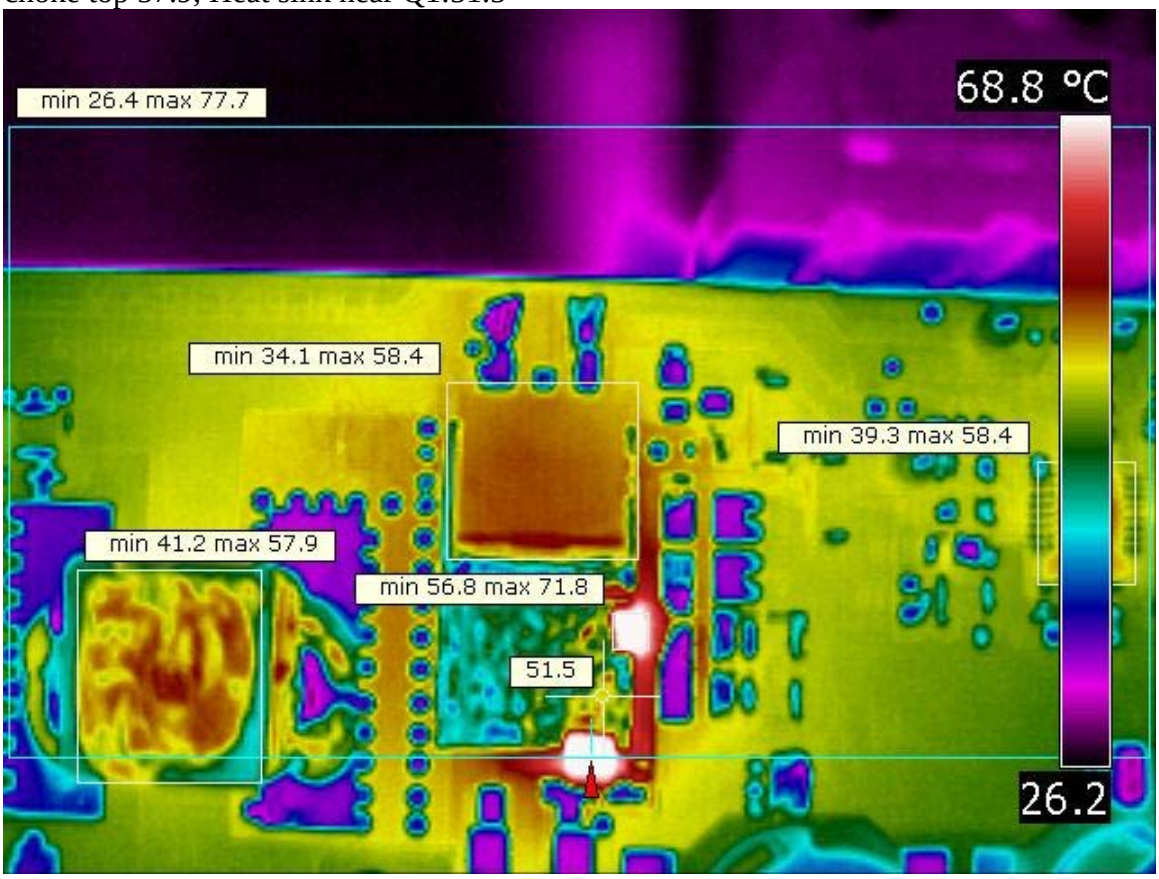
Fall time: 48Vin 12.07Vout at 4A



Qq

Next: a 4.7ohm resistor placed in series with hi side gate drive bias cap C10 to slow down turn on, but not turn off. Losses increased by about 50mW, but peak Vds on low side Q4 dropped from 60V to below 56V.

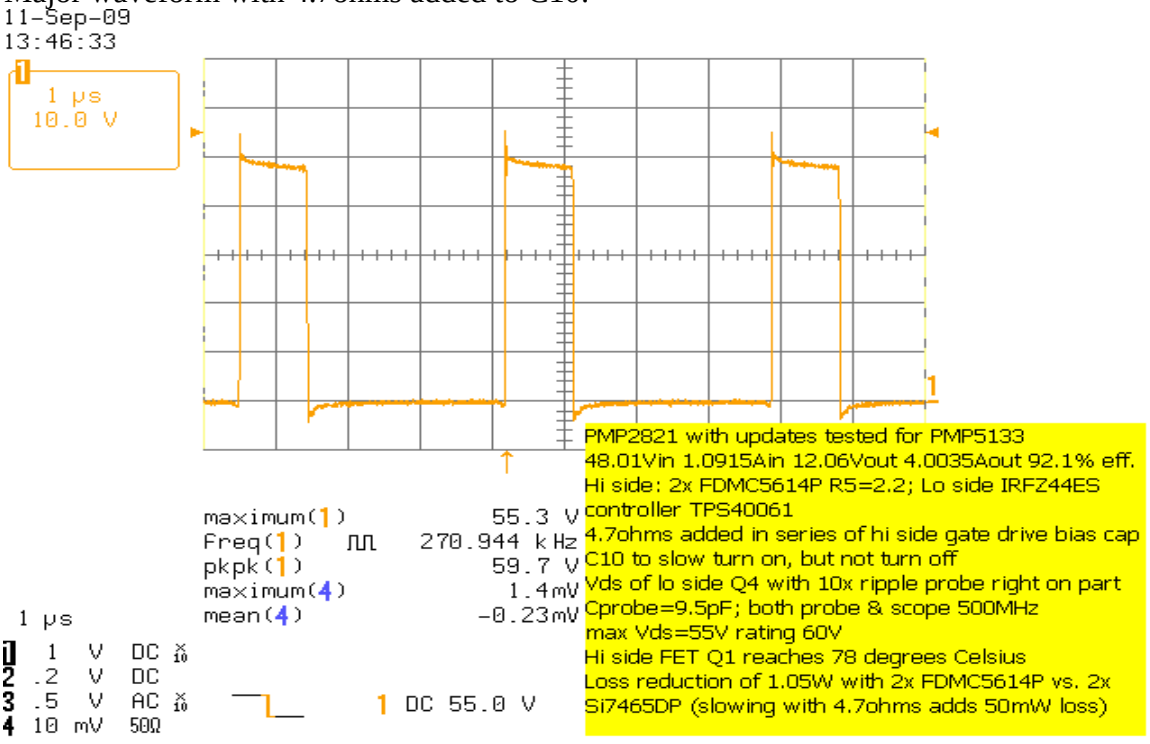
PMP5133 with 2xFDMC5614P 4.7Ohms C10, R5=2.2
48.01Vin 1.0915Ain 12.06Vout 4.0035Aout 4.12Watts on bd
ambient 23-25; Hot spot Q1 hi side 77.7, Q2 at 71.8, Lo side Q4 at 58.4, controller 58.4, choke top 57.9, Heat sink near Q1:51.5



Qq
The high temperatures on Q1 & Q2 are due to the less than ideal coupling of their thermal pads to the “heat sink” copper pad on the board. This pad was painted black along with the top of the choke, so the thermal camera could properly detect the surface temperature. There is a 26 degree drop from the Q1 hot spot to the pad location shown only about 3 mm from the part.

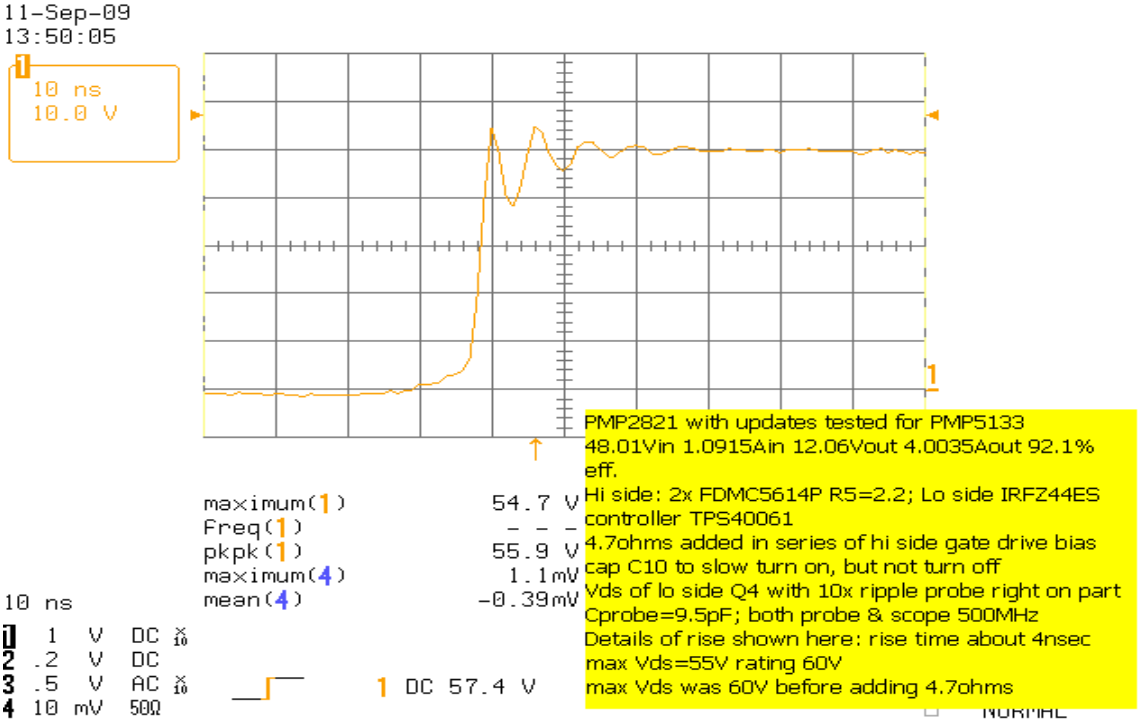
The thermal pad for the hi side FET(s) were designed for either one TO-220 SMD or two 5mm by 6mm power pad devices. With the smaller 3mm by 3mm parts that the FDMC5614Ps are, once the gate and source connections are made, very little thermal pad gets connected to the part. With a layout dedicated to 3x3 parts, much better heat sinking should be achieved.
Qq

Major waveform with 4.7ohms added to C10:



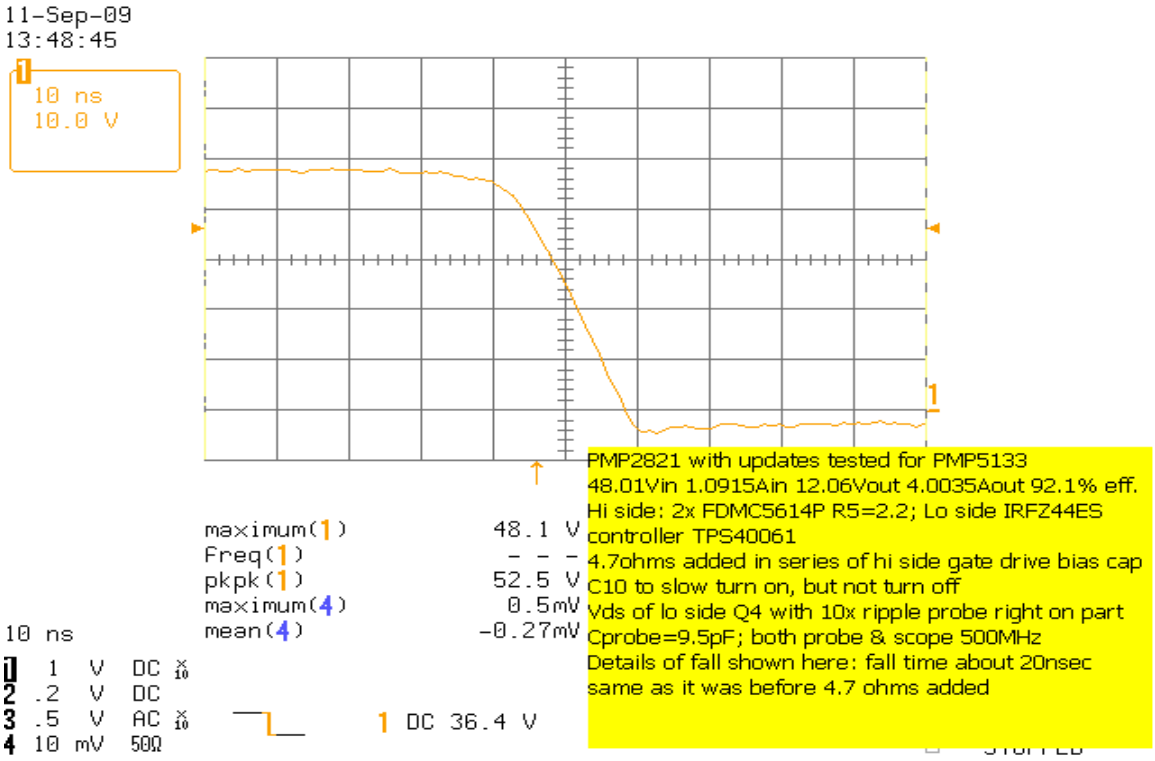
Qq

Rise time detail:



Qq

Fall time detail:



General conclusion:

When switching losses are several times conduction losses as in the high side MOSFETs, you are overinvested in silicon!!! In this application as the high side MOSFETs the FDMC5614Ps have 50% more on resistance than the Si7465DPs, but still managed to reduce losses by over 1 Watt!

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