

### Introduction

The converter board has been developed for a Spoerle (Arrow) embedded DC/DC platform. Therefore the mechanical and electrical specification are intended to satisfy or improve the request. Signals for Power Good and Enable are available to enable sequencing, voltage scaling, diagnosis.

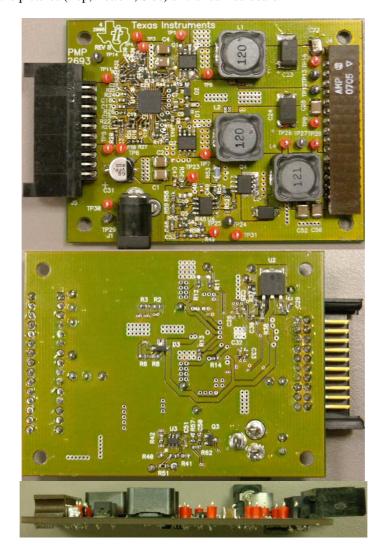
It operates from DC 24V +/- 15% with three Buck topology to three different ouputs:

- 12V@1A, Buck controlled by TPS40200 (current limitation 2A)
- 5V@5A, Synch-Buck controlled by TPS40140 together with the 3.3V ouput (requested is 2A, actual current limitation 5.7A);
- 3.3V@5A, Synch-Buck controlled by TPS40140 together with the 5V ouput (requested is 2A, actual current limitation 5.7A)

Fot the 12V output (TPS40200) the switching frequency is 280kHz, for the other two outputs (TPS40140) the switching frequency is 350kHz.

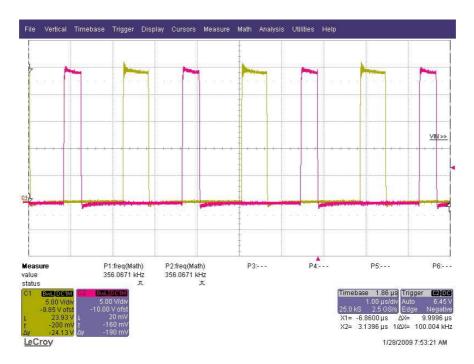
Full MatchCad sheet of the three converters are also provided with complete calculation of power stage and control.

In the following the pictures (Top, Bottom, Side) of the realized board.





## 1 Main Waveforms

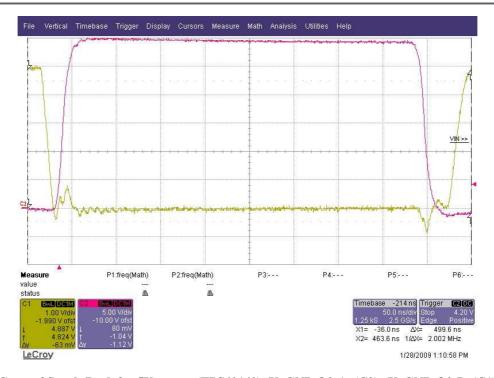


Switch Nodes of Synch-Buck (TPS40140): Vds Q1:B, TP8 (C2), Vds Q2:B, TP7 (C1)

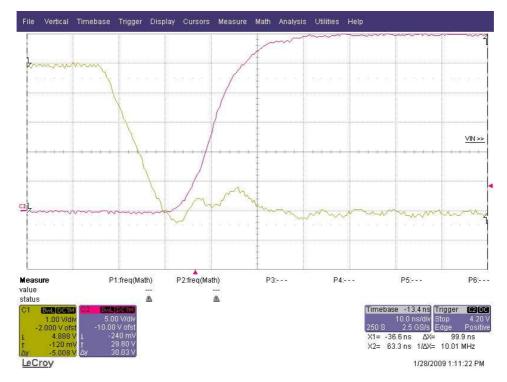


Low Side Mosfet Gates of Synch-Buck (TPS40140): Vgs Q1:B, (C2), Vgs Q2:B, (C1)



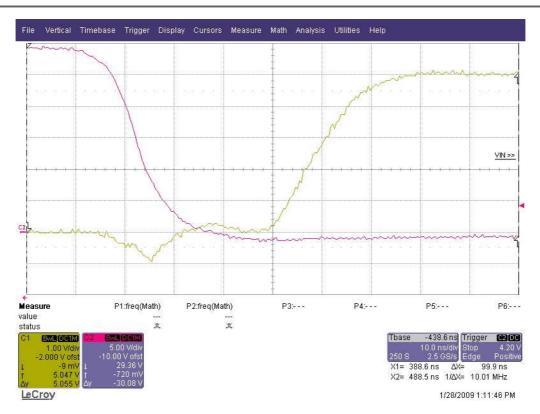


Gates of Synch-Buck for 5V output (TPS40140): VgGND Q2:A, (C2), VgGND Q2:B, (C1)

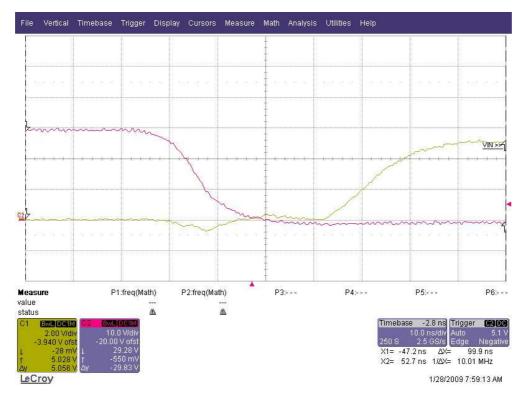


Gates of Synch-Buck for 5V output (TPS40140): VgGND Q2:A, (C2), VgGND Q2:B, (C1)



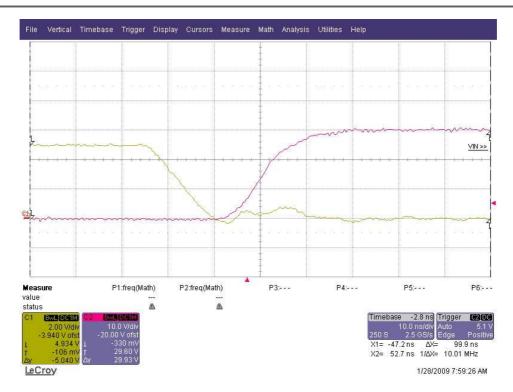


Gates of Synch-Buck for 5V output (TPS40140): VgGND Q2:A, (C2), VgGND Q2:B, (C1)

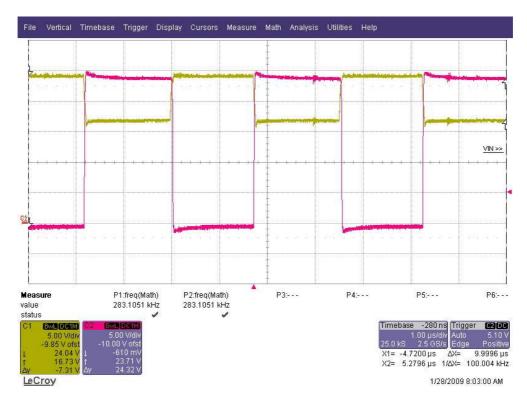


Gates of Synch-Buck for 3.3V output (TPS40140): VgGND Q1:A, (C2), VgGND Q1B, (C1)





Gates of Synch-Buck for 3.3V output (TPS40140): VgGND Q1:A, (C2), VgGND Q1B, (C1)

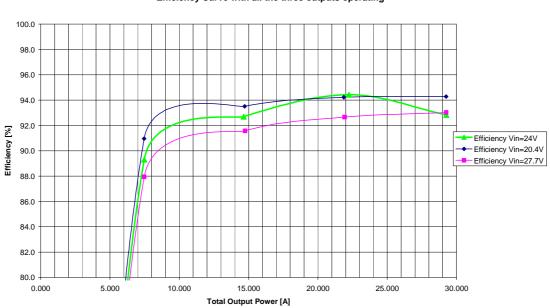


Switch Node and High Side Mosfet Gate of the 12V output Buck (TPS40200): VdGND Q4, TP26



# 2 Efficiency and Load Regulation

The efficiency diagrams are shown in the figure below for 6.5V, 9V, 12V input voltage, as a function of the output current.

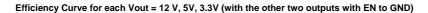


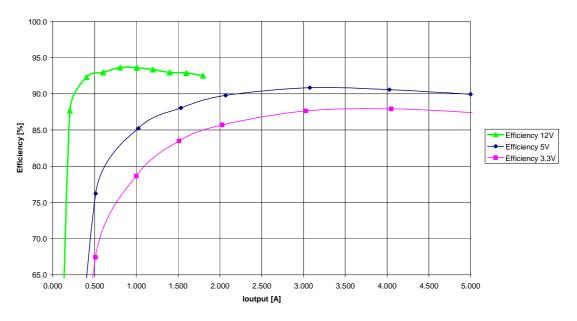
#### Efficiency Curve with all the three outputs operating

The following table shows the measured values:

Vin[V]	lin[mA]	Vout1[V]	lout1[mA]	Vout2[V]	lout2[mA]	Vout3[V]	lout3[mA]	Pin[W]	Pout[W]	η%
24.26	0.027	12.23	0.000	5.04	0.000	3.35	0.000	0.655	0.000	0.0
24.18	0.346	12.23	0.256	5.03	0.511	3.35	0.529	8.366	7.472	89.3
24.09	0.656	12.23	0.504	5.03	1.004	3.34	1.027	15.803	14.648	92.7
24.08	0.978	12.23	0.775	5.02	1.513	3.34	1.546	23.550	22.237	94.4
24.01	1.313	12.22	1.006	5.02	2.016	3.34	2.054	31.525	29.266	92.8
20.08	0.028	12.23	0.000	5.04	0.000	3.35	0.000	0.562	0.000	0.0
20.68	0.397	12.24	0.256	5.04	0.516	3.33	0.520	8.210	7.468	91.0
20.60	0.764	12.24	0.504	5.03	1.017	3.34	1.028	15.738	14.717	93.5
20.55	1.129	12.24	0.755	5.02	1.495	3.34	1.530	23.201	21.861	94.2
20.44	1.518	12.23	1.006	5.01	2.013	3.35	2.051	31.028	29.253	94.3
27.79	0.028	12.23	0.000	5.04	0.000	3.35	0.000	0.770	0.000	0.0
27.68	0.307	12.23	0.256	5.03	0.511	3.35	0.529	8.498	7.473	87.9
27.67	0.582	12.23	0.504	5.03	1.021	3.34	1.032	16.104	14.746	91.6
27.65	0.856	12.23	0.755	5.02	1.504	3.34	1.541	23.668	21.931	92.7
27.59	1.140	12.23	1.006	5.02	2.012	3.34	2.052	31.453	29.257	93.0







The following table shows the measured values, of each output power measured with the other two outputs shut-off by the Enable pin connected to Ground. The efficiency is effected however by the performance of the linear regulator, when the 5V output is shut-off, because in this condition the regulator provides the supply to the TPS40140.

Vin[V]	lin[mA]	Vout1[V]	lout1[mA]	Pin[W]	Pout2[W]	η%
24.44	0.013	12.23	0.000	0.318	0.000	0.0
24.41	0.117	12.22	0.205	2.856	2.505	87.7
24.37	0.220	12.22	0.405	5.361	4.949	92.3
24.35	0.326	12.22	0.604	7.938	7.381	93.0
24.32	0.433	12.22	0.807	10.531	9.862	93.6
24.32	0.540	12.22	1.006	13.133	12.293	93.6
24.24	0.648	12.22	1.200	15.708	14.664	93.4
24.26	0.758	12.22	1.399	18.389	17.096	93.0
24.22	0.868	12.22	1.598	21.023	19.528	92.9
24.21	0.981	12.22	1.798	23.750	21.972	92.5
24.43	0.029	5.04	0.000	0.708	0.000	0.0
24.40	0.139	5.03	0.514	3.392	2.585	76.2
24.39	0.248	5.03	1.025	6.049	5.156	85.2
24.36	0.359	5.02	1.534	8.745	7.701	88.1
24.34	0.475	5.02	2.068	11.562	10.381	89.8
24.26	0.699	5.01	3.075	16.958	15.406	90.8
24.20	0.917	4.99	4.028	22.191	20.100	90.6
24.13	1.147	4.98	4.999	27.677	24.895	89.9
24.44	0.032	3.35	0.000	0.770	0.000	0.0
24.42	0.104	3.35	0.511	2.540	1.712	67.4
24.41	0.174	3.34	1.000	4.247	3.340	78.6

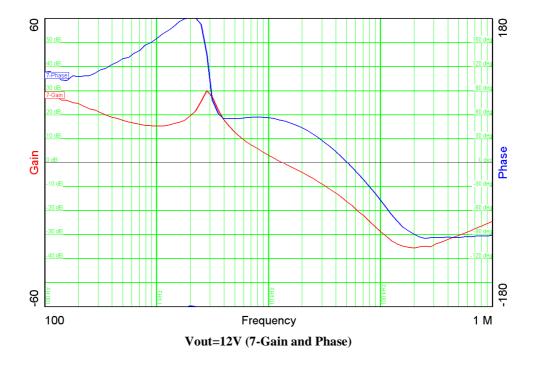
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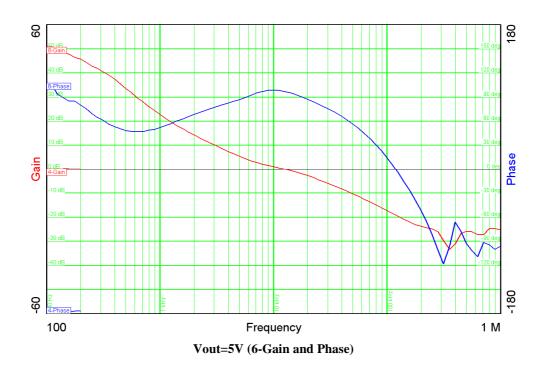
24.39	0.248	3.34	1.512	6.049	5.050	83.5
24.38	0.324	3.34	2.027	7.899	6.770	85.7
24.33	0.473	3.33	3.029	11.508	10.087	87.6
24.29	0.631	3.33	4.047	15.327	13.477	87.9
24.25	0.786	3.32	5.019	19.061	16.663	87.4

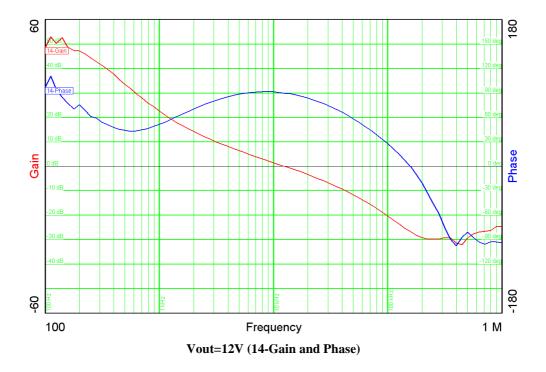
# 3 Control Loop Frequency Response

The figures below show the open loop response for Vout=12V, Vout=5V, and Vout=3.3V at full output load and Vin=24V.







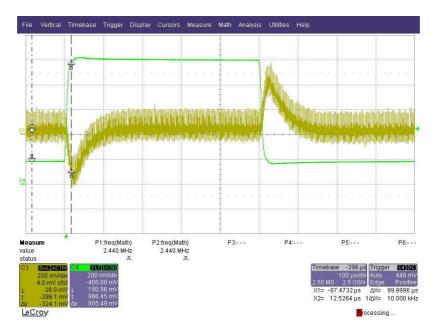




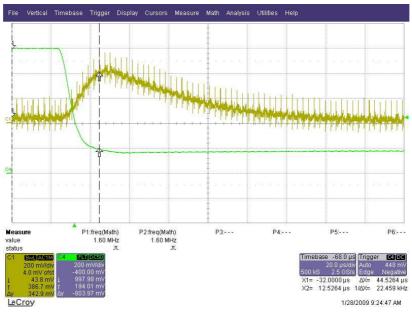
### 4 Load Transients

The figure below show the response to load transients applied to each output.

The current on the Output is stepping from minimum continous mode load to full load (1A for Vout=12V and 2A for Vout=5V and Vout=3.3V) and viceversa, with Vin=24V.

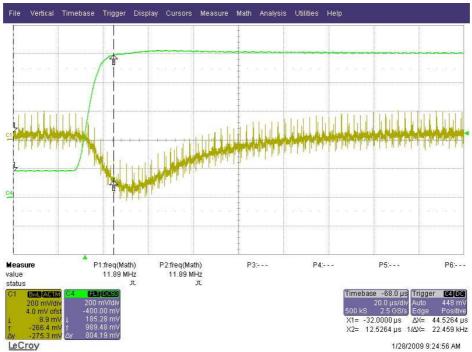


Vout=12V (C2), Iout (C4, 200mA/V current probe)

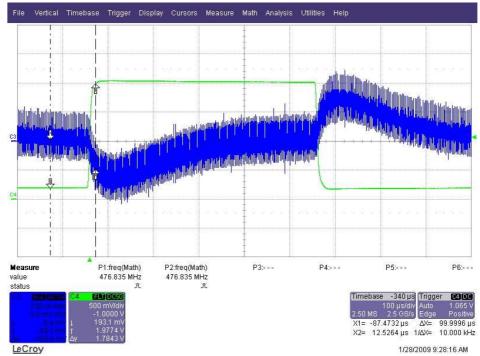


Vout=12V (C2), Iout (C4, 200mA/V current probe)



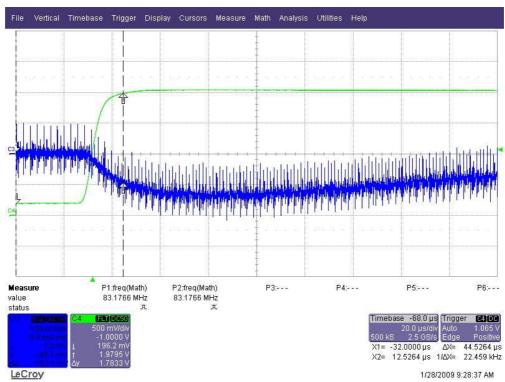


Vout=12V (C2), Iout (C4, 200mA/V current probe)

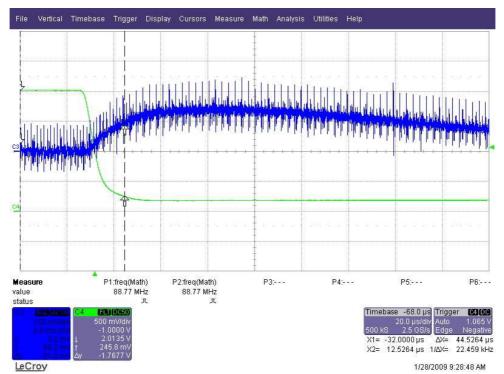


Vout=5V (C2), Iout (C4, 500mA/V current probe)



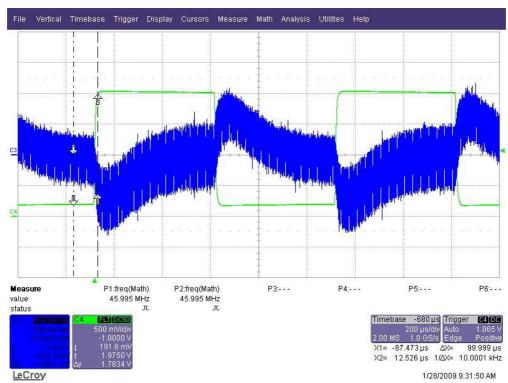


Vout=5V (C2), Iout (C4, 500mA/V current probe)

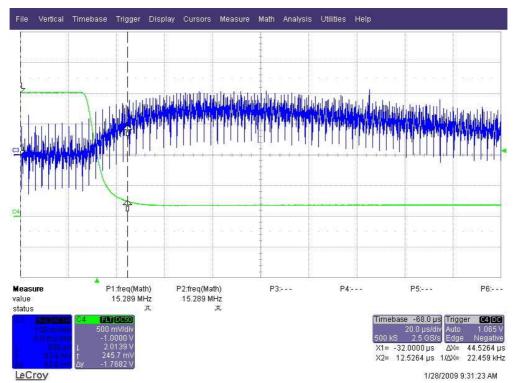


Vout=5V (C2), Iout (C4, 500mA/V current probe)



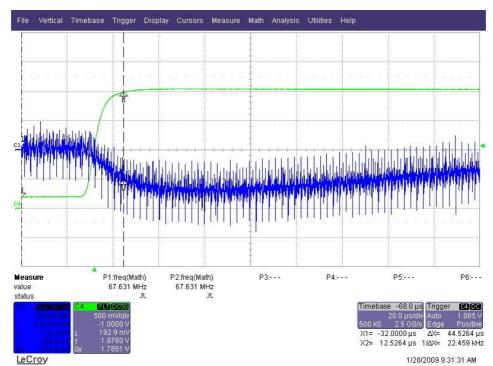


Vout=3.3V (C2), Iout (C4, 500mA/V current probe)



Vout=3.3V (C2), Iout (C4, 500mA/V current probe)



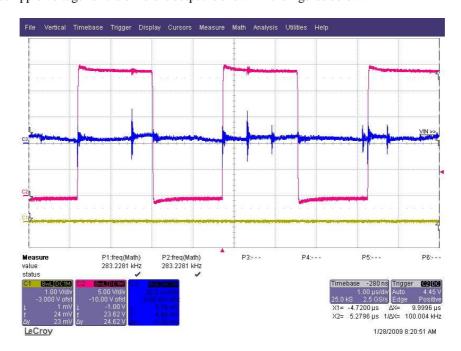


Vout=3.3V (C2), Iout (C4, 500mA/V current probe)

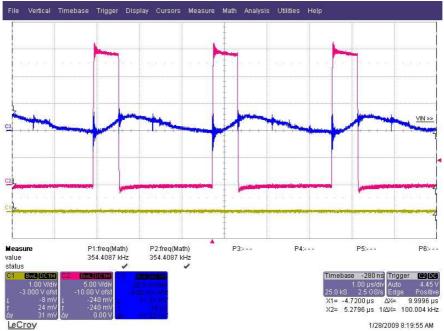


## 5 Output and Input Ripple Voltage

The output ripple voltage for the different output is shown in the figures below:



Output ripple at the V=12V ouput (C3), Switch node TP26 (C2), at Iout=1A



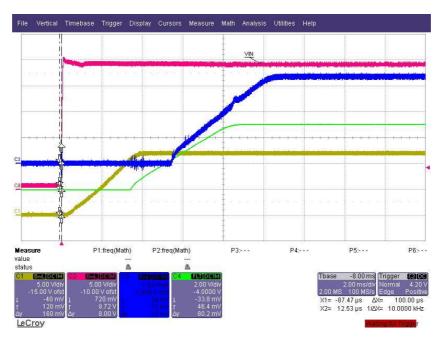
Output ripple at the V=5V ouput (C3), Switch node TP7 (C2), at Iout=2A





Output ripple at the V=3.3V ouput (C3), Switch node TP8 (C2), at Iout=2A

## 6 Start-up Waveforms



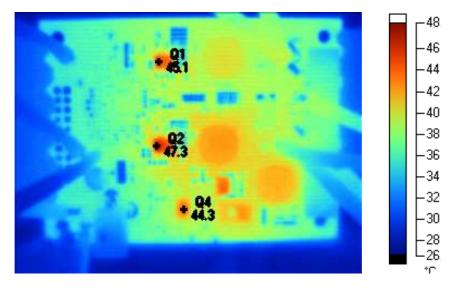
Input Voltage start Start-up Waveforms: Input voltage (C2), Output Voltage 12V (C1) @1A Output Voltage 5V (C4) @2A, output Voltage 3.3V (C3) @2A



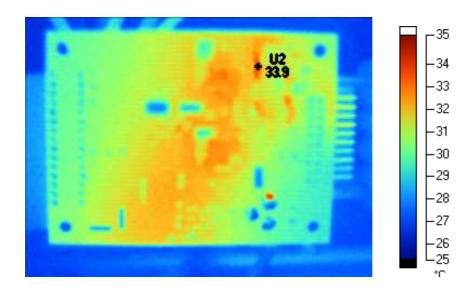
## 7 Thermal Images

The thermal images of board are taken for the Top Side and Bottom side of the board at the temperature of  $T=25^{\circ}C$  ambient, at output load Vout=12@1A Vout=5@2A Vout=3.3@2A.

In every picture the hottest spot is indicated, together with the temperature of the most significant components.



Top Side
Output Load Vout=12V@1A, Vout=5@2A, Vout=3.3V@2A, Output Power 30W



Bottom Side
Output Load Vout=12V@1A, Vout=5@2A, Vout=3.3V`@2A,Output Power=30W

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