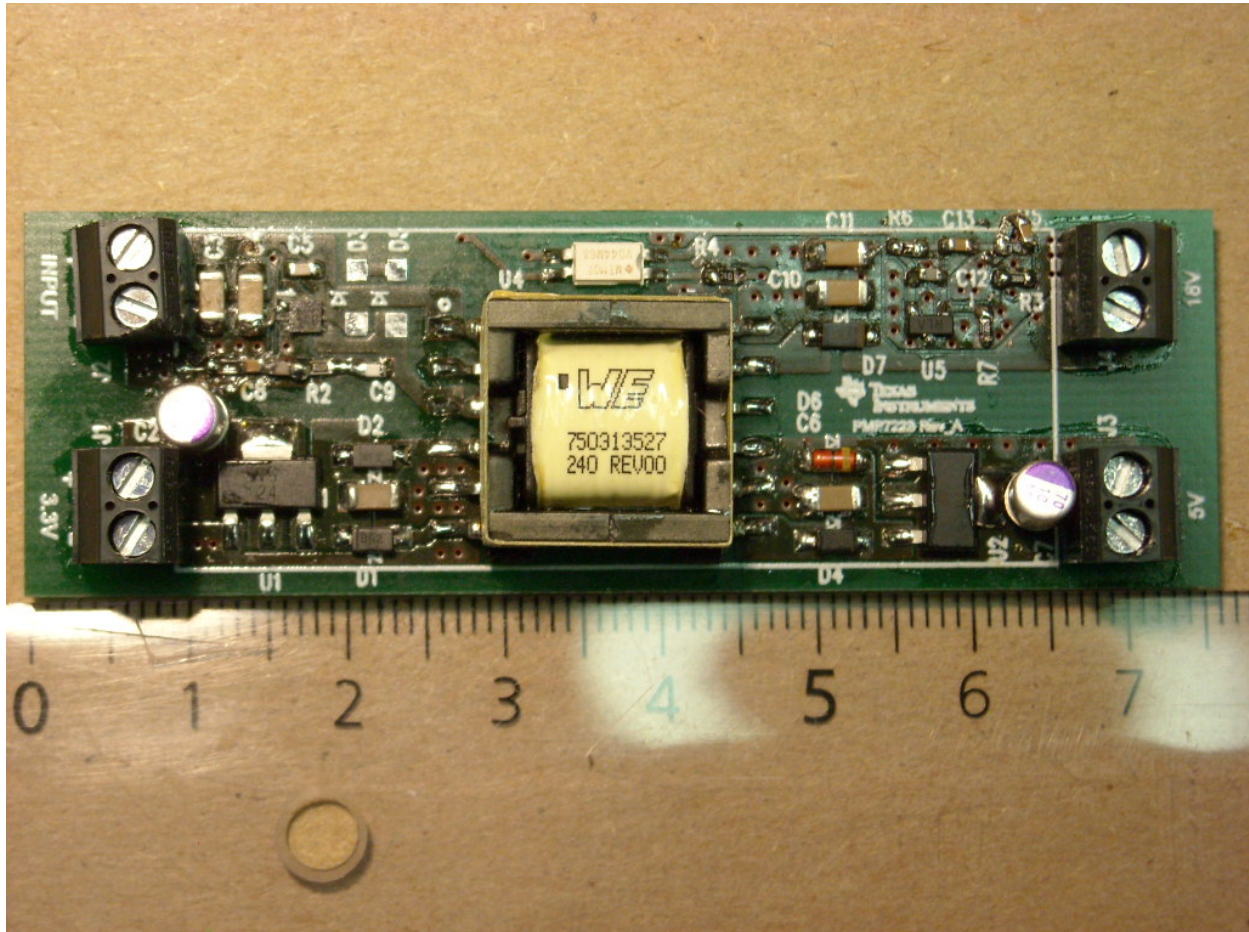


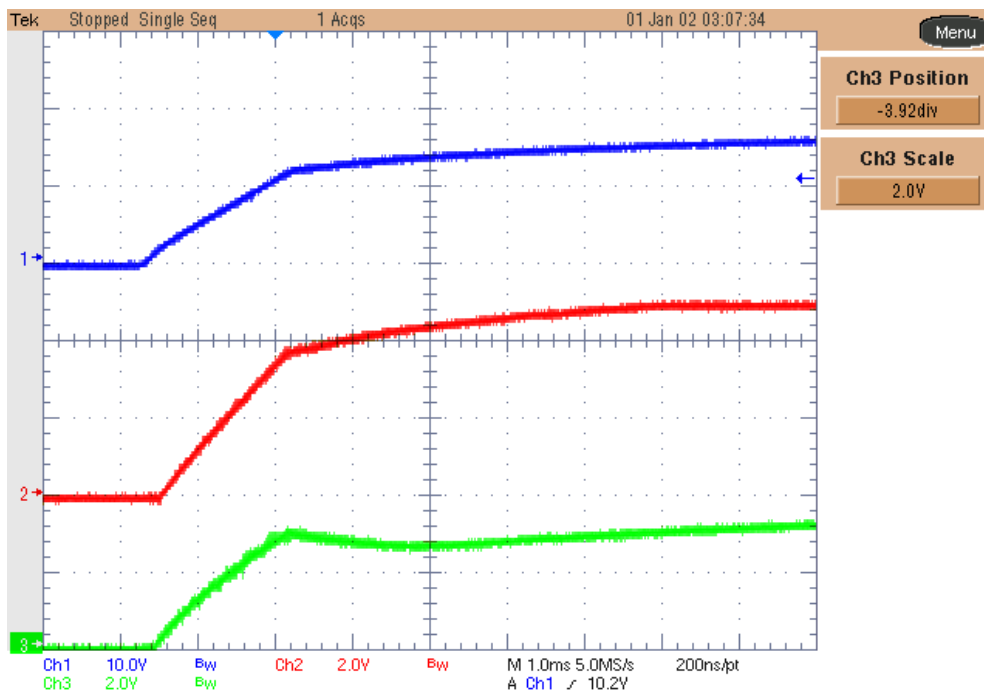
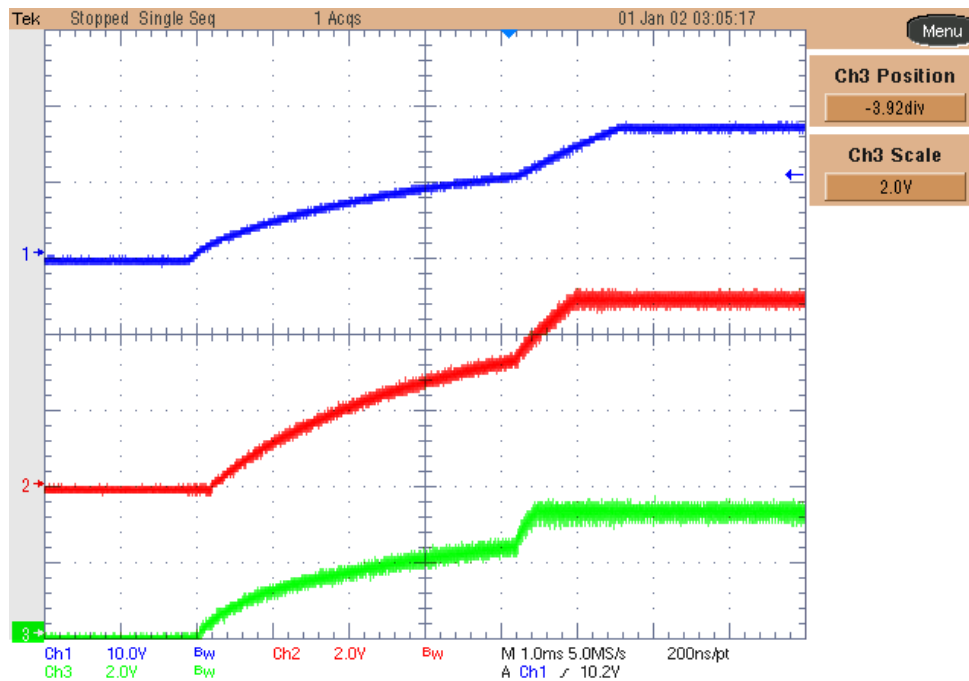
1. PHOTO OF THE PROTOTYPE



Startup

The output voltages at startup are shown in the images below. The input voltage was set to 4.5V. The load was set to full power (upper picture) and no power (bottom picture). The bandwidth limit for all channels was 20MHz.

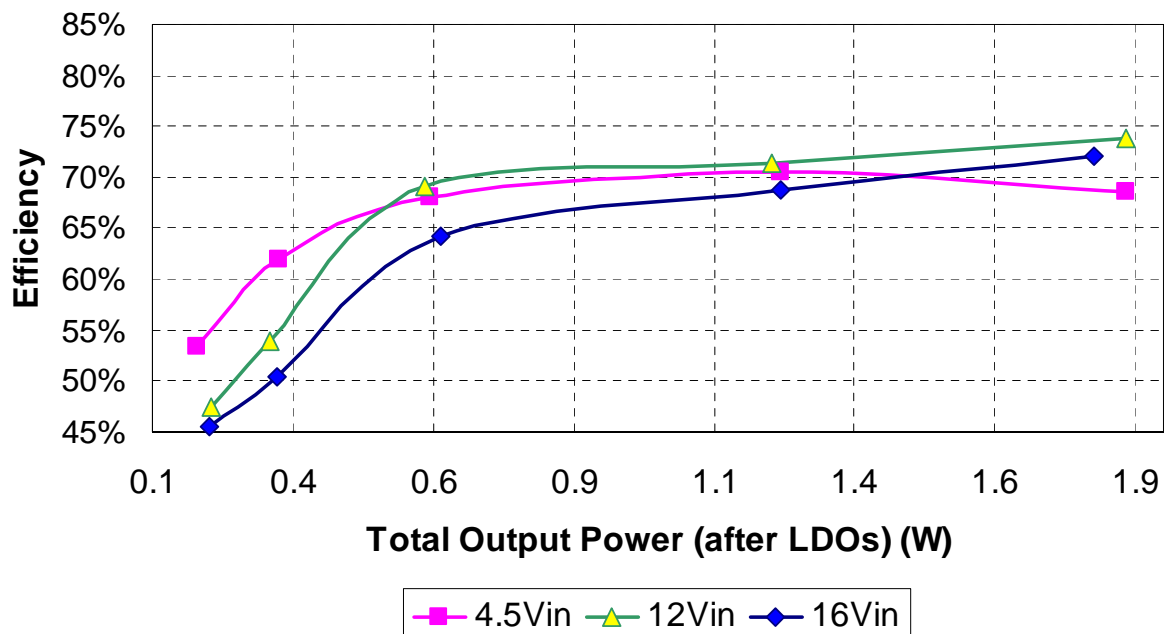
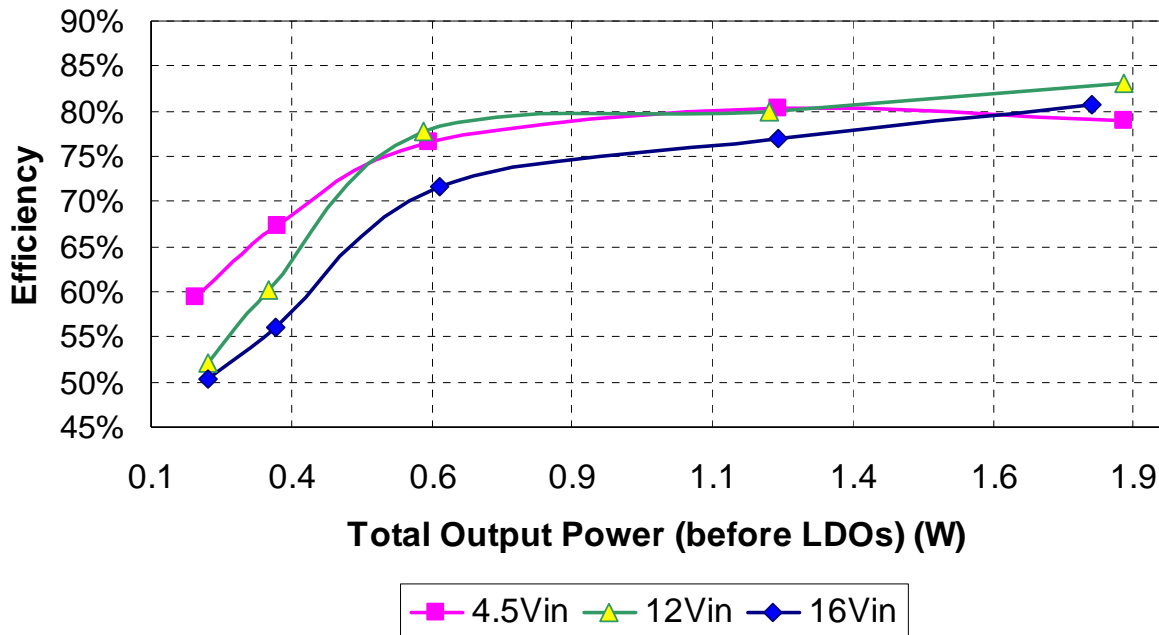
Ch1: 18Vout (10 V/div, 1msec/div), Ch2: 5Vout, (2 V/div), Ch3: 3.3Vout (2 V/div)



2. Efficiency

The efficiency data is shown in the tables and graphs below.

The measurements were taken at three different input voltages, 4.5V, 12V and 16V. The top graph refers to the efficiency without LDOs (measured at the inputs of them) and the bottom one shows the total efficiency.



Vin (V)	Iin (mA)	V18 (V)	V6 (V)	V4 (V)	V5 (V)	V3.3 (V)	I18 (mA)	I5 (mA)	I3.3 (mA)	Pout (W)	Pin (W)	Ploss (W)	Eff. (%) before LDO	Eff. (%) Total
4.541	14.6	17.97	5.856	3.857	4.748	2.910	0.0	0.0	0.00	0.000	0.07	0.07	0.0%	0.0%
4.539	66.8	17.95	6.929	4.521	5.000	3.302	6.3	5.1	7.00	0.180	0.30	0.12	59.4%	53.3%
4.535	106.5	17.95	6.292	4.565	5.000	3.302	12.0	10.0	10.20	0.325	0.48	0.16	67.3%	61.9%
4.526	171.5	17.94	6.912	4.678	5.000	3.302	20.2	20.0	20.00	0.594	0.78	0.18	76.6%	68.1%
4.505	336.7	17.94	6.935	5.006	5.002	3.301	40.8	41.1	40.00	1.217	1.52	0.30	80.2%	70.5%
4.564	507.9	17.92	7.007	5.318	5.003	3.300	60.8	60.0	60.60	1.832	2.32	0.49	79.0%	68.6%

Vin (V)	Iin (mA)	V18 (V)	V6 (V)	V4 (V)	V5 (V)	V3.3 (V)	I18 (mA)	I5 (mA)	I3.3 (mA)	Pout (W)	Pin (W)	Ploss (W)	Eff. (%) before LDO	Eff. (%) Total
12.06	8.5	17.96	6.410	4.267	5.001	3.244	0.0	0.0	0.0	0.000	0.10	0.10	0.0%	0.0%
12.05	32.3	17.93	6.919	4.606	5.000	3.302	7.6	5.0	7.0	0.203	0.39	0.19	52.2%	47.4%
12.05	42.8	17.92	6.919	4.579	5.001	3.303	10.9	10.0	10.0	0.310	0.52	0.21	60.2%	54.0%
12.06	62.5	17.95	6.933	4.536	5.002	3.303	19.6	20.3	20.5	0.586	0.75	0.17	77.7%	69.1%
12.04	124.7	17.91	6.909	4.622	5.003	3.302	41.2	40.2	40.2	1.201	1.50	0.30	80.0%	71.4%
12.03	183.3	17.90	6.907	4.729	5.004	3.301	62.7	61.8	60.0	1.833	2.21	0.37	83.1%	73.9%

Vin (V)	Iin (mA)	V18 (V)	V6 (V)	V4 (V)	V5 (V)	V3.3 (V)	I18 (mA)	I5 (mA)	I3.3 (mA)	Pout (W)	Pin (W)	Ploss (W)	Eff. (%) before LDO	Eff. (%) Total
16.05	7.3	17.95	6.494	4.307	5.001	3.263	0.0	0.0	0.0	0.000	0.12	0.12	0.0%	0.0%
16.05	24.8	17.92	6.927	4.649	5.001	3.303	7.4	5.0	7.1	0.200	0.40	0.20	50.3%	45.5%
16.04	35.7	17.89	6.899	4.603	5.001	3.302	11.5	10.0	10.0	0.321	0.57	0.25	56.0%	50.4%
16.04	53.3	17.90	6.921	4.566	5.002	3.302	21.3	20.3	20.0	0.613	0.85	0.24	71.7%	64.2%
16.03	98.8	17.88	6.902	4.574	5.003	3.302	42.1	41.0	40.0	1.219	1.58	0.37	76.9%	68.8%
16.02	137.3	17.87	6.893	4.634	5.004	3.301	60.7	60.0	60.2	1.777	2.20	0.42	80.8%	72.0%

Where:

V18 = 18V output voltage on J4

V6 = Voltage on C6 (input of U2)

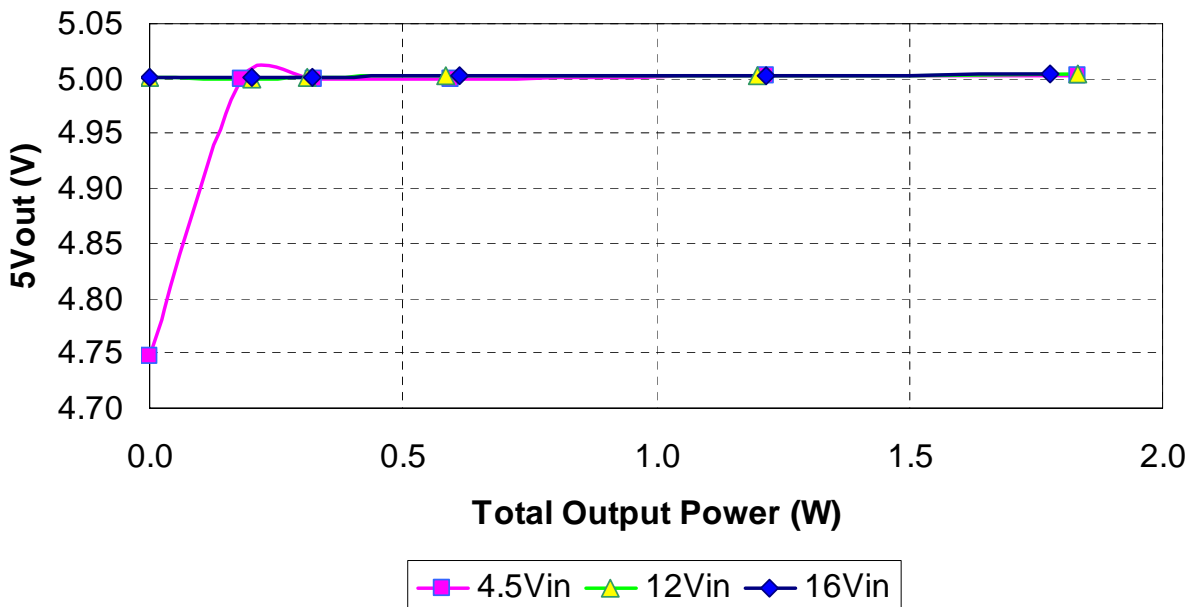
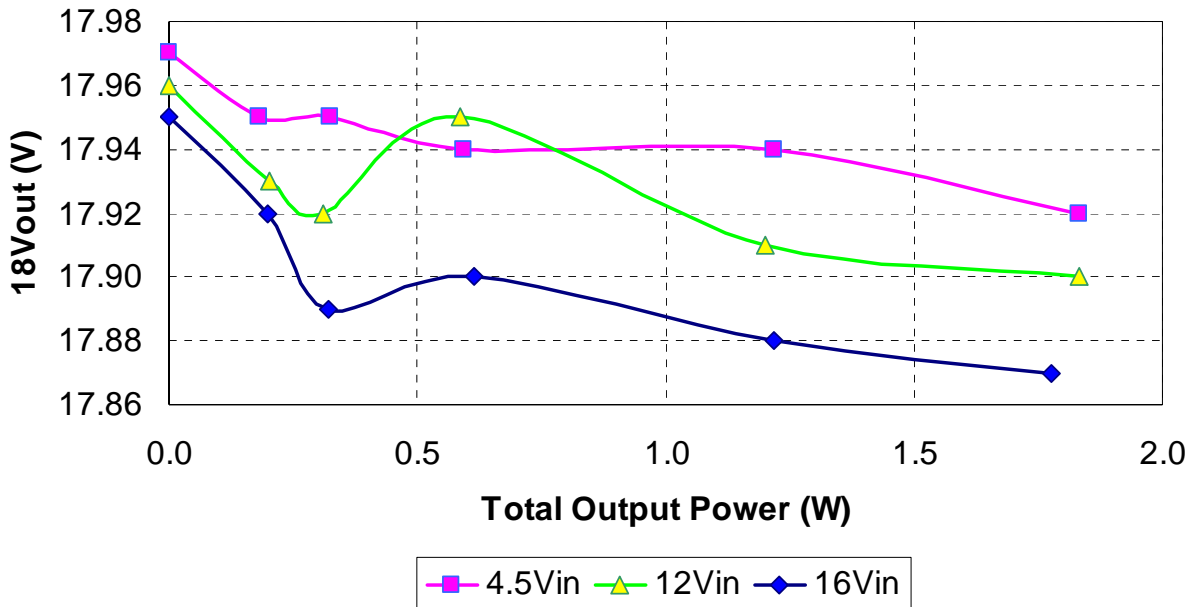
V4 = Voltage on C1 (input of U1)

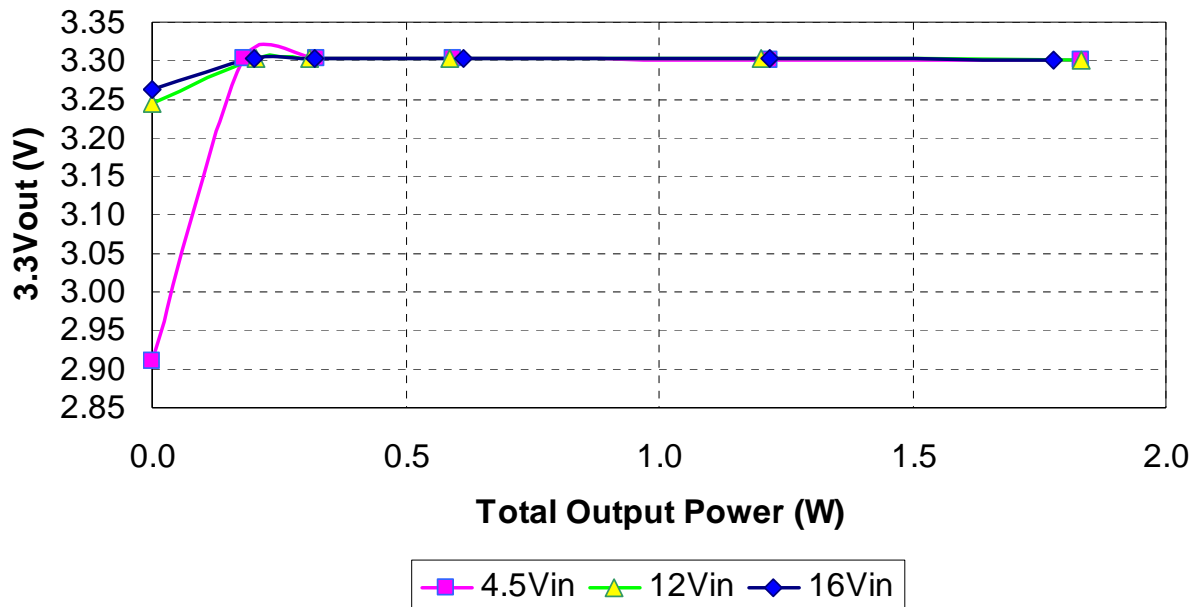
V5 = 5V output voltage on J3

V3.3 = 3.3V output voltage on J1

3. Output Voltage Regulation

The output voltage regulation for each output versus load (increased at the same time for all outputs) at 4.5V, 12V and 16V input voltage is shown in the graphs below.



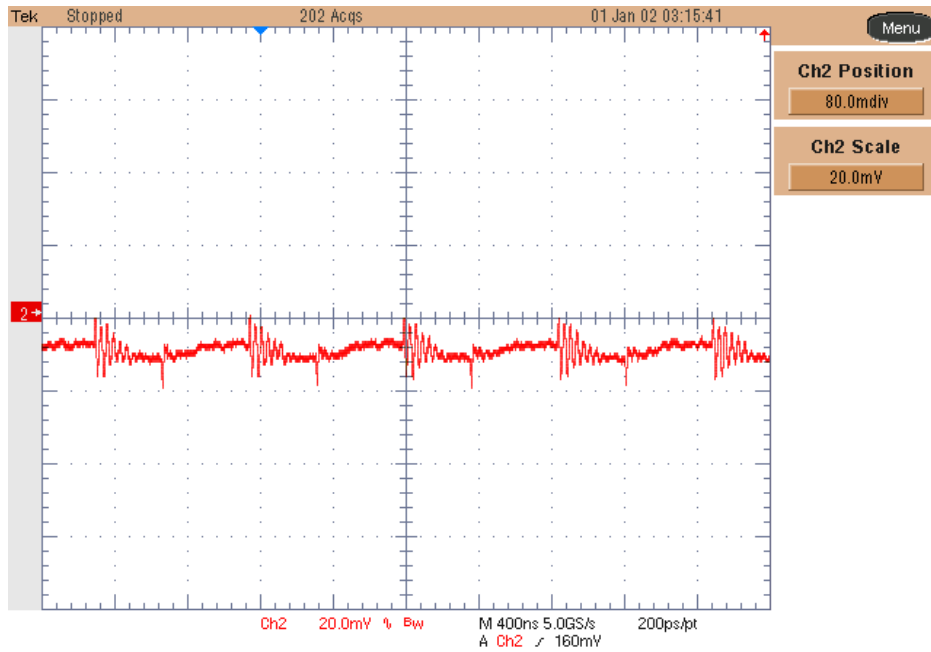


As shown in the graphs above, the 3.3V and 5V outputs go out of regulation if the load is too small. A minimum load of 8mA is necessary on the output of 18V to get the 5Vout and 3.3Vout stable for loads on these outputs comprised between zero and full load.

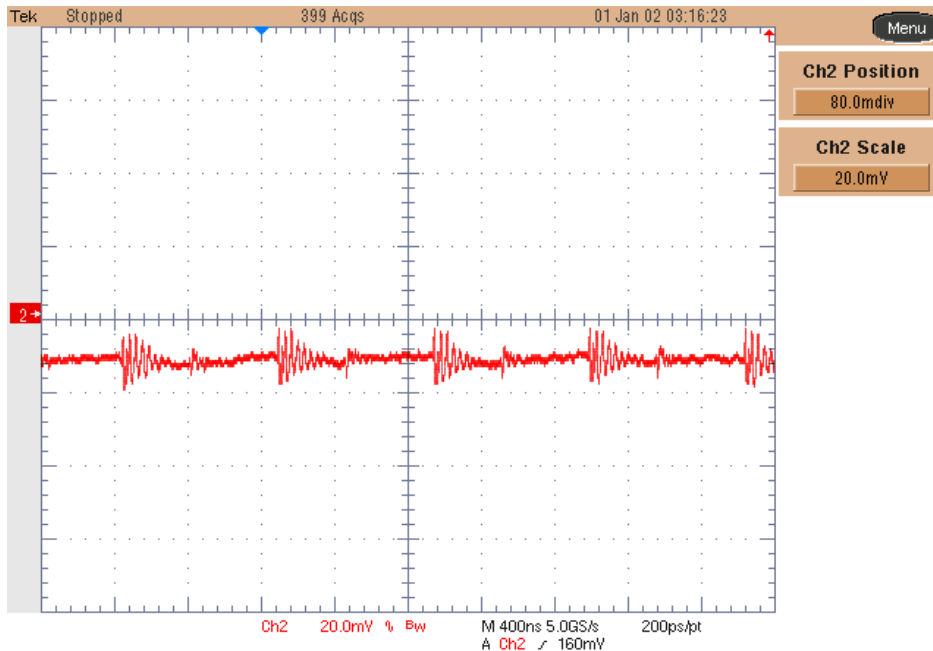
4. Input and Output Ripple Voltage

The ripple voltage waveforms measured at the terminal blocks are shown in the plots below. The input was set to 12V and the outputs fully loaded.

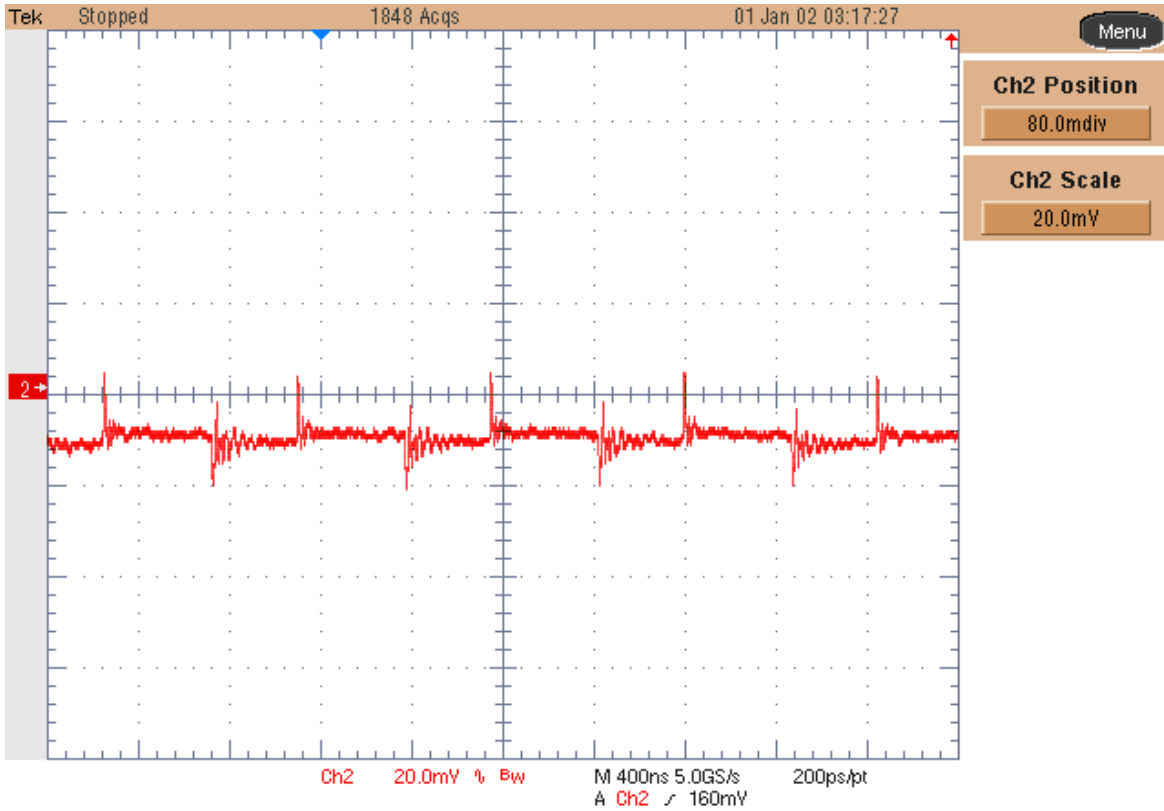
Ch2: 18Vout ripple voltage (20 mV/div, 400 nsec/div, AC coupled, 20MHz BW limit).



Ch2: 5Vout ripple voltage (20 mV/div, 400nsec/div, AC coupled, 20MHz BW limit).



Ch2: 3.3Vout ripple voltage (20 mV/div, 400nsec/div, AC coupled, 20MHz BW limit).

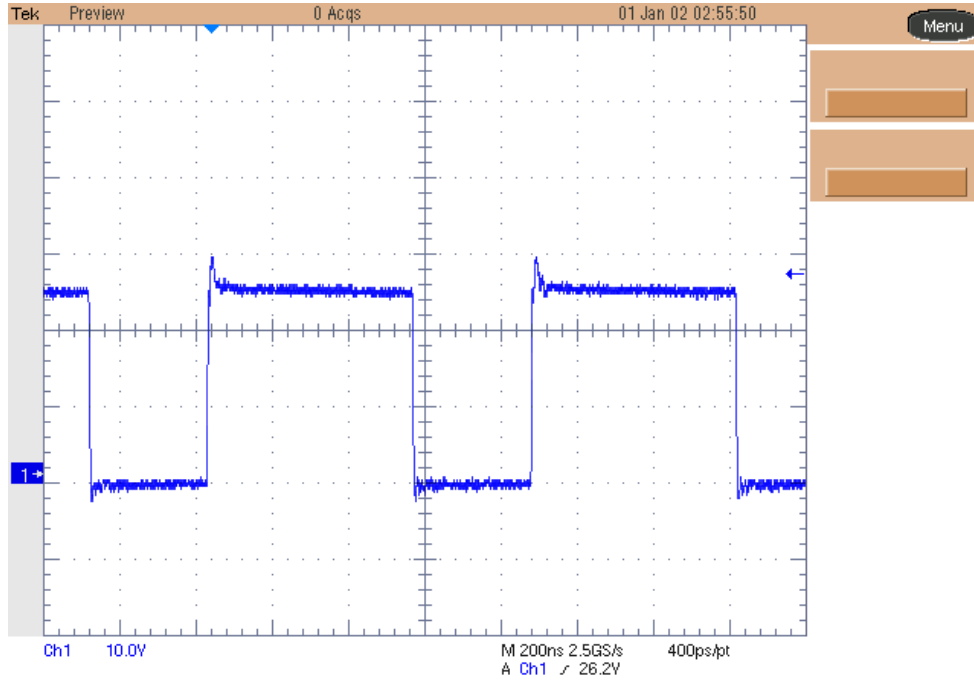


5. Switching Waveforms

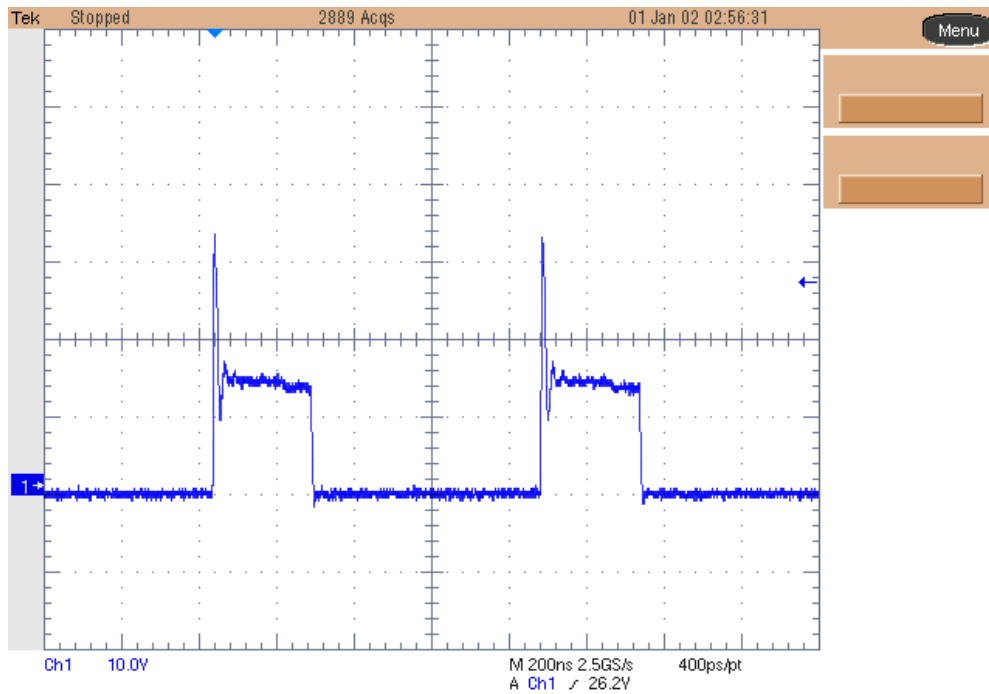
The images below show the drain-to-source waveforms of the SW pin of U3 at full load.

Ch1: SW node, (10V/div, 200nsec/div), no bandwidth limit

16Vin:



4.5Vin:

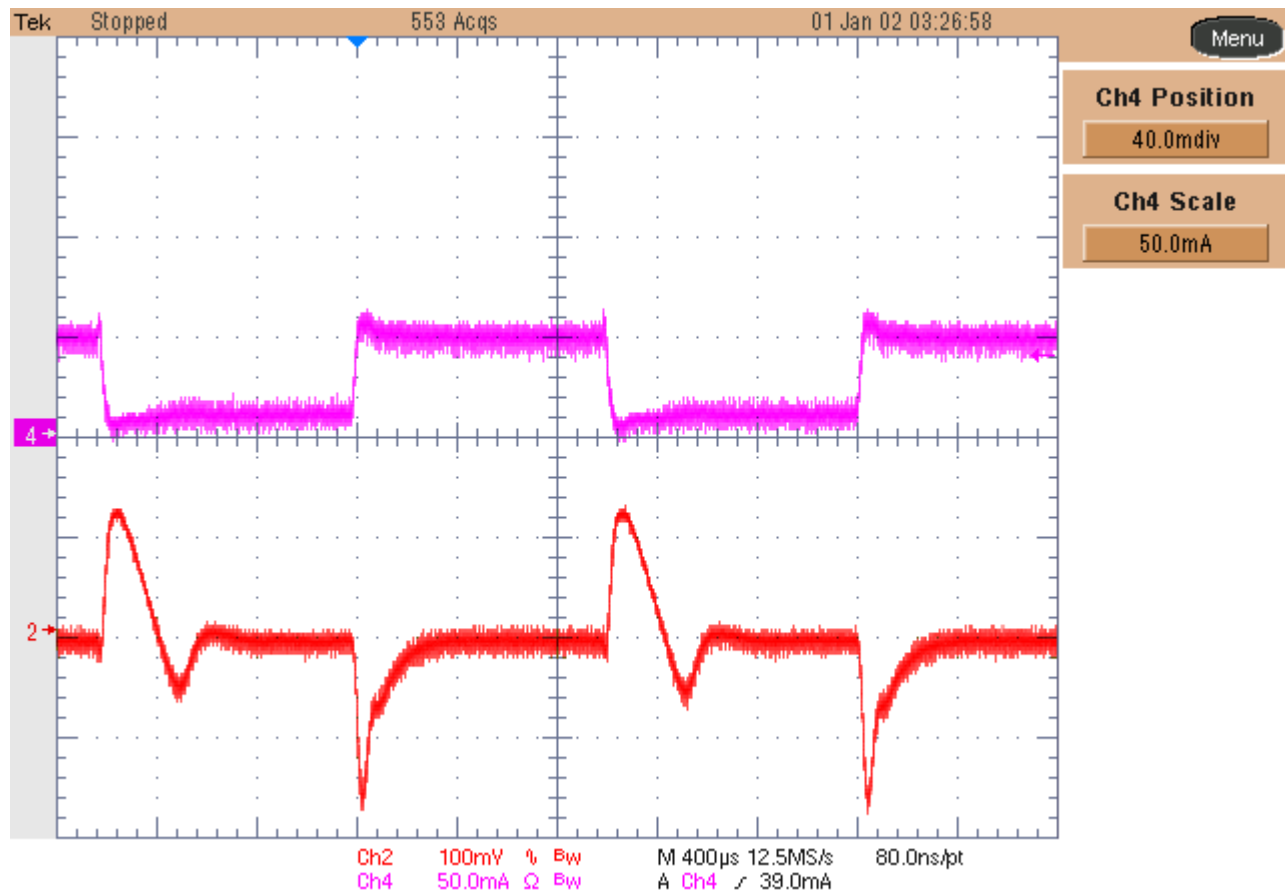


6. Transient Response

The image below shows the transient response behavior of the 18Vout. The input voltage was set to the nominal voltage (12V) and the load on the 18Vout switched between 0 and 60mA, while the other outputs were kept at 60mA.

Channel 2: 18Vout output voltage (100mV/div, AC coupled, 400usec/div, 20MHz BWL)

Channel 4: 18Vout output current (50mA/div, DC coupled, 20MHz BWL)



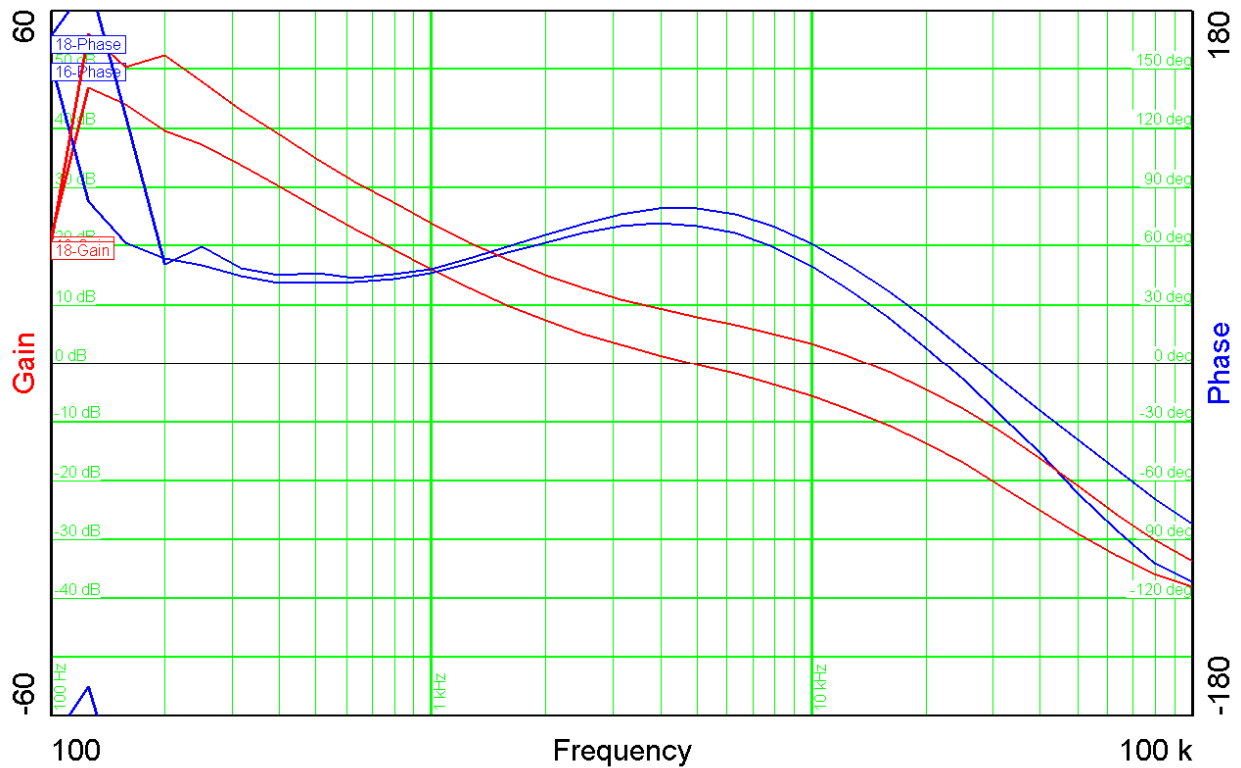
7. Loop Analysis

The graph below shows the loop measurement at 5Vin and 16Vin while the load was 80mA on the 18Vout and the 5V and 3.3V unloaded.

The crossover frequency and phase margin was:

@ 4.5Vin: Fco = 4.9 KHz, Phase margin = 70.64 deg.

@ 16Vin: Fco = 14 KHz, Phase margin = 44.12 deg.



8. Thermal Analysis

The image and table below describe the thermal behavior of the board, supplied at 4.5V_{in} for the upper image and at 16V_{in} for the bottom one. The thermal shots have been taken 20 minutes after power on, and the board has been placed horizontal on the bench.

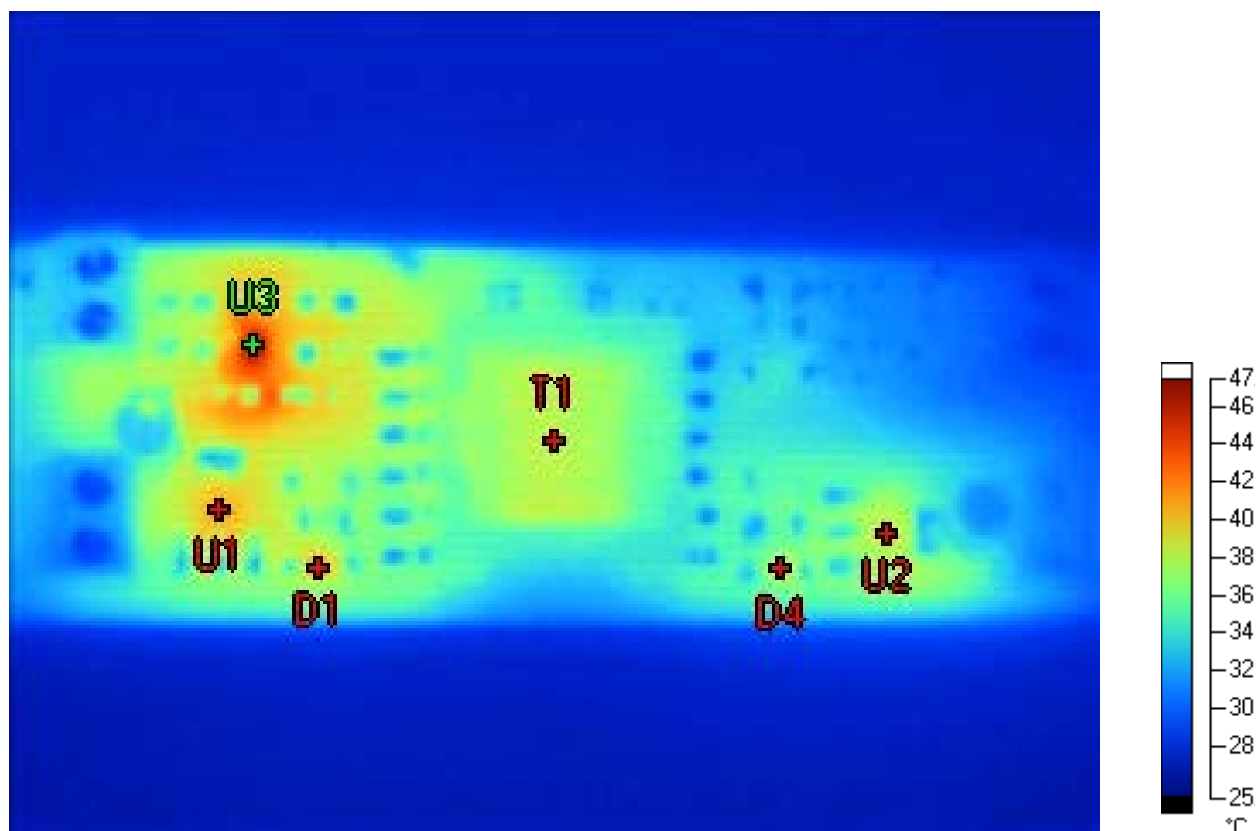


Image Info

Average Temperature	30.5 °C
Camera Model	Ti40FT
Image Range	26.3 °C to 46.5 °C
Image Time	11/22/2012 12:41:31 PM
Manufacturer	Fluke
Camera Serial Number	Ti40FT-070263

Markers

Label	Temperature	Emissivity	Background
U3	45.8 °C	0.95	25.0 °C
T1	38.0 °C	0.95	25.0 °C
U1	40.3 °C	0.95	25.0 °C
D1	40.0 °C	0.95	25.0 °C
D4	37.5 °C	0.95	25.0 °C
U2	38.4 °C	0.95	25.0 °C

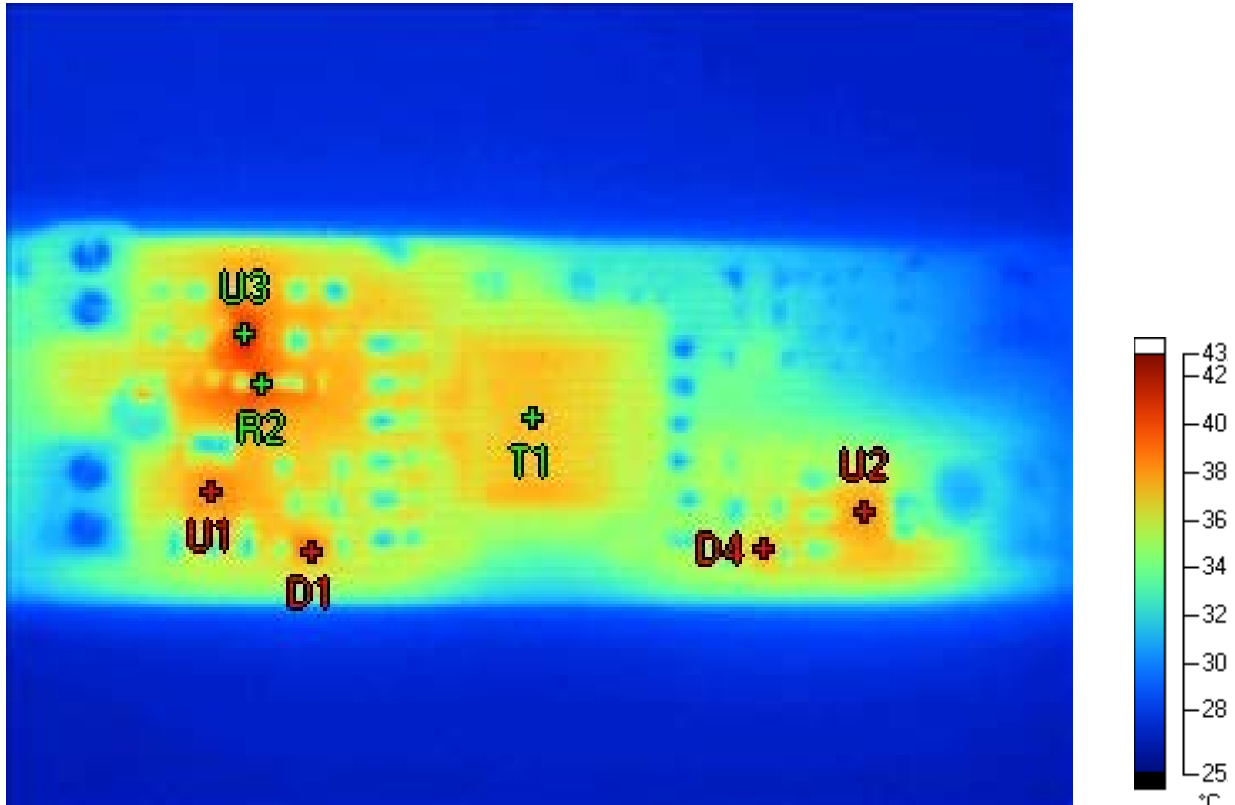


Image Info

Average Temperature	30.4 °C
Camera Model	Ti40FT
Image Range	26.3 °C to 41.8 °C
Image Time	11/22/2012 12:42:45 PM
Manufacturer	Fluke
Camera Serial Number	Ti40FT-070263

Markers

Label	Temperature	Emissivity	Background
U3	41.3 °C	0.95	25.0 °C
R2	41.8 °C	0.95	25.0 °C
U1	38.3 °C	0.95	25.0 °C
D1	38.9 °C	0.95	25.0 °C
T1	37.1 °C	0.95	25.0 °C
D4	37.8 °C	0.95	25.0 °C
U2	38.1 °C	0.95	25.0 °C

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