



ABSTRACT

The TPSI2140Q1EVM helps designers evaluate the operation and performance of the TPSI2140-Q1. This user's guide provides the connectors, test point descriptions, operational modes, schematic, bill of materials, and board layout of the EVM. The TPSI2140-Q1 is a 3.75-kV_{rms} reinforced isolated switch driver. The inputs and output connections to the board are terminal blocks, which allow for easily wired connections. The TPSI2140Q1EVM contains multiple test points for monitoring the TPSI2140-Q1 functionality.





 WARNING	<p>Danger</p>	<p>Do not use EVM to test Isolation above $V_{IOWM} = 1414-V_{DC}$ High voltage</p>
	<p>Caution</p>	<p>Caution hot surface Contact can cause burns Do not touch!</p>
	<p>Caution</p>	<p>Read the user's guide before use</p>
	<p>Caution</p>	<p>Do not leave EVM powered when unattended</p>

Table of Contents

General Texas Instruments High Voltage Evaluation (TI HV EMV) User Safety Guidelines.....	2
1 Introduction.....	4
1.1 Features.....	4
1.2 Applications.....	4
1.3 Description.....	4
2 Connection Descriptions.....	6
3 Test Equipment.....	7
4 Recommended Test Setup.....	8
4.1 Waveforms.....	8
4.2 S2 Voltage Divider.....	9
5 Schematic.....	10
6 PCB Layout.....	11
7 Bill of Materials.....	12

Trademarks

All trademarks are the property of their respective owners.

General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines



Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center [http://ti.com/customer support](http://ti.com/customer-support) for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety:
 - a. Keep work area clean and orderly.
 - b. Qualified observer(s) must be present anytime circuits are energized.
 - c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
 - d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
 - e. Use stable and non-conductive work surface.
 - f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:
 - a. As a precautionary measure, it is always good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
 - b. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
 - c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
 - d. Once EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety

- a. Wear personal protective equipment e.g. latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

1 Introduction

The TPSI2140-Q1 is an isolated solid state relay designed for high voltage automotive and industrial applications such as battery management systems, EV/HEV onboard chargers, mechanical relay replacement, DC link pre-charging, and more. The TPSI2140-Q1 seamlessly replaces relays without need for a secondary side supply while leveraging unique isolation technology integrated in a compact SOIC package. The entire primary side of the device requires only 5 mA of input current, enabling the user to drive the VDD and EN pins from a single microcontroller GPIO and eliminating the need for an external low side switch used in Photomos solutions. The secondary side consists of back-to-back MOSFETs with a standoff voltage of ± 1.4 kV from S1 to S2. The TPSI2140-Q1 MOSFETs' avalanche robustness and thermally conscious package design allow it to survive system level High Potential (HiPot) screening and DC fast charger surge currents of up to 2 mA without requiring any external components.

1.1 Features

- Reinforced isolation: 3.75 kVRMS
- Integrated avalanche rated MOSFETs with 1400-V standoff voltage
- Qualified for automotive applications: AEC-Q100
- Low primary side supply current, 5-mA ON state, 1- μ A OFF state
- Test points available for every pin and voltage supply to ensure correct functionality

1.2 Applications

- HEV/EV insulation resistance monitoring
- Solar inverter
- Industrial motor drive
- Battery management system
- Onboard charger

1.3 Description

The TPSI2140Q1EVM is a two-copper layer board containing multiple test points and jumpers in order to fully evaluate the functionality of the device. The primary side consists of four differential drivers which deliver power and enable logic information to each of the internal MOSFETs on the secondary side. Each MOSFET on the secondary side has a dedicated full-bridge rectifier to form its local power supply. When the enable pin is brought HI, the oscillator starts and the drivers send power and a logic HI across the barrier. The avalanche robust MOSFETs and the thermal benefits of the widened pins on the 11 DWQ package enable the TPSI2140-Q1 to withstand High Potential (HiPot) screening and DC fast charger surge currents of up to 2 mA without requiring any external protection components.

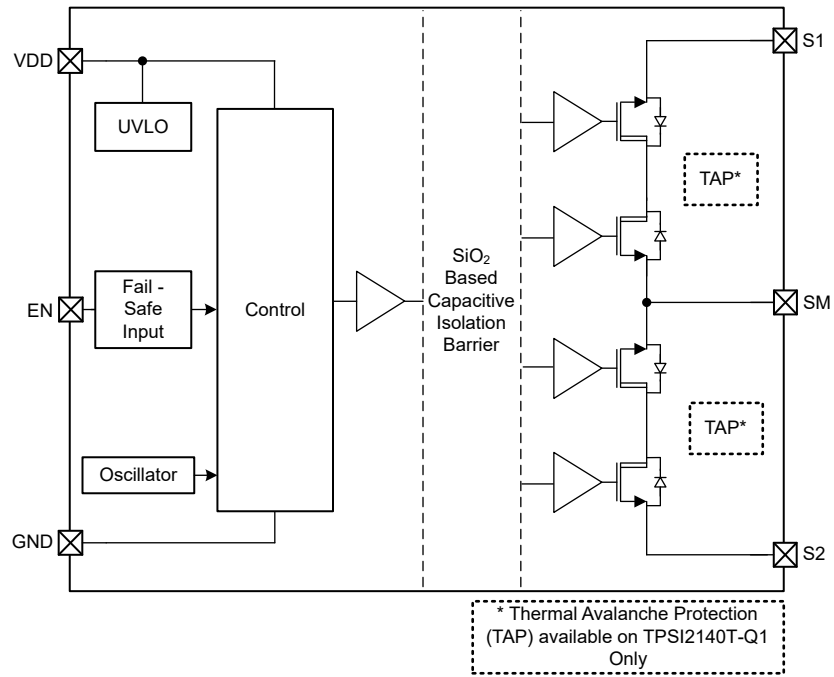


Figure 1-1. TPSI2140-Q1 Functional Block Diagram

Table 1-1. Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPSI2140-Q1	SOIC 11 pin (DWQ)	10.3 mm × 7.5 mm

2 Connection Descriptions

Table 2-1 shows an overview of the input/output connectors. Table 2-2 shows the test points and jumpers.

Table 2-1. Input and Output Connector Descriptions

Connector	Label	Description
J1	HV+	Secondary side positive input
J2	S2	Voltage sense output
J3	HV-	Secondary side negative input
J4	VDD	Primary Side supply
J5	GND	Primary Side GND
J6	EN_EXT	External Enable signal

Table 2-2. Test Point and Jumper Descriptions

Test Point, Jumper	Label	Description
TP1	VDD	Primary side supply test point
TP2	EN	EN test point
TP3, TP4	GND	Primary side ground test point
TP5	S1	Secondary side HV+ voltage after resistor chain
TP6	SM	Thermal Pin,
TP7	S2	Voltage sense output test point
TP8	HV-	HV- secondary side test point
TP11, TP14	GND2	Secondary side ground
TP13	SM	TBD
J7	VDD/EN/EN_EXT	Connects VDD to EN, or EN to EN_EXT. Allows for external enable signal to be used instead of EN being signaled by VDD

3 Test Equipment

The testing of the TPSI2140Q1EVM recommends the following equipment:

- Adjustable power supplies for the input
- Oscilloscope
- A function generator to toggle the EN pin

4 Recommended Test Setup

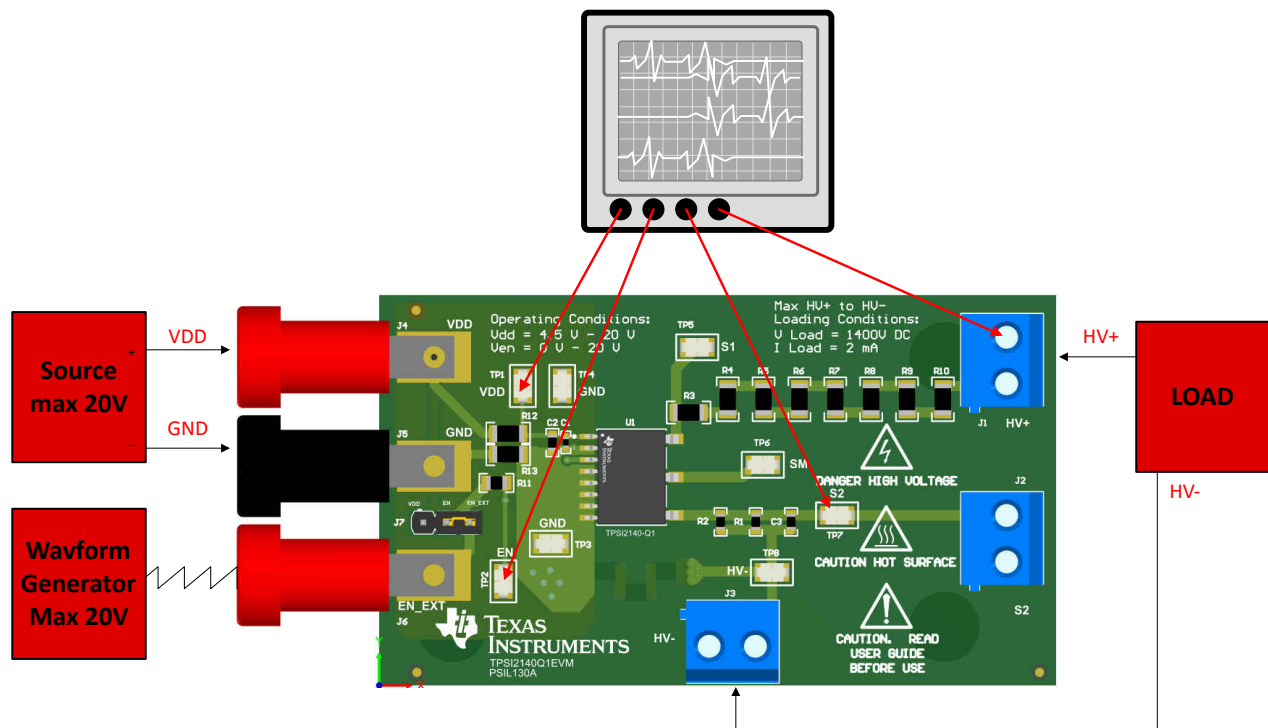


Figure 4-1. TPSI2140Q1EVM Test Setup

Ensure that the TPSI2140Q1EVM has the following setting on the jumpers:

1. J7 – Shunt is connecting EN and EN_EXT
2. If not using a waveform generator as shown above, set the shunt to be between VDD and EN. This action causes the enable signal to be on if the device is on.

4.1 Waveforms

If connected as described above, the following channels must be displayed in the waveforms below:

- CH 3 = VDD
- CH 2 = EN
- CH 1 = HV+
- CH 4 = S2

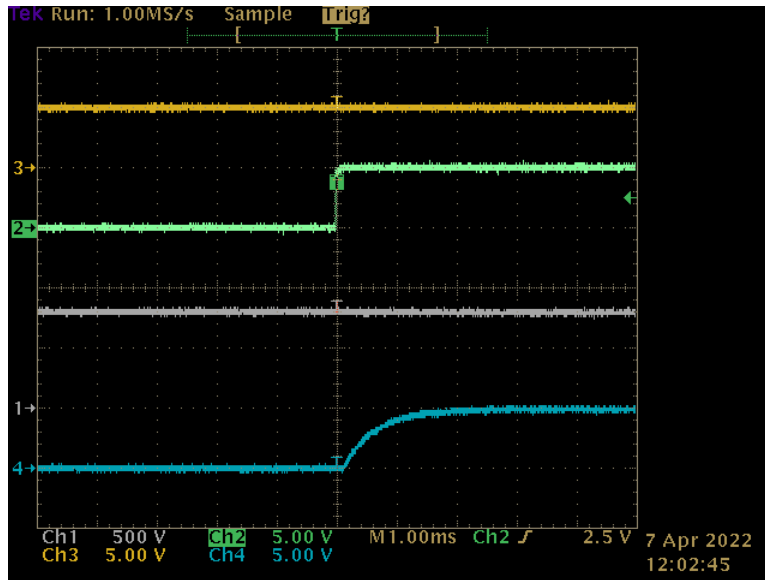


Figure 4-2. Enable On

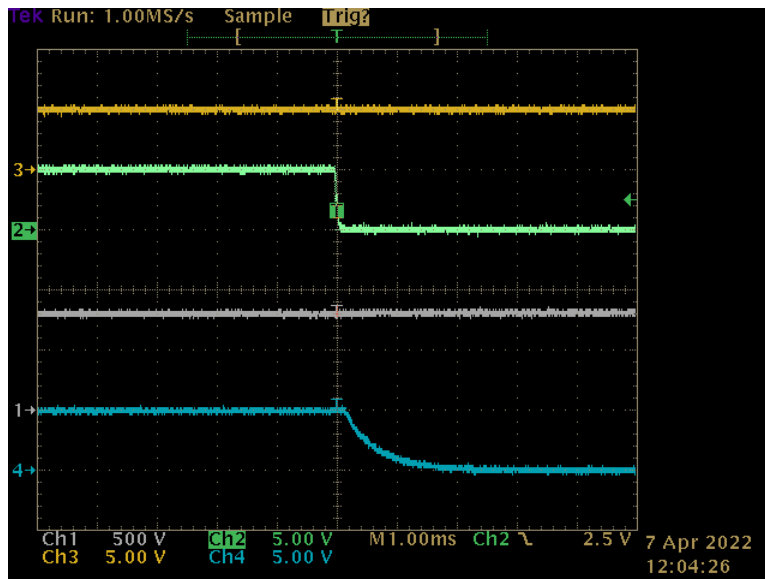


Figure 4-3. Enable Off

4.2 S2 Voltage Divider

S2 (TP7) will be the voltage divider measurement. The voltage measured is dependent on parallel resistors R1 and R2, and the resistor network R3-R10. It can be calculated by the following equation:

$$V_{S2} = \frac{R1 || R2}{(R3 + R4 \dots + R10) + (R1 || R2)} \times V_{LOAD} \quad (1)$$

5 Schematic

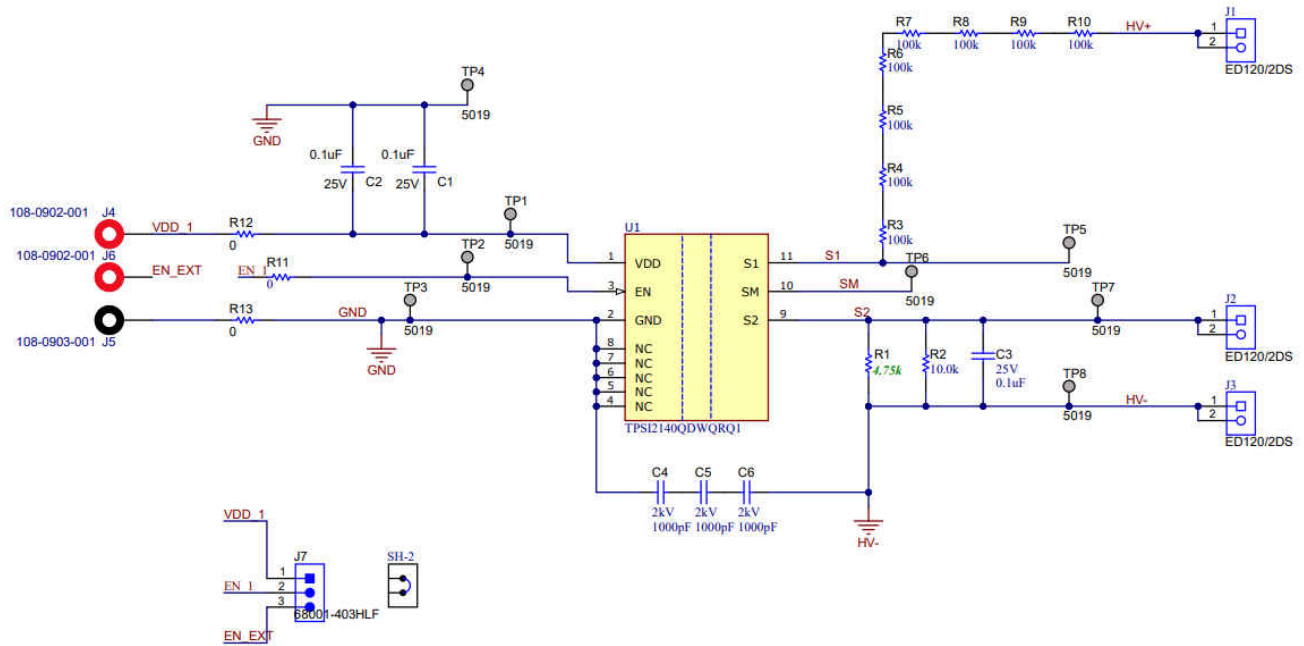


Figure 5-1. TPSI2140Q1EVM Schematic

6 PCB Layout

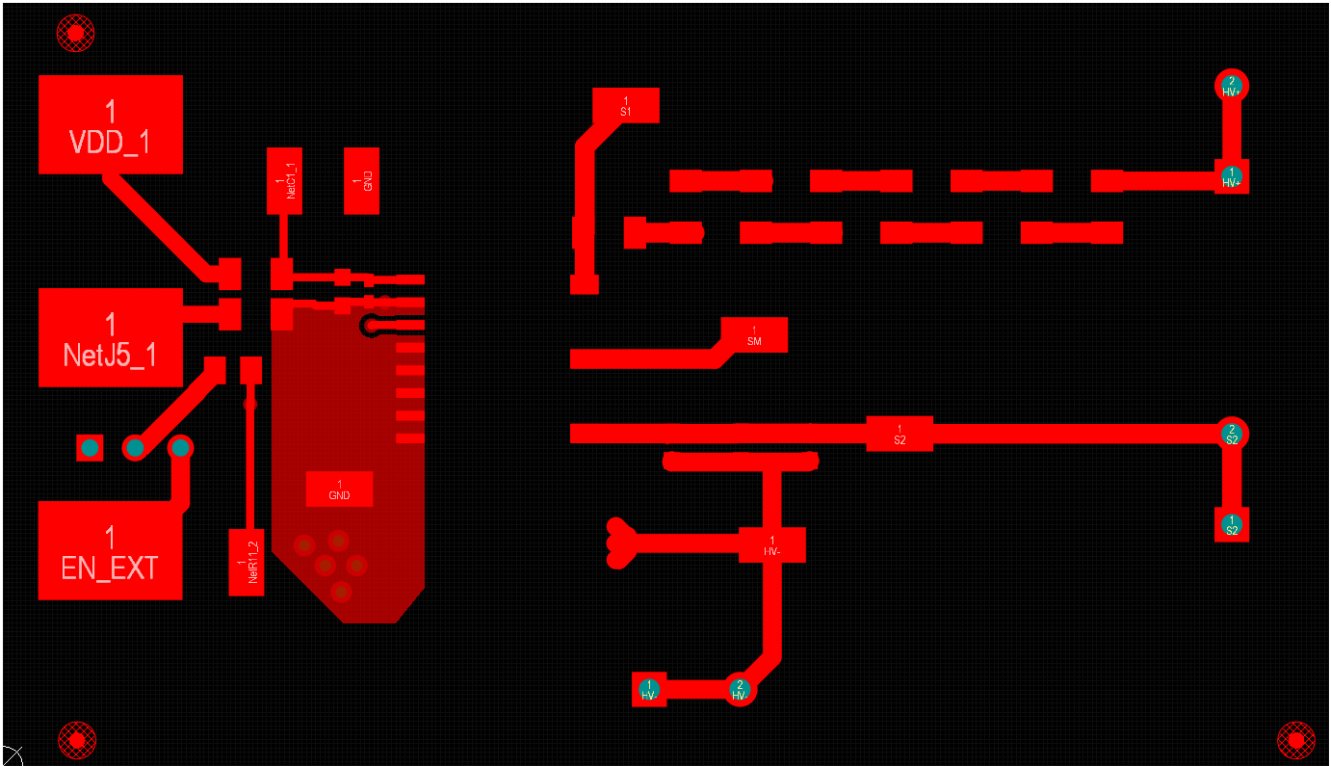


Figure 6-1. TPSI2140Q1EVM Top Layer

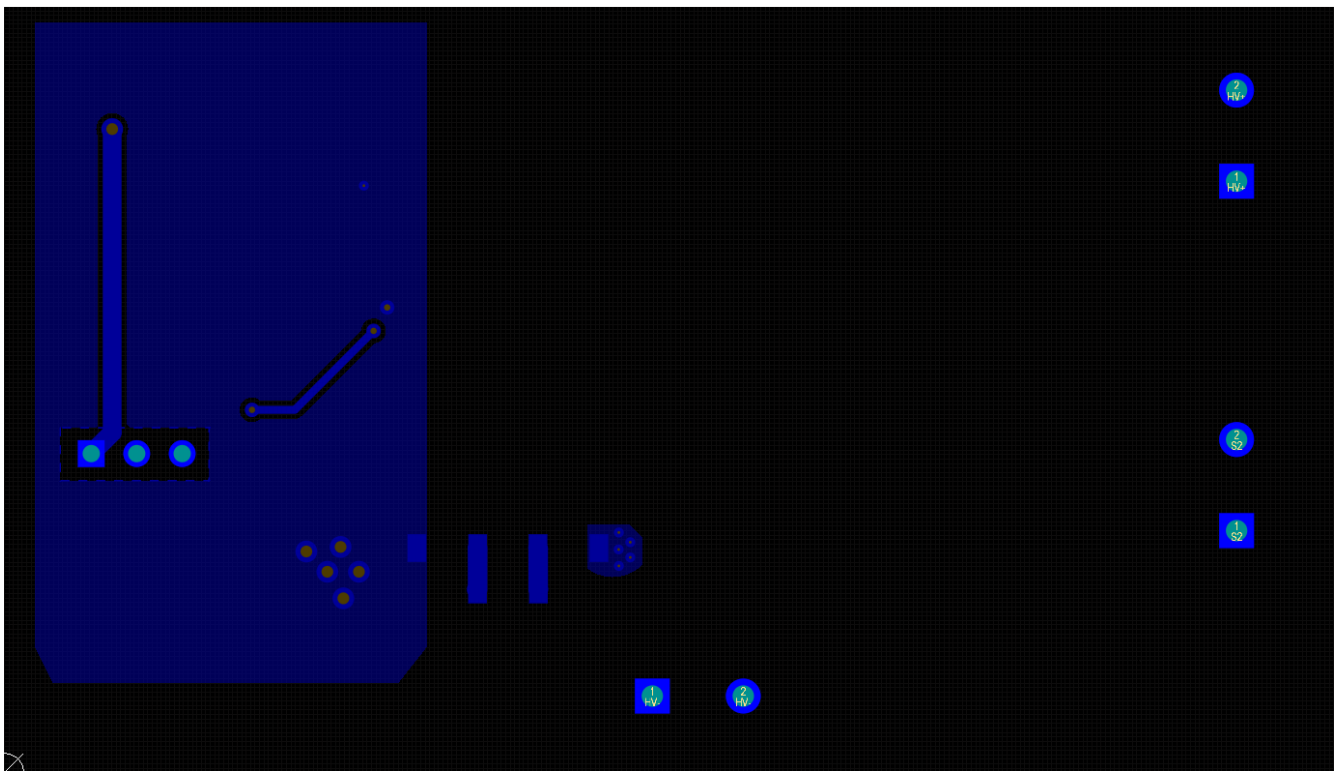


Figure 6-2. TPSI2140Q1EVM Bottom Layer

7 Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
PCB	1		Printed Circuit Board		PSIL130	Any
C1	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402	402	GRM155R71E104KE14D	MuRata
C2	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E2X7R1E104K080A A	TDK
C3	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	603	C0603C104K3RACTU	Kemet
C4, C5, C6	3	1000pF	CAP, CERM, 1000 pF, 2000 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206	C1206C102KGRACAUTO	Kemet
H1, H2, H3, H4	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J1, J2, J3	3		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J4, J6	2		Banana Jack Insul Nylon Red, TH	Banana Jack Insul Nylon Red, TH	108-0902-001	Cinch Connectivity
J5	1		Banana Jack Insul Nylon Black, TH	Banana Jack Insul Nylon Black, TH	108-0903-001	Cinch Connectivity
J7	1		Header, 2.54mm, 3x1, Tin, TH	Header, 2.54mm, 3x1, TH	68001-403HLF	FCI
R1, R2	2	10.0k	RES, 10.0 k, 0.1%, 0.1 W, 0603	603	RT0603BRD0710KL	Yageo America
R3, R4, R5, R6, R7, R8, R9	7	100k	RES, 100 k, 0.1%, 0.4 W, AEC-Q200 Grade 1, 1206	1206	TNPW1206100KBEEA	Vishay-Dale
R10	1	100k	RES, 100 k, 0.1%, 0.25 W, AEC-Q200 Grade 1, 1206	1206	TNPW1206100KBEEA	Vishay-Dale
R11	1	0	RES, 0, 5%, 0.125 W, 0805	805	MCR10EZPJ000	Rohm
R12, R13	2	0	RES, 0, 5%, 0.25 W, 1206	1206	RC1206JR-070RL	Yageo America
SH-2	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	8		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		Isolated Solid State Relay	SOIC11	TPSI2140QDWQRQ1	Texas Instruments

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated