GC5018 Daughtercard

SLWU031 – February 2006

GC Studio Reference

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

IMPORTANT NOTICE

THE PRODUCTS ORDERED HEREUNDER ARE EXPERIMENTAL, DEVELOPMENTAL OR PROTOTYPE PRODUCTS. THE PRODUCT SPECIFICATIONS ARE PRELIMINARY & SUBJECT TO CHANGE WITHOUT NOTICE. TI MAKES NO WARRANTY, EITHER EXPRESSED, IMPLIED OR STATUTORY, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A SPECIFIC PURPOSE, AS TO THESE PRODUCTS AND TI DOES NOT REPRESENT THAT A FINAL PRODUCTION VERSION WILL BE SOLD BY TI.

Contents

1. GC5018 Daughtercard and GC101 EVM Setup

The GC5018 daughtercard combined with the GC101 motherboard provide a hardware evaluation platform for development of application specific settings for the GC5018. To operate the system, simply plug the GC5018 daughtercard into the DIMM socket on the GC101 motherboard, connect the parallel port interface cable to the GC101 and Host Computer (PC), and connect the power supply to the GC101.

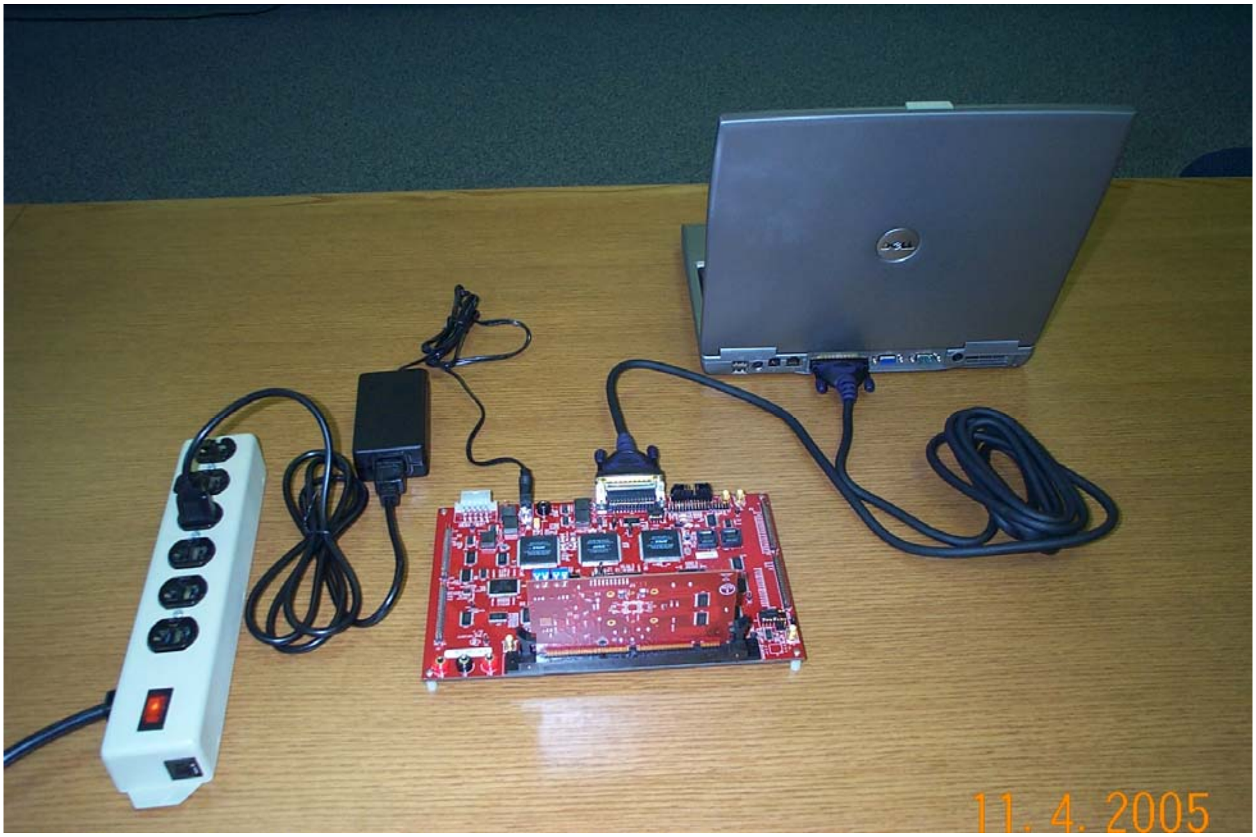


Figure 1. GC101 EVM and GC5018 Daughtercard

2. GC Studio and the GC5018/GC101 Evaluation Hardware

GC Studio includes a software “plug-in” to control the GC101 motherboard, GC5018 daughtercard and the GC5018 device. Input data from a text file on the host computer (PC) is loaded into the GC101 input memory and used to stimulate the GC5018 input ports. Output data from the GC5018 is captured in the GC101 capture memory and transferred to the host computer. GC Studio configures the GC5018 internal registers using the interactive GUI.

Several GC Studio projects for the GC5018 are included in the installation. These projects can be used as the starting point for creating new experiments as desired.

2.1. GC Studio Installation

2.1.1. Required Elements

GC101 evaluation motherboard, the external 5V power supply for the GC101 and a ECP parallel port enhanced speed cable.

GC Studio software, downloaded or provided on a CD

GC5018 Rev B or Rev C daughtercard

Host Computer (PC) with BIOS supporting ECP mode for LPT1, running Win98 Rel 2, WinME, Win2000 SP1, WinXP Home or WinXP Professional.

Administrator Group Privileges

2.1.2. GC Studio Installation Instructions

Locate the “GC Studio_Setup.exe” file on the CD or in the downloaded location on the host computer and double click on it to install.

2.2. GC Studio Projects

Several projects (sometimes referred to as experiments) are provided for the GC5018 in the GC Studio release. Users can execute these existing projects and create and save new projects using the GC Studio GUI interface.

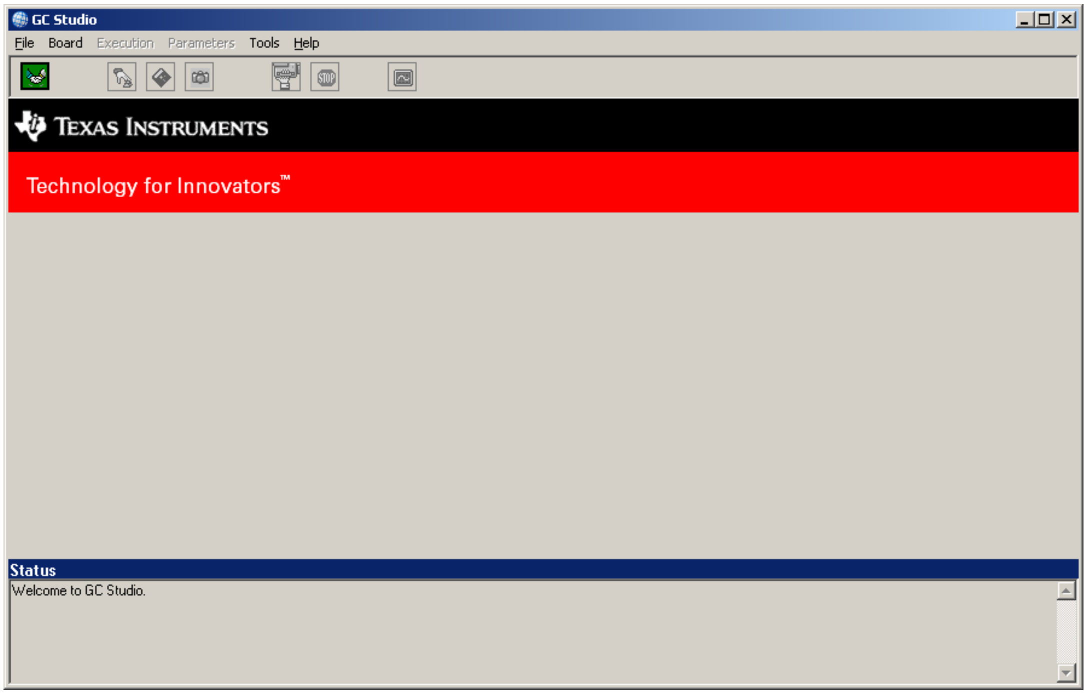
GC Studio will come with Example files, and if modifying those, it is suggested to save the new file under different name from the original one.

2.2.1. Creating a New GC Studio Project for a UMTS Configuration

For this example, the new project will configure the GC5018 to process a UMTS signal. The GC5018 configuration details are as follows:

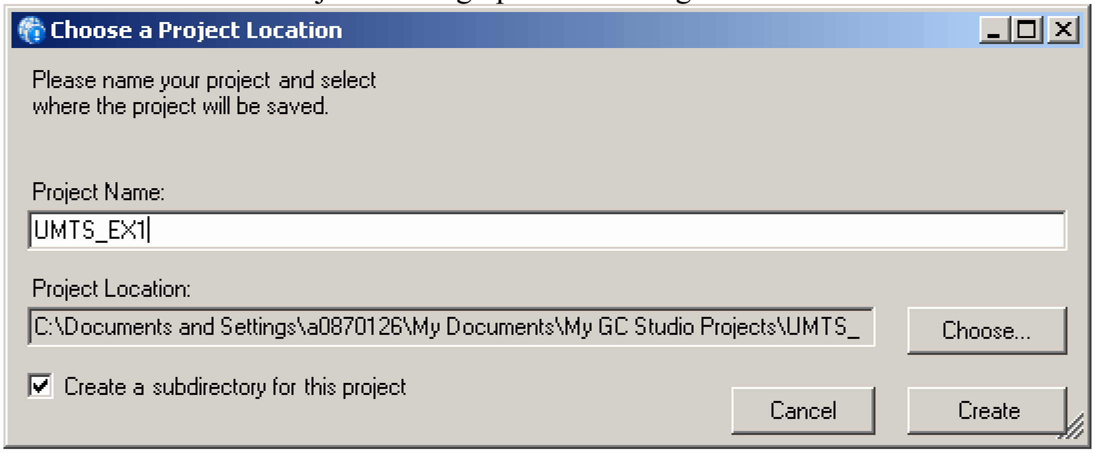
- A single real UMTS carrier is applied to the GC5018 rxin_a inputs with a simulated sample rate of 76.8Msps and an IF frequency of 19.2MHz.
- Simulated rxclk to the gc5018 is 153.6MHz
- Receive FIFOs are enabled
- Receive AGC is bypassed
- Receive Channel 0 is configured to process the signal
- The mixer/nco shifts the real 19.2MHz IF to a complex signal centered at DC.
- The DC centered signal is zero stuffed to increase the rate from 76.8Msps to 153.6Msps. This is required, as the CIC uses only full rxclk rate input signals.
- The CIC filter is programmed to decimate by 10 using a m=2 comb section configuration. The output sample rate at the CIC output is 15.36Msps
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 40 tap filter, which is the maximum length that can be computed with rxclk at 153.6MHz and the CFIR output rate of 7.68Msps.
- The 64 tap PFIR provides final symbol shaping and filtering.
- Channel AGC is configured as fixed unity gain
- Baseband data is transmitted and captured using the serial interface at the full rxclk rate.

Start GC Studio



Welcome to GC Studio.

Click on File > New Project to bring up the following window.



Please name your project and select where the project will be saved.

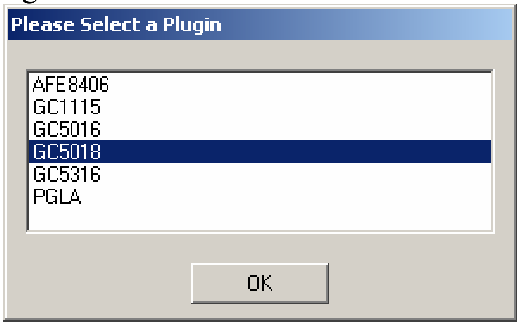
Project Name:
UMTS_EX1

Project Location:
C:\Documents and Settings\a0870126\My Documents\My GC Studio Projects\UMTS_

☑ Create a subdirectory for this project

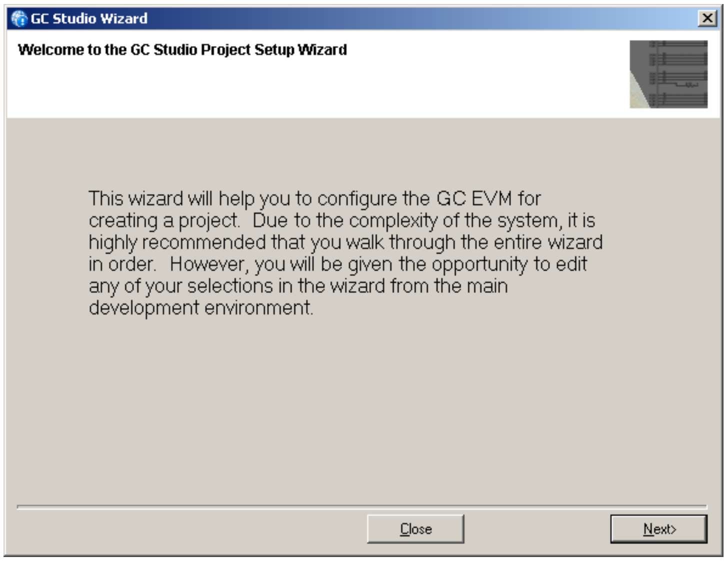
Choose a name for this new project, and click create.

Select GC5018 for the Plugin and click OK. Click next on the following pop-up.



Please Select a Plugin

AFE8406
GC1115
GC5016
GC5018
GC5316
PGLA

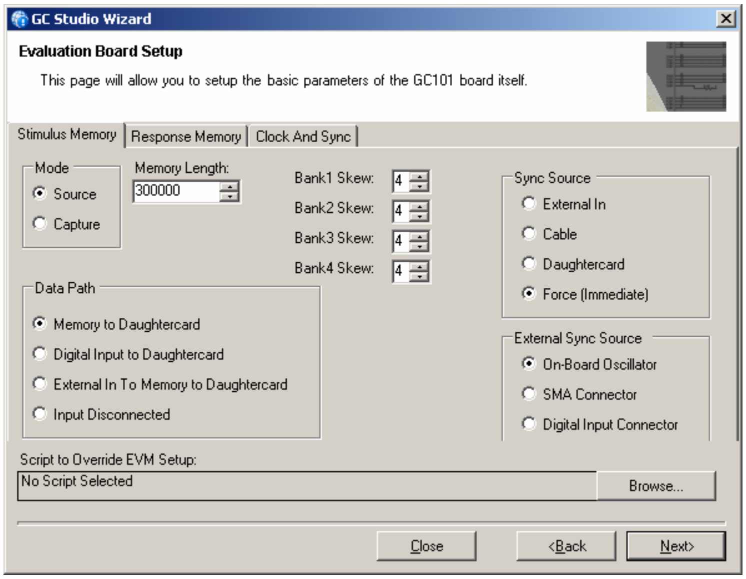


GC Studio Wizard

Welcome to the GC Studio Project Setup Wizard

This wizard will help you to configure the GC EVM for creating a project. Due to the complexity of the system, it is highly recommended that you walk through the entire wizard in order. However, you will be given the opportunity to edit any of your selections in the wizard from the main development environment.

Using the wizard style interface, setup the GC101 evaluation board, then click next. The memory length should be set to “N” frames of data (300000 is the default value).



GC Studio Wizard

Evaluation Board Setup

This page will allow you to setup the basic parameters of the GC101 board itself.

Mode
● Source
○ Capture

Memory Length: 300000

Bank1 Skew: 4
Bank2 Skew: 4
Bank3 Skew: 4
Bank4 Skew: 4

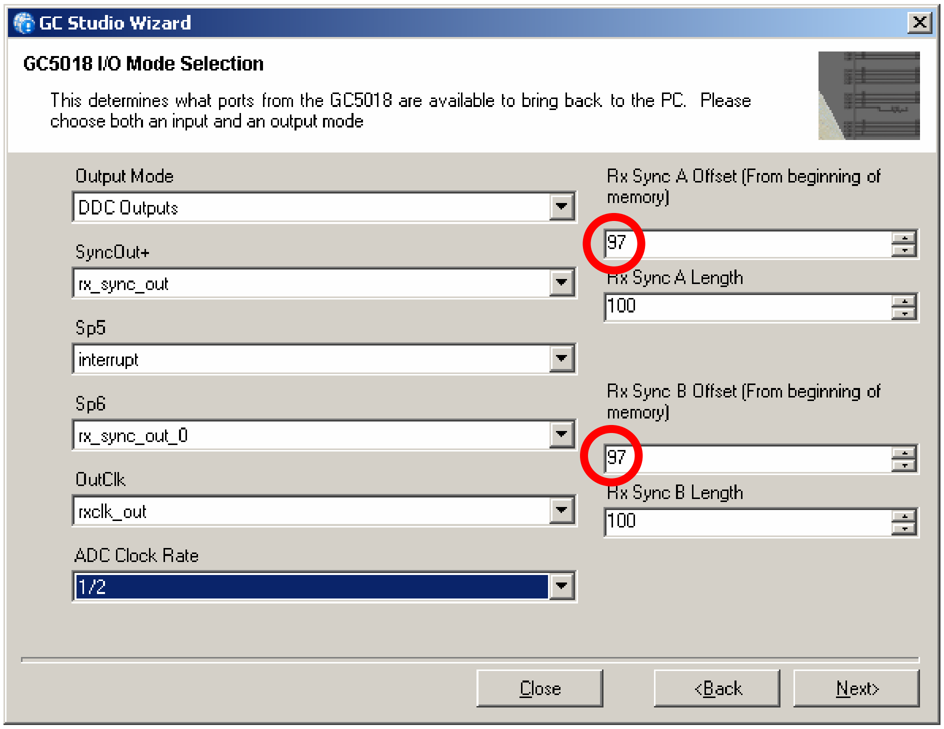
Sync Source
○ External In
○ Cable
○ Daughtercard
● Force (Immediate)

Data Path
● Memory to Daughtercard
○ Digital Input to Daughtercard
○ External In To Memory to Daughtercard
○ Input Disconnected

External Sync Source
● On-Board Oscillator
○ SMA Connector
○ Digital Input Connector

Script to Override EVM Setup: No Script Selected

Setup the GC5018 I/O mode selection as shown and click next. In this example, be sure the ADC clock rate is set to ½. The parameters on the right tell the capture when the data is valid and how long the SYNC is. The top parameter (circled in red below) should match the length of the capture memory, or be longer.



GC Studio Wizard

GC5018 I/O Mode Selection

This determines what ports from the GC5018 are available to bring back to the PC. Please choose both an input and an output mode

Output Mode: DDC Outputs

SyncOut+: rx_sync_out

Sp5: interrupt

Sp6: rx_sync_out_0

OutClk: rxclk_out

ADC Clock Rate: 1/2

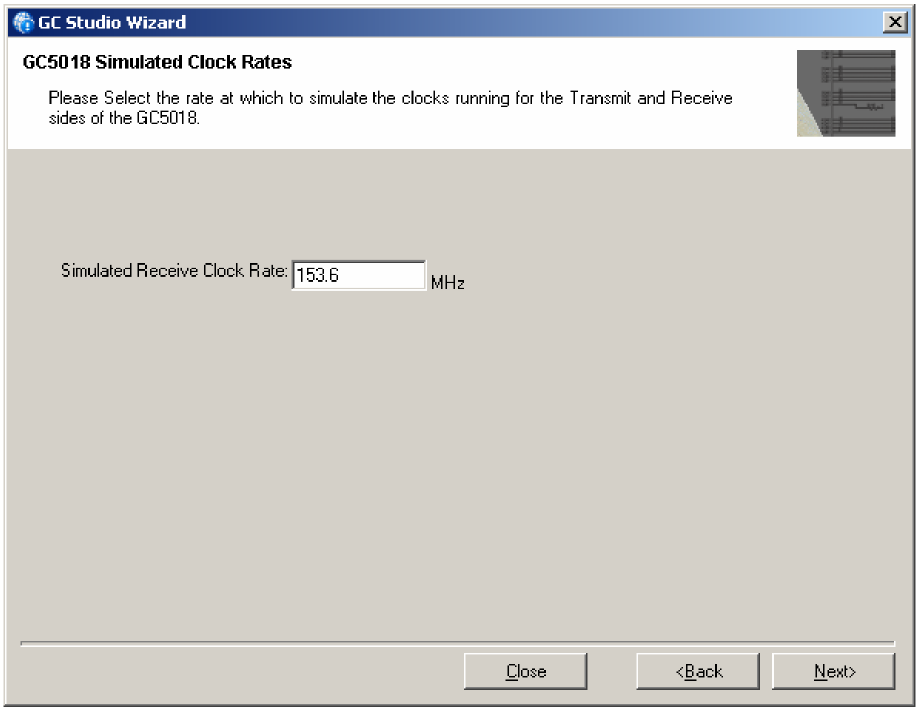
Rx Sync A Offset (From beginning of memory): 97

Rx Sync A Length: 100

Rx Sync B Offset (From beginning of memory): 97

Rx Sync B Length: 100

Set the simulated clock rate to 153.6MHz and click next.

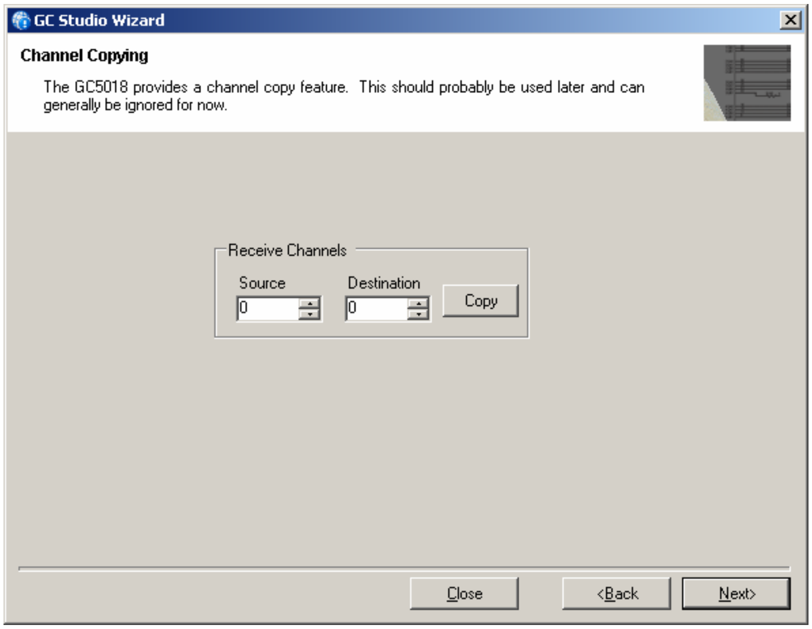


GC Studio Wizard

GC5018 Simulated Clock Rates

Please Select the rate at which to simulate the clocks running for the Transmit and Receive sides of the GC5018.

Simulated Receive Clock Rate: 153.6 MHz


GC Studio Wizard

Channel Copying

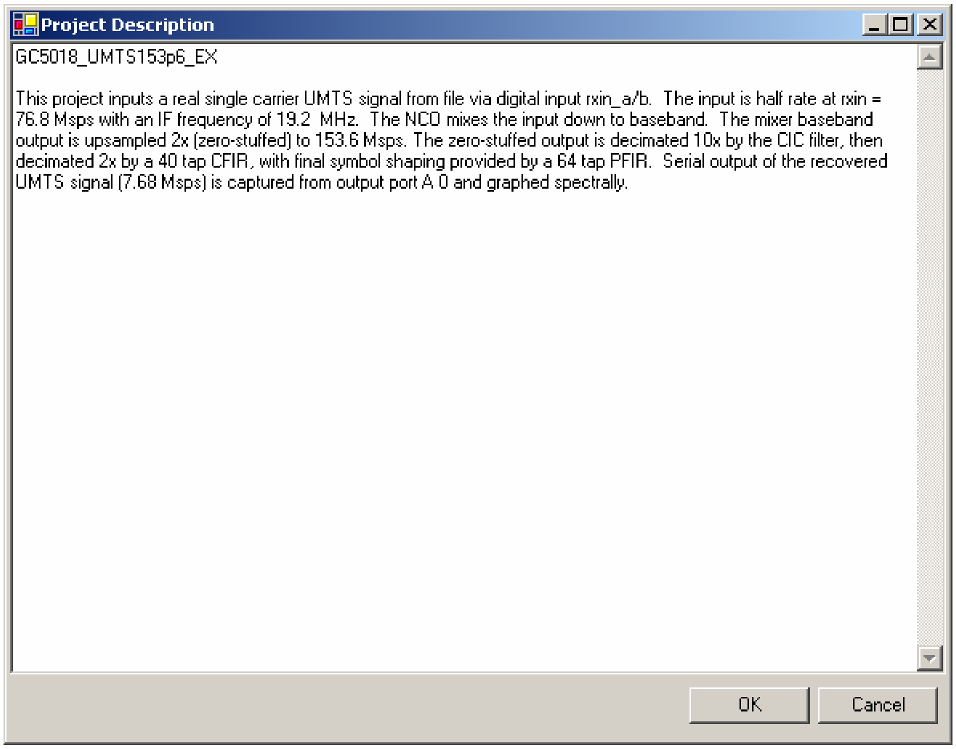
The GC5018 provides a channel copy feature. This should probably be used later and can generally be ignored for now.

Receive Channels

Source: 0

Destination: 0

Channel Copying will be skipped for now, click Next.


Project Description

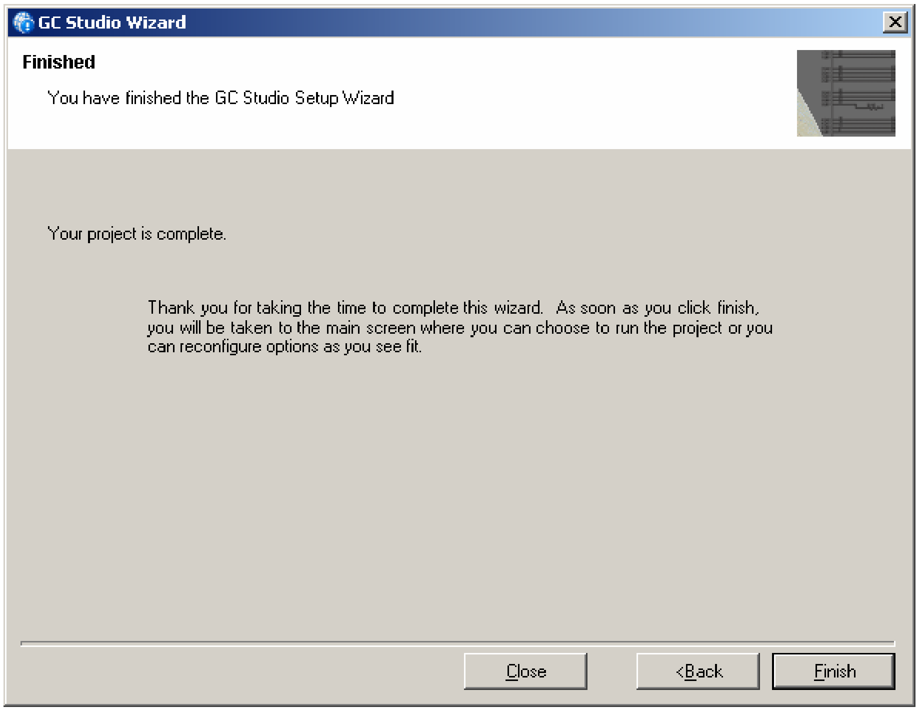
GC5018_UMTS153p6_EX

This project inputs a real single carrier UMTS signal from file via digital input rxin_a/b. The input is half rate at rxin = 76.8 Msps with an IF frequency of 19.2 MHz. The NCO mixes the input down to baseband. The mixer baseband output is upsampled 2x (zero-stuffed) to 153.6 Msps. The zero-stuffed output is decimated 10x by the CIC filter, then decimated 2x by a 40 tap CFIR, with final symbol shaping provided by a 64 tap PFIR. Serial output of the recovered UMTS signal (7.68 Msps) is captured from output port A 0 and graphed spectrally.

Project Description allows user to briefly describe the project details and will appear every time the project is selected for loading.

Click Next.

Click Finish.



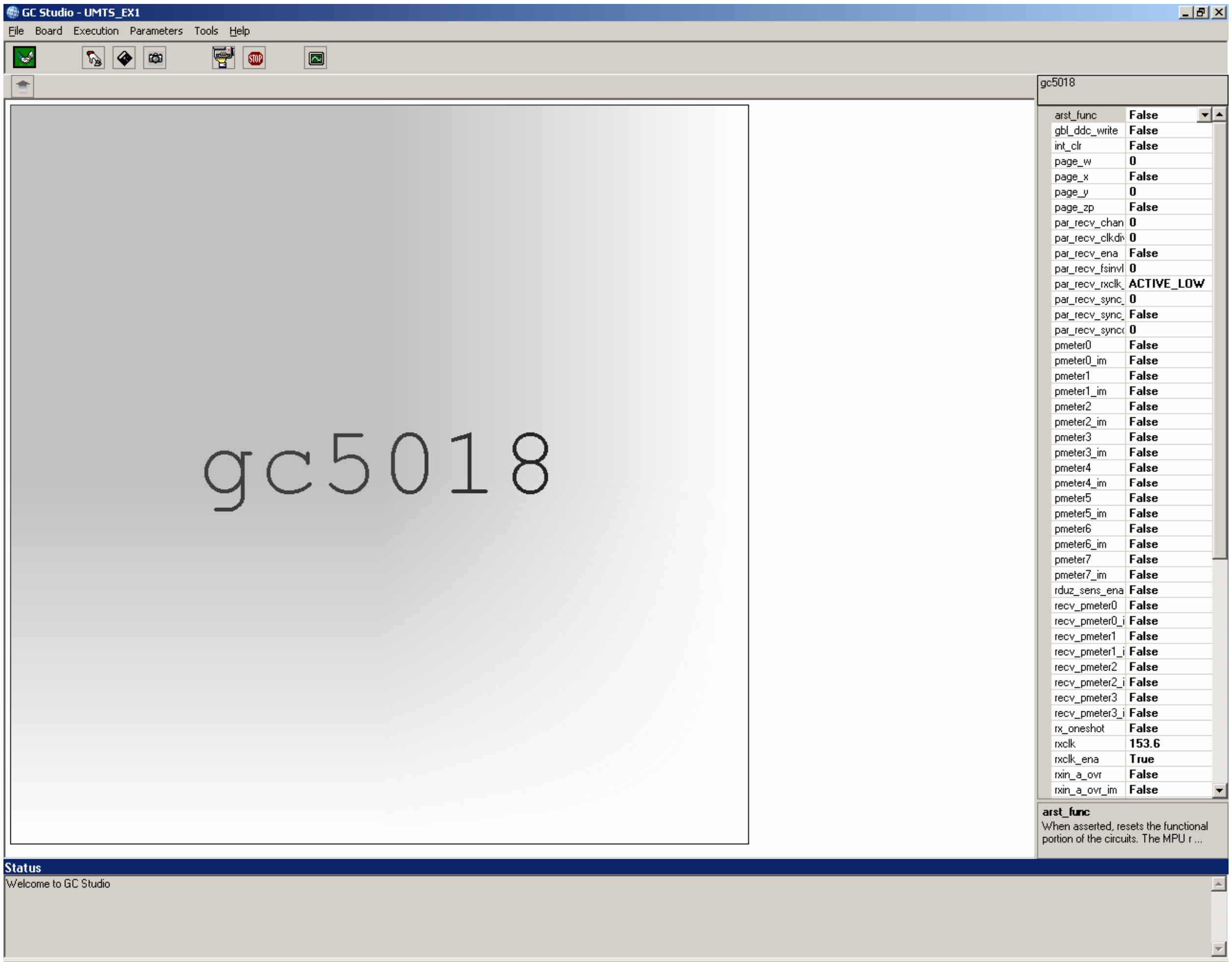
Finished

You have finished the GC Studio Setup Wizard

Your project is complete.

Thank you for taking the time to complete this wizard. As soon as you click finish, you will be taken to the main screen where you can choose to run the project or you can reconfigure options as you see fit.

Click on the large gc5018 box to display the global control registers.



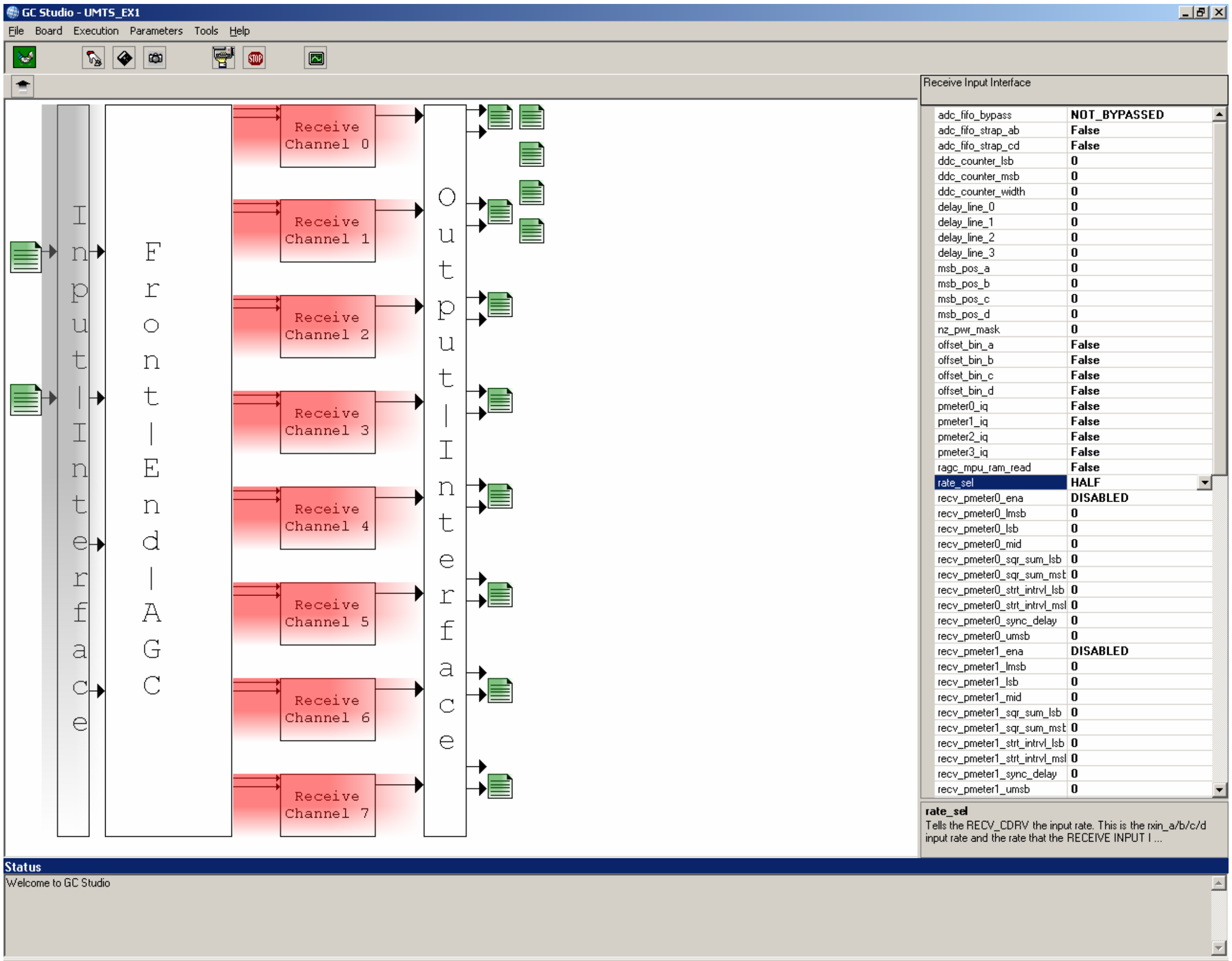
gc5018

arst_func	False
gbl_ddc_write	False
int_clr	False
page_w	0
page_x	False
page_y	0
page_zp	False
par_recv_chan	0
par_recv_clkdiv	0
par_recv_ena	False
par_recv_fsinvl	0
par_recv_rxclk_	ACTIVE_LOW
par_recv_sync_	0
par_recv_sync_	False
par_recv_syncc	0
pmeter0	False
pmeter0_im	False
pmeter1	False
pmeter1_im	False
pmeter2	False
pmeter2_im	False
pmeter3	False
pmeter3_im	False
pmeter4	False
pmeter4_im	False
pmeter5	False
pmeter5_im	False
pmeter6	False
pmeter6_im	False
pmeter7	False
pmeter7_im	False
rduz_sens_ena	False
recv_pmeter0	False
recv_pmeter0_i	False
recv_pmeter1	False
recv_pmeter1_i	False
recv_pmeter2	False
recv_pmeter2_i	False
recv_pmeter3	False
recv_pmeter3_i	False
rx_oneshot	False
rxclk	153.6
rxclk_ena	True
rxin_a_ovr	False
rxin_a_ovr_im	False

arst_func
When asserted, resets the functional portion of the circuits. The MPU r ...

Welcome to GC Studio

Next, double click on the gc5018 block to “push down” one level into the gc5018.
This level contains the blocks of: Input Data File, Input Interface, Front End AGC, Eight Receive Channels, Output interface and Output Data Files.
Click on the Input Interface block to display and edit the receive input interface registers.
Set rate_sel to half; this will configure the GC5018 for input samples at ½ the rxclk rate.
Set adc_fifo_bypass to NOT BYPASSED to enable the rxin_a/b/c/d input FIFO circuits.
The input data format can be set to offset binary or twos complement.
Also, Receive Power Meters (Wideband Power Meters) are provided for the inputs and could be set according to the datasheet explanation. This example will not use Power Meter Functions.



Receive Input Interface

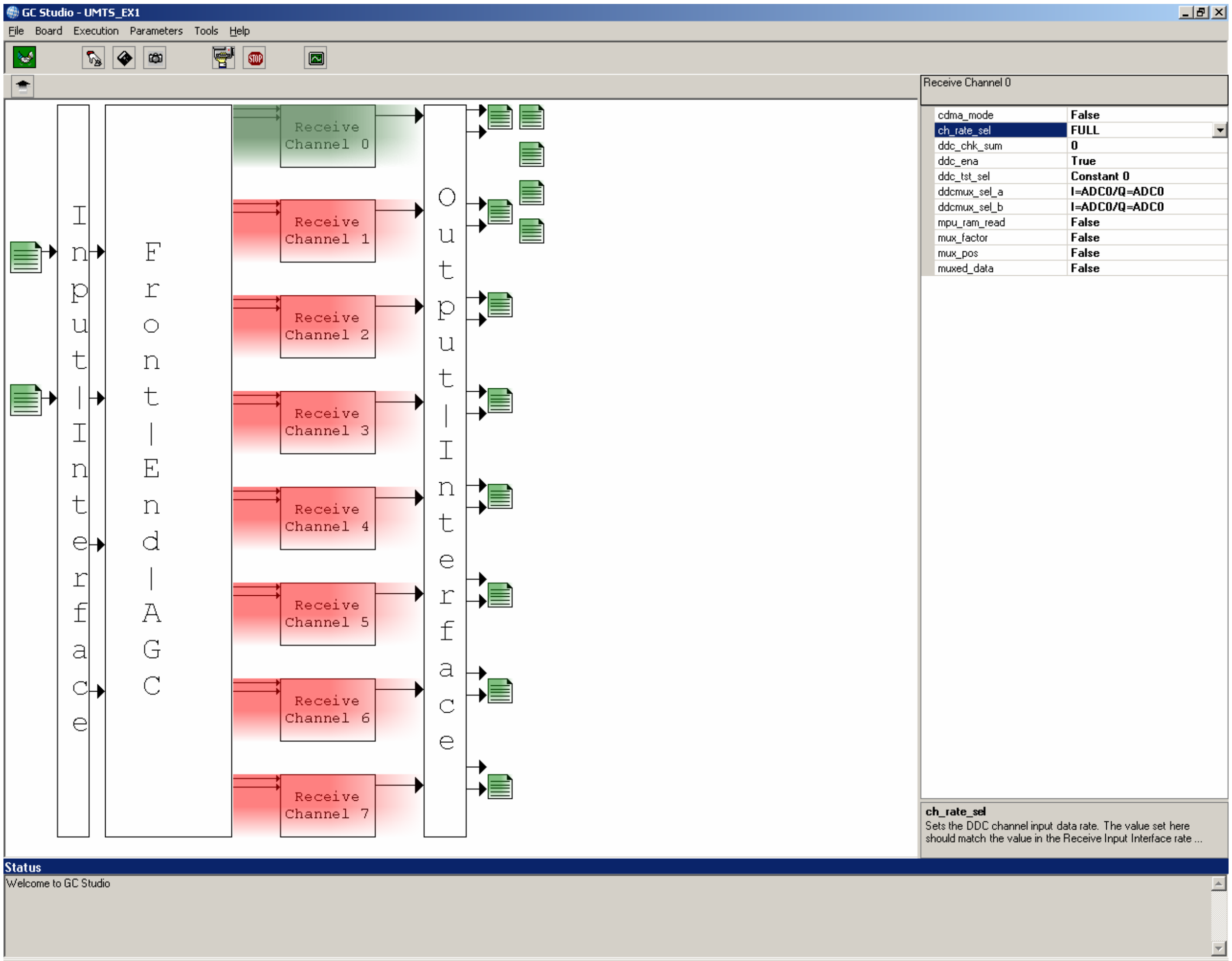
adc_fifo_bypass	NOT_BYPASSED
adc_fifo_strap_ab	False
adc_fifo_strap_cd	False
ddc_counter_lsb	0
ddc_counter_msb	0
ddc_counter_width	0
delay_line_0	0
delay_line_1	0
delay_line_2	0
delay_line_3	0
msb_pos_a	0
msb_pos_b	0
msb_pos_c	0
msb_pos_d	0
nz_pwr_mask	0
offset_bin_a	False
offset_bin_b	False
offset_bin_c	False
offset_bin_d	False
pmeter0_iq	False
pmeter1_iq	False
pmeter2_iq	False
pmeter3_iq	False
ragc_mpu_ram_read	False
rate_sel	HALF
recv_pmeter0_ena	DISABLED
recv_pmeter0_lmsb	0
recv_pmeter0_lsb	0
recv_pmeter0_mid	0
recv_pmeter0_sqr_sum_lsb	0
recv_pmeter0_sqr_sum_msb	0
recv_pmeter0_strt_intrvl_lsb	0
recv_pmeter0_strt_intrvl_msl	0
recv_pmeter0_sync_delay	0
recv_pmeter0_umsb	0
recv_pmeter1_ena	DISABLED
recv_pmeter1_lmsb	0
recv_pmeter1_lsb	0
recv_pmeter1_mid	0
recv_pmeter1_sqr_sum_lsb	0
recv_pmeter1_sqr_sum_msb	0
recv_pmeter1_strt_intrvl_lsb	0
recv_pmeter1_strt_intrvl_msl	0
recv_pmeter1_sync_delay	0
recv_pmeter1_umsb	0

rate_sel
Tells the RECV_CDRV the input rate. This is the rxin_a/b/c/d input rate and the rate that the RECEIVE INPUT I ...

Welcome to GC Studio

Front End AGC is not used in this example, and the function and parameters are discussed in the datasheet. An example file demonstrating the performance of the Front End AGC (RAGC) could be supplied upon request.

Click on the upper Receive Channel 0 block , the top most red block in the previous picture. Set ddc_ena to True. The top most receive channel will be changed to green since it has been enabled.
“cdma_mode” is set to FALSE, setting the channel for UMTS function. In this setting, the DDC can process 8 UMTS carriers.



Receive Channel 0

cdma_mode	False
ch_rate_sel	FULL
ddc_chk_sum	0
ddc_ena	True
ddc_tst_sel	Constant 0
ddcmux_sel_a	I=ADC0/Q=ADC0
ddcmux_sel_b	I=ADC0/Q=ADC0
mpu_ram_read	False
mux_factor	False
mux_pos	False
muxed_data	False

ch_rate_sel
Sets the DDC channel input data rate. The value set here should match the value in the Receive Input Interface rate ...

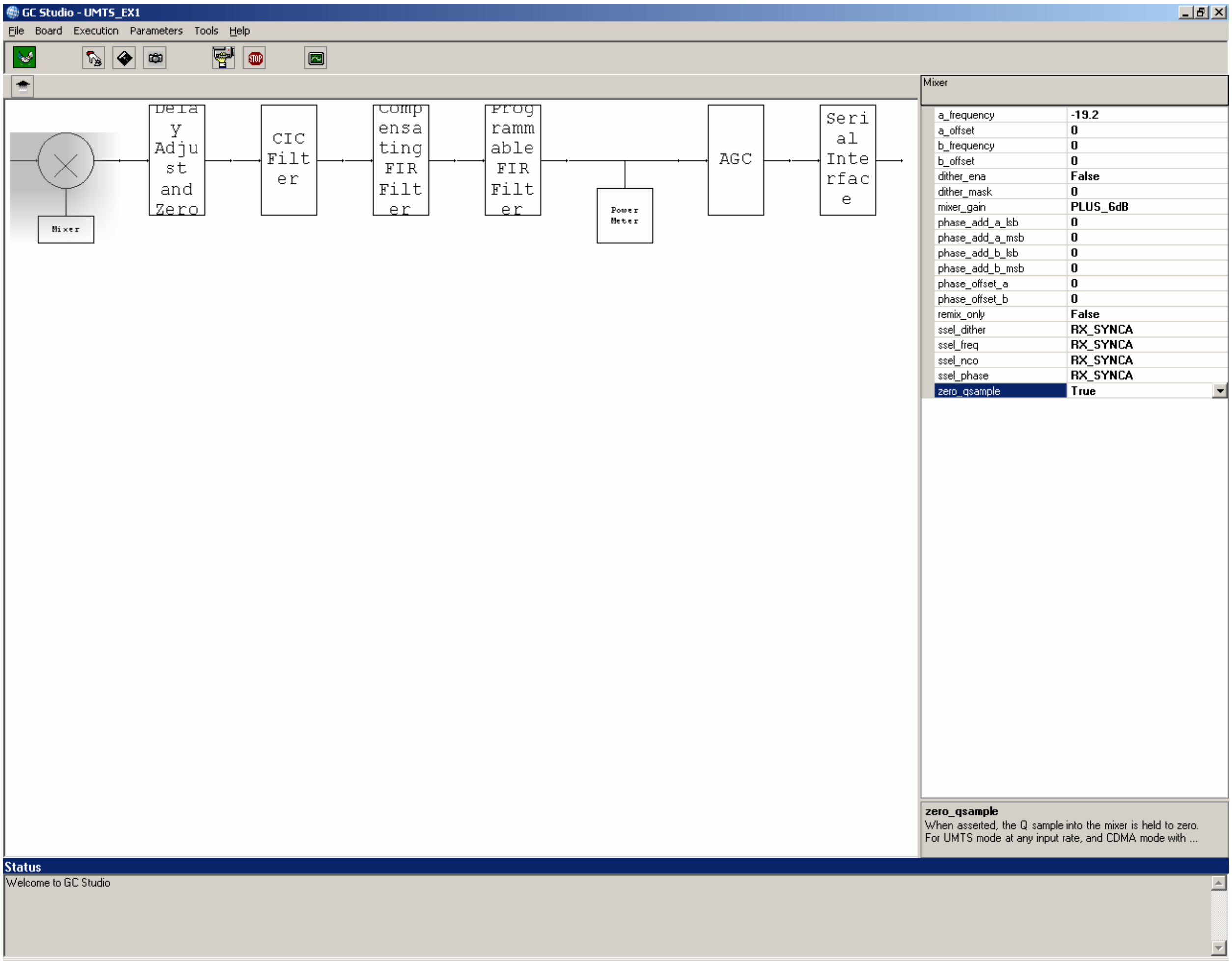
Welcome to GC Studio

“ddcmux_sel_X” (where X = a or b) determines where the data comes from into the Receive channel. ADC0 is the top file input, ADC1 is the bottom. Other inputs are not used for the GC5018 board.

Double click on the Receive Channel 0 block to push down into this channel. The block diagram now shows the sub blocks in the receive channel, and the registers to configure it.

Select the mixer/nco block (left most block). Since the input is a real signal, set the a_frequency to either +19.2 MHz or -19.2 MHz. The b_frequency setting is not used when the channel is in UMTS mode. Set zero_qsample to True (only I input is valid).

GC Studio will calculate the required values for the phase_add_a_msb and phase_add_a_lsb registers after the experiment is executed.



Mixer

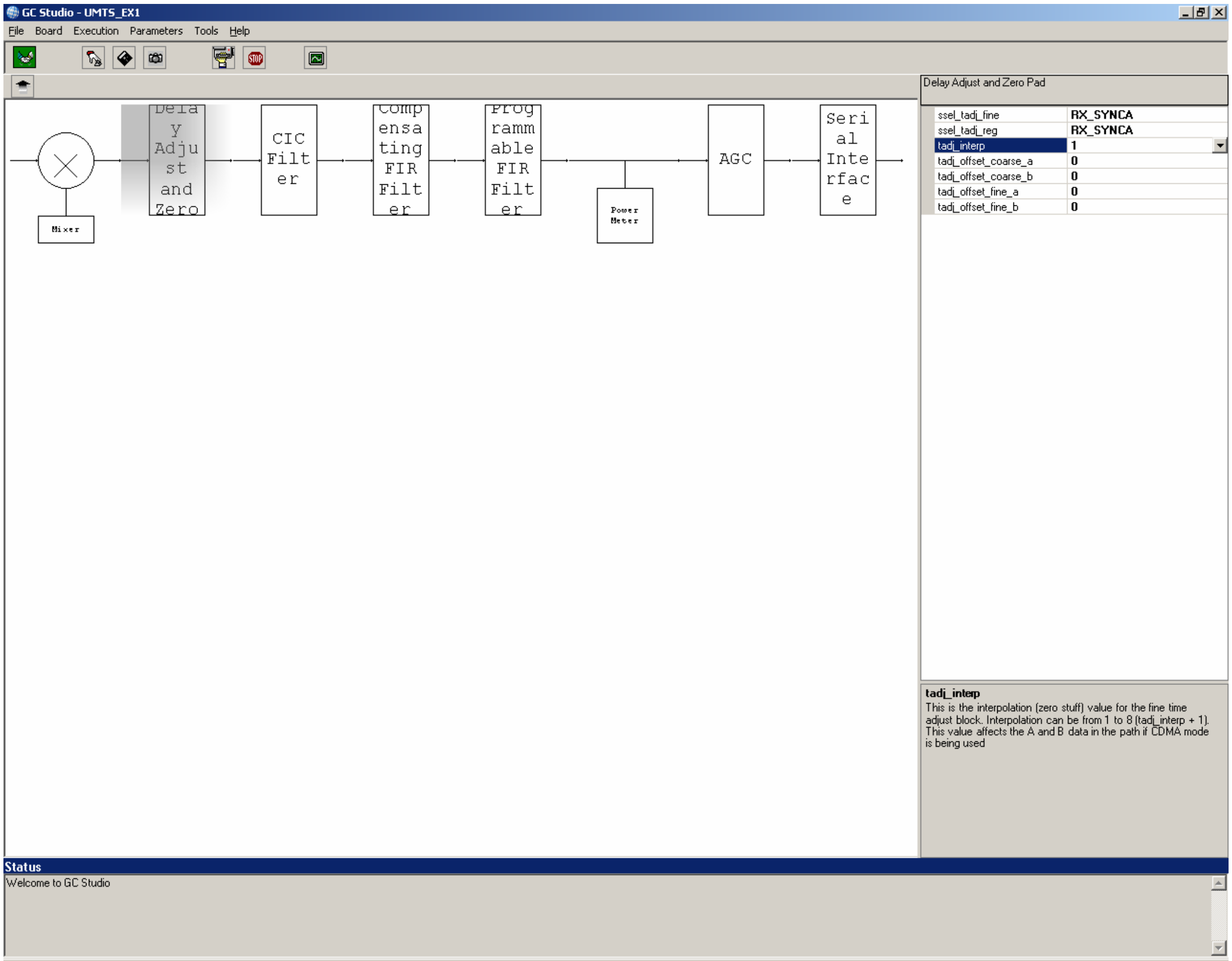
a_frequency	-19.2
a_offset	0
b_frequency	0
b_offset	0
dither_ena	False
dither_mask	0
mixer_gain	PLUS_6dB
phase_add_a_lsb	0
phase_add_a_msb	0
phase_add_b_lsb	0
phase_add_b_msb	0
phase_offset_a	0
phase_offset_b	0
remix_only	False
ssel_dither	RX_SYNCA
ssel_freq	RX_SYNCA
ssel_nco	RX_SYNCA
ssel_phase	RX_SYNCA
zero_qsample	True

zero_qsample
When asserted, the Q sample into the mixer is held to zero.
For UMTS mode at any input rate, and CDMA mode with ...

Welcome to GC Studio

There will be a 6 dB loss through the mixer due to the complex mixing. Therefore, the “mixer_gain” option can add 6 dB gain if set.

Select the Delay Adjust and Zero Stuff block. Because the input sample rate is set to ½ the rxclk rate, this block is automatically configured by GC Studio to interpolation by 2, inserting a zero sample between each actual sample before being applied to the CIC filter. “tadj_interp” is set to 1 for an interpolation by 2.
This moves the 76.8Msps input signal stream to the 153.6Msps rxclk rate. The tadj_offset_coarse and tadj_offset_fine settings allow the user to adjust the delay between various receive channels if desired.



Delay Adjust and Zero Pad

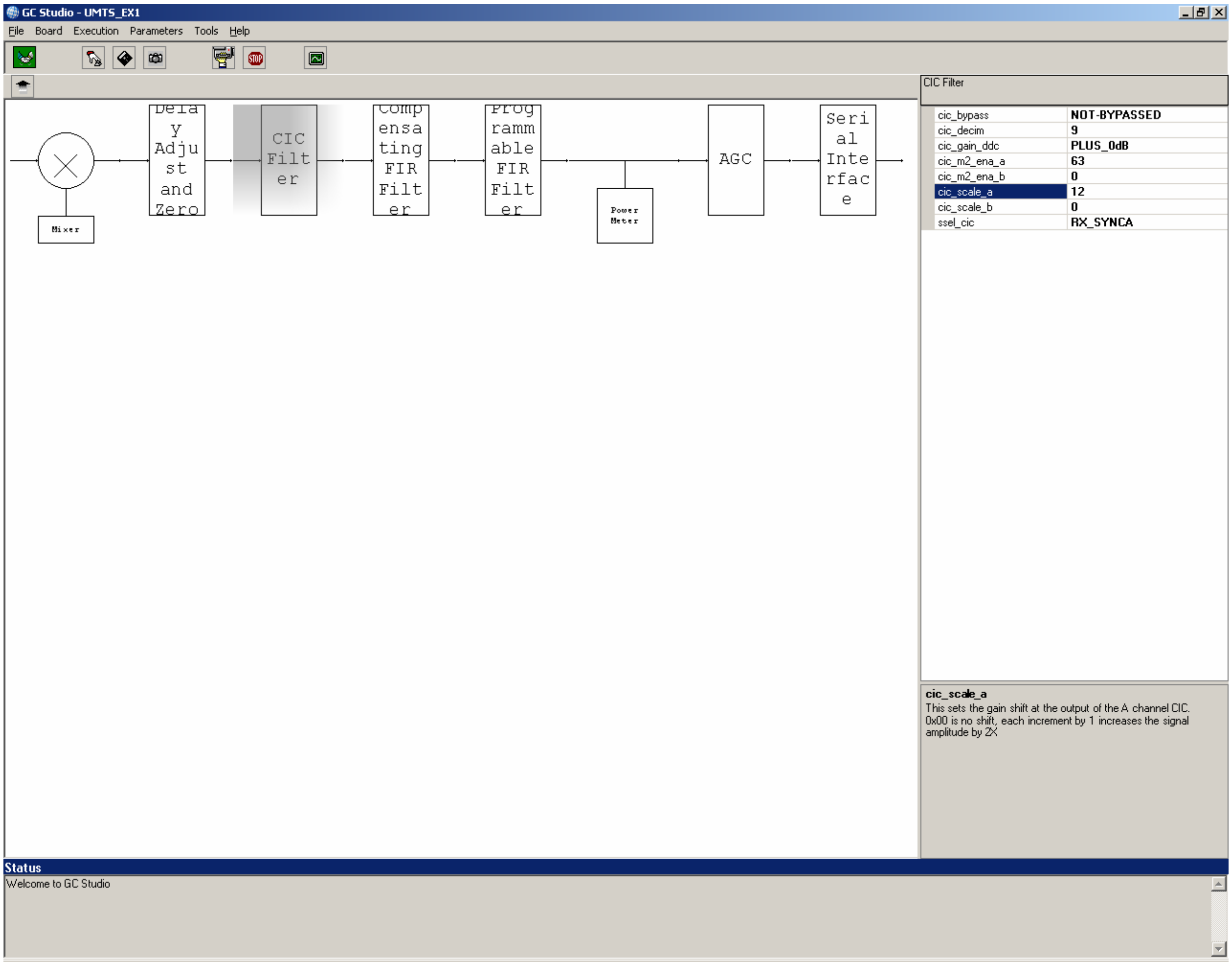
ssel_tadj_fine	RX_SYNCA
ssel_tadj_reg	RX_SYNCA
tadj_interp	1
tadj_offset_coarse_a	0
tadj_offset_coarse_b	0
tadj_offset_fine_a	0
tadj_offset_fine_b	0

tadj_interp
This is the interpolation (zero stuff) value for the fine time adjust block. Interpolation can be from 1 to 8 (tadj_interp + 1). This value affects the A and B data in the path if CDMA mode is being used

Status
Welcome to GC Studio

Click on the CIC filter block and set the registers as shown in the following panel. The decimation in the CIC is set to 10x, resulting in a 15.36Msps CIC output rate. The "cic_decim" parameter should be set to the desired decimation (10) minus one. Therefore, the output rate of the CIC block (input to the CFIR block) is at 4x symbol rate for UMTS (15.36 MSPS).

For this example, all 6 CIC comb stages are set to m=2 (63 decimal = 111111 in binary).



CIC Filter

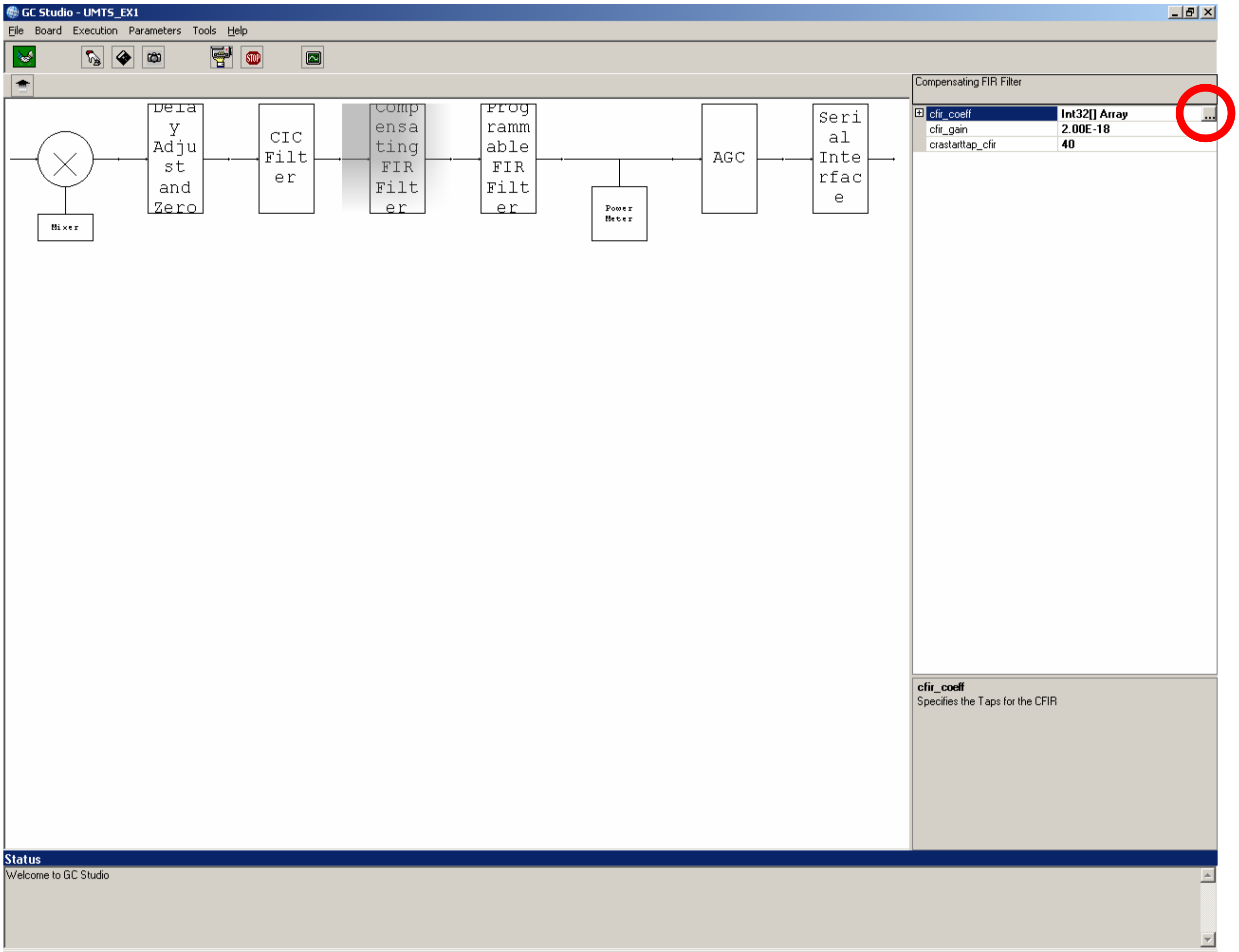
cic_bypass	NOT-BYPASSED
cic_decim	9
cic_gain_ddc	PLUS_0dB
cic_m2_ena_a	63
cic_m2_ena_b	0
cic_scale_a	12
cic_scale_b	0
ssel_cic	RX_SYNCA

cic_scale_a
This sets the gain shift at the output of the A channel CIC. 0x00 is no shift, each increment by 1 increases the signal amplitude by 2X

Welcome to GC Studio

See the datasheet CIC gain equation for appropriate "cic_scale_X" (where X = a or b) parameter setting, and to avoid CIC block saturation.

Select the CFIR block and set the cfir_gain to 2.00E-18, and the cra_starttap_cfir to 40 taps. The maximum number of taps in CFIR for UMTS example is calculated as twice the rxclk rate over the CFIR output rate – in this case 2 x 153.6e6 / 7.68e6 = 40 taps. See the datasheet CFIR description for more details on CFIR tap calculation.



cfir_coeff	Int32[] Array
cfir_gain	2.00E-18
crastarttap_cfir	40

cfir_coeff
Specifies the Taps for the CFIR

Welcome to GC Studio

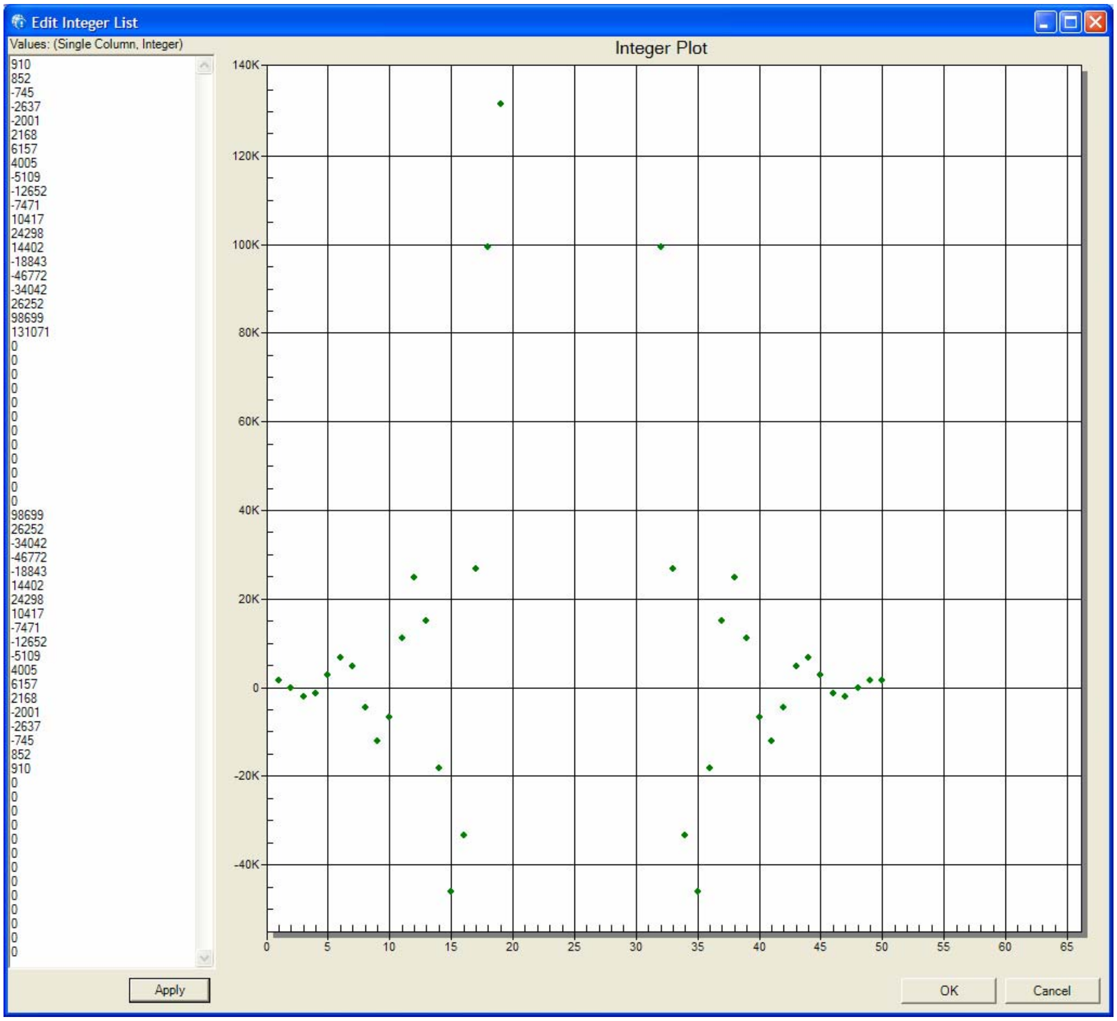
Next, select the cfir_coeff register setting by clicking on it, and then click on the browse button, circled in red on the panel above, to open the Edit Filter window and fill in the CFIR filter tap weights.

The CFIR is the compensation filter that compensates for the CIC droop. Therefore, the user should realize that the maximum number of taps actually is the convolved response of the filter and compensation filter (usually a three tap filter).

The CFIR tap weights are entered as shown. Note the first 20 taps are entered as the first 20 entries, and then 12 lines are skipped before entering the second 20. This is due to the GC5018 coefficient RAM being split into (2) 32 word blocks. See the datasheet for more details if necessary.

For this example, the CFIR tap weights are …

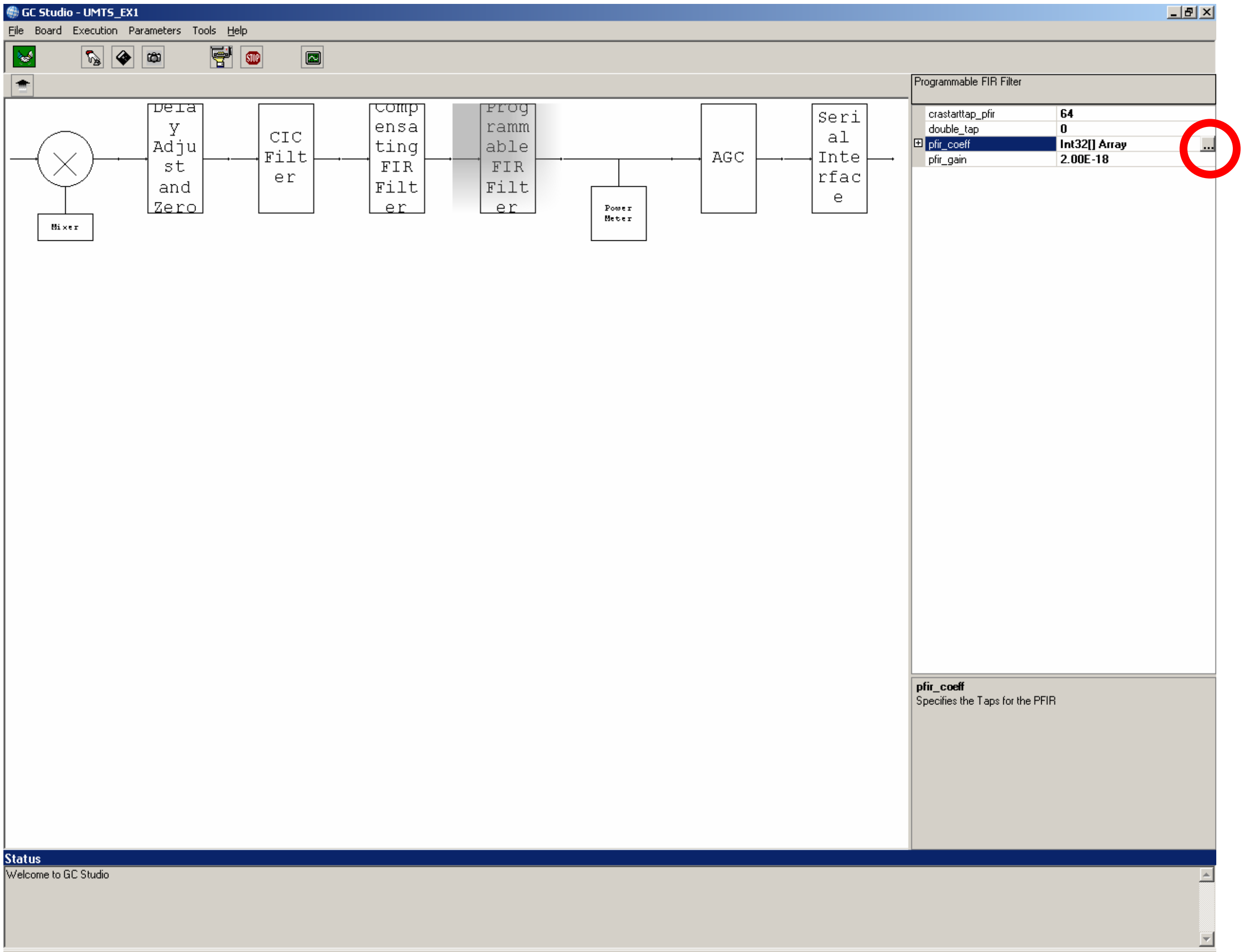
910
852
-745
-2637
-2001
2168
6157
4005
-5109
-12652
-7471
10417
24298
14402
-18843
-46772
-34042
26252
98699
131071
98699
26252
-34042
-46772
-18843
14402
24298
10417
-7471
-12652
-5109
4005
6157
2168
-2001
-2637
-745
852
910
0



Values: (Single Column, Integer)

910
852
-745
-2637
-2001
2168
6157
4005
-5109
-12652
-7471
10417
24298
14402
-18843
-46772
-34042
26252
98699
131071
0
0
0
0
0
0
0
0
0
0
0
0
98699
26252
-34042
-46772
-18843
14402
24298
10417
-7471
-12652
-5109
4005
6157
2168
-2001
-2637
-745
852
910
0
0
0
0
0
0
0
0
0
0
0
0
0

Select the PFIR block, set the pfir_gain to 2.00E-18, and crastarttap_pfir to 64. Select the pfir_coeff register, and again select the browse button. The maximum number of taps in PFIR for UMTS example is calculated as four times the rxclk rate over the CFIR output rate – The maximum number of available taps in PFIR is 64, therefore, all 64 taps are available for this example. See the datasheet CFIR description for more details on CFIR tap calculation.



Programmable FIR Filter

crastarttap_pfir	64
double_tap	0
pfir_coeff	Int32[] Array
pfir_gain	2.00E-18

pfir_coeff
Specifies the Taps for the PFIR

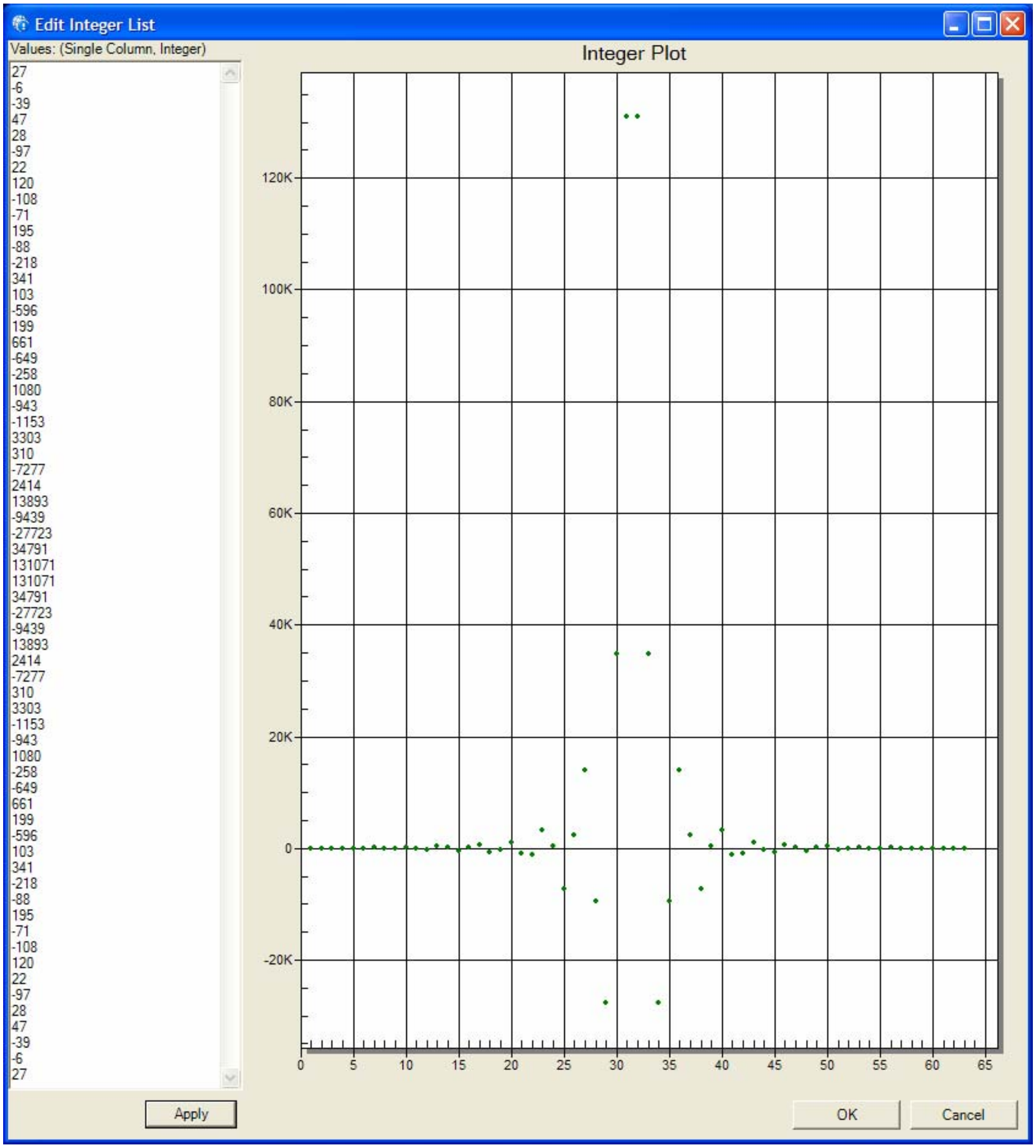
Status
Welcome to GC Studio

Next, select the pfir_coeff register settings by clicking on it, and then click on the browse button, circled in red on the panel above, to open the Edit Filter window and fill in the PFIR filter tap weights.

The PFIR in this example is an RRC filter with a = 0.22. However, the user must understand that the shape of the filter will slightly change if windowing is used, and that needs to be compensated appropriately.

The PFIR tap weights are entered as shown. For the 64 tap PFIR in this example, all coefficient are used. For this example, the PFIR tap weights are …

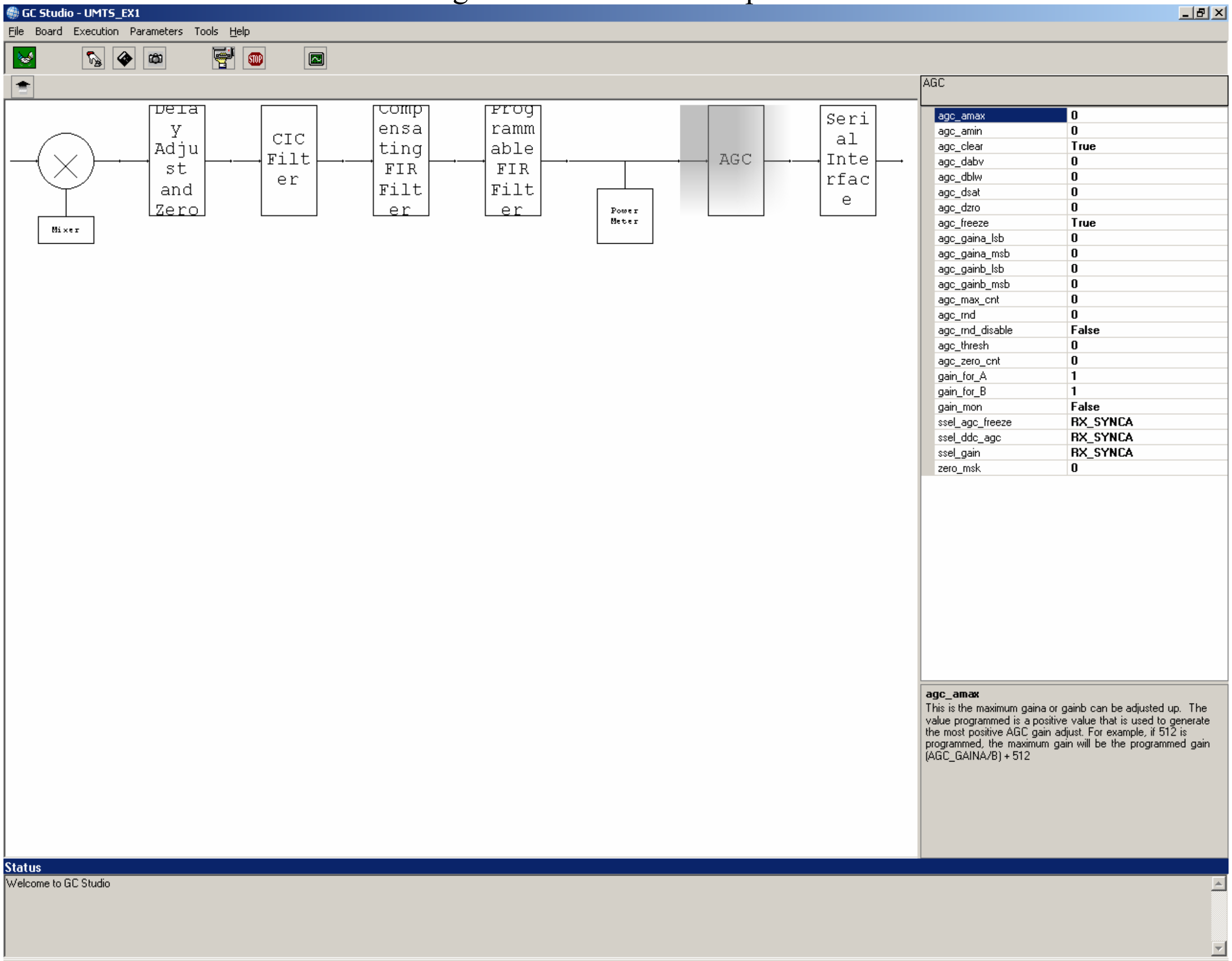
27
-6
-39
47
28
-97
22
120
-108
-71
195
-88
-218
341
103
-596
199
661
-649
-258
1080
-943
-1153
3303
310
-7277
2414
13893
-9439
-27723
34791
131071
131071
34791
-27723
-9439
13893
2414
-7277
310
3303
-1153
-943
1080
-258
-649
661
199
-596
103
341
-218



```
27
-6
-39
47
28
-97
22
120
-108
-71
195
-88
-218
341
103
-596
199
661
-649
-258
1080
-943
-1153
3303
310
-7277
2414
13893
-9439
-27723
34791
131071
131071
34791
-27723
-9439
13893
2414
-7277
310
3303
-1153
-943
1080
-258
-649
661
199
-596
103
341
-218
-88
195
-71
-108
120
22
-97
28
47
-39
-6
27
```

-88
195
-71
-108
120
22
-97
28
47
-39
-6
27

Select the AGC block and set the registers as shown in the panel below.



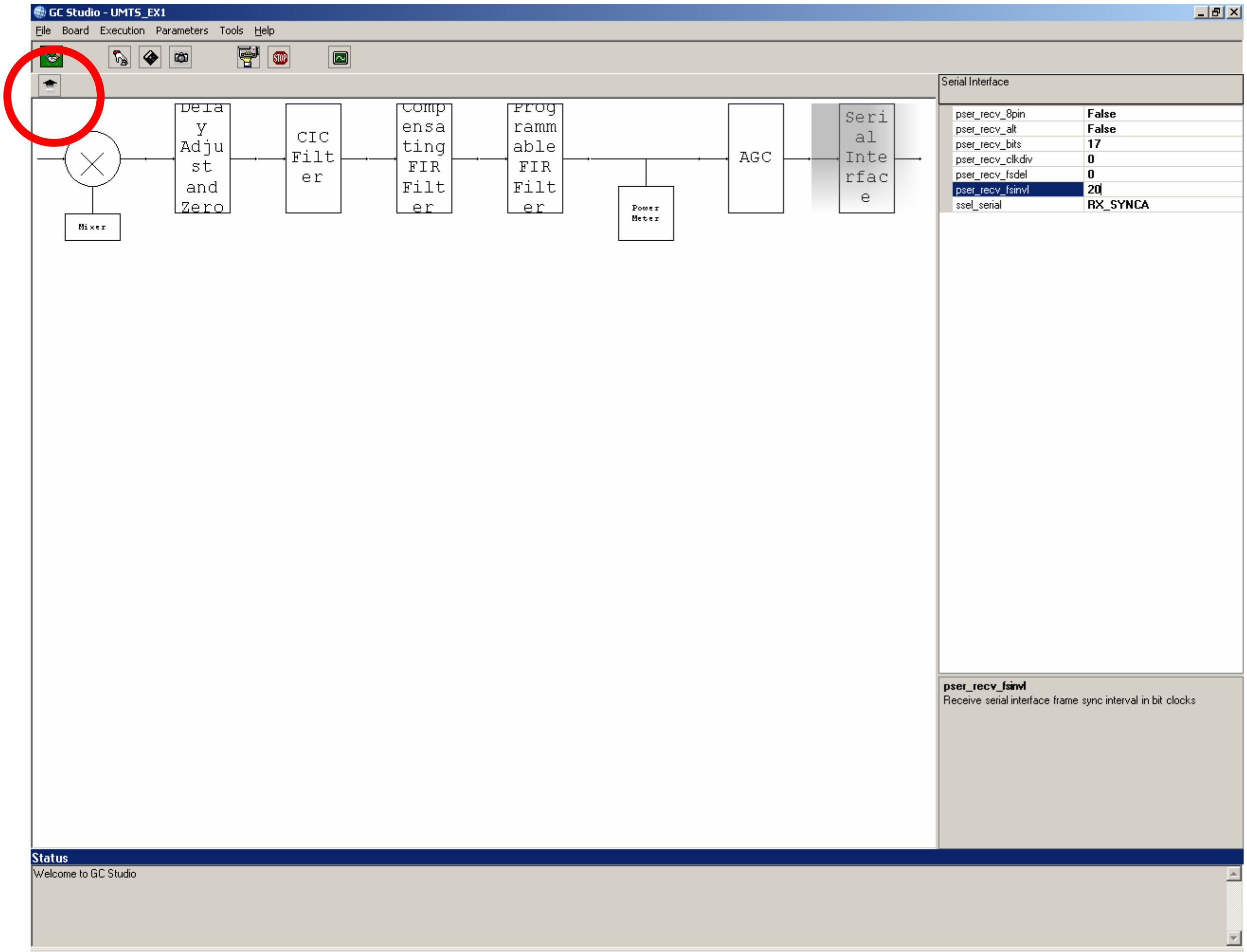
agc_amax	0
agc_amin	0
agc_clear	True
agc_dabv	0
agc_dblw	0
agc_dsat	0
agc_dzro	0
agc_freeze	True
agc_gaina_lsb	0
agc_gaina_msb	0
agc_gainb_lsb	0
agc_gainb_msb	0
agc_max_cnt	0
agc_rnd	0
agc_rnd_disable	False
agc_thresh	0
agc_zero_cnt	0
gain_for_A	1
gain_for_B	1
gain_mon	False
ssel_agc_freeze	RX_SYNCA
ssel_ddc_agc	RX_SYNCA
ssel_gain	RX_SYNCA
zero_msk	0

agc_amax
This is the maximum gaina or gainb can be adjusted up. The value programmed is a positive value that is used to generate the most positive AGC gain adjust. For example, if 512 is programmed, the maximum gain will be the programmed gain (AGC_GAINA/B) + 512

Welcome to GC Studio

The gain_for_A value is set unity, the agc_freeze and agc_clear are both set to True for this example. This puts the AGC in unity fixed gain mode. *GC Studio will calculate the required values for the agc_gaina_msb and the agc_gaina_lsb registers after the experiment is executed.*

Select the Serial Interface block and set the parameters as indicated. The maximum number of data bits on the serial output is 18. Since the overall decimation is greater than that (CIC decimation = 10 times CFIR decimation = 2) all 18 bits are available on the output, and "pser_recv_bits" parameter is set to 17 (# of output bits – 1).
"pser_recv_fsinvl" parameter determines how often the frame sync will come on the serial output and in this case is equal to the overall decimation (20).
"pser_recv_clkdiv" parameter allows the user to divide the output clock rate from the rxclk. This is an useful feature at high input data rates and high decimations, to slow down the output clock (that may be used) for baseband processing.



Serial Interface

pser_recv_8pin	False
pser_recv_alt	False
pser_recv_bits	17
pser_recv_clkdiv	0
pser_recv_fsdel	0
pser_recv_fsinvl	20
ssel_serial	RX_SYNCA

pser_recv_fsinvl
Receive serial interface frame sync interval in bit clocks

Status
Welcome to GC Studio

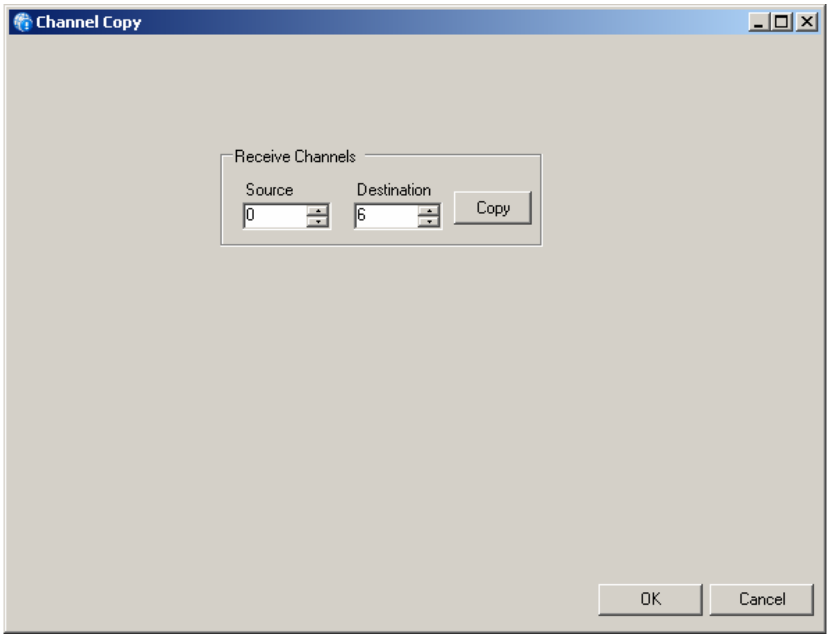
After verifying the values for the serial interface, click the arrow circled in red in panel above to pop up one level in the GC5018 hierarchy.

Receive Channel 0 has now been configured to process:

a UMTS signal at 76.8Msps with a 19.2MHz IF
mixer/nco block shifts the signal to DC
zero stuff block interpolates by 2x, moving the 76.8Msps signal to 153.6Msps
CIC block decimates by 10x to 15.36Msps
40 tap CFIR compensates for the CIC droop, filters and decimates the signal to 7.68Msps
64 tap PFIR filters the signal
channel AGC is set to a fixed gain of unit
serial interface is used to output the baseband signal

The GC5018 daughter card configuration uses rx_sync_out_6 as the strobe indicating when the serial output data starts each transfer. We'll copy the receive channel 0 configuration to receive channel 6 so the strobe will be present in the captured GC101 data.

Select "Parameters > GC5018 Channel Copy" to bring up the Channel Copy panel below. With channel 0 selected as the source, and channel 6 is selected as the destination, click Copy, and then click OK.

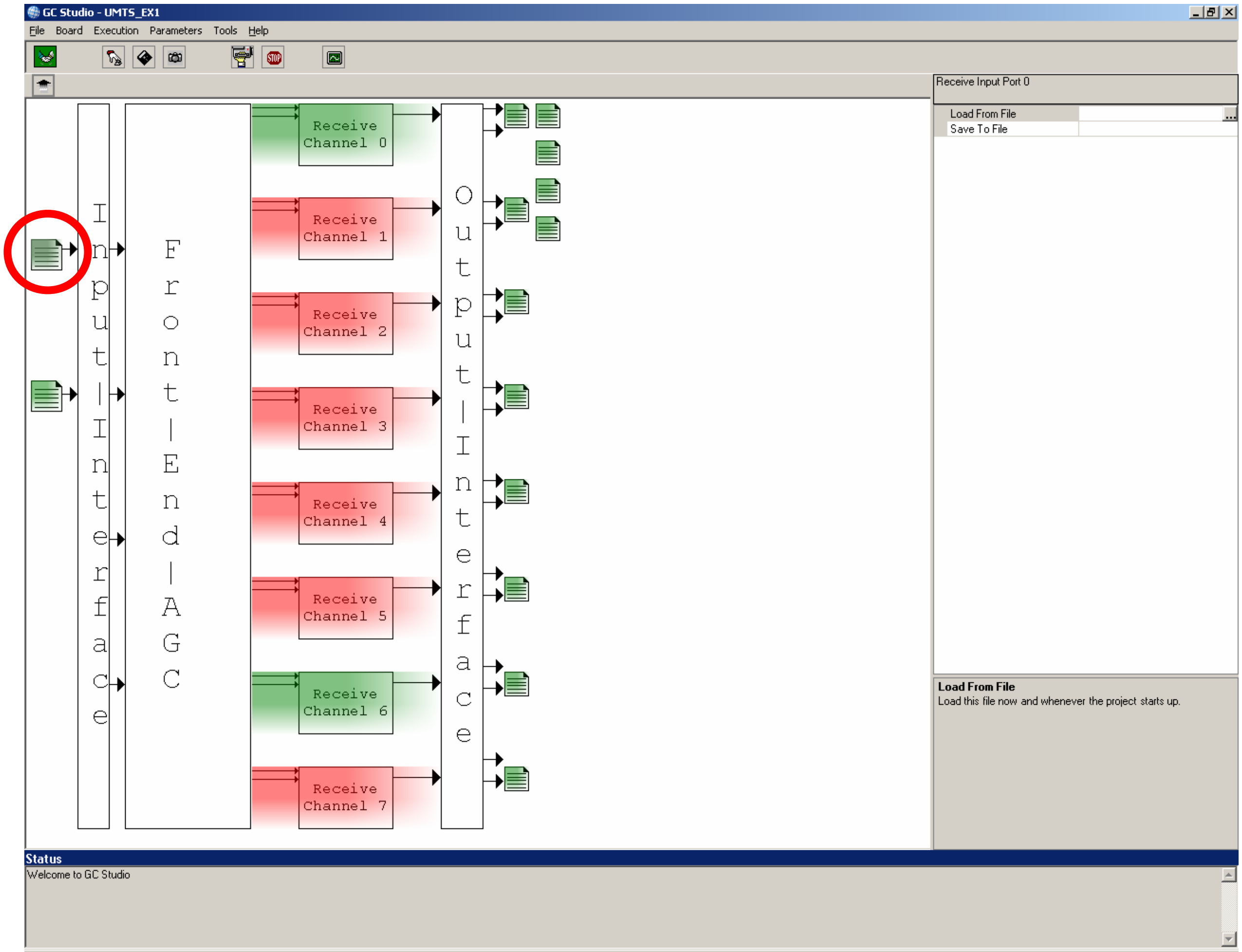


Source: 0

Destination: 6

The block diagram should now show both channels 0 and 6 active (green).

Input data presented to the gc5018 pins comes from text format data files. Two input file icons can be seen in the block diagram to the left of the Input Interface block. Click on the top icon, circled in red below.

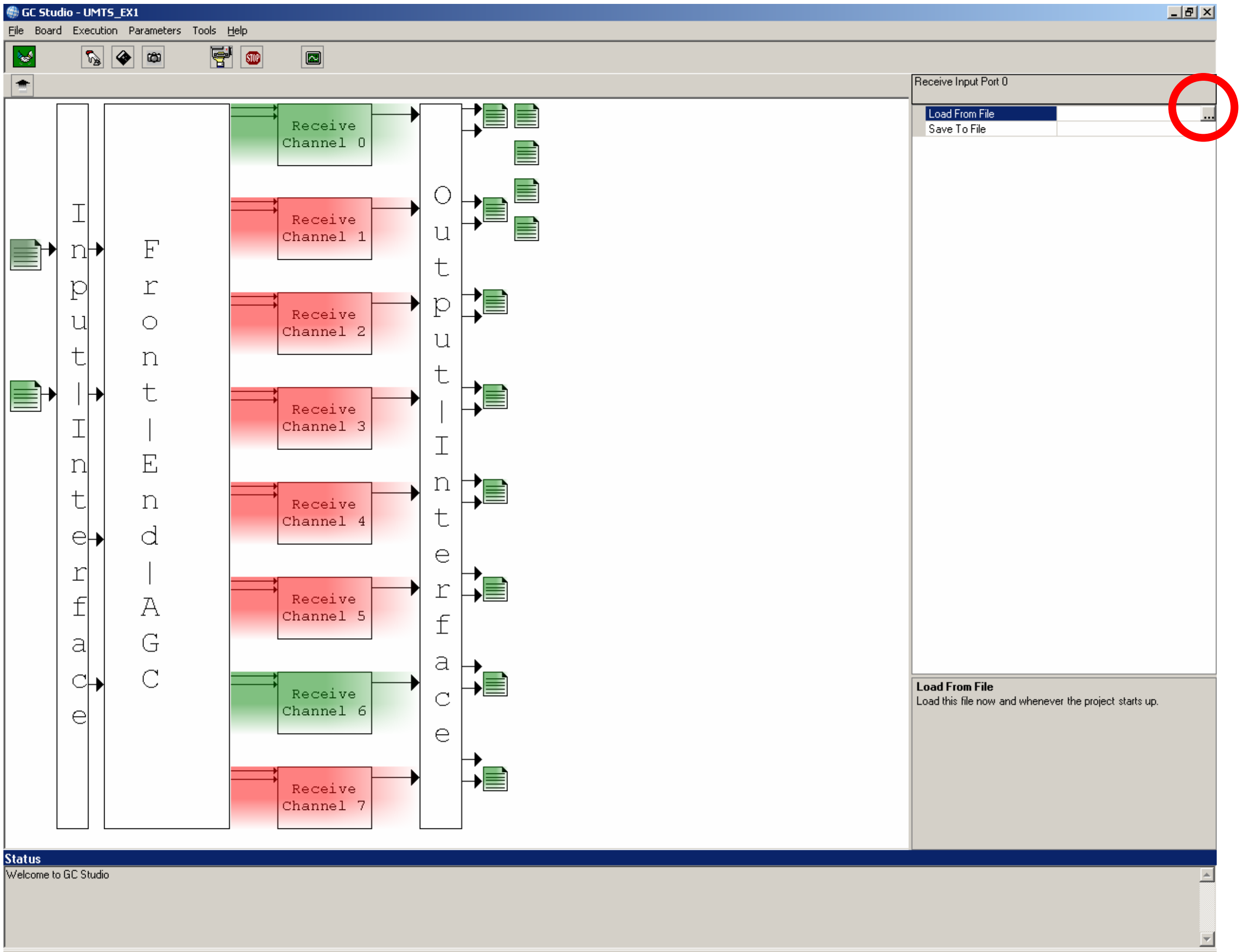


Load From File
Load this file now and whenever the project starts up.

Welcome to GC Studio

The upper file icon is connected to the rxin_a input port, and the lower is connected to the rxin_b input port.

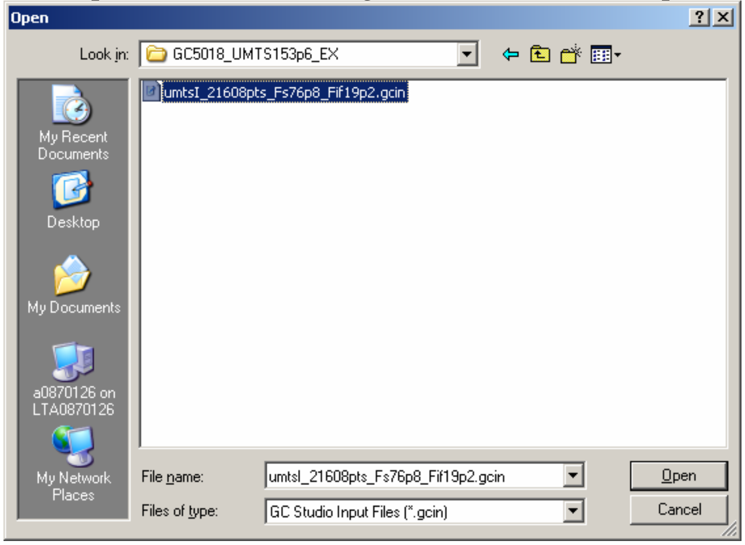
Next, click on the browse icon, circled in red below, to bring up the open file window.



Load From File
Load this file now and whenever the project starts up.

Welcome to GC Studio

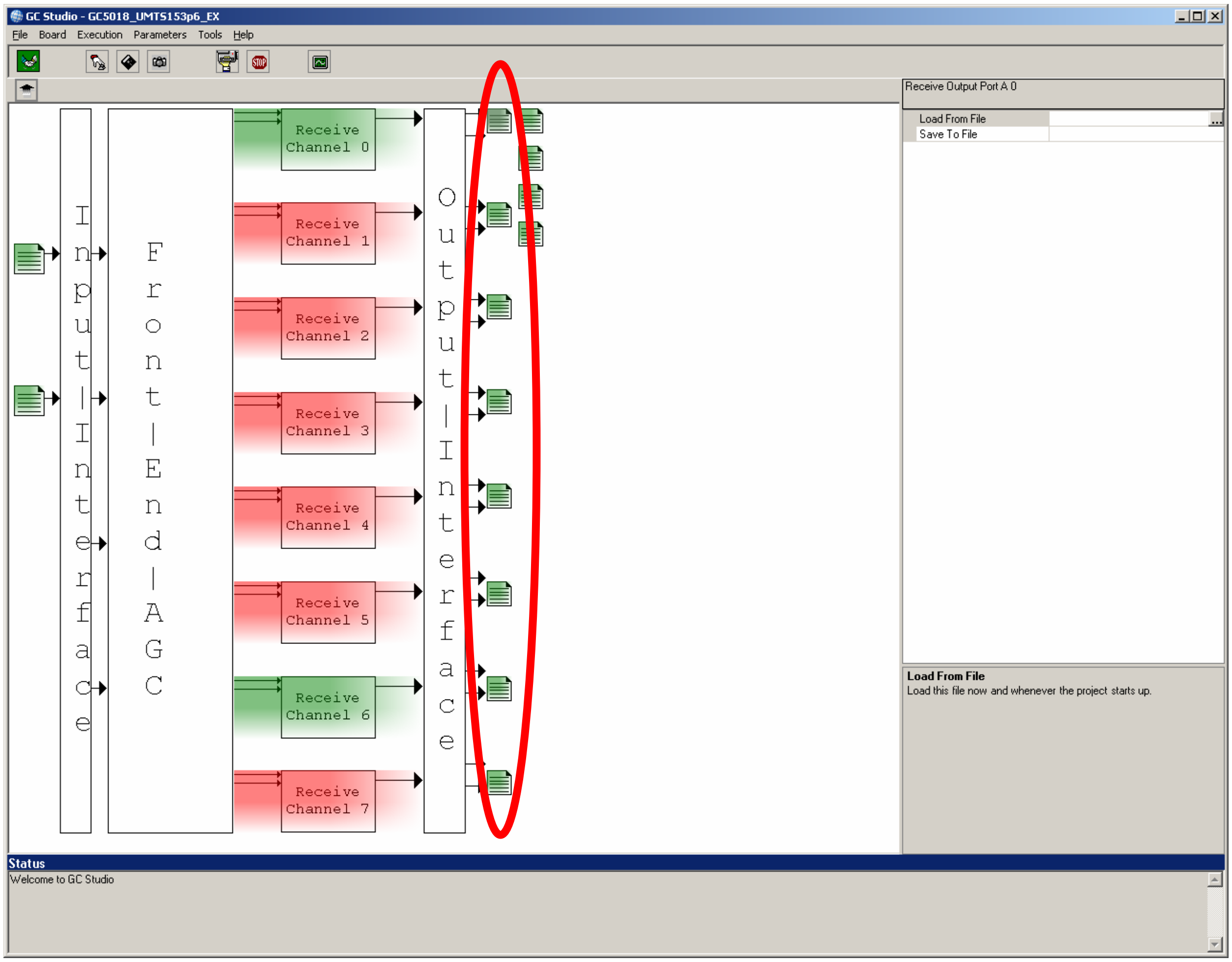
Navigate to and select the “umtsI_21608pts_Fs76p8_Fif19p2.gcin” file, and click open. Repeat for the lower input file icon, selecting the same file as the input file.



File name: umtsI_21608pts_Fs76p8_Fif19p2.gcin

Files of type: GC Studio Input Files (*.gcin)

Also, the output data can be stored in the output file.



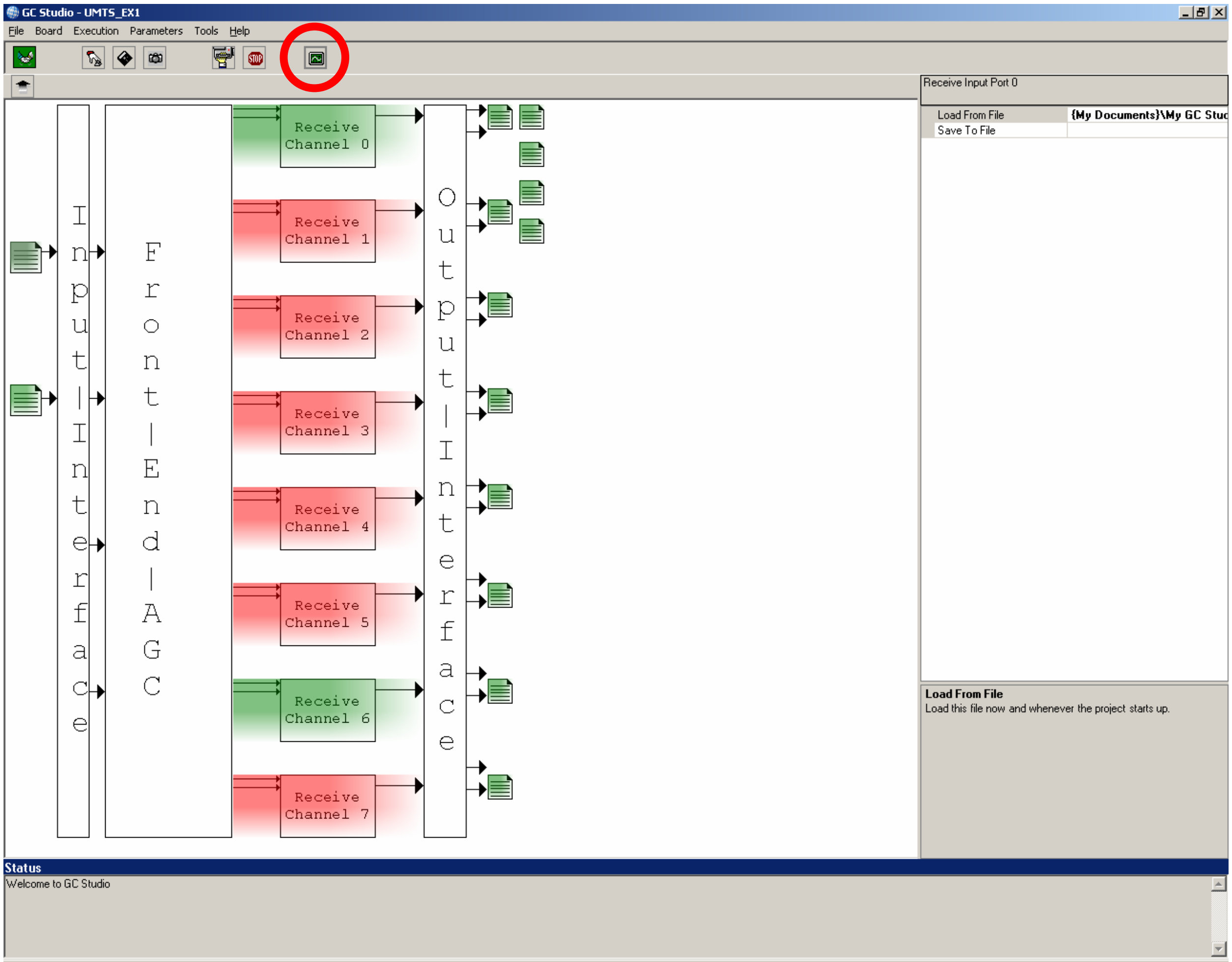
Receive Output Port A 0

Load From File	
Save To File	

Load From File
Load this file now and whenever the project starts up.

Welcome to GC Studio

Next, click on the graph button, circled in red below, to open the graph panel.

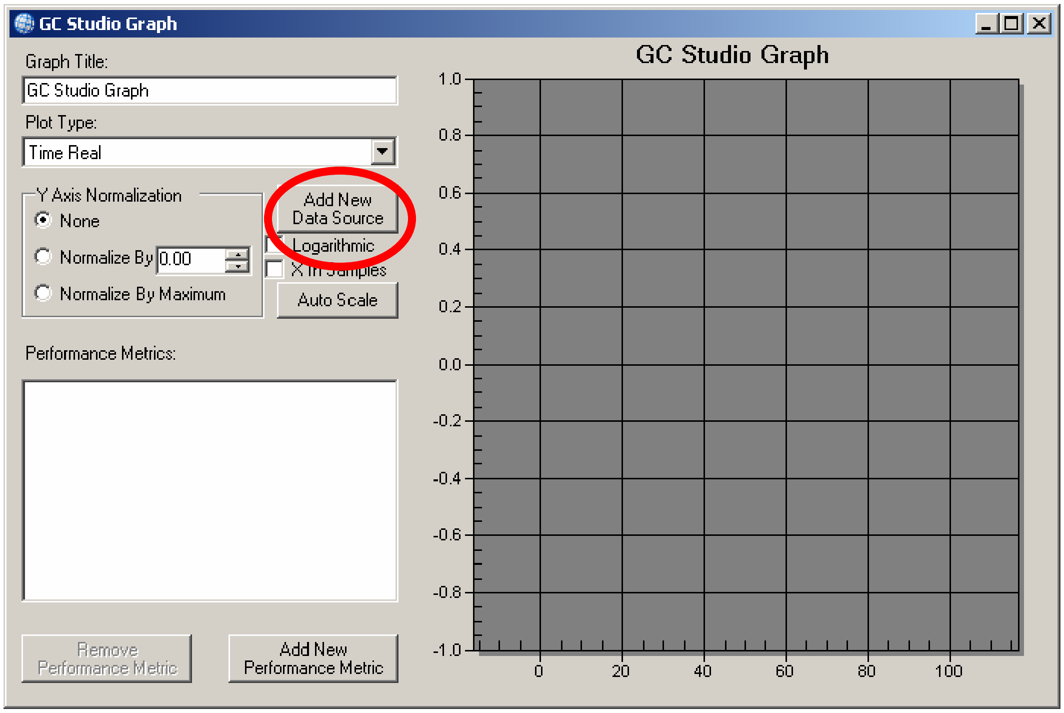


Receive Input Port 0

Load From File	{My Documents}\My GC Stuc
Save To File	

Load From File
Load this file now and whenever the project starts up.

Status
Welcome to GC Studio



Graph Title: GC Studio Graph

Plot Type: Time Real

Y Axis Normalization

● None

○ Normalize By 0.00

○ Normalize By Maximum

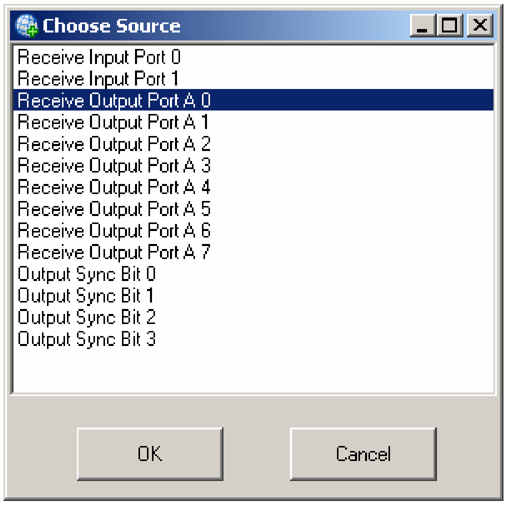
□ Logarithmic

□ X In Samples

Performance Metrics:

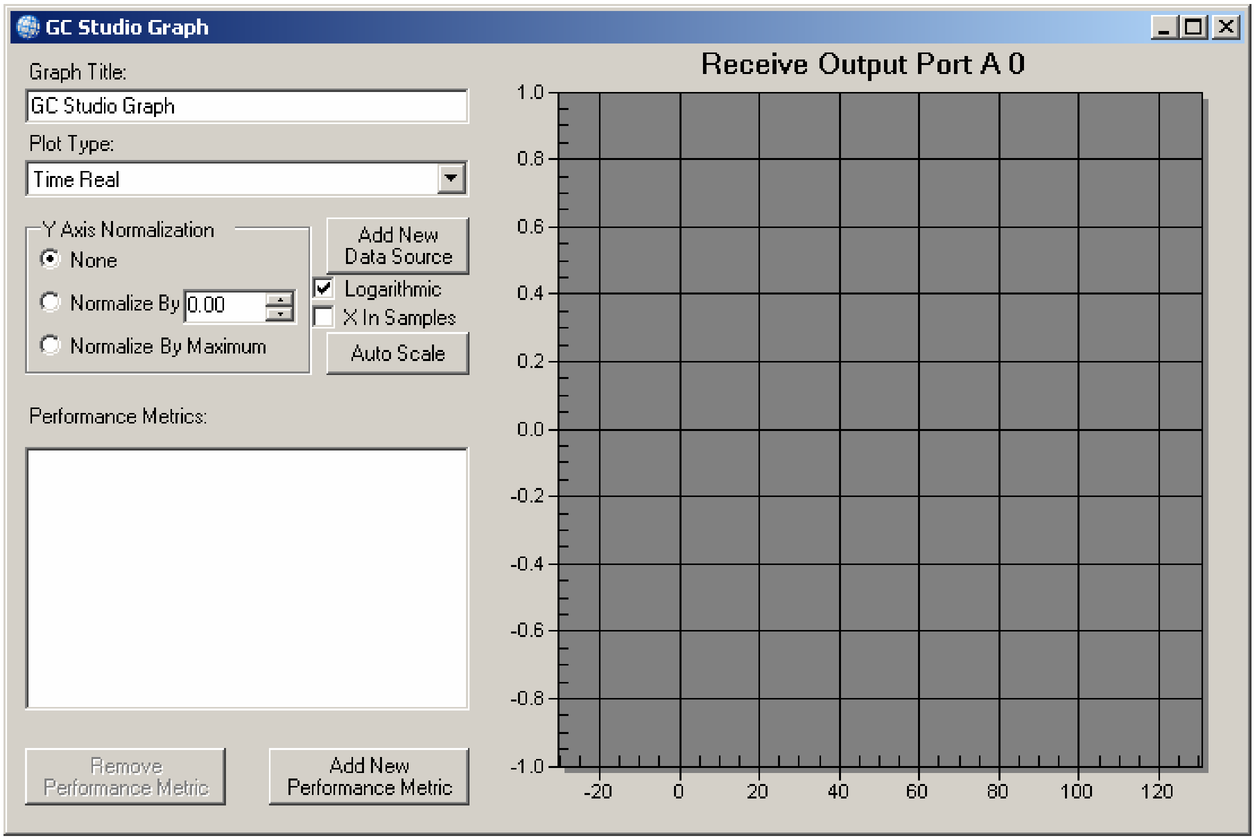
Click the Add New Data Source button circled in red above.

In the Choose Source panel, select both Receive Output Port A 0, and click OK.



Receive Input Port 0
Receive Input Port 1
Receive Output Port A 0
Receive Output Port A 1
Receive Output Port A 2
Receive Output Port A 3
Receive Output Port A 4
Receive Output Port A 5
Receive Output Port A 6
Receive Output Port A 7
Output Sync Bit 0
Output Sync Bit 1
Output Sync Bit 2
Output Sync Bit 3

In the graph panel, set the Plot Type to Spectral Magnitude, and check Logarithmic.



GC Studio Graph

Graph Title: GC Studio Graph

Plot Type: Time Real

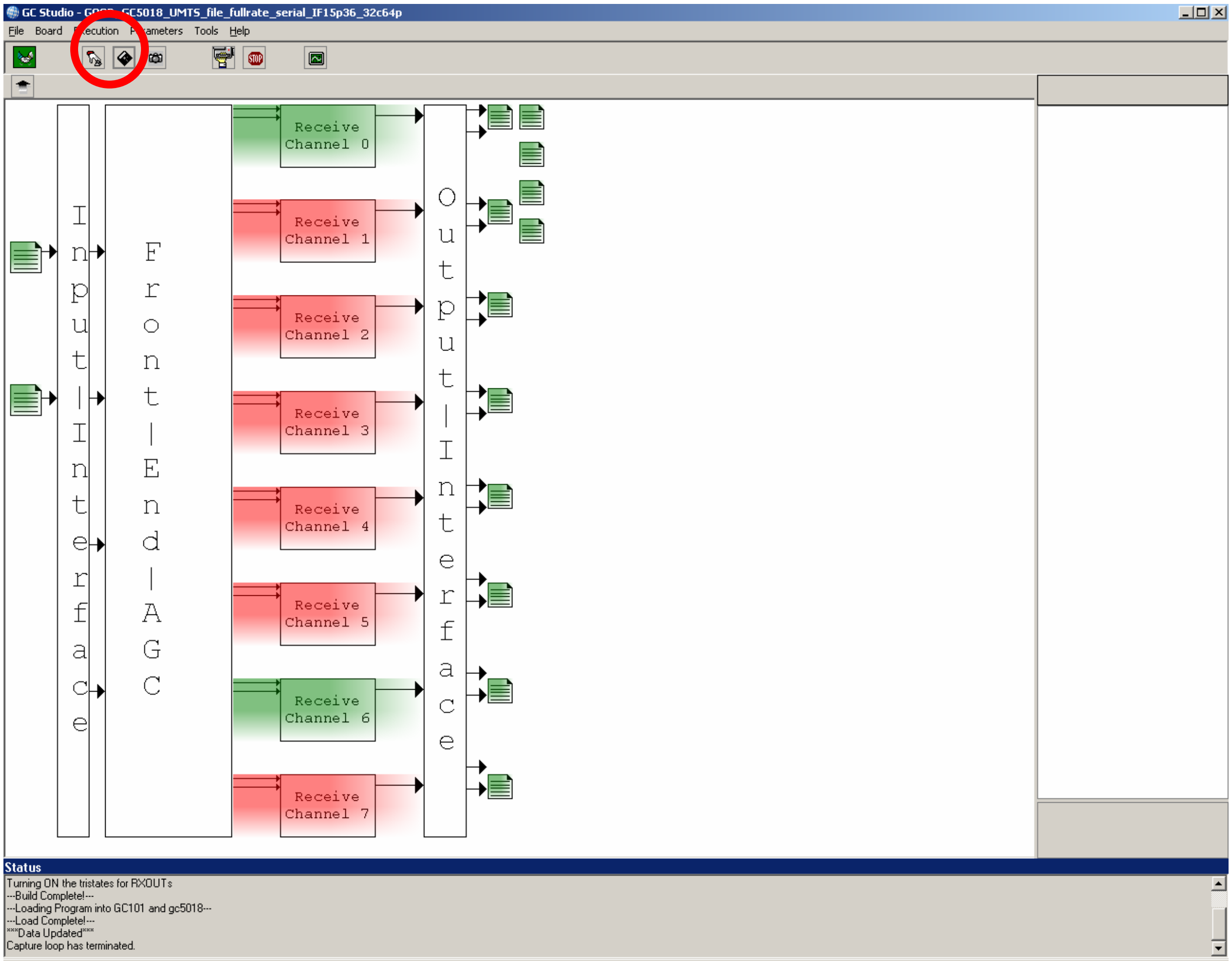
Y Axis Normalization
- ● None
- ○ Normalize By 0.00
- ○ Normalize By Maximum

☑ Logarithmic

□ X In Samples

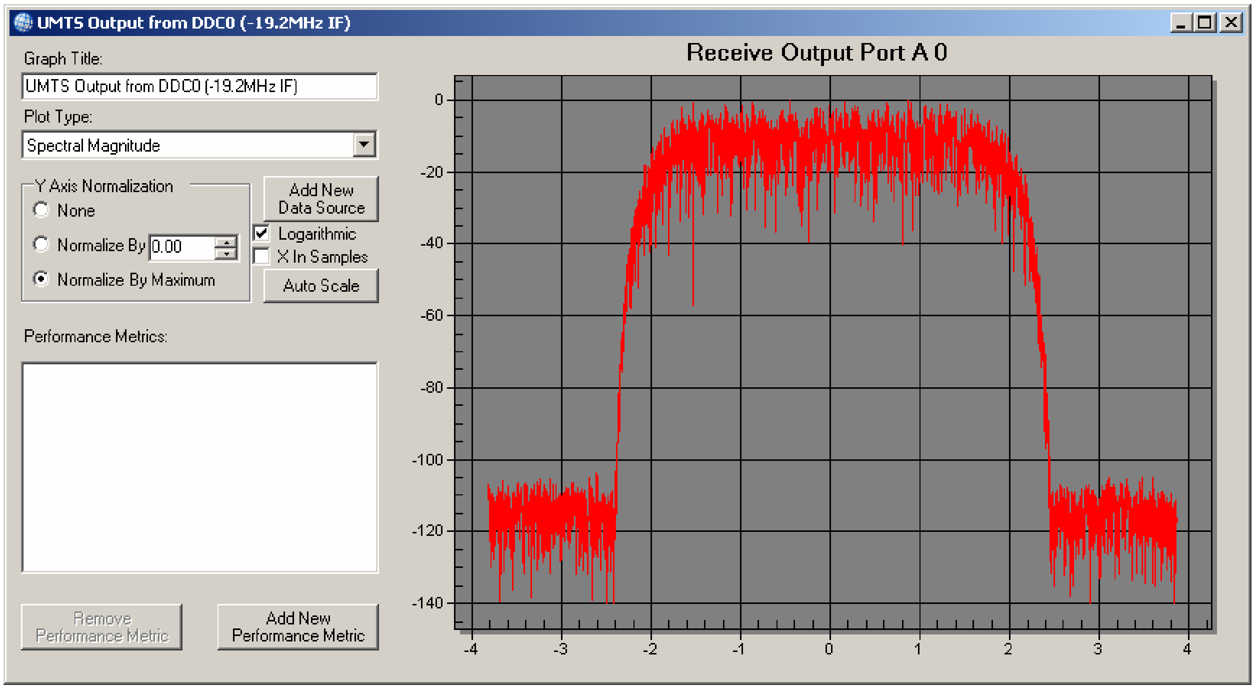
Performance Metrics:

On the GC Studio panel, click the Build and Load buttons, circled in red below. The buttons will turn grey while the project is running.



```
Turning ON the tristates for RXOUTs
---Build Complete!---
---Loading Program into GC101 and gc5018---
---Load Complete!---
***Data Updated***
Capture loop has terminated.
```

The graph window will be automatically updated with the results.



UMTS Output from DDC0 (-19.2MHz IF)

Graph Title: UMTS Output from DDC0 (-19.2MHz IF)

Plot Type: Spectral Magnitude

Y Axis Normalization

○ None

○ Normalize By 0.00

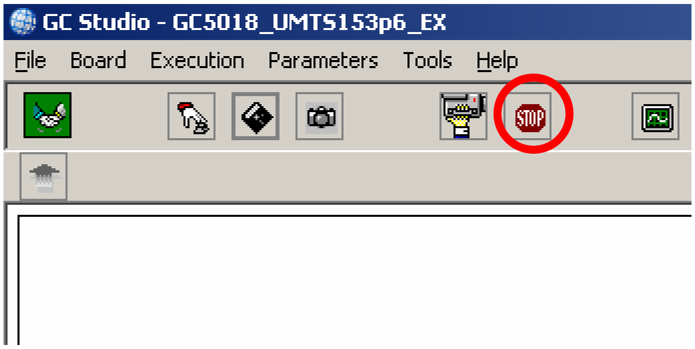
● Normalize By Maximum

☑ Logarithmic

□ X In Samples

Performance Metrics:

On the GC Studio panel, click on the stop button, shown circled in red below, to stop the experiment, then select File > Save Project to save this project.

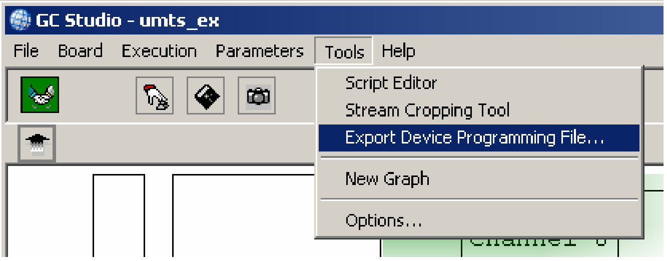


GC Studio - GC5018_UMTS153p6_EX

Close the GC Studio Graph Window.

The GC Studio software also allows the user to extract the internal register values into the file that could make programming the device much less complicated than doing it “by hand”

Select “Tools”, then “Export Device Programming File…”



The file will be saved in a two-column format where the first column is the register locations, and the second is the 16-bit values:

```
0060 0FFF
0000 0003
0001 0002
0002 0001
0003 0003
0004 0000
0005 0003
0006 0002
0007 0000
0008 0000
0009 0001
000A 0003
000B 0000
000C 0002
```

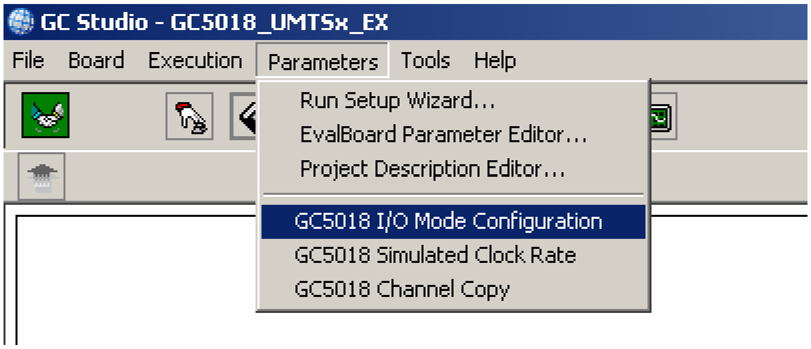
2.2.2. Capturing the GC5018 Test Bus Output

The GC5018 includes a test bus allowing the user to view internal digital signals. When the test bus is enabled, the rxin_c and rxin_d digital ADC input ports become outputs and the dvga_c and dvga_d ports are multiplexed to carry test bus data. The result is a 36 bit wide output port and 3 additional signals.

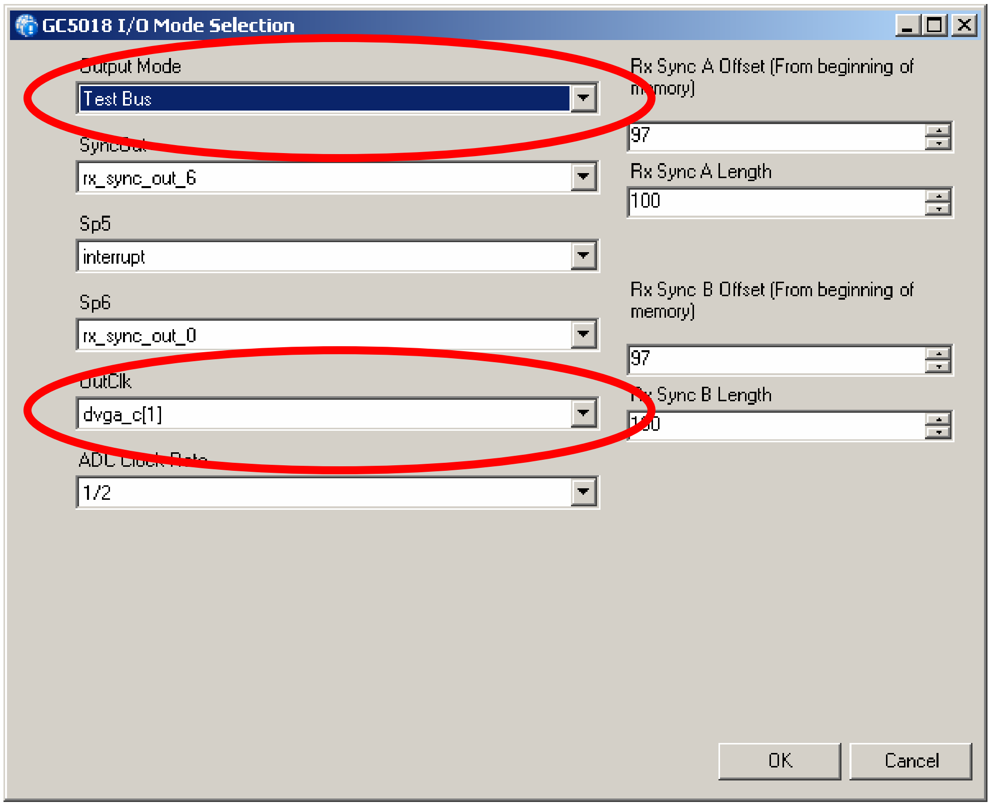
testbus(35:0)	rxin_d(15:0), dvga_c(3:2), rxin_c(15:0), dvga_c(5:4)
dvga_c(1)	test bus clock
dvga_c(0)	test bus sync
dvga_d(5)	test bus aflag

The GC101 evaluation platform captures a 36 bit signal into the response memory. When selecting the various test bus sources, the signals selected in the I/O Mode Selection window must be set correctly.

Starting from the previous UMTS example experiment, select Parameters > GC5018 I/O Mode Configuration.


GC Studio - GC5018_UMTSx_EX
File
Board
Execution
Parameters
Tools
Help
Run Setup Wizard...
EvalBoard Parameter Editor...
Project Description Editor...
GC5018 I/O Mode Configuration
GC5018 Simulated Clock Rate
GC5018 Channel Copy

The Output Mode is set to Test Bus and the test bus output clock on dvga_c(1) is selected as the OutClk source when using the test bus.



Output Mode: Test Bus

SyncOut: rx_sync_out_6

Sp5: interrupt

Sp6: rx_sync_out_0

OutClk: dvga_c[1]

ADC Clock Rate: 1/2

Rx Sync A Offset (From beginning of memory): 97

Rx Sync A Length: 100

Rx Sync B Offset (From beginning of memory): 97

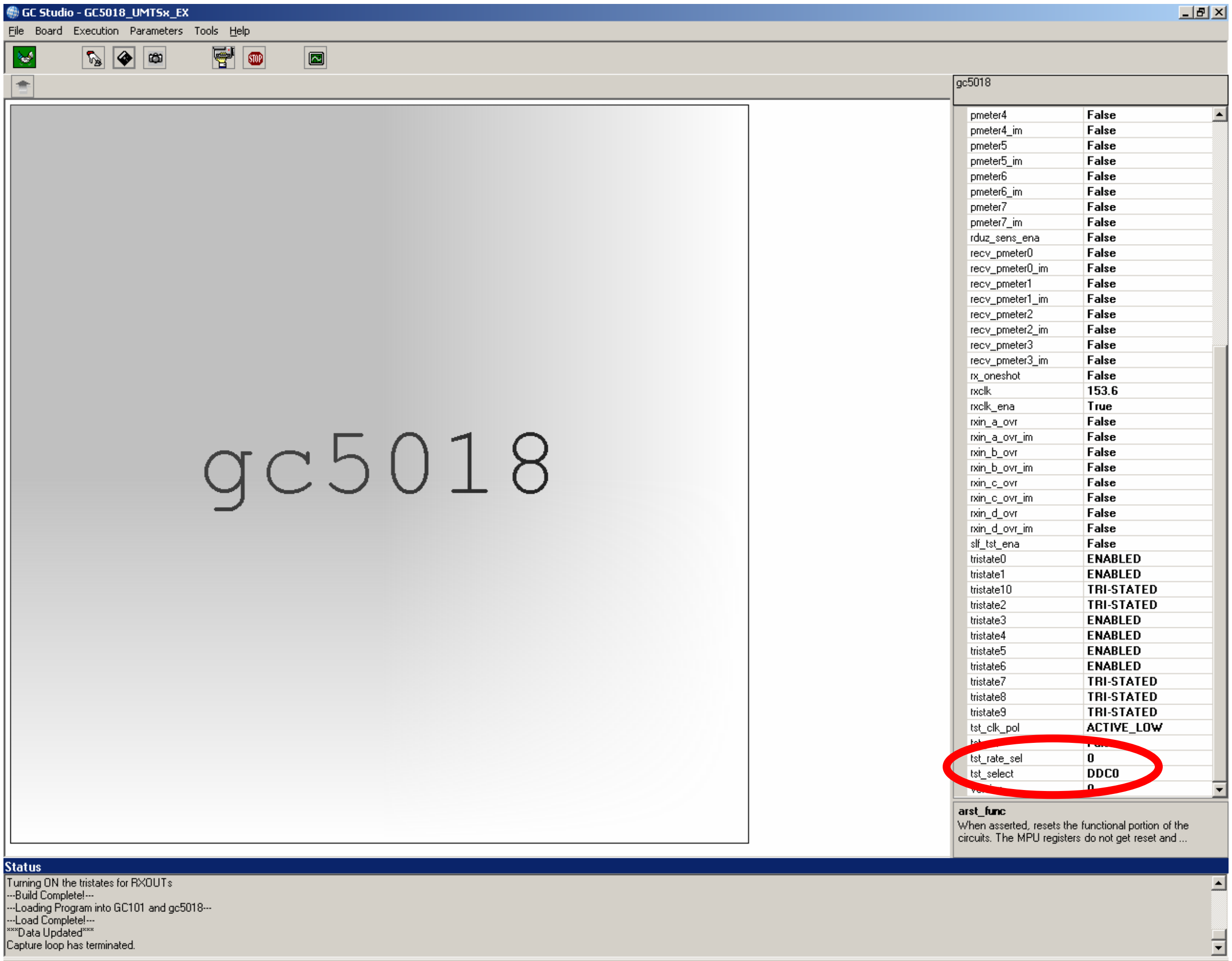
Rx Sync B Length: 100

The other signals captured as SyncOut+, Sp5 and Sp6 should be configured as required for the specific test bus signal (Sp7 is always dvga_c(5)). The test bus output clock is used to load the response memory, and is controlled by the tst_rate_sel.

Test Bus Signal	**SyncOut+**	**Sp5**	**Sp6**	**OutClk**	**tst_rate_sel**
DDC PFIR in UMTS mode	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	2*CIC decimation
DDC PFIR in CDMA mode	dvga_c(2)	*dvga_d(5)*	dvga_c(4)	dvga_c(1)	RXCLK Rate
DDC CFIR in UMTS mode	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	2*CIC decimation
DDC PFIR in CDMA mode	dvga_c(2)	*dvga_d(5)*	dvga_c(4)	dvga_c(1)	RXCLK Rate
DDC TADJ-A	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	RXCLK Rate
DDC TADJ-B CDMA mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	RXCLK Rate
DDC NCO-SINE in UMTS mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC Clock Rate
DDC NCO-COSINE in UMTS mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC Clock Rate
DDC CIC in UMTS mode	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	CIC decimation
DDC CIC in CDMA mode	dvga_c(2)	*dvga_d(5)*	dvga_c(4)	dvga_c(1)	RXCLK Rate
DDC AGC in UMTS mode	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	2*CIC decimation
DDC AGC in CDMA mode	dvga_c(2)	*dvga_d(5)*	dvga_c(4)	dvga_c(1)	RXCLK Rate
DDC MIXER-A	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC Clock Rate
DDC MIXER-B CDMA mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC Clock Rate
DDC DDCMUX-A	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC Clock Rate
DDC DDCMUX-B CDMA mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC Clock Rate
RXIN_A and RXINB FIFO	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC Clock Rate

Using the setup from the previous UMTS example, the NCO sine test bus source is a 20 bit signal output on the dvga_c(3:2) + rxin_c(15:0) + dvga_c(5:4) pins. Selecting dvga_c(4) for Sp6, dvga_c(3) for Sp5 and dvga_c(2) for SyncOut+ is required. The daughtercard always connects dvga_c(5) to the capture memory Sp7 bit. The 20 bit sine and cosine signals can be captured and analyzed using the I/O mode selection as shown above.

The NCO clock runs at the same clock frequency as the input data. The test clock should therefore be configured to provide a rxclk/2 output by setting tst_rate_sel to 1. The test bus output in this example is using DDC0 as set by tst_sel.

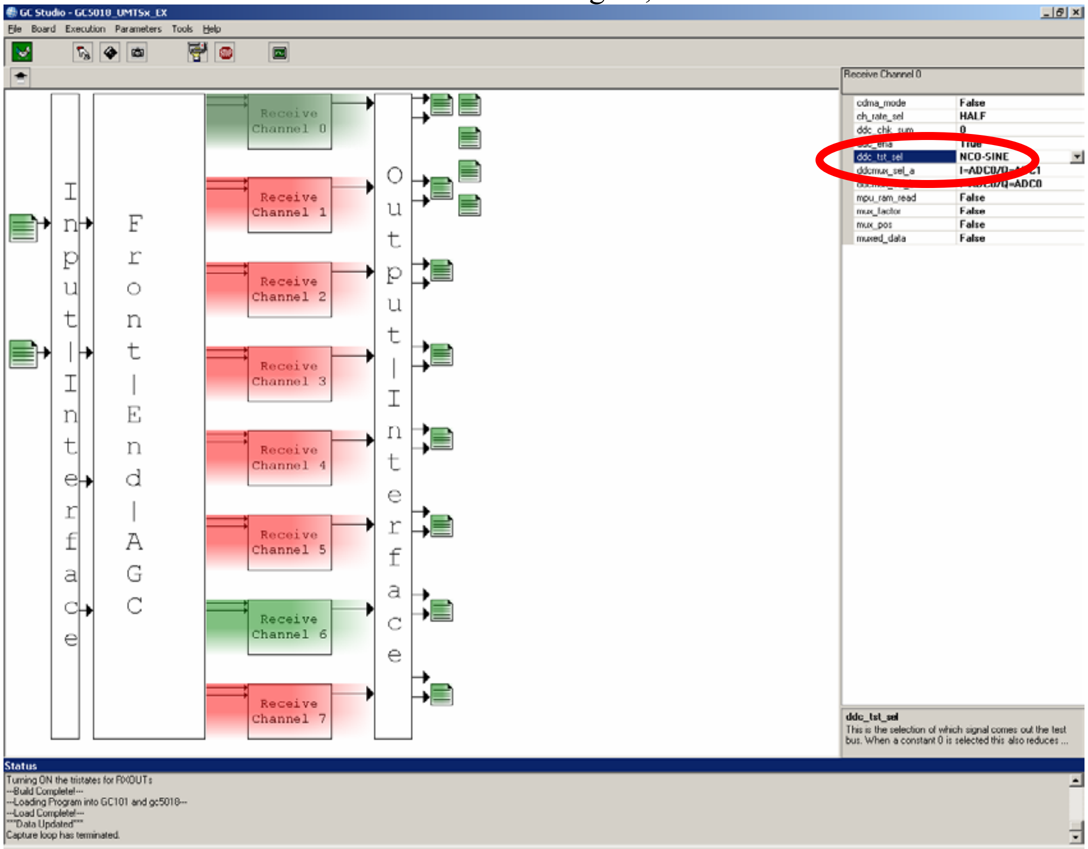


pmeter4	False
pmeter4_im	False
pmeter5	False
pmeter5_im	False
pmeter6	False
pmeter6_im	False
pmeter7	False
pmeter7_im	False
rduz_sens_ena	False
recv_pmeter0	False
recv_pmeter0_im	False
recv_pmeter1	False
recv_pmeter1_im	False
recv_pmeter2	False
recv_pmeter2_im	False
recv_pmeter3	False
recv_pmeter3_im	False
rx_oneshot	False
rxclk	153.6
rxclk_ena	True
rxin_a_ovr	False
rxin_a_ovr_im	False
rxin_b_ovr	False
rxin_b_ovr_im	False
rxin_c_ovr	False
rxin_c_ovr_im	False
rxin_d_ovr	False
rxin_d_ovr_im	False
slf_tst_ena	False
tristate0	ENABLED
tristate1	ENABLED
tristate10	TRI-STATED
tristate2	TRI-STATED
tristate3	ENABLED
tristate4	ENABLED
tristate5	ENABLED
tristate6	ENABLED
tristate7	TRI-STATED
tristate8	TRI-STATED
tristate9	TRI-STATED
tst_clk_pol	ACTIVE_LOW
tst_rate_sel	0
tst_select	DDC0

arst_func
When asserted, resets the functional portion of the circuits. The MPU registers do not get reset and ...

```
Turning ON the tristates for RXOUTs
---Build Complete!---
---Loading Program into GC101 and gc5018---
---Load Complete!---
***Data Updated***
Capture loop has terminated.
```

Push down into DDC0 to select the test bus signal, NCO-SIN is selected.



Receive Channel 0

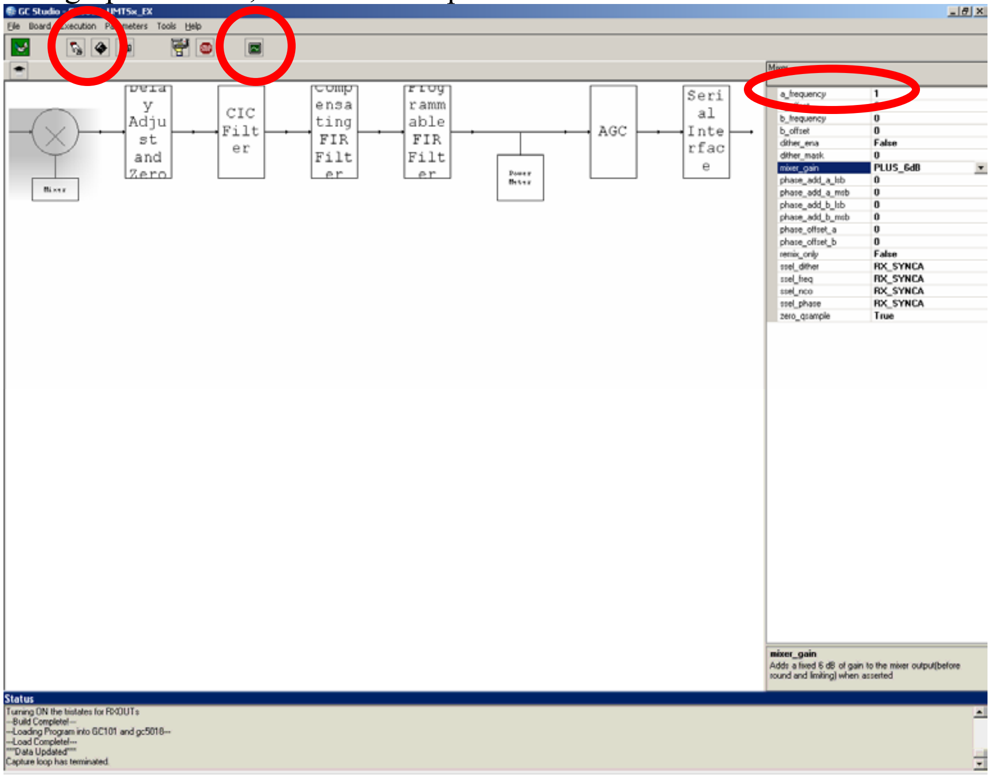
cdma_mode	False
ch_rate_sel	HALF
ddc_chk_sum	0
ddc_ena	True
ddc_tst_sel	NCO-SINE
ddcmux_sel_a	I=ADC0/Q=ADC1
ddcmux_sel_b	I=ADC0/Q=ADC0
mpu_ram_read	False
mux_factor	False
mux_pos	False
muxed_data	False

ddc_tst_sel
This is the selection of which signal comes out the test bus. When a constant 0 is selected this also reduces ...

Status

```
Turning ON the tristates for RXOUTs
---Build Complete!---
---Loading Program into GC101 and gc5018---
---Load Complete!---
"""Data Updated"""
Capture loop has terminated.
```

Push down into DDC0, and select the Mixer block. Set a_frequency to 1MHz. Open a new graph window, and run the experiment.



Mixer

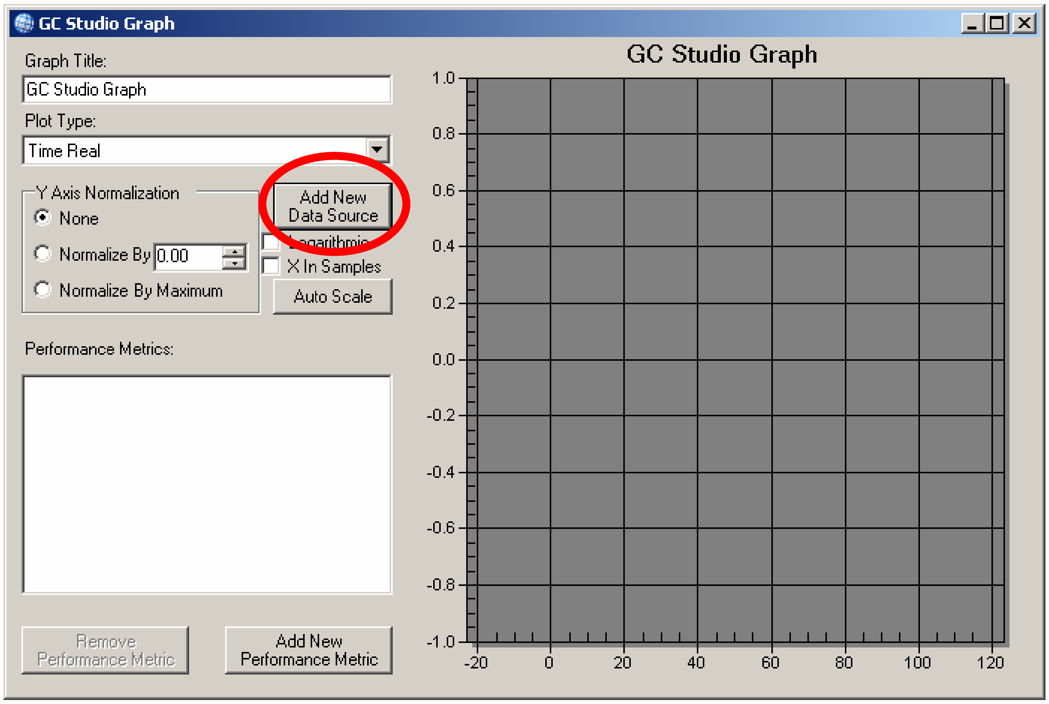
a_frequency	1
a_offset	0
b_frequency	0
b_offset	0
dither_ena	False
dither_mask	0
mixer_gain	PLUS_6dB
phase_add_a_lsb	0
phase_add_a_msb	0
phase_add_b_lsb	0
phase_add_b_msb	0
phase_offset_a	0
phase_offset_b	0
remix_only	False
ssel_dither	RX_SYNCA
ssel_freq	RX_SYNCA
ssel_nco	RX_SYNCA
ssel_phase	RX_SYNCA
zero_qsample	True

mixer_gain
Adds a fixed 6 dB of gain to the mixer output(before round and limiting) when asserted

Status

```
Turning ON the tristates for RXOUTs
---Build Complete!---
---Loading Program into GC101 and gc5018---
---Load Complete!---
"""Data Updated"""
Capture loop has terminated.
```

Click the Add New Data Source button on the graph panel.



GC Studio Graph

Graph Title: GC Studio Graph

Plot Type: Time Real

Y Axis Normalization

● None

○ Normalize By 0.00

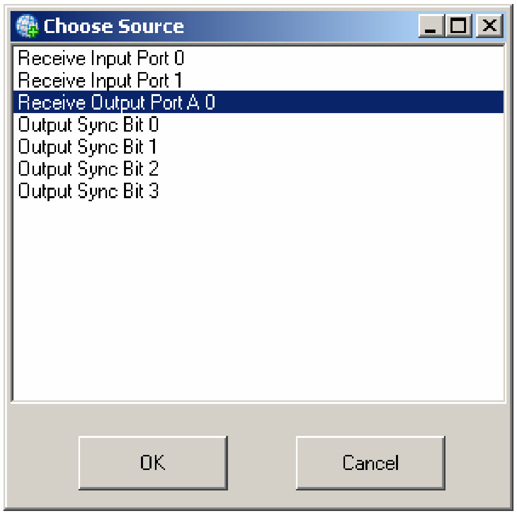
○ Normalize By Maximum

□ Logarithmic

□ X In Samples

Performance Metrics:

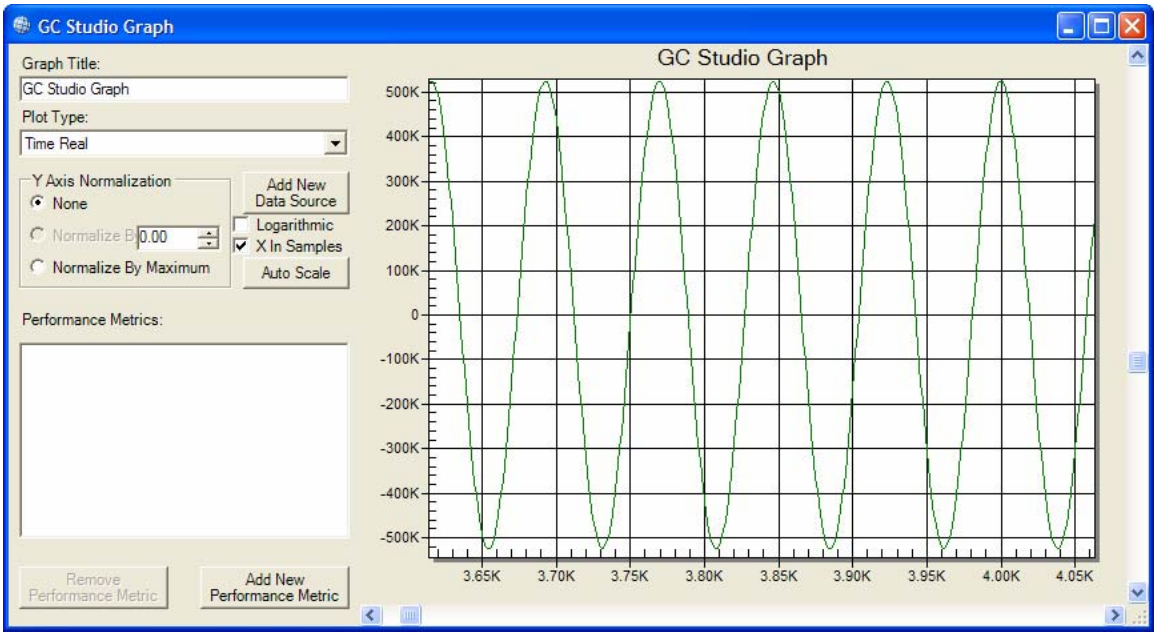
When the Test Bus is selected as the Output Mode, only the one Output Port is available. Select Receive Output Port A 0 and click OK.



Choose Source

Receive Input Port 0
Receive Input Port 1
Receive Output Port A 0
Output Sync Bit 0
Output Sync Bit 1
Output Sync Bit 2
Output Sync Bit 3

Click the X in Samples box. With the DDC0 NCO programmed for 1MHz, the output can be viewed in the graph panel. To zoom in, left click and drag in the graph – to zoom in this far, you'll need to zoom in a few times.


Graph Title: GC Studio Graph

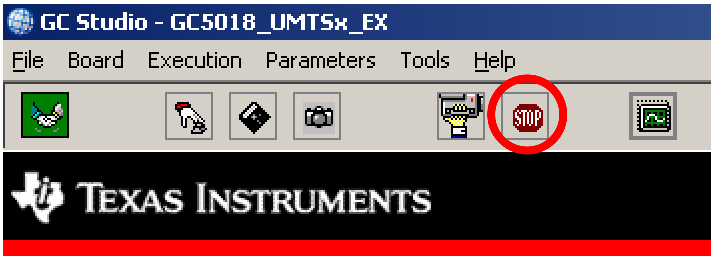
Plot Type: Time Real

Y Axis Normalization
● None
○ Normalize B 0.00
○ Normalize By Maximum

□ Logarithmic
☑ X In Samples

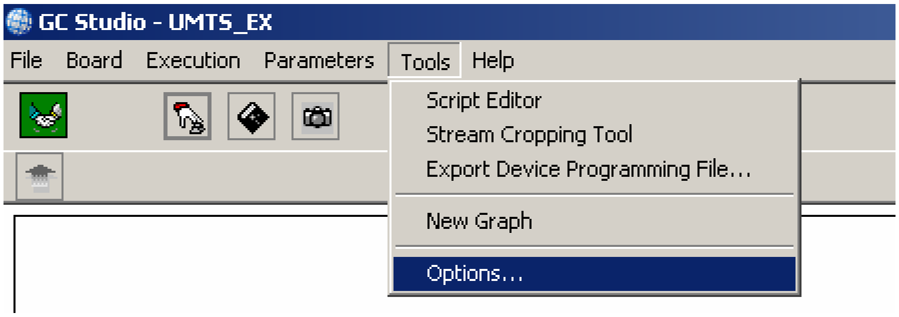
Performance Metrics:

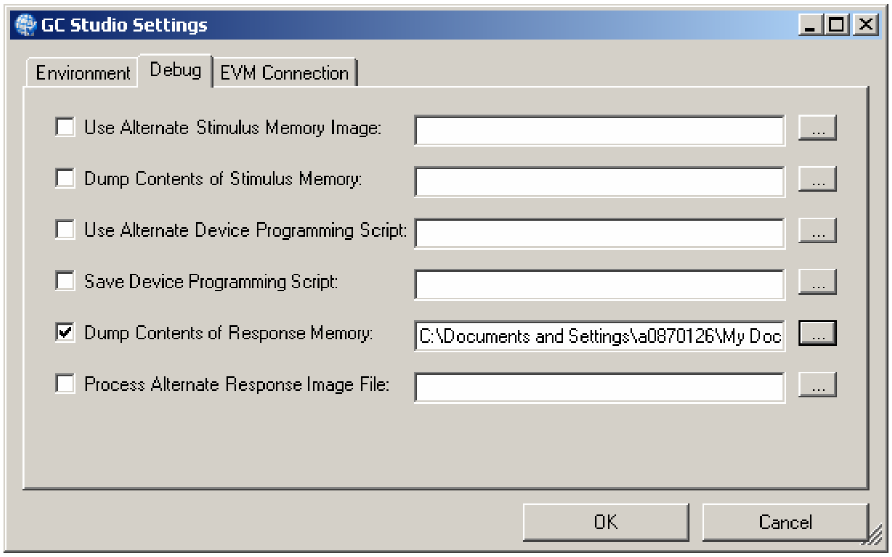
Stop the experiment, then select File > Save Project As … to save this project under a new name.



Close the Graph window.

The raw response memory can be captured in a text format by selecting the option in the Tools > Options window.





□ Use Alternate Stimulus Memory Image:

□ Dump Contents of Stimulus Memory:

□ Use Alternate Device Programming Script:

□ Save Device Programming Script:

☑ Dump Contents of Response Memory: C:\Documents and Settings\a0870126\My Doc

□ Process Alternate Response Image File:

The format of the file is hexadecimal, with the 32 bit response memory as the first 8 characters, a space, and then a single character for the other 4 special bits {sp7, sp6, sp5, syncout+}.

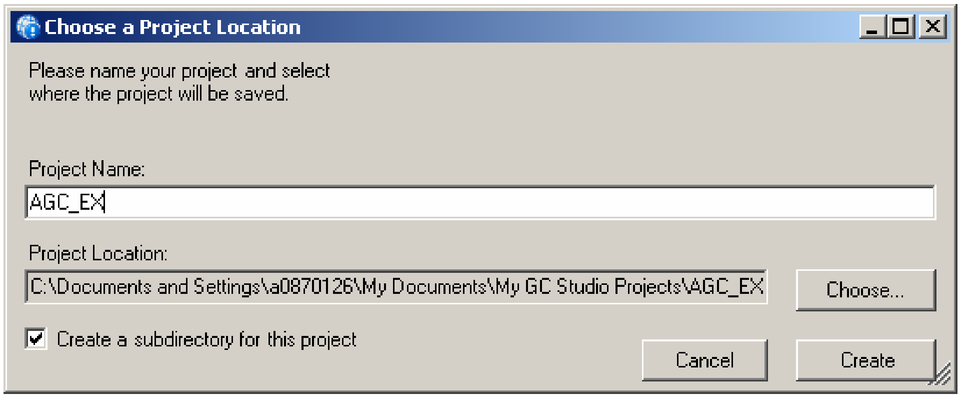
```
0000F0A0 0
0000F0A0 0
28D80000 0
28D80000 0
0000F2C6 0
0000F2C6 0
26750000 0
26750000 0
0000F580 0
0000F580 0
```

2.2.3. Creating a New GC Studio Project to exercise the Channel AGC

For this example, the new project will use the GC5018 self test circuits to force a constant as the input signal, set the channel NCO to generate a tone, and exercise the channel AGC function in CDMA mode.

Start GC Studio

Click on File > New Project to bring up the following window.



Choose a Project Location

Please name your project and select
where the project will be saved.

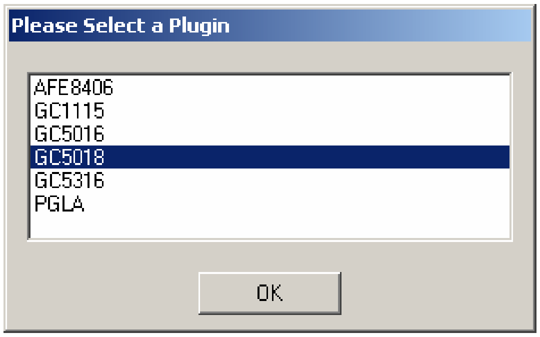
Project Name:
AGC_EX

Project Location:
C:\Documents and Settings\a0870126\My Documents\My GC Studio Projects\AGC_EX

☑ Create a subdirectory for this project

Choose a name for this new project, and click create.

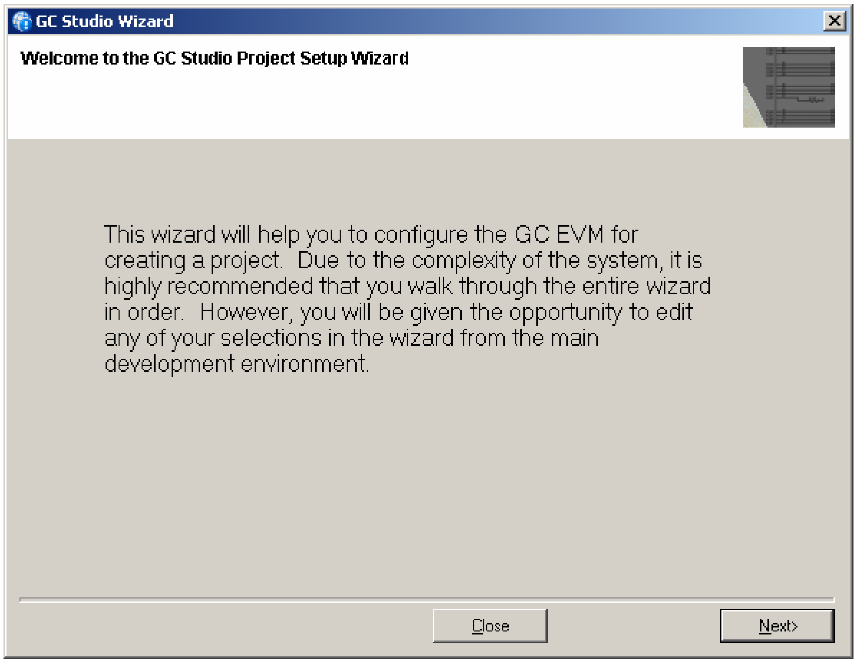
Select GC5018 for the Plugin and click OK. Click next on the following pop-up.



Please Select a Plugin

AFE8406
GC1115
GC5016
GC5018
GC5316
PGLA

Using the wizard style interface, setup the GC101 evaluation board, then click next.

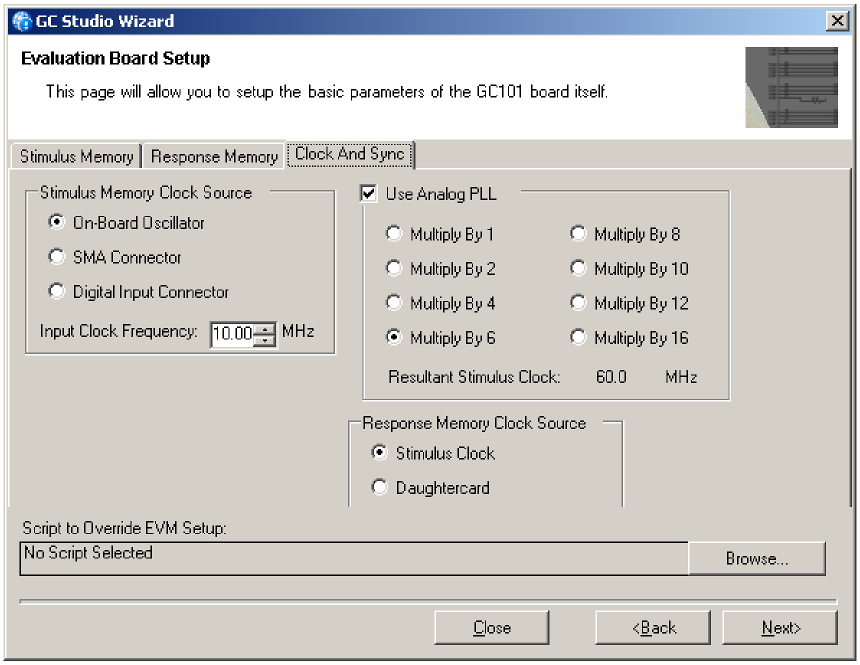


GC Studio Wizard

Welcome to the GC Studio Project Setup Wizard

This wizard will help you to configure the GC EVM for creating a project. Due to the complexity of the system, it is highly recommended that you walk through the entire wizard in order. However, you will be given the opportunity to edit any of your selections in the wizard from the main development environment.

Set up the Stimulus Memory and Response Memory parameters. Then, set up the clock parameters:



GC Studio Wizard

Evaluation Board Setup

This page will allow you to setup the basic parameters of the GC101 board itself.

Stimulus Memory Clock Source
● On-Board Oscillator
○ SMA Connector
○ Digital Input Connector

Input Clock Frequency: 10.00 MHz

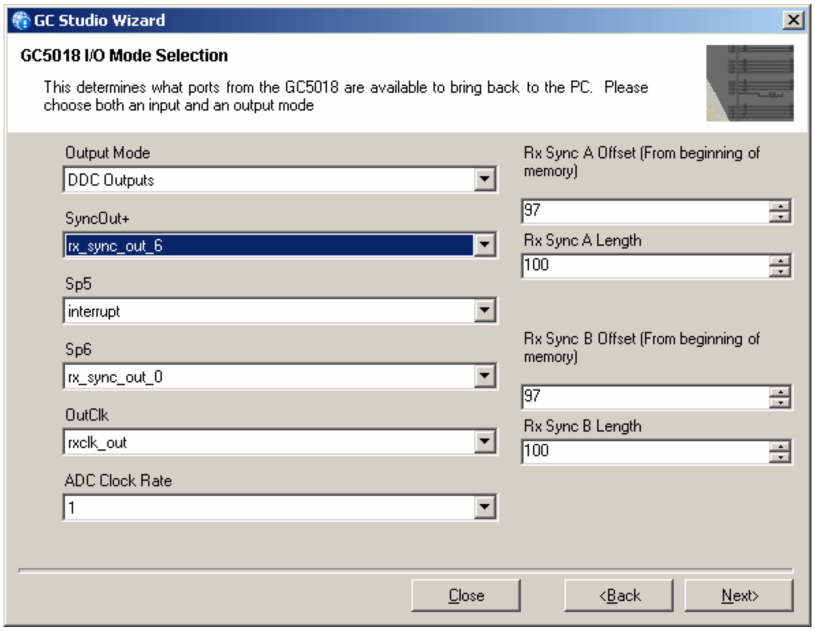
☑ Use Analog PLL
○ Multiply By 1 ○ Multiply By 8
○ Multiply By 2 ○ Multiply By 10
○ Multiply By 4 ○ Multiply By 12
● Multiply By 6 ○ Multiply By 16

Resultant Stimulus Clock: 60.0 MHz

Response Memory Clock Source
● Stimulus Clock
○ Daughtercard

Script to Override EVM Setup: No Script Selected

Setup the GC5018 I/O mode selection and click next.



GC5018 I/O Mode Selection

This determines what ports from the GC5018 are available to bring back to the PC. Please choose both an input and an output mode

Output Mode: DDC Outputs

SyncOut+: rx_sync_out_6

Sp5: interrupt

Sp6: rx_sync_out_0

OutClk: rxclk_out

ADC Clock Rate: 1

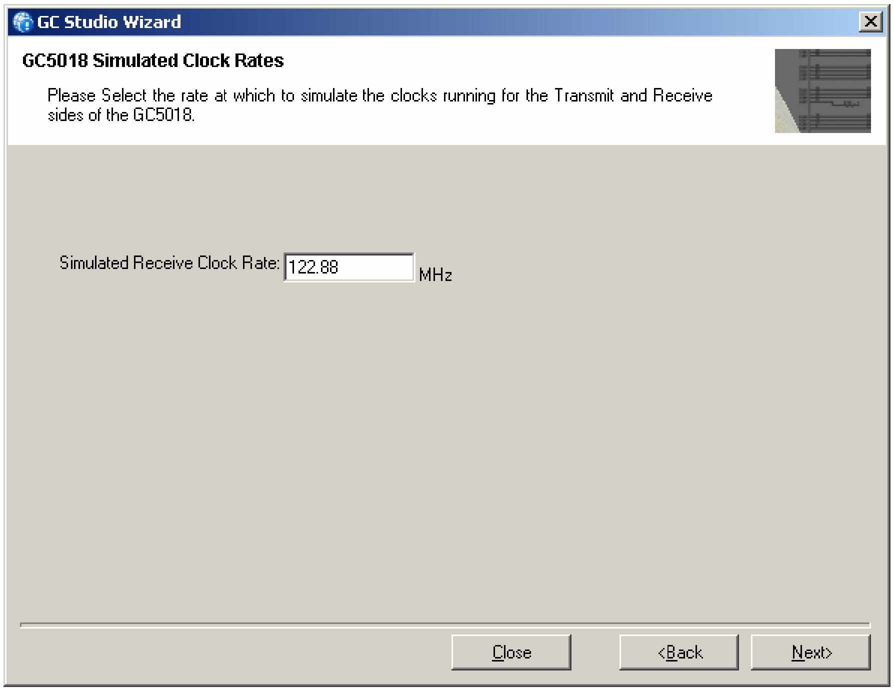
Rx Sync A Offset (From beginning of memory): 97

Rx Sync A Length: 100

Rx Sync B Offset (From beginning of memory): 97

Rx Sync B Length: 100

Set the simulated clock rate to 122.88MHz and click next.

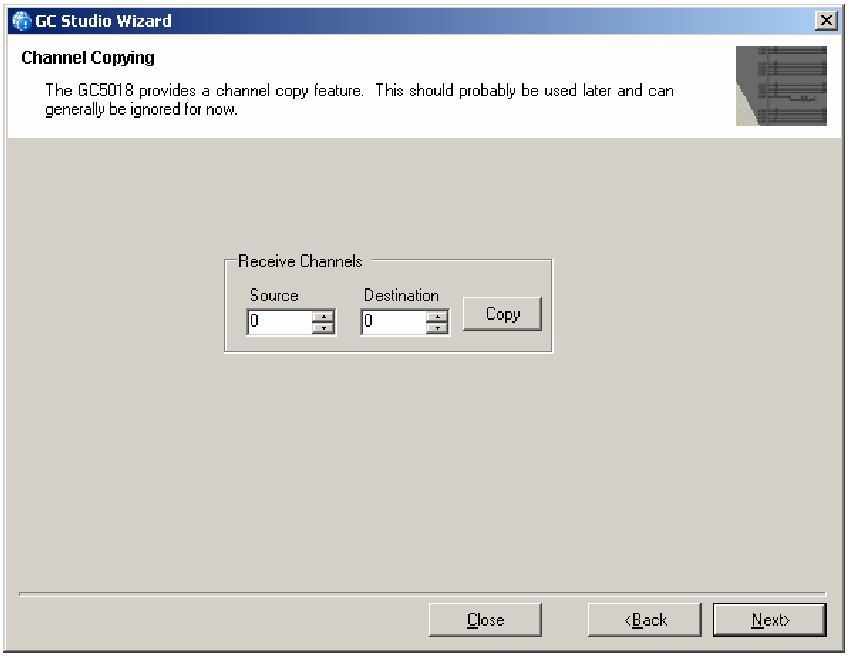


GC5018 Simulated Clock Rates

Please Select the rate at which to simulate the clocks running for the Transmit and Receive sides of the GC5018.

Simulated Receive Clock Rate: 122.88 MHz

Click Next on Channel Copying.



GC Studio Wizard

Channel Copying

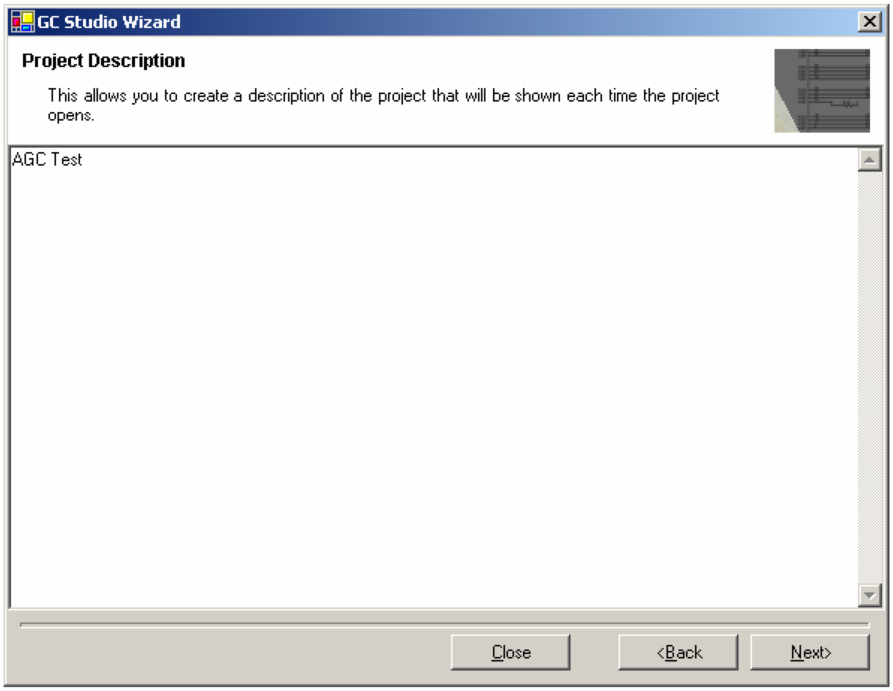
The GC5018 provides a channel copy feature. This should probably be used later and can generally be ignored for now.

Receive Channels

Source: 0

Destination: 0

Click Next



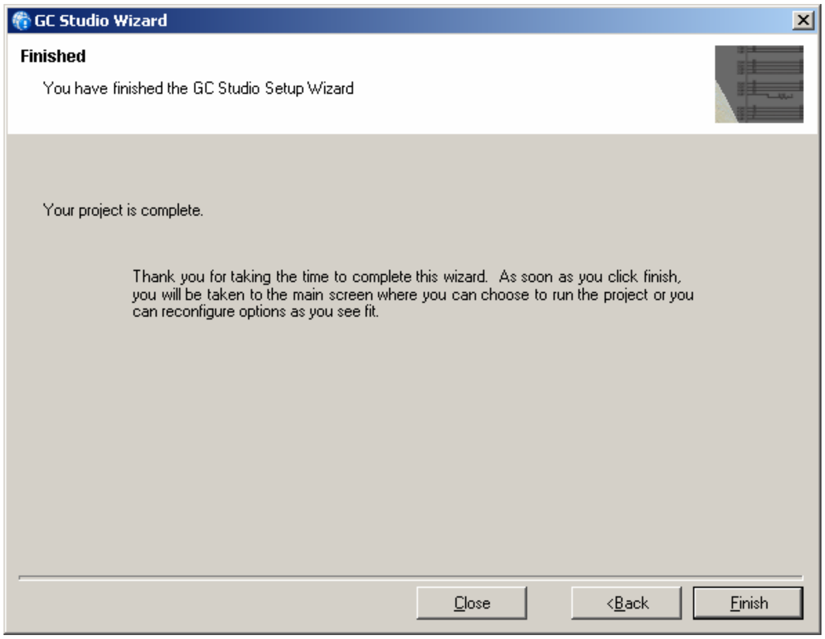
GC Studio Wizard

Project Description

This allows you to create a description of the project that will be shown each time the project opens.

AGC Test

Project Description allows user to enter a brief description of the project including the key parameters. When done, click Next.



Finished

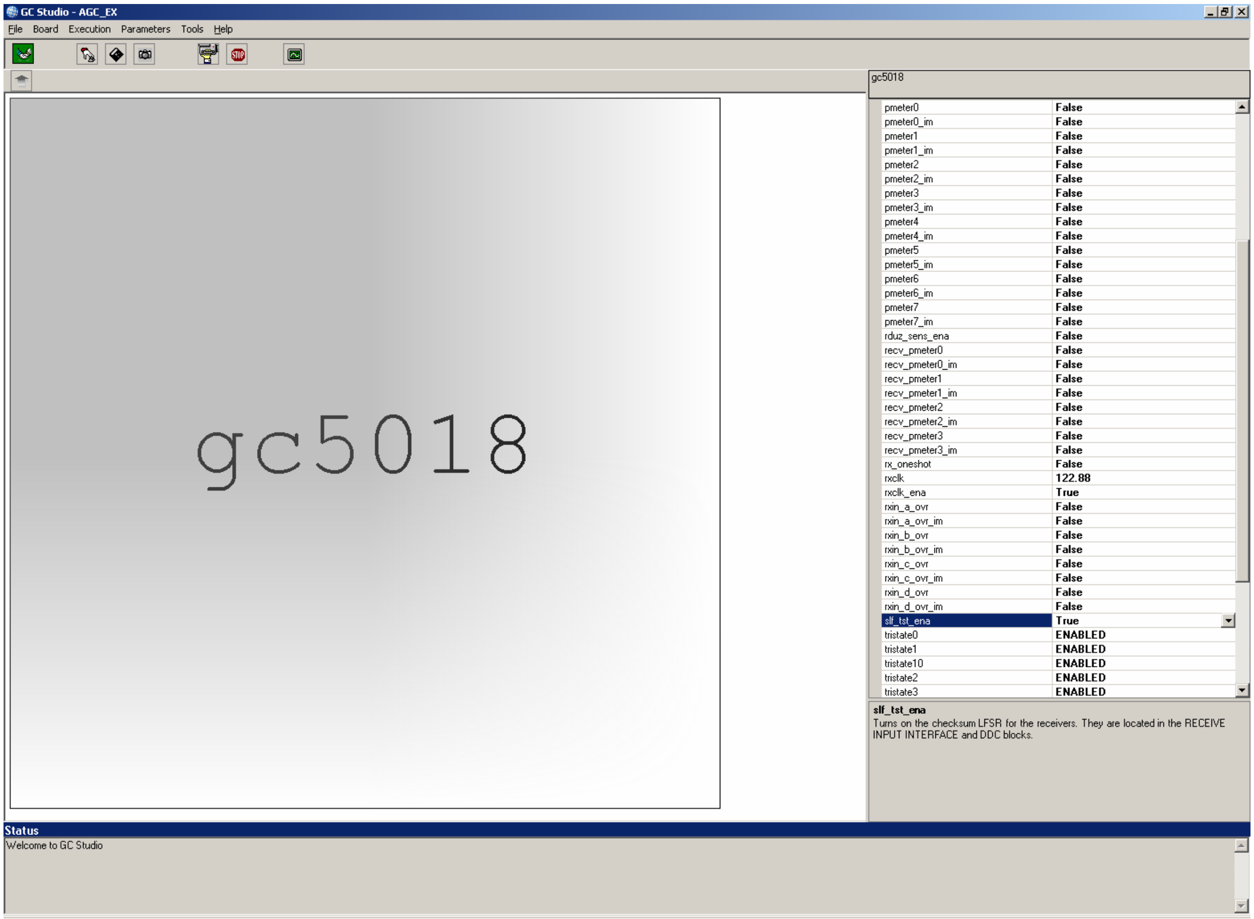
You have finished the GC Studio Setup Wizard

Your project is complete.

Thank you for taking the time to complete this wizard. As soon as you click finish, you will be taken to the main screen where you can choose to run the project or you can reconfigure options as you see fit.

Click Finish.

Click on the large gc5018 box to display the global control registers. Set slf_tst_ena to True to enable the self test circuits.

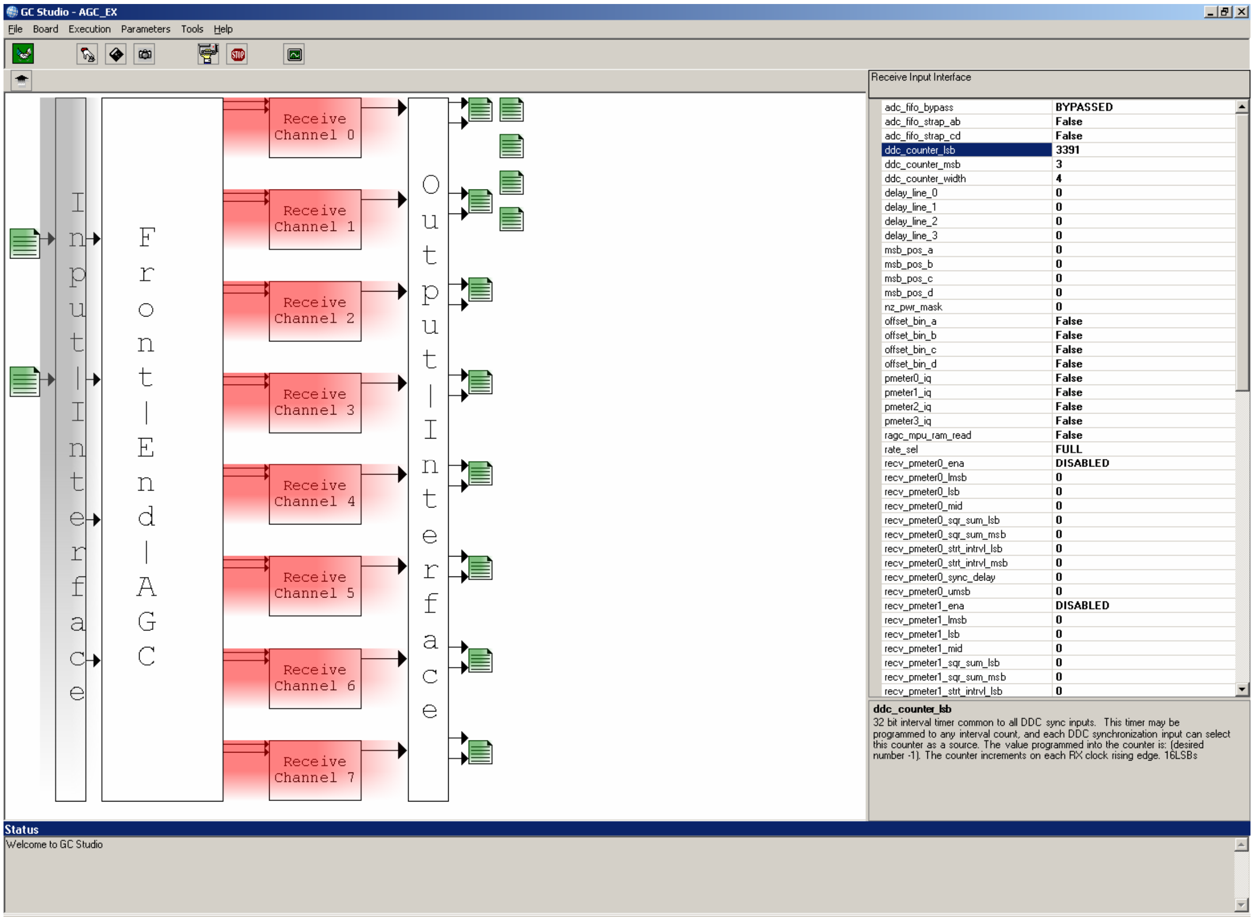


pmeter0	False
pmeter0_im	False
pmeter1	False
pmeter1_im	False
pmeter2	False
pmeter2_im	False
pmeter3	False
pmeter3_im	False
pmeter4	False
pmeter4_im	False
pmeter5	False
pmeter5_im	False
pmeter6	False
pmeter6_im	False
pmeter7	False
pmeter7_im	False
rduz_sens_ena	False
recv_pmeter0	False
recv_pmeter0_im	False
recv_pmeter1	False
recv_pmeter1_im	False
recv_pmeter2	False
recv_pmeter2_im	False
recv_pmeter3	False
recv_pmeter3_im	False
rx_oneshot	False
rxclk	122.88
rxclk_ena	True
rxin_a_ovr	False
rxin_a_ovr_im	False
rxin_b_ovr	False
rxin_b_ovr_im	False
rxin_c_ovr	False
rxin_c_ovr_im	False
rxin_d_ovr	False
rxin_d_ovr_im	False
slf_tst_ena	True
tristate0	ENABLED
tristate1	ENABLED
tristate10	ENABLED
tristate2	ENABLED
tristate3	ENABLED

slf_tst_ena
Turns on the checksum LFSR for the receivers. They are located in the RECEIVE INPUT INTERFACE and DDC blocks.

Welcome to GC Studio

Next, double click on the gc5018 block to “push down” one level into the gc5018. Click on the Input Interface block to display and edit the receive input interface registers. The DDC counter will be used in this experiment to internally generate a repetitive synchronization pulse. Program the adc_fifo_bypass to BYPASSED, the ddc_counter_width to 4, the ddc_counter_msb to 3 and the ddc_counter_lsb to 3391.



Receive Input Interface

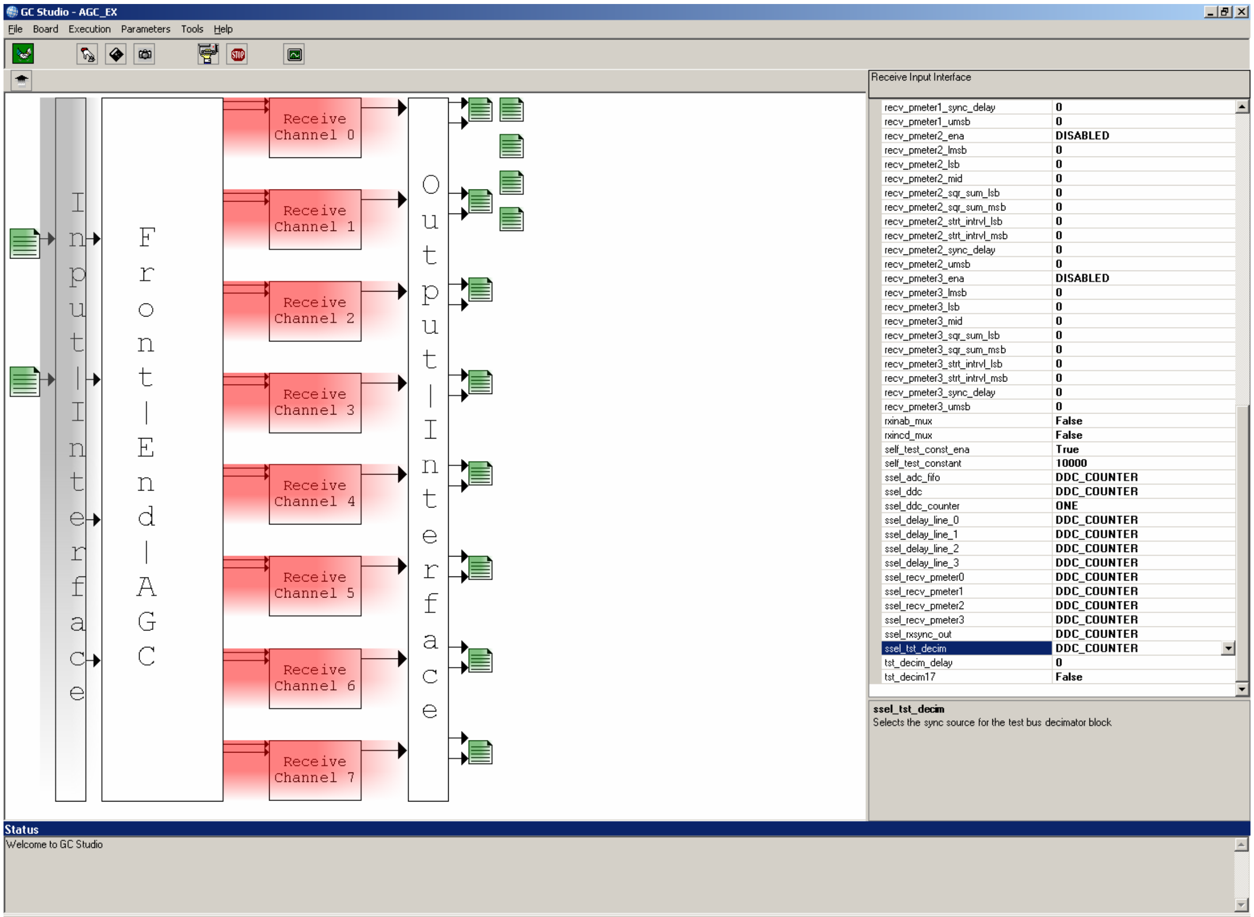
adc_fifo_bypass	BYPASSED
adc_fifo_strap_ab	False
adc_fifo_strap_cd	False
ddc_counter_lsb	3391
ddc_counter_msb	3
ddc_counter_width	4
delay_line_0	0
delay_line_1	0
delay_line_2	0
delay_line_3	0
msb_pos_a	0
msb_pos_b	0
msb_pos_c	0
msb_pos_d	0
nz_pwr_mask	0
offset_bin_a	False
offset_bin_b	False
offset_bin_c	False
offset_bin_d	False
pmeter0_iq	False
pmeter1_iq	False
pmeter2_iq	False
pmeter3_iq	False
ragc_mpu_ram_read	False
rate_sel	FULL
recv_pmeter0_ena	DISABLED
recv_pmeter0_lmsb	0
recv_pmeter0_lsb	0
recv_pmeter0_mid	0
recv_pmeter0_sqr_sum_lsb	0
recv_pmeter0_sqr_sum_msb	0
recv_pmeter0_strt_intrvl_lsb	0
recv_pmeter0_strt_intrvl_msb	0
recv_pmeter0_sync_delay	0
recv_pmeter0_umsb	0
recv_pmeter1_ena	DISABLED
recv_pmeter1_lmsb	0
recv_pmeter1_lsb	0
recv_pmeter1_mid	0
recv_pmeter1_sqr_sum_lsb	0
recv_pmeter1_sqr_sum_msb	0
recv_pmeter1_strt_intrvl_lsb	0

ddc_counter_lsb
32 bit interval timer common to all DDC sync inputs. This timer may be programmed to any interval count, and each DDC synchronization input can select this counter as a source. The value programmed into the counter is: (desired number -1). The counter increments on each RX clock rising edge. 16LSBs

Welcome to GC Studio

With the Input Interface block still selected, scroll down (using the scroll bar at the right edge of the window) and set the remaining registers. Set the self_test_const_ena register to True, and the self_test_constant to 10000. These settings will replace the input data normally presented at the rxin_a/b/c/d input ports with an internally generated constant value.

Set the ssel_adc_fifo, ssel_ddc, ssel_delay_line_0, ssel_delay_line_1, ssel_delay_line_2, ssel_delay_line_3, ssel_recv_pmeter0, ssel_ recv_pmeter1, ssel_ recv_pmeter2, ssel_ recv_pmeter3, ssel_rxsync_out and ssel_tst_decim to DDC_COUNTER. Set ssel_ddc_counter to ONE.



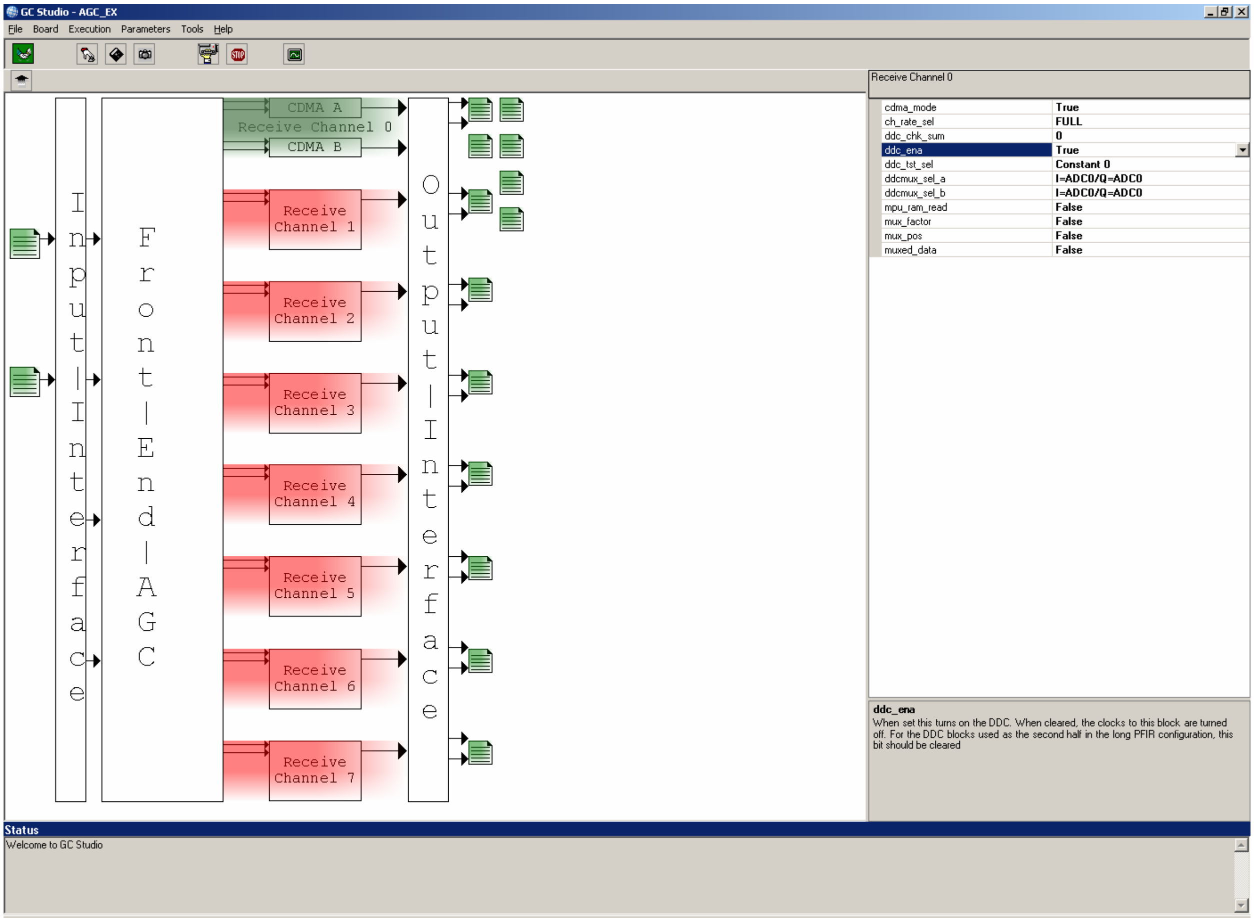
Receive Input Interface

recv_pmeter1_sync_delay	0
recv_pmeter1_umsb	0
recv_pmeter2_ena	DISABLED
recv_pmeter2_lmsb	0
recv_pmeter2_lsb	0
recv_pmeter2_mid	0
recv_pmeter2_sqr_sum_lsb	0
recv_pmeter2_sqr_sum_msb	0
recv_pmeter2_strt_intrvl_lsb	0
recv_pmeter2_strt_intrvl_msb	0
recv_pmeter2_sync_delay	0
recv_pmeter2_umsb	0
recv_pmeter3_ena	DISABLED
recv_pmeter3_lmsb	0
recv_pmeter3_lsb	0
recv_pmeter3_mid	0
recv_pmeter3_sqr_sum_lsb	0
recv_pmeter3_sqr_sum_msb	0
recv_pmeter3_strt_intrvl_lsb	0
recv_pmeter3_strt_intrvl_msb	0
recv_pmeter3_sync_delay	0
recv_pmeter3_umsb	0
rxinab_mux	False
rxincd_mux	False
self_test_const_ena	True
self_test_constant	10000
ssel_adc_fifo	DDC_COUNTER
ssel_ddc	DDC_COUNTER
ssel_ddc_counter	ONE
ssel_delay_line_0	DDC_COUNTER
ssel_delay_line_1	DDC_COUNTER
ssel_delay_line_2	DDC_COUNTER
ssel_delay_line_3	DDC_COUNTER
ssel_recv_pmeter0	DDC_COUNTER
ssel_recv_pmeter1	DDC_COUNTER
ssel_recv_pmeter2	DDC_COUNTER
ssel_recv_pmeter3	DDC_COUNTER
ssel_rxsync_out	DDC_COUNTER
ssel_tst_decim	DDC_COUNTER
tst_decim_delay	0
tst_decim17	False

ssel_tst_decim
Selects the sync source for the test bus decimator block

Welcome to GC Studio

Click on the upper Receive Channel 0 block , the top most red block in the previous picture. Set cdma_mode to True and ddc_ena to True. The top most receive channel will be re-drawn as a split (or shared CDMA channel) and changed to green since it has been enabled. The split Receive Channel 0 figure indicates channel 0 is configured to process two CDMA streams.



Receive Channel 0

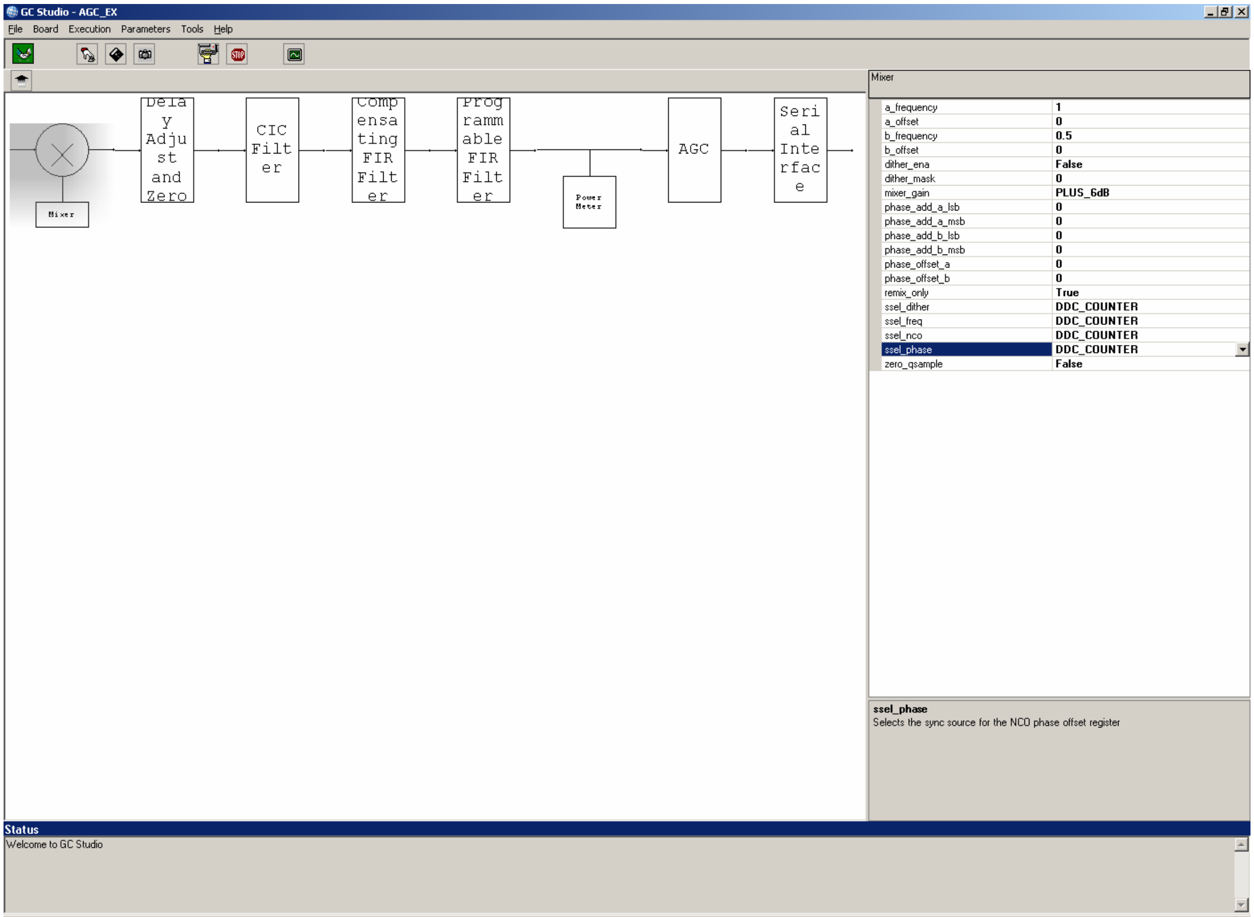
cdma_mode	True
ch_rate_sel	FULL
ddc_chk_sum	0
ddc_ena	True
ddc_tst_sel	Constant 0
ddcmux_sel_a	I=ADC0/Q=ADC0
ddcmux_sel_b	I=ADC0/Q=ADC0
mpu_ram_read	False
mux_factor	False
mux_pos	False
muxed_data	False

ddc_ena
When set this turns on the DDC. When cleared, the clocks to this block are turned off. For the DDC blocks used as the second half in the long PFIR configuration, this bit should be cleared

Welcome to GC Studio

Double click on the split Receive Channel 0 block to push down into this channel. The block diagram now shows the sub blocks in the receive channel, and the registers to configure it.

Select the mixer/nco block (left most block). In CDMA mode, the receive channel processed two streams, listed in the registers as a and b settings. Set the a_frequency to 1 MHz and the b_frequency to 0.5 MHz as shown below. *GC Studio will calculate the required values for the phase_add registers after the experiment has been run.* Set the ssel_dither, ssel_freq, ssel_nco and ssel_phase to DDC_COUNTER. Set remix_only to True.



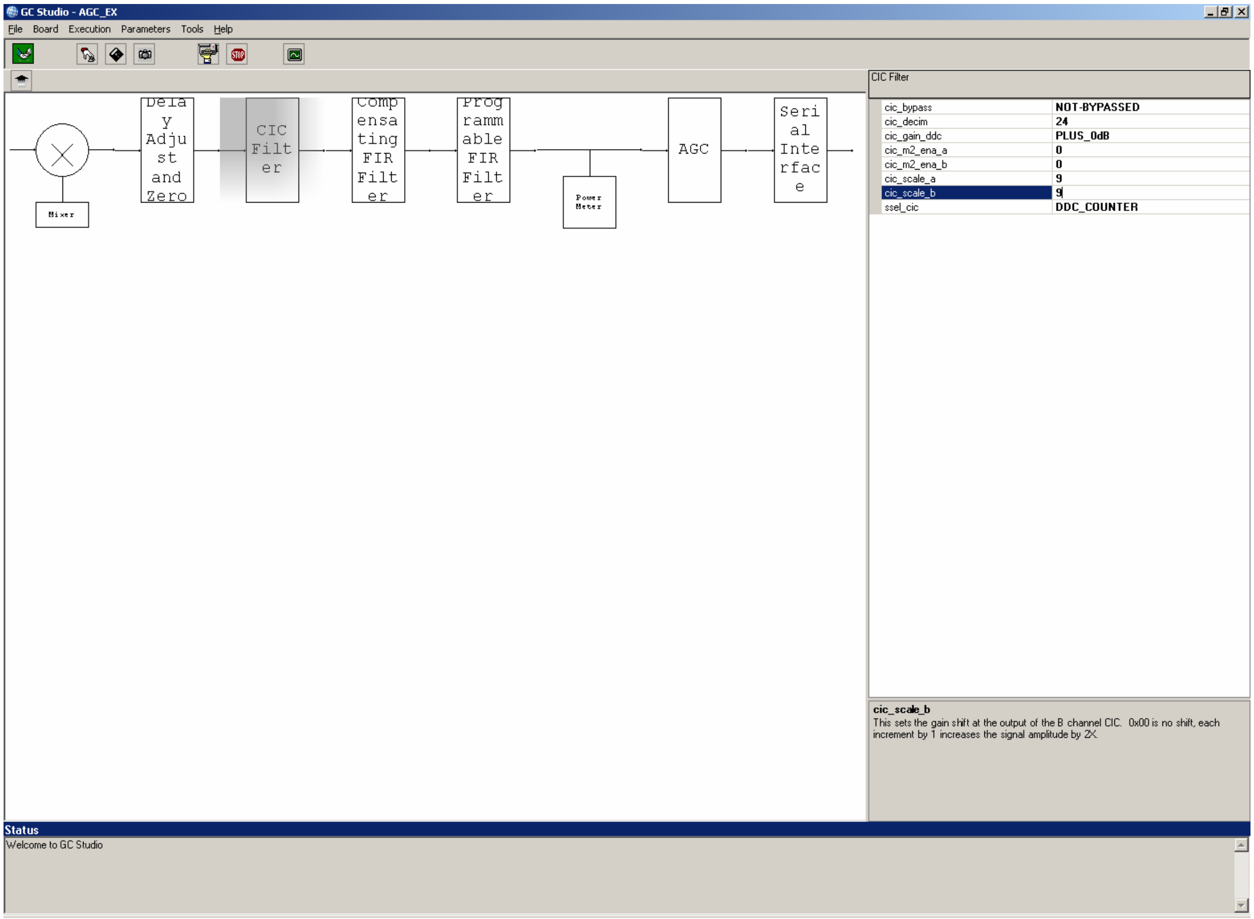
Mixer

a_frequency	1
a_offset	0
b_frequency	0.5
b_offset	0
dither_ena	False
dither_mask	0
mixer_gain	PLUS_6dB
phase_add_a_lsb	0
phase_add_a_msb	0
phase_add_b_lsb	0
phase_add_b_msb	0
phase_offset_a	0
phase_offset_b	0
remix_only	True
ssel_dither	DDC_COUNTER
ssel_freq	DDC_COUNTER
ssel_nco	DDC_COUNTER
ssel_phase	DDC_COUNTER
zero_qsample	False

ssel_phase
Selects the sync source for the NCO phase offset register

Welcome to GC Studio

Click on the CIC filter block and set the registers as shown in the following panel.



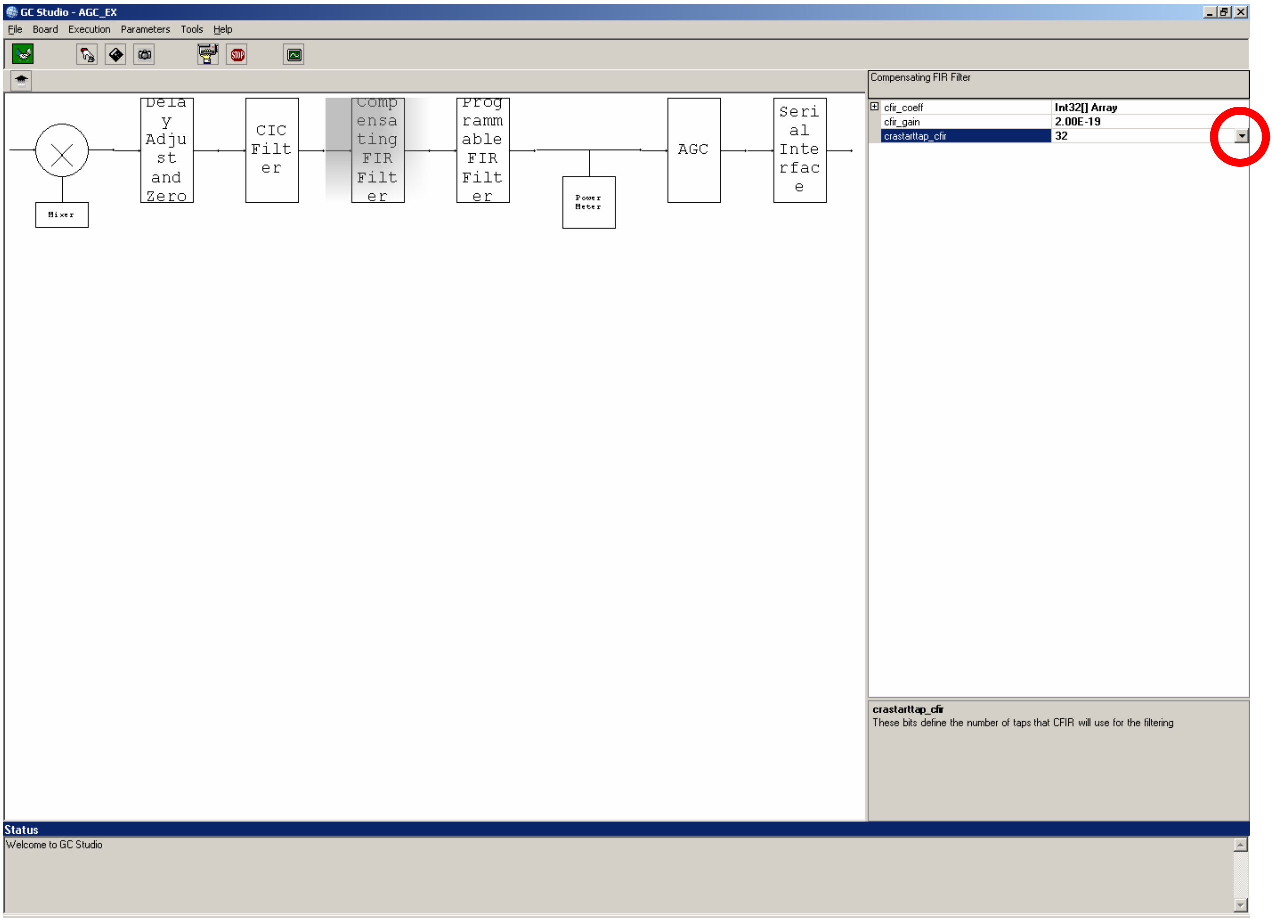
CIC Filter

cic_bypass	NOT-BYPASSED
cic_decim	24
cic_gain_ddc	PLUS_0dB
cic_m2_ena_a	0
cic_m2_ena_b	0
cic_scale_a	9
cic_scale_b	9
ssel_cic	DDC_COUNTER

cic_scale_b
This sets the gain shift at the output of the B channel CIC. 0x00 is no shift, each increment by 1 increases the signal amplitude by 2X.

Status
Welcome to GC Studio

Select the CFIR block and set the cfir_gain to 2.00E-19, and the cra_starttap_cfir to 32.



Compensating FIR Filter

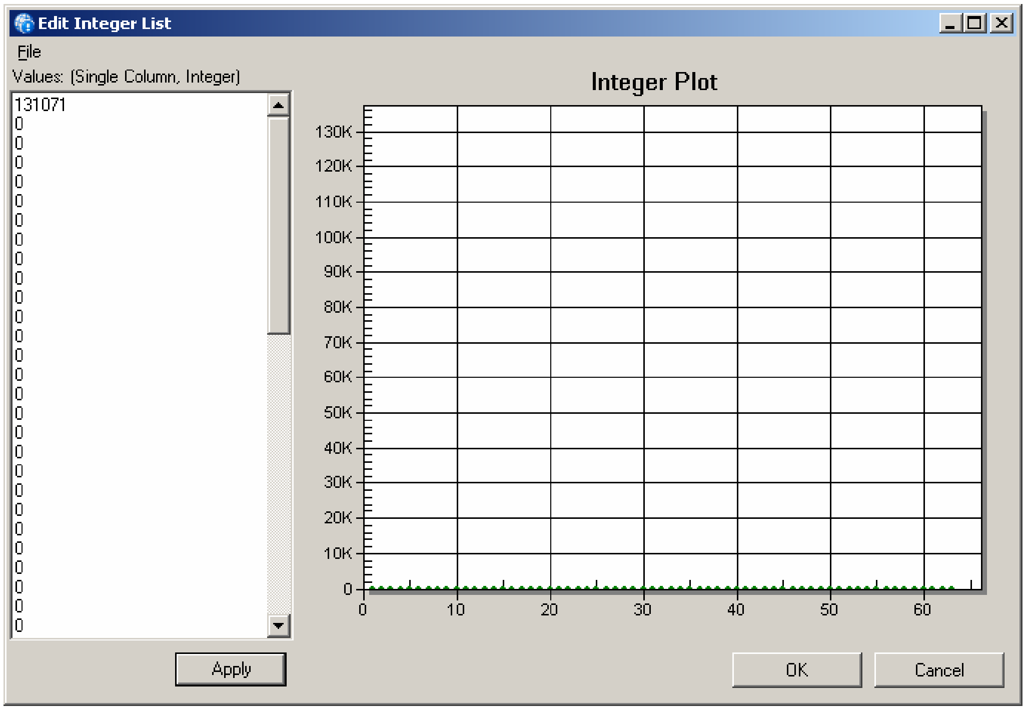
⊞ cfir_coeff	**Int32[] Array**
cfir_gain	**2.00E-19**
crastarttap_cfir	**32**

crastarttap_cfir
These bits define the number of taps that CFIR will use for the filtering

Welcome to GC Studio

Next, select the cfir_coeff register setting by clicking on it, and then click on the browse button, circled in red on the panel above, to open the Edit Filter window and fill in the CFIR filter tap weights.

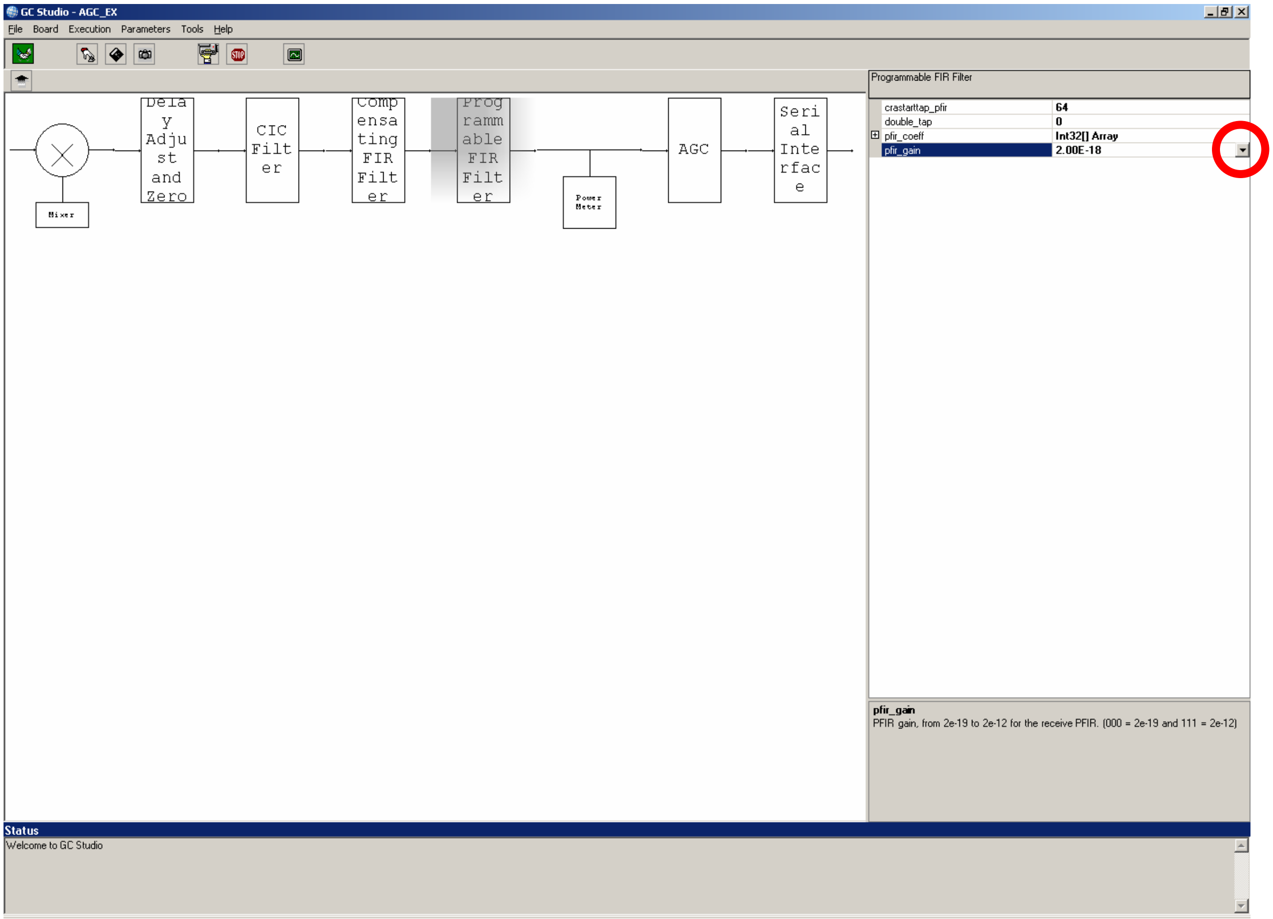
For this project, we will set just the first tap weight to full scale (131071) and the 63 others to zero. Click OK after entering all the values.



Values: (Single Column, Integer)

```
131071
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
```

Select the PFIR block, set the pfir_gain to 2.00E-18, and crastarttap_pfir to 64. Select the pfir_coeff register, and again select the browse button.



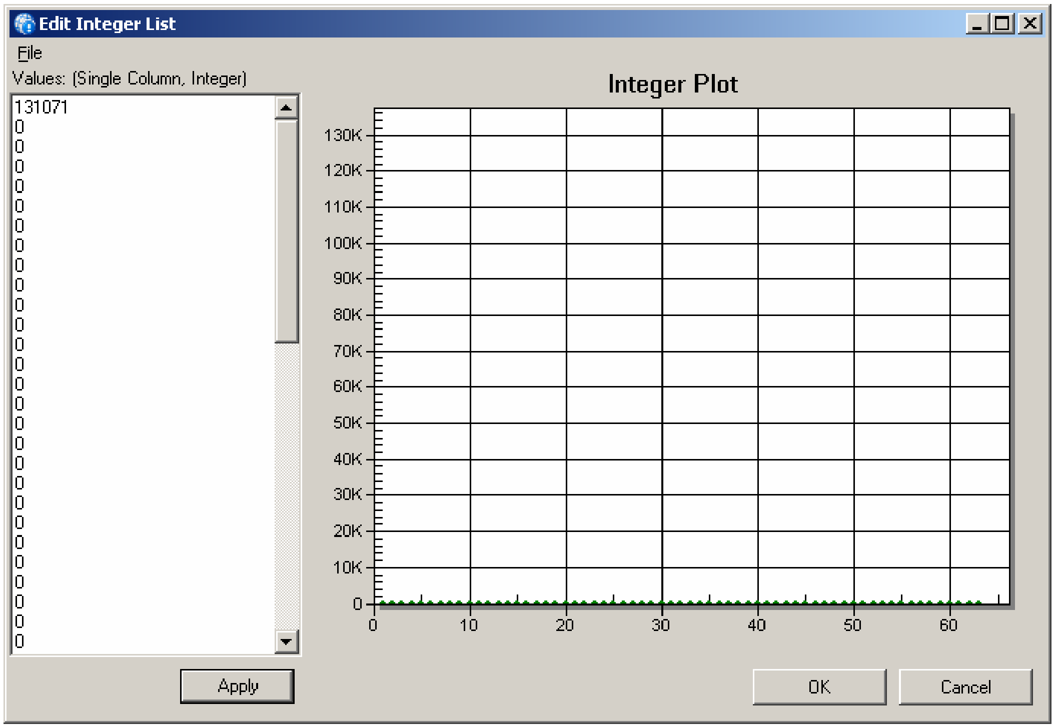
Programmable FIR Filter

crastarttap_pfir	64
double_tap	0
⊞ pfir_coeff	Int32[] Array
pfir_gain	2.00E-18

pfir_gain
PFIR gain, from 2e-19 to 2e-12 for the receive PFIR. (000 = 2e-19 and 111 = 2e-12)

Welcome to GC Studio

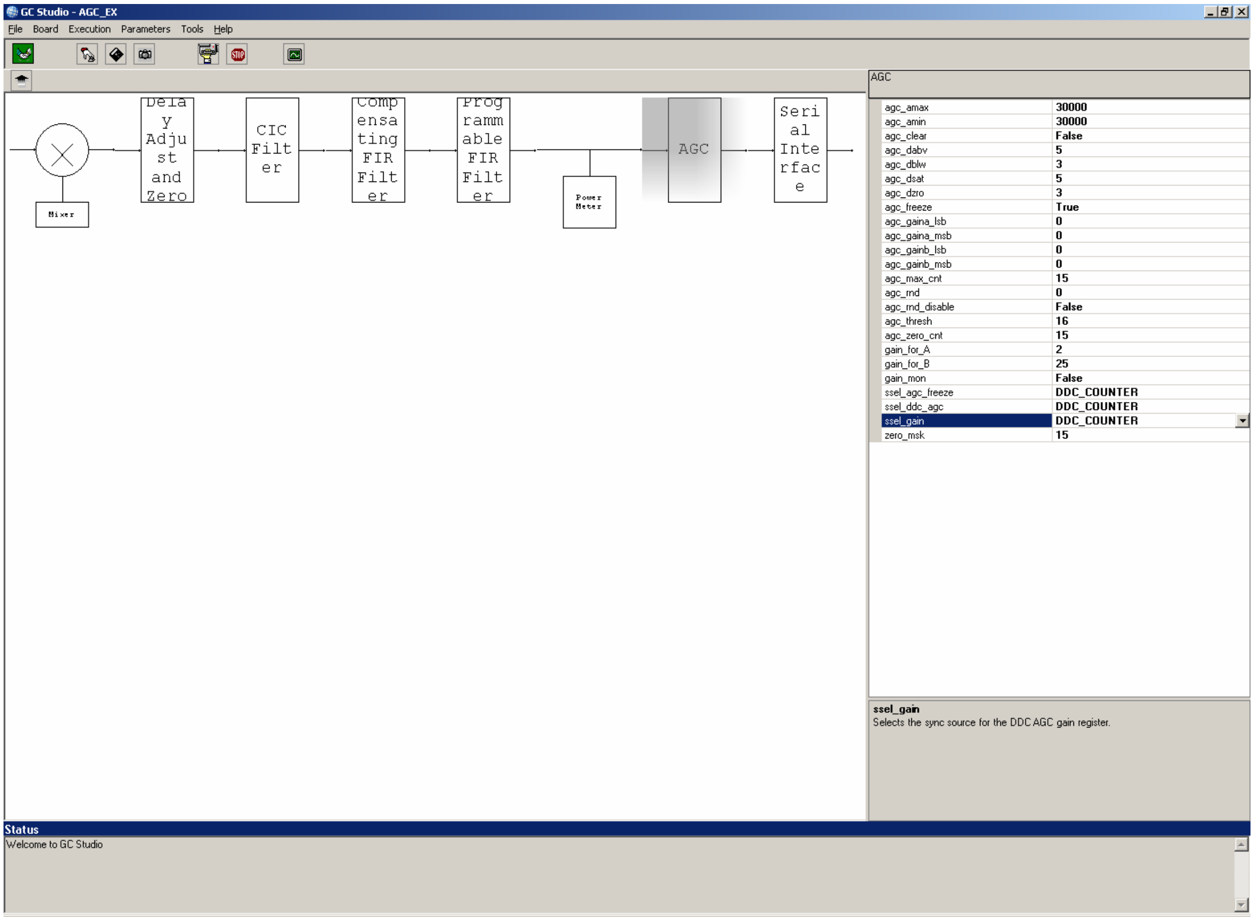
Set just the first tap weight to full scale (131071) and 63 other to zero in the Edit Filter panel.



Values: (Single Column, Integer)

```
131071
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
0
```

Select the AGC block and set the registers as shown in the panel below.



AGC

agc_amax	30000
agc_amin	30000
agc_clear	False
agc_dabv	5
agc_dblw	3
agc_dsat	5
agc_dzro	3
agc_freeze	True
agc_gaina_lsb	0
agc_gaina_msb	0
agc_gainb_lsb	0
agc_gainb_msb	0
agc_max_cnt	15
agc_rnd	0
agc_rnd_disable	False
agc_thresh	16
agc_zero_cnt	15
gain_for_A	2
gain_for_B	25
gain_mon	False
ssel_agc_freeze	DDC_COUNTER
ssel_ddc_agc	DDC_COUNTER
ssel_gain	DDC_COUNTER
zero_msk	15

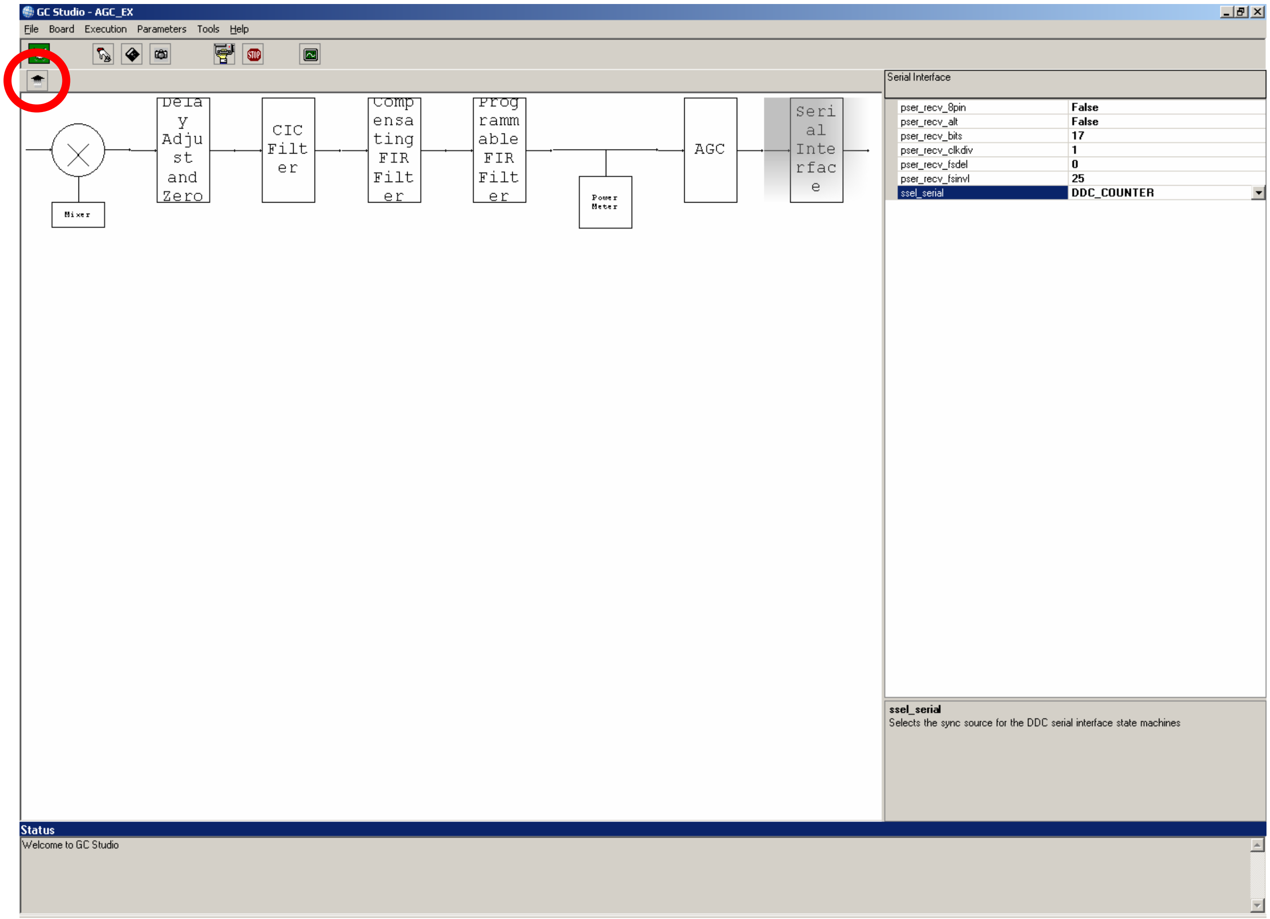
ssel_gain
Selects the sync source for the DDC AGC gain register.

Status
Welcome to GC Studio

The gain_for_A value is set to an initial gain of 2 which will produce a signal much lower than the target signal level. GC Studio converts this variable to the appropriate register setting for agc_gaina_msb and agc_gain_lsb. Similarly, the gain_for_B value is set to 25 which will produce a signal much larger than the target signal level. *GC Studio will calculate the required values for the agc_gaina_lsb, agc_gaina_msb, agc_gainb_lsb and agc_gainb_msb registers after the experiment has been run.*

Each time the DDC_COUNTER initializes the AGC, the loop will respond to the signal level present and increase the a channel gain while decreasing the b channel gain.

Select the Serial Interface block and set the parameters as indicated.



Serial Interface

pser_recv_8pin	False
pser_recv_alt	False
pser_recv_bits	17
pser_recv_clkdiv	1
pser_recv_fsdel	0
pser_recv_fsinvl	25
ssel_serial	DDC_COUNTER

ssel_serial
Selects the sync source for the DDC serial interface state machines

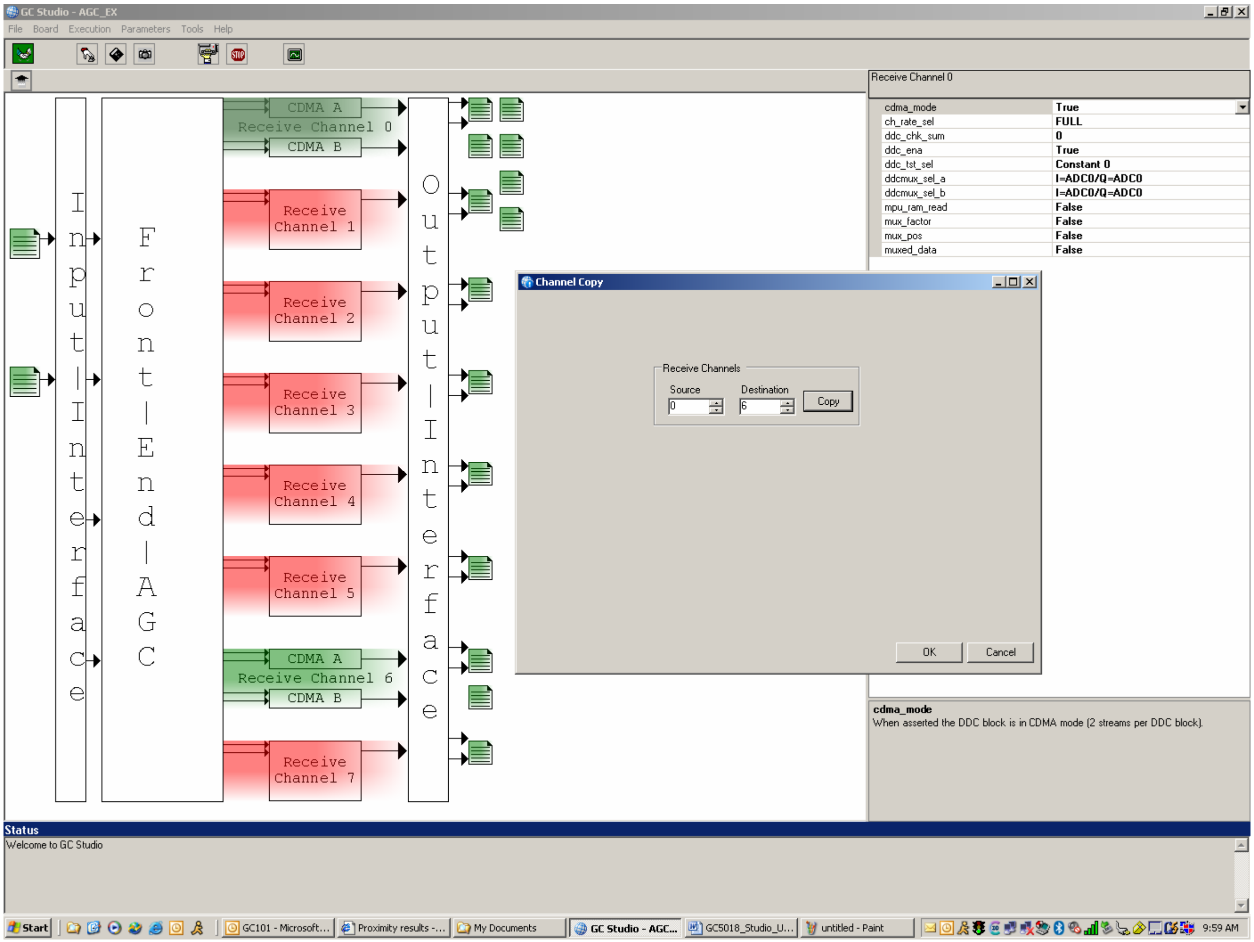
Welcome to GC Studio

After verifying the values for the serial interface, click the arrow circled in red in panel above to pop up one level in the GC5018 hierarchy.

Receive Channel 0 has now been configured to generate sinusoidal inputs using a constant and the nco block. The CIC is configured to decimate by 25, and the CFIR and PFIR filters are programmed with a single full scale non-zero coefficient to pass the decimated sinusoids to the AGC block.

The GC5018 daughter card configuration uses rx_sync_out_6 as the strobe indicating when the serial output data starts each transfer. We'll copy the receive channel 0 configuration to receive channel 6 so the strobe will be present in the captured GC101 data.

Select Parameters > GC5018 Channel Copy to bring up the Channel Copy panel below. With channel 0 is selected as the source, and channel 6 is selected as the destination, click Copy, and then click OK.



Receive Channel 0

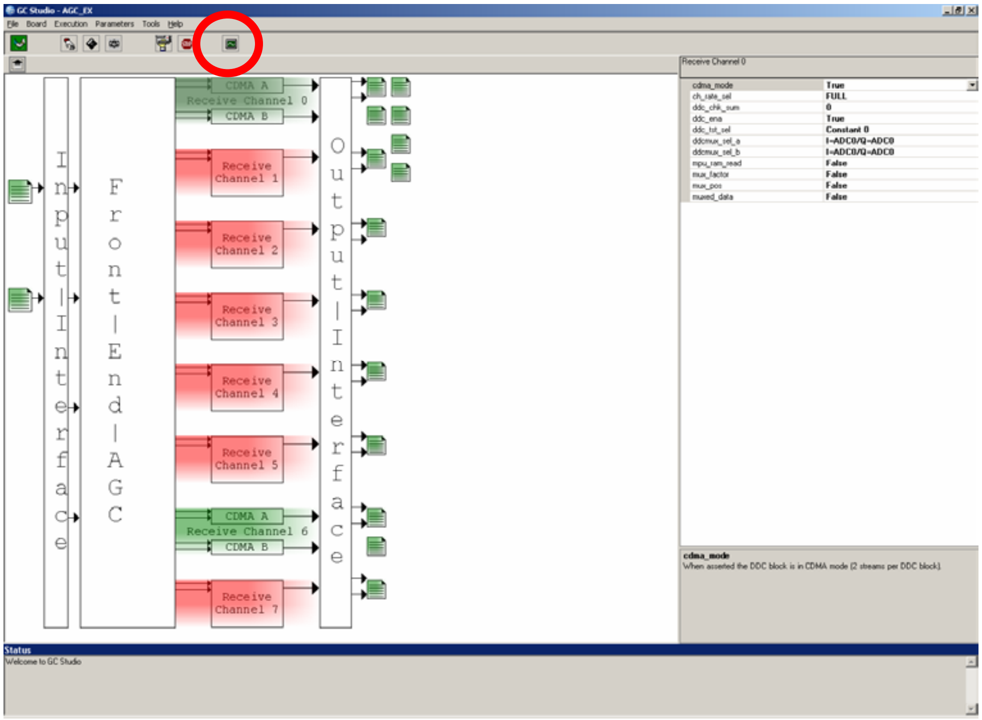
cdma_mode	True
ch_rate_sel	FULL
ddc_chk_sum	0
ddc_ena	True
ddc_tst_sel	Constant 0
ddcmux_sel_a	I=ADC0/Q=ADC0
ddcmux_sel_b	I=ADC0/Q=ADC0
mpu_ram_read	False
mux_factor	False
mux_pos	False
muxed_data	False

Source: 0
Destination: 6

cdma_mode
When asserted the DDC block is in CDMA mode (2 streams per DDC block).

Welcome to GC Studio

The block diagram should now show both channels 0 and 6 active (green).



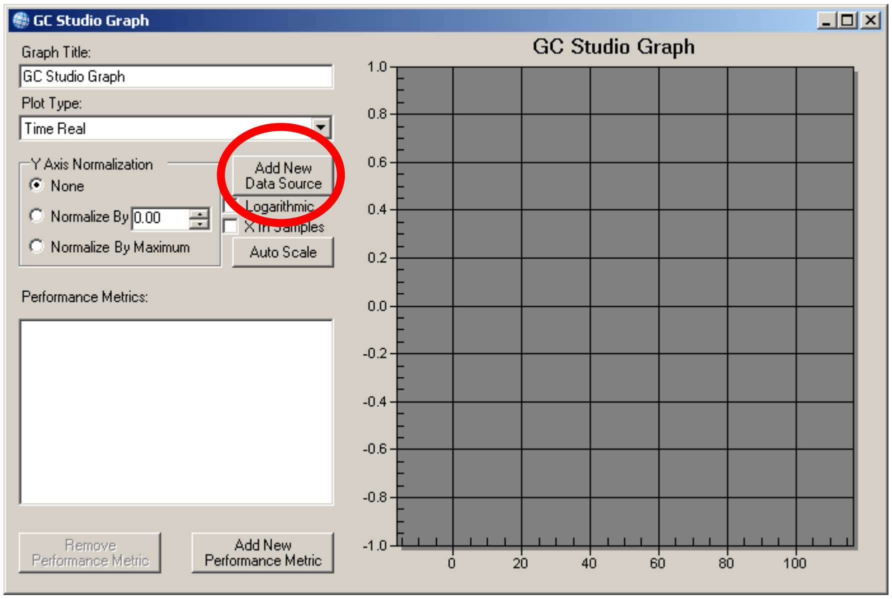
Receive Channel 0

cdma_mode	True
ch_rate_sel	FULL
ddc_chk_sum	0
ddc_ena	True
ddc_tst_sel	Constant 0
ddcmux_sel_a	I=ADC0/Q=ADC0
ddcmux_sel_b	I=ADC0/Q=ADC0
mpu_ram_read	False
mux_factor	False
mux_pos	False
muxed_data	False

cdma_mode
When asserted the DDC block is in CDMA mode (2 streams per DDC block)

Welcome to GC Studio

Click on the graph button, circled in red above, to open the graph panel shown below.



Graph Title: GC Studio Graph

Plot Type: Time Real

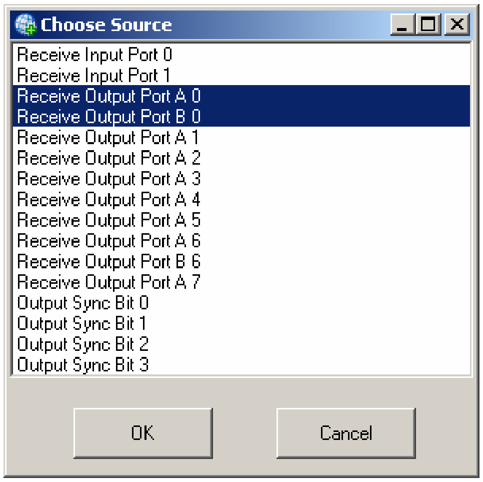
● None

○ Normalize By 0.00

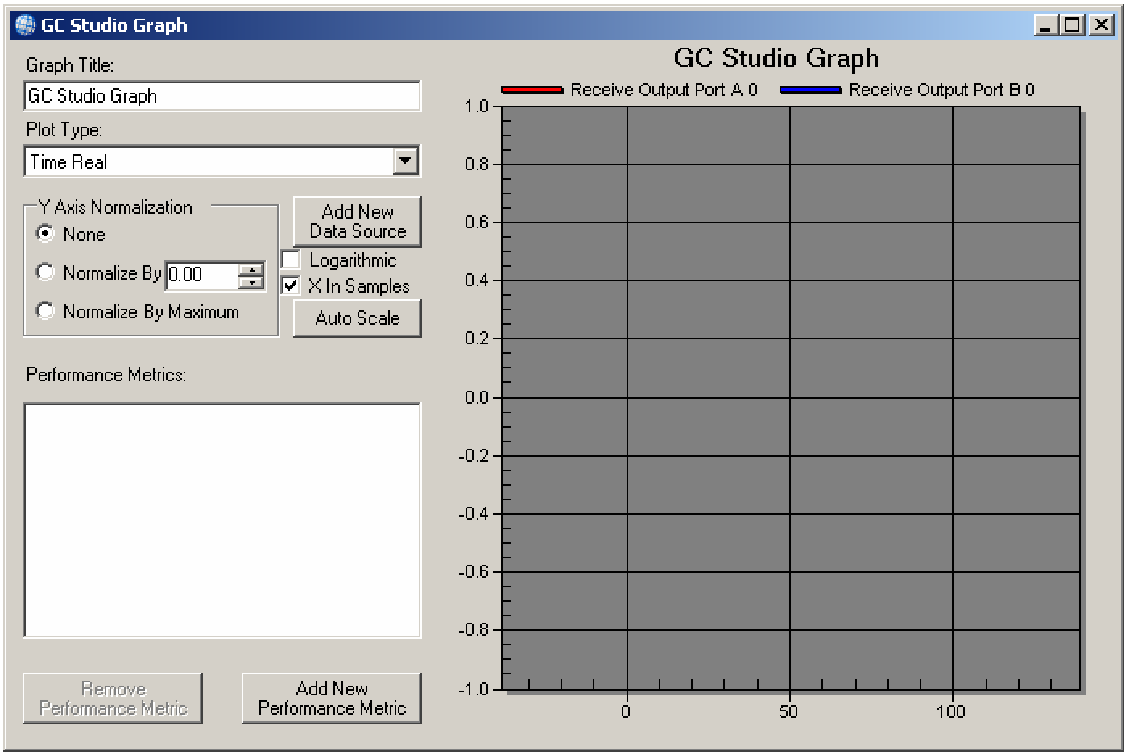
○ Normalize By Maximum

Click the Add New Data Source button circled in red above.

In the Choose Source panel, select both Receive Output Port A 0 and Receive Output Port B 0.



In the graph panel, set the Plot Type to Time Real, and check the X in Samples box.


GC Studio Graph

Graph Title: GC Studio Graph

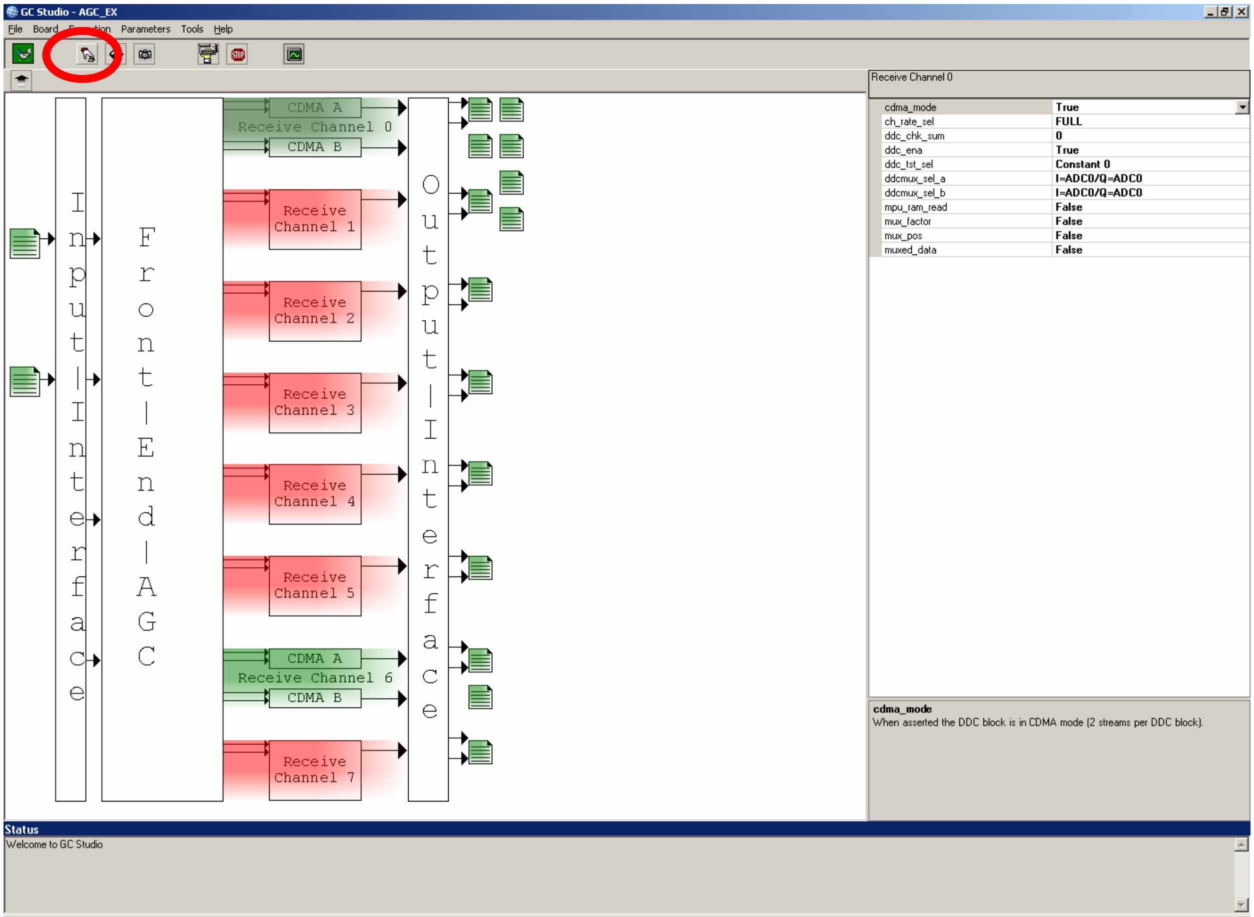
Plot Type: Time Real

Y Axis Normalization
● None
○ Normalize By 0.00
○ Normalize By Maximum

□ Logarithmic
☑ X In Samples

Performance Metrics:

On the GC Studio panel, click the run button, circled in red below.



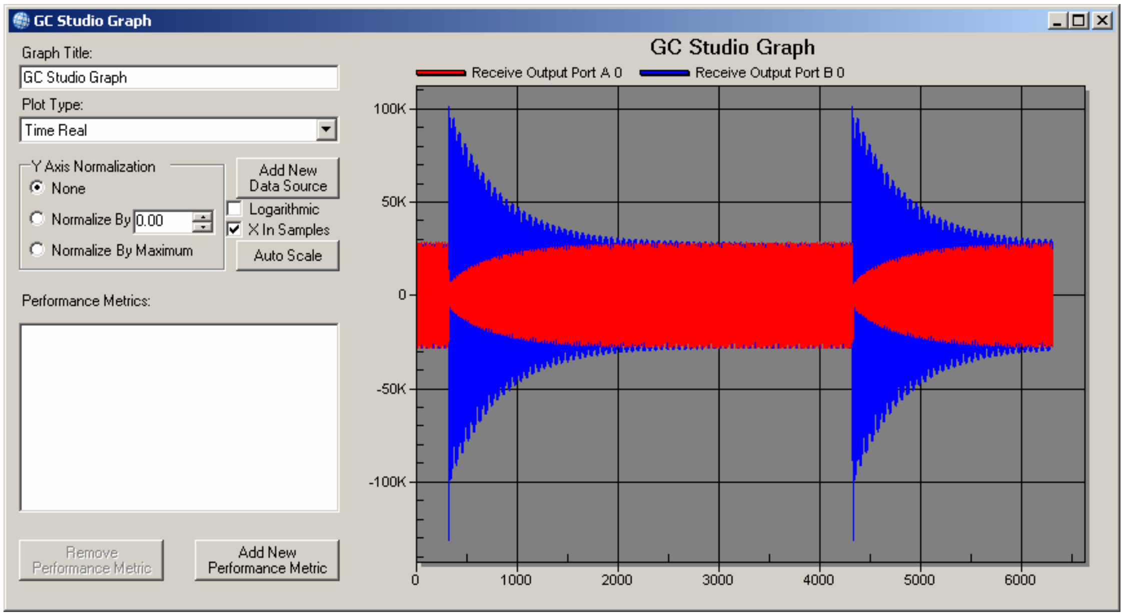
Receive Channel 0

cdma_mode	True
ch_rate_sel	FULL
ddc_chk_sum	0
ddc_ena	True
ddc_tst_sel	Constant 0
ddcmux_sel_a	I=ADC0/Q=ADC0
ddcmux_sel_b	I=ADC0/Q=ADC0
mpu_ram_read	False
mux_factor	False
mux_pos	False
muxed_data	False

cdma_mode
When asserted the DDC block is in CDMA mode (2 streams per DDC block).

Status
Welcome to GC Studio

The graph window will be automatically updated with the results.



GC Studio Graph

Graph Title: GC Studio Graph

Plot Type: Time Real

Y Axis Normalization

● None

○ Normalize By 0.00

○ Normalize By Maximum

□ Logarithmic

☑ X In Samples

Performance Metrics:

The B channel gain initially is too large and the A channel gain is initially too small. The AGC loop adjusts the gain of both channels to the same programmed target level. Each time the internally generated DDC counter generates a pulse, the AGC loop accumulator is reset and acquisition is restarted.

On the GC Studio panel, click File > Save Project to save this project.

2.2.4. GC5018 Projects included in the GC Studio Release

The following example projects are included in the GC Studio Release

UMTS153p6

- A UMTS carrier is applied to the GC5018 inputs with a simulated sample rate of 76.8Msps and an IF frequency of 19.2MHz.
- Simulated rxclk to the gc5018 is 153.6MHz
- Receive FIFOs are enabled
- Receive AGC is bypassed
- Receive Channel 0 is configured to process the signal
- The mixer/nco shifts the 19.2MHz IF to DC.
- The DC centered signal is zero stuffed to increase the rate from 76.8Msps to 153.6Msps. This is required, as the CIC uses only full rxclk rate input signals.
- The CIC filter is programmed to decimate by 10 using a m=2 comb section configuration. The output sample rate at the CIC output is 15.36Msps
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 40 tap filter, which is the maximum length that can be computed with rxclk at 153.6MHz and the CFIR output rate of 7.68Msps.
- The 64 tap PFIR provides final symbol shaping and filtering.
- Channel AGC is configured as fixed unity gain
- Baseband data is transmitted and captured using the serial interface at the full rxclk rate.

UMTS

- A UMTS carrier is applied to the GC5018 inputs with a simulated sample rate of 61.44Msps and an IF frequency of 15.36MHz.
- Simulated rxclk to the gc5018 is 122.88MHz
- Receive FIFOs are enabled
- Receive AGC is bypassed
- Receive Channel 0 is configured to process the signal
- The mixer/nco shifts the 15.36MHz IF to DC.
- The DC centered signal is zero stuffed to increase the rate from 61.44Msps to 122.88Msps. This is required, as the CIC uses only full rxclk rate input signals.
- The CIC filter is programmed to decimate by 8 using a m=2 comb section configuration. The output sample rate at the CIC output is 15.36Msps
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 32 tap filter, which is the maximum length that can be computed with rxclk at 122.88MHz and the CFIR output rate of 7.68Msps.
- The 64 tap PFIR provides final symbol shaping and filtering.
- Channel AGC is configured as fixed unity gain
- Baseband data is transmitted and captured using the serial interface at the full rxclk rate.

CDMA2000

- A 3 carrier CDMA2000 signal is applied to the GC5018 inputs with a simulated sample rate of 78.6432Msps and an IF frequency of 9.83MHz.
- Simulated rxclk to the gc5018 is 78.6432MHz
- Receive FIFOs are enabled
- Receive AGC is bypassed
- Receive Channel 0 is configured in CDMA mode and therefore processes two CDMA channels, referred to as A and B.
- A channel mixer/nco shifts the 11.08MHz carrier to DC, the B channel shifts the 8.58MHz carrier to DC.
- The CIC filter is programmed to decimate by 16 using a m=2 comb section configuration. The output sample rate at the CIC output is 4.9152Msps
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 32 tap filter, which is the maximum length that can be computed with rxclk at 78.6432MHz and the CFIR output rate of 4.9152Msps.
- The 64 tap PFIR provides final symbol shaping and filtering.
- Channel AGC is configured as fixed unity gain
- Baseband data is transmitted and captured using the serial interface at the full rxclk rate.

TD-SCDMA

- A 3 carrier TD-SCDMA signal is applied to the GC5018 inputs with a simulated sample rate of 76.8Msps and an IF frequency of 9.6MHz.
- Simulated rxclk to the gc5018 is 76.8MHz
- Receive FIFOs are enabled
- Receive AGC is bypassed
- Receive Channel 0 is configured in CDMA mode and therefore processes two TD-SCDMA channels, referred to as A and B.
- A channel mixer/nco shifts the 11.2MHz carrier to DC, the B channel shifts the 8MHz carrier to DC.
- The CIC filter is programmed to decimate by 15 using a m=2 comb section configuration. The output sample rate at the CIC output is 5.12Msps
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 28 tap filter, which is the maximum length that can be computed with rxclk at 76.8MHz and the CFIR output rate of 5.12Msps.
- The 60 tap PFIR provides final symbol shaping and filtering. 60 taps is the maximum length that can be computed with a 76.8MHz rxclk and 5.12Msps output rate
- Channel AGC is configured as fixed unity gain
- Baseband data is decimated by 2 in the output interface, and then transmitted and captured using the serial interface at the full rxclk rate.

2.2.5. GC Studio References

For more information on GC Studio, see the GC Studio User's Manual included with the software distribution. GC Studio also contains a powerful scripting language for expert users, see the SCR GC101 Language Reference also included in the software distribution. Selecting Help > User's Manuals in the GC Studio menu to these documents.

3. GC5018 Daughtercard Description

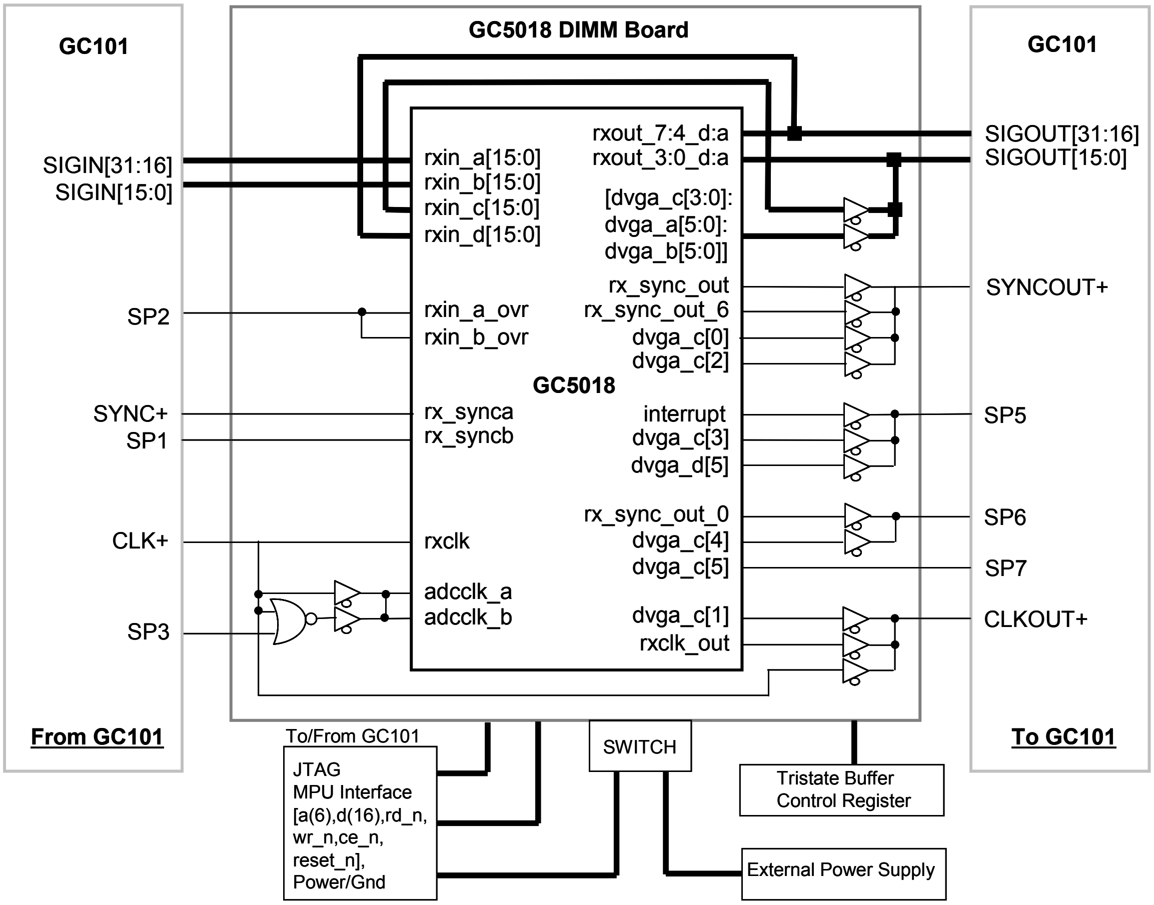


Figure 2. GC5018 Daughtercard Block Diagram

3.1. GC5018 Daughtercard to GC101 Motherboard Signal Description

The GC5018 Daughtercard has a PC-133 form-factor that utilizes the 168 pin DIMM memory connector. The 168 pin interface signals are divided into several groups:

<u>Memory Input Bus – 36 data inputs used to stimulate the GC5018 inputs</u>

SIGIN(35)	also called SP3	clock gating signal for adcclk_a and adcclk_b
SIGIN(34)	also called SP2	rxin_a_ovr and rxin_b_ovr input signals
SIGIN(33)	also called SP1	sync_b input signal
SIGIN(32)	also called SYNC+	sync_a input signal
SIGIN(31:16)		rxin_a(15:0) input data
SIGIN(15:0)		rxin_b(15:0) input data

<u>Memory Output Bus – 36 data output from selected GC5018 outputs captured by the GC101</u>

SIGOUT(35)	also called SP7	dvga_c(5)
SIGOUT(34)	also called SP6	dvga_c(4) or rx_sync_out_0
SIGOUT(33)	also called SP5	dvga_c(3), dvga_d(5) or interrupt
SIGOUT(32)	also called SYNCOUT+	rx_sync_out, rx_sync_out_6, dvga_c(0) or dvga_c(2)
SIGOUT(31:16)		rxout_7:4_d:a baseband DDC data or rxin_d(15:0) testbus output
SIGOUT(15:0)		rxout_3:0_d:a baseband DDC data or rxin_c(15:0) testbus output

<u>Clock</u>

CLK+ rxclk clock for GC5018; can be used as a full rate or gated clock source when combined with the gating signal SP3 for the adcclk_a and adcclk_b inputs.

CLKOUT clock signal from the daughtercard to the GC101; rxclk, rxclk_out from the gc5018 or dvga_c(1).

<u>Microprocessor Control Bus – Bus to program the internal registers</u>

16 bit bidirectional data	d(15:0)
11 bit address	lower 6 bits connect to a(5:0) on the GC5018 bit 7 is used to address a control registers on the GC5018 daughter card
CE#, RD#, WR#, and RST#	ce_n, rd_n, wr_n and rst_n on the GC5018

<u>JTAG</u>

JTAG – 5 pin JTAG Test Port for GC5018

TRST#, TCK, TMS, TDI, TDO	trst_n, tck, tms, tdi and tdo on the GC5018

Power and Ground

VDUT1 – 3.3V power from GC101 EVM to the daughtercard
GND

See the GC101 EVM Manual for the 168 pin connector table. Detailed schematics for the GC5018 daughtercard can be found in Section 4.

3.2. GC5018 Daughtercard Jumpers

3.3V power for the GC5018 daughtercard can be supplied by the GC101 motherboard or an external power supply. A regulator on the daughtercard can be used to generate the 1.5V core supply voltage or an external supply can be used.

Jumper W1 Selects source for GC5018 core 1.5V power
position 1:2 selects an external supply connected to J2 for the 1.5V core supply
position 2:3 selects the regulator on the daughtercard as the 1.5V core supply

Jumper U13 Enables the +1.5V regulator when jumper in 2:3 (center:on) position
Disables the +1.5V regulator when jumper in 1:2 (off:center) position

Jumper W2 Selects source for GC5018 I/O 3.3V power
position 1:2 selects an external supply connected to J3 for the 3.3V I/O supply
position 2:3 selects the GC101 motherboard as the source for the 3.3V I/O supply

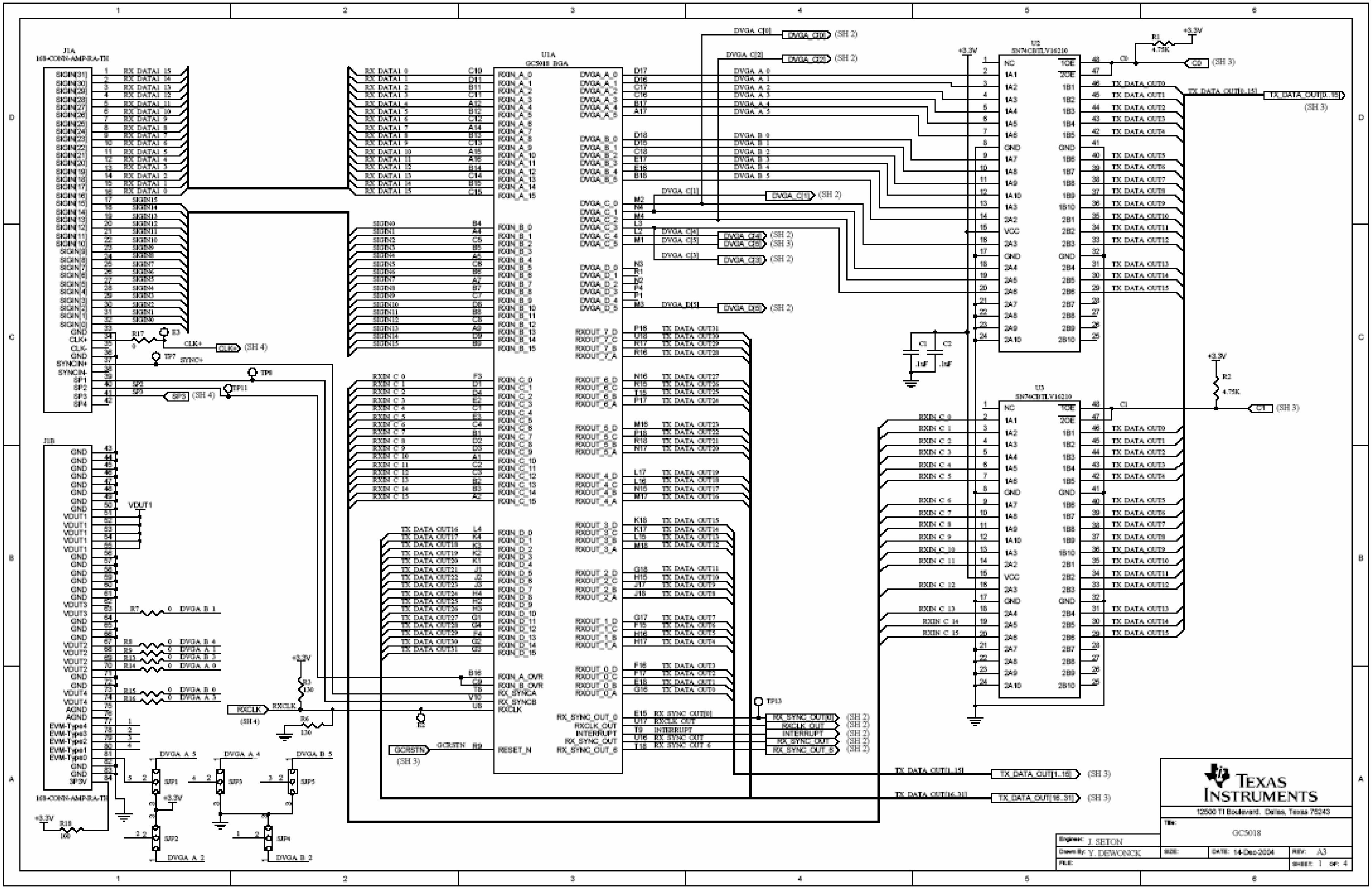
Jumper W3 pin 1 is DVDDMON testpoint, DO NOT INSTALL A JUMPER.
Jumper W4 pin 1 is DVSSMON testpoint, DO NOT INSTALL A JUMPER.

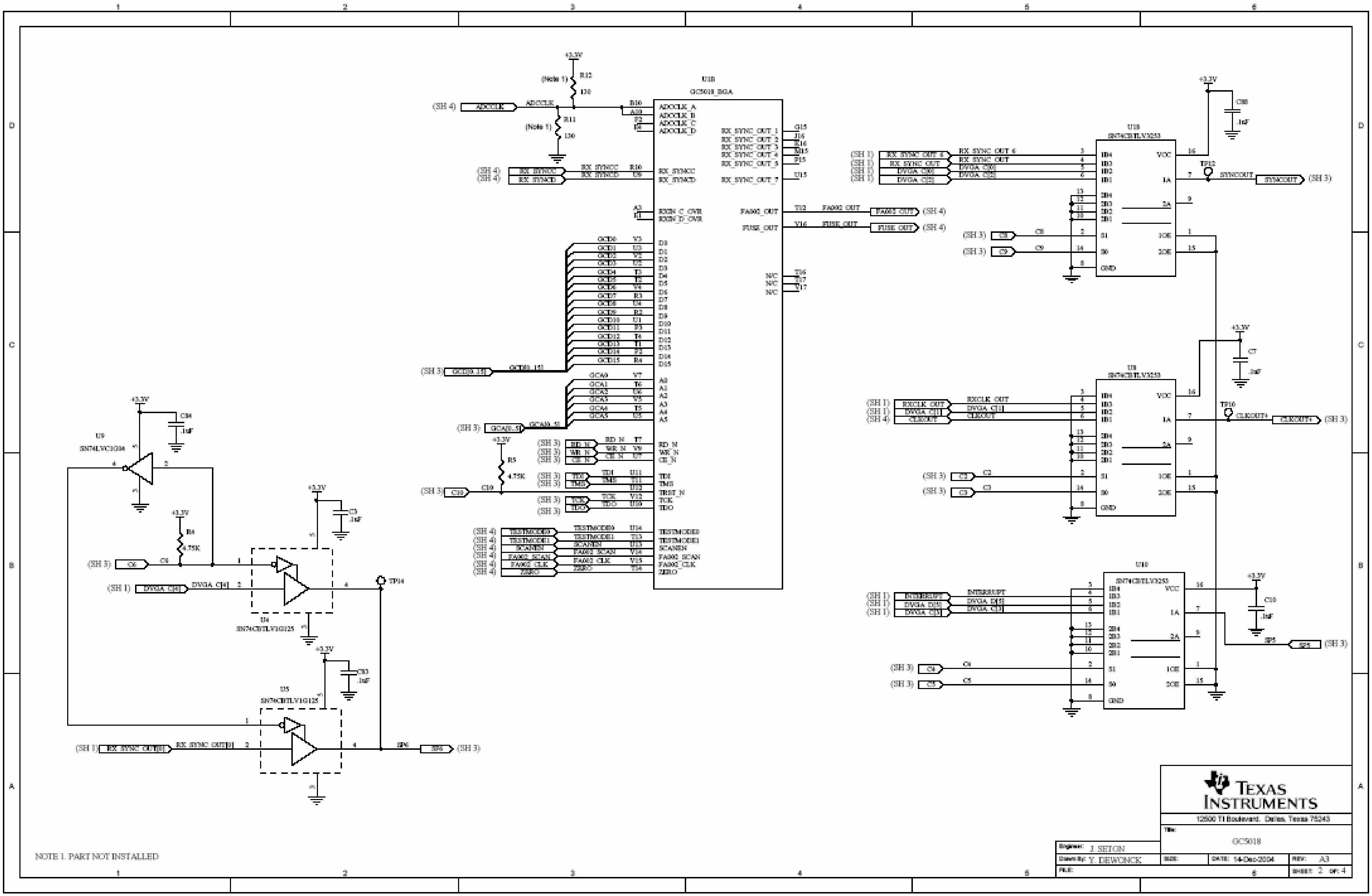
3.3. GC5018 Daughtercard Power Supplies

The GC5018 core power supply is 1.5V. The daughtercard includes a regulator that can be used to supply this 1.5V to the GC5018 or an external power supply can be connected at J2. The regulator can be enabled or disabled via the jumper located below U13 and above TP3.

The GC5018 I/O power supply is 3.3V, and can be supplied by the GC101 motherboard or an external power supply connected to J3.

4. Detailed GC5018 Daughtercard Schematic





NOTE 1. PART NOT INSTALLED

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title: GC5018

Engineer: J. SETON

Drawn By: Y. DEWONCK

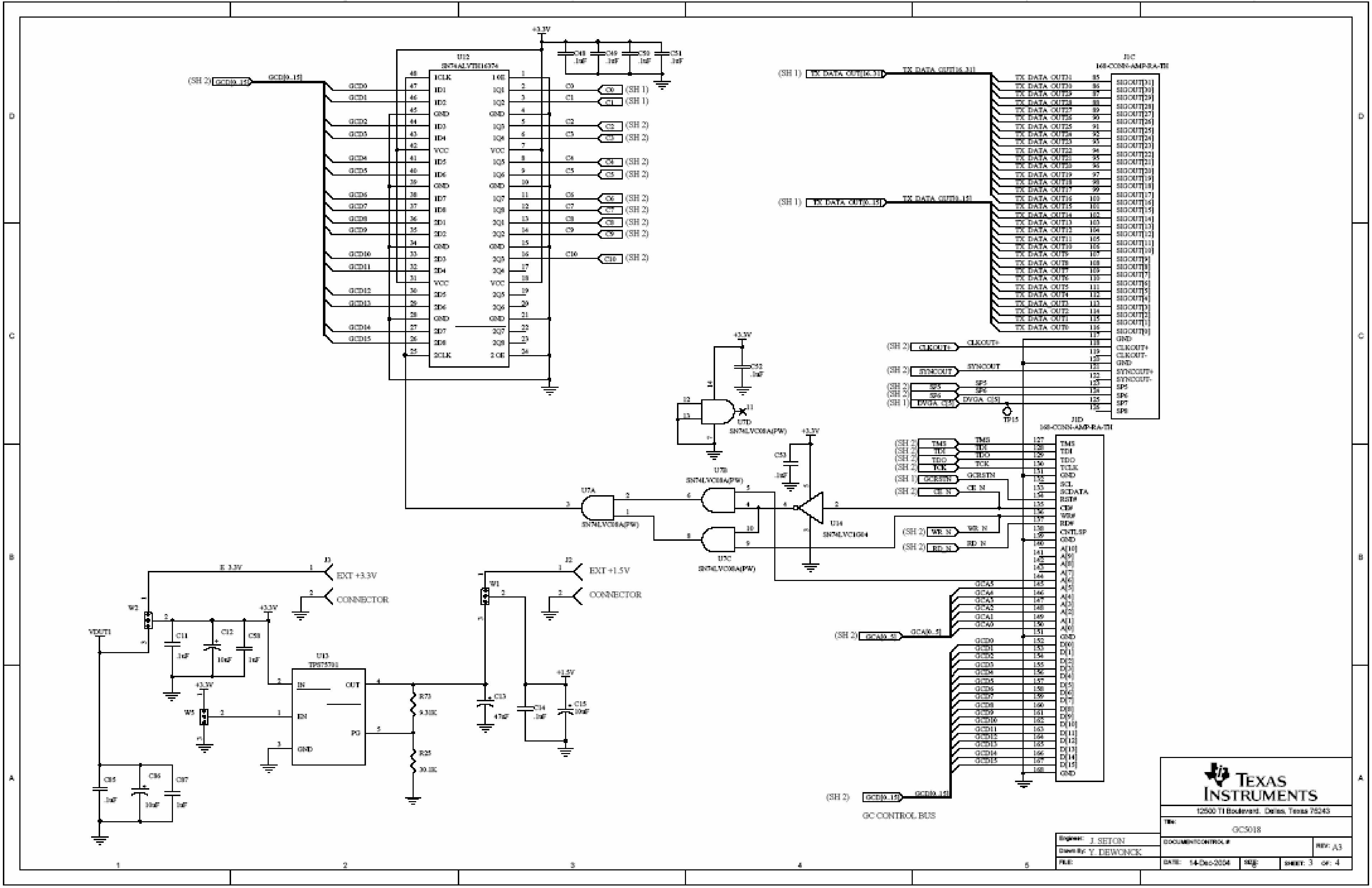
SIZE:

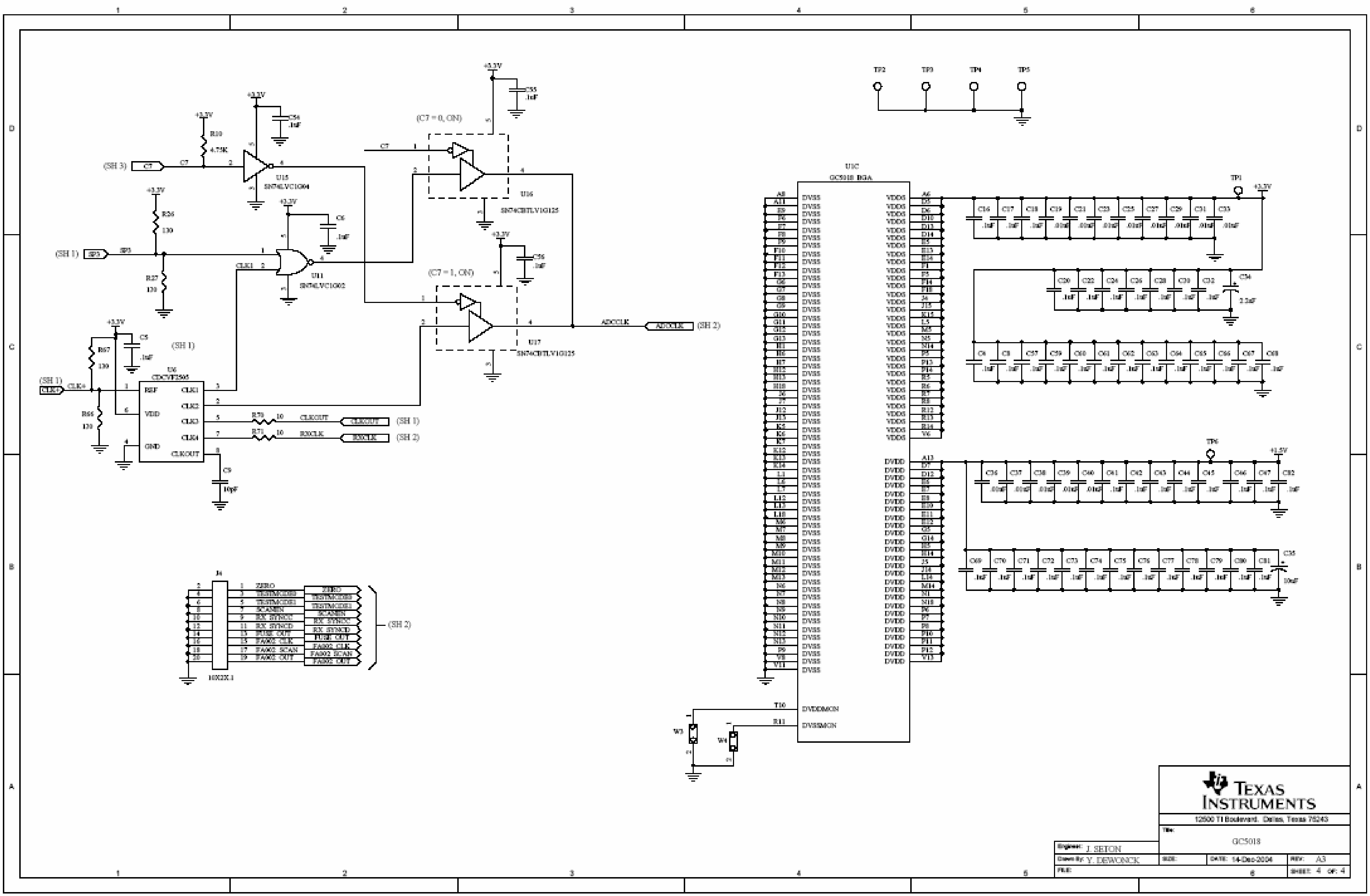
DATE: 14-Dec-2004

REV: A3

FILE:

SHEET: 2 OF: 4


U12
SN74ALVTH16374
+3.3V
C48 .1uF
C49 .1uF
C50 .1uF
C51 .1uF
(SH 2) GCD[0..15]
GCD0
GCD1
GCD2
GCD3
GCD4
GCD5
GCD6
GCD7
GCD8
GCD9
GCD10
GCD11
GCD12
GCD13
GCD14
GCD15
C0 (SH 1)
C1 (SH 1)
C2 (SH 2)
C3 (SH 2)
C4 (SH 2)
C5 (SH 2)
C6 (SH 2)
C7 (SH 2)
C8 (SH 2)
C9 (SH 2)
C10 (SH 2)
J1C
168-CONN-AMP-RA-TH
(SH 1) TX DATA OUT[16..31]
(SH 1) TX DATA OUT[0..15]
SIGOUT[31]
SIGOUT[0]
(SH 2) CLKOUT+
(SH 2) SYNCOUT
(SH 2) SP5
(SH 2) SP6
(SH 1) DVGA C[5]
TP15
J1D
168-CONN-AMP-RA-TH
TMS
TDI
TDO
TCK
GCRSTN
CE N
WR N
RD N
U7A
U7B
U7C
U7D
SN74LVC08A(PW)
U14
SN74LVC1G04
C52 .1uF
C53 .1uF
(SH 2) GCA[0..5]
GCA0
GCA1
GCA2
GCA3
GCA4
GCA5
(SH 2) GCD[0..15]
GC CONTROL BUS
J3
EXT +3.3V
CONNECTOR
J2
EXT +1.5V
CONNECTOR
E 3.3V
W2
W1
W5
VDUT1
C11 .1uF
C12 10uF
C58 1uF
U13
TPS75701
IN
OUT
EN
PG
GND
R73 9.31K
R25 30.1K
C13 47uF
C14 .1uF
C15 10uF
+1.5V
C85 .1uF
C86 10uF
C87 1uF
TEXAS INSTRUMENTS
12500 TI Boulevard, Dallas, Texas 75243
Title: GC5018
Engineer: J. SETON
Drawn By: Y. DEWONCK
FILE:
DOCUMENT CONTROL #
REV: A3
DATE: 14-Dec-2004
SIZE: B
SHEET: 3 OF: 4


(SH 3)
C7
R10
4.75K
U15
SN74LVC1G04
+3.3V
C54
.1uF
(C7 = 0, ON)
U16
SN74CBTLV1G125
C55
.1uF
(SH 1)
SP3
R26
130
R27
130
U11
SN74LVC1G02
CLK1
C6
.1uF
(C7 = 1, ON)
U17
SN74CBTLV1G125
C56
.1uF
ADCCLK
(SH 2)
R67
130
C5
.1uF
U6
CDCVF2505
CLK+
REF
VDD
GND
CLK1
CLK2
CLK3
CLK4
CLKOUT
R66
130
R70
10
R71
10
CLKOUT
RXCLK
C9
10pF
J4
10X2X.1
ZERO
TESTMODE0
TESTMODE1
SCANIN
RX_SYNCC
RX_SYNCD
FUSE_OUT
FA002_CLK
FA002_SCAN
FA002_OUT
TP2
TP3
TP4
TP5
U1C
GC5018_BGA
DVSS
VDDS
DVDD
DVDDMON
DVSSMON
T10
R11
W3
W4
TP1
+3.3V
TP6
+1.5V
C34
2.2uF
C35
10uF
.1uF
.01uF
Texas Instruments
12500 TI Boulevard, Dallas, Texas 75243
Title:
GC5018
Engineer: J. SETON
Drawn By: Y. DEWONCK
SIZE:
DATE: 14-Dec-2004
REV: A3
FILE:
SHEET: 4 OF: 4