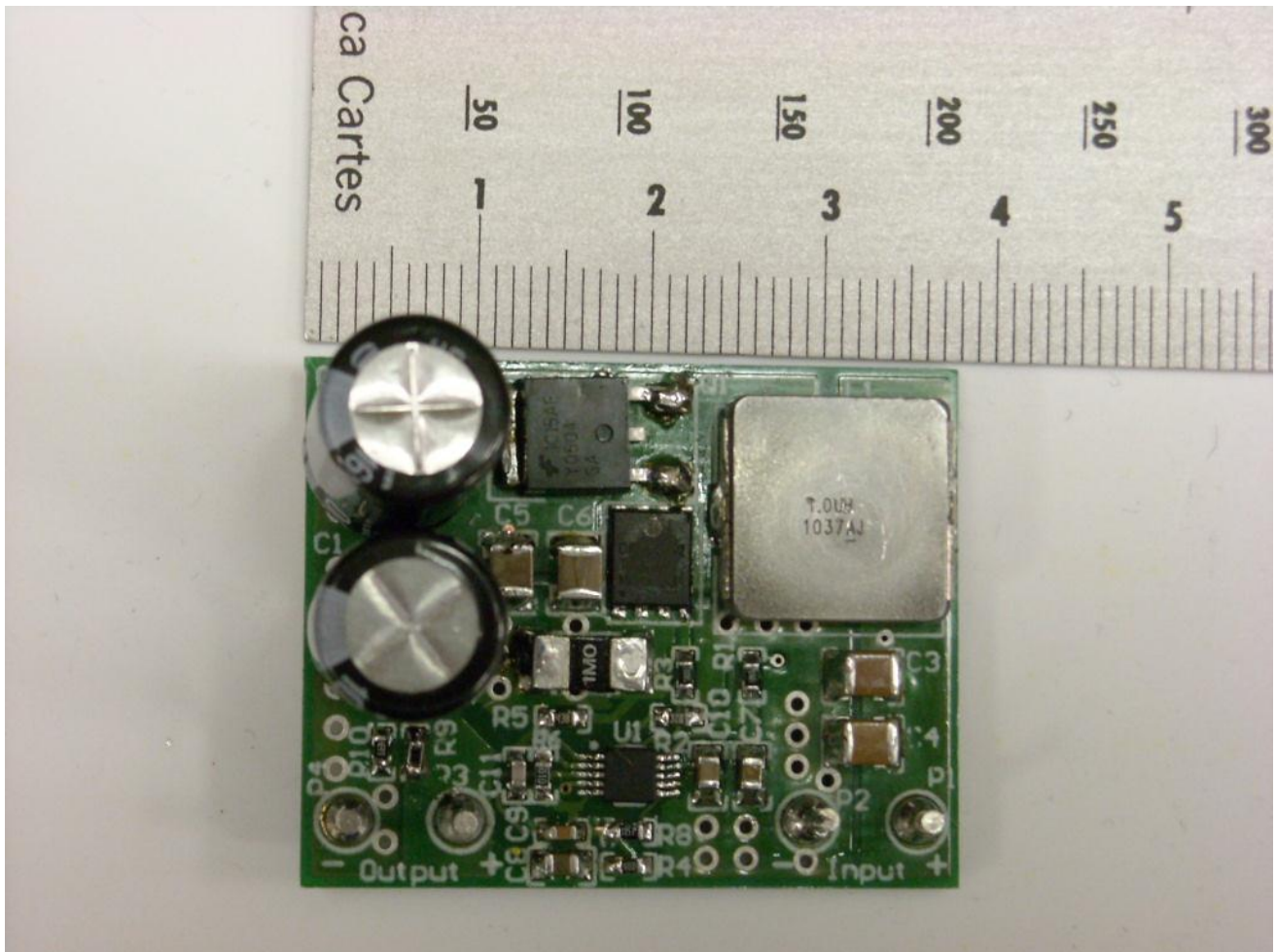


PICTURE OF THE BOARD:

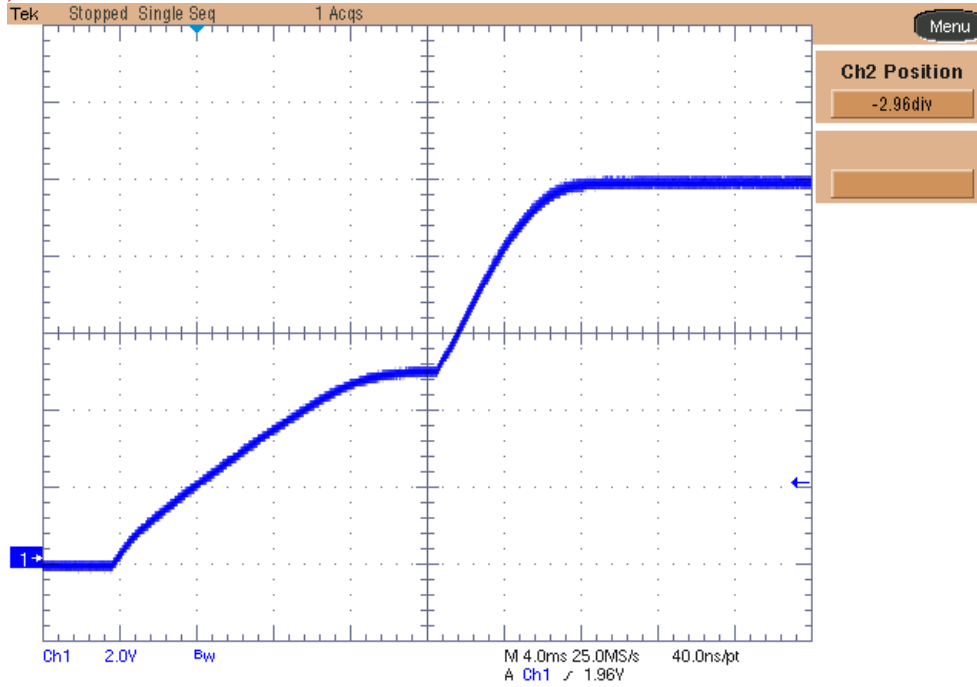


1. Startup

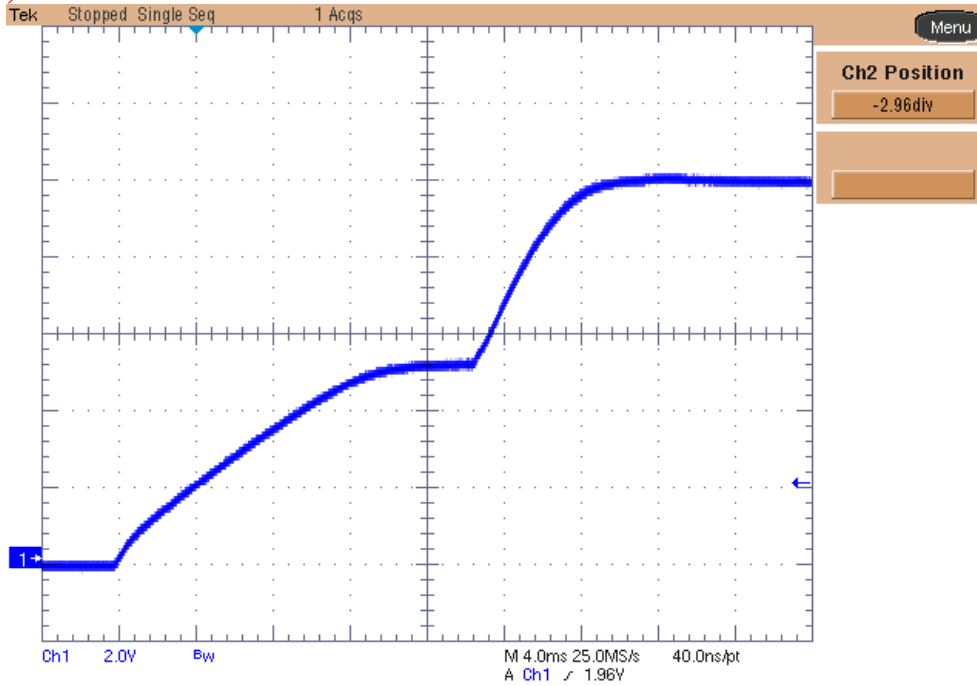
The output voltage behavior at startup is shown in the images below. The input voltage was set to 5.5V. The converter was loaded @ 1A for the upper picture and unloaded for the bottom one.

Ch.1: Output voltage (2V/div, 4ms/div, DC coupling, 20MHz BWL)

I_{out} = 1A;

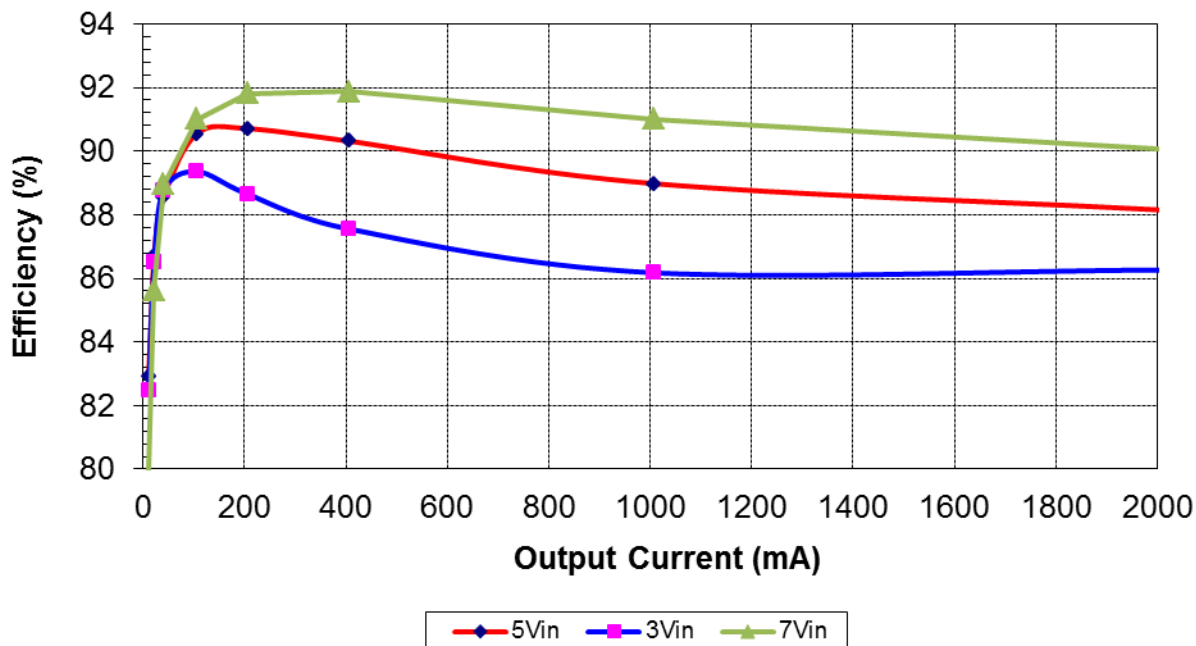


I_{out} = 0A;



1 Efficiency

The efficiency data are shown in the tables and graph below. A DC voltage source has been set to 3V, 5V and 7V and the load varied from 0 to 2A.



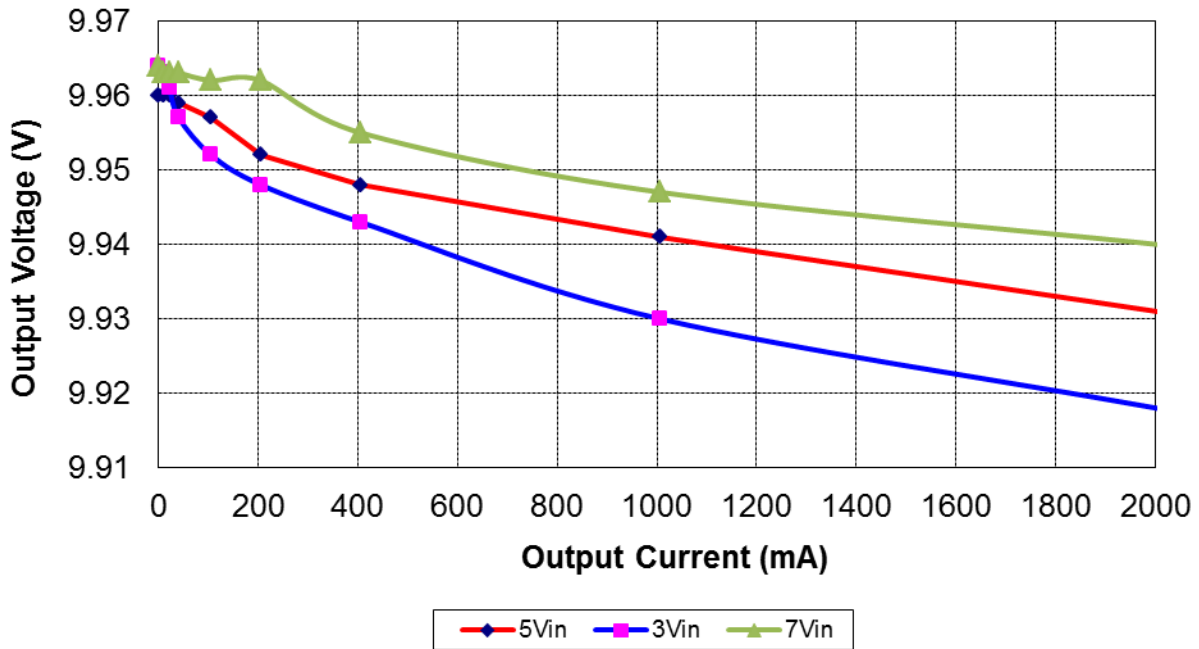
Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (Vdc)	Pin (W)	Ploss (W)	Eff (%)
0	9.960	0	2.8	5.003	0.014	0.0140	0.00
11.2	9.960	0.112	26.9	5.000	0.135	0.0229	82.94
22.0	9.960	0.219	50.4	5.015	0.253	0.0336	86.69
40.9	9.959	0.407	91.8	5.010	0.460	0.0526	88.56
105.7	9.957	1.052	231.4	5.023	1.162	0.1099	90.55
205.5	9.952	2.045	447.6	5.037	2.255	0.2094	90.71
405.3	9.948	4.032	889.1	5.021	4.464	0.4322	90.32
1007.4	9.941	10.015	2251	5.000	11.255	1.2404	88.98
2007	9.931	19.932	4514	5.009	22.611	2.6791	88.15

Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (Vdc)	Pin (W)	Ploss (W)	Eff (%)
0	9.964	0	3.2	3.007	0.010	0.0096	0.00
11.2	9.963	0.112	45.1	3.000	0.135	0.0237	82.47
22.0	9.961	0.219	84.2	3.008	0.253	0.0341	86.52
41.0	9.957	0.408	153.3	3.000	0.460	0.0517	88.77
105.7	9.952	1.052	391.1	3.010	1.177	0.1253	89.36
205.6	9.948	2.045	763.7	3.021	2.307	0.2618	88.65
405.4	9.943	4.031	1529	3.011	4.604	0.5729	87.56
1007.4	9.930	10.003	3854	3.012	11.608	1.6048	86.18
2005	9.918	19.886	7603	3.032	23.052	3.1667	86.26

Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (Vdc)	Pin (W)	Ploss (W)	Eff (%)
0	9.964	0	2.8	7.017	0.020	0.0196	0.00
11.2	9.963	0.112	19.9	7.016	0.140	0.0280	79.92
22.0	9.963	0.219	36.5	7.014	0.256	0.0368	85.62
41.0	9.963	0.408	65.5	7.011	0.459	0.0507	88.95
105.7	9.962	1.053	165.3	7.000	1.157	0.1041	91.00
205.6	9.962	2.048	318.5	7.004	2.231	0.1826	91.82
405.4	9.955	4.036	627.5	7.000	4.393	0.3567	91.88
1007.4	9.947	10.021	1570	7.014	11.012	0.9914	91.00
2004	9.940	19.920	3159	7.002	22.119	2.1996	90.06

2 Output Voltage Regulation

The output voltage variation as function of load and input voltage is shown below:



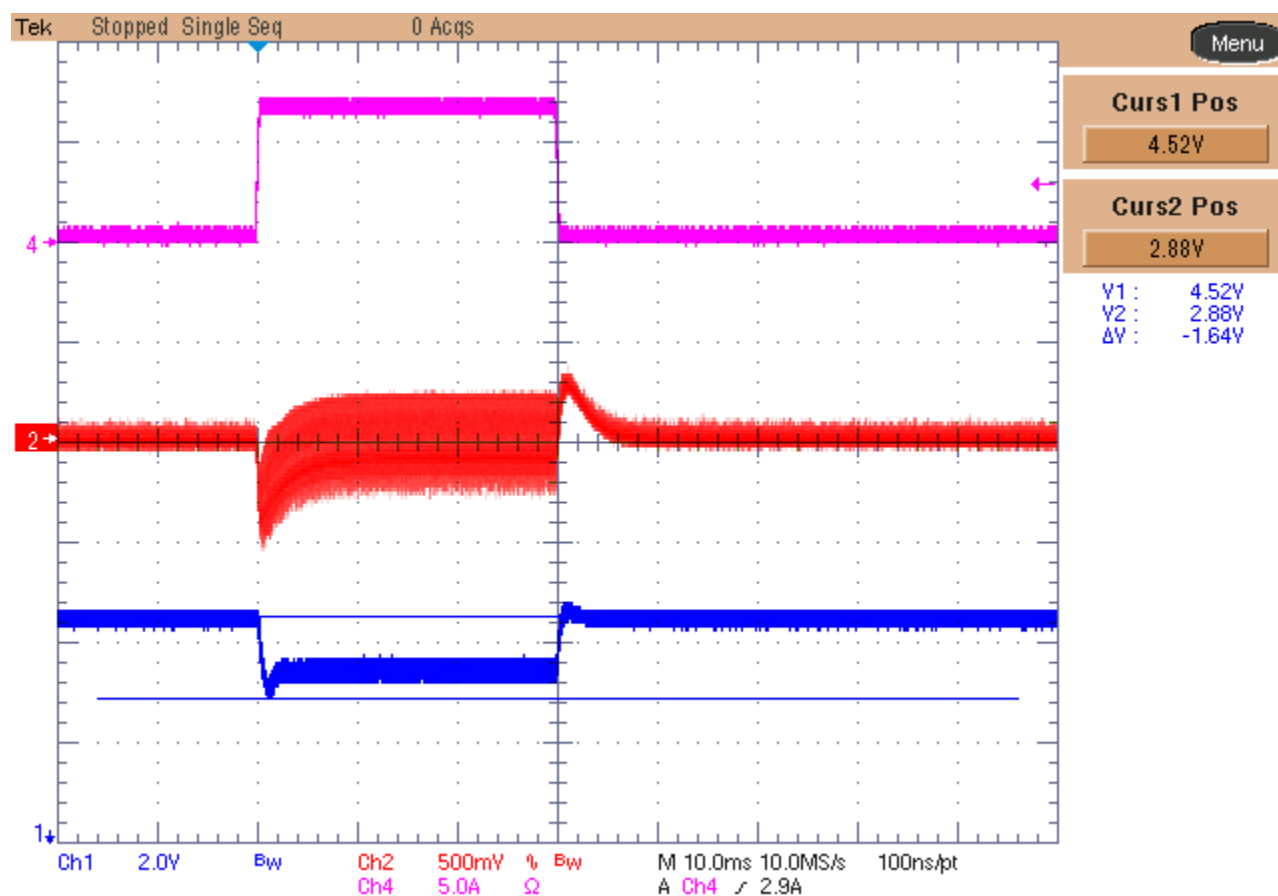
3 Transient Response

The image below shows the transient response on the output voltage when the load has been switched between 0.5A and 7A. The input voltage was 4.5V. The Vin trace shows that, due to non-zero impedance of cabling, the input voltage is as low as 2.88V. It is also possible to measure the peak-peak ripple voltage on the output terminals during the 7A load, which is 500mVpk-pk.

Ch1: Input Voltage (2V/div, 10ms/div, DC coupled, 20MHz BWL)

Ch2: Output Voltage (500mV/div, AC coupled, 20MHz BWL)

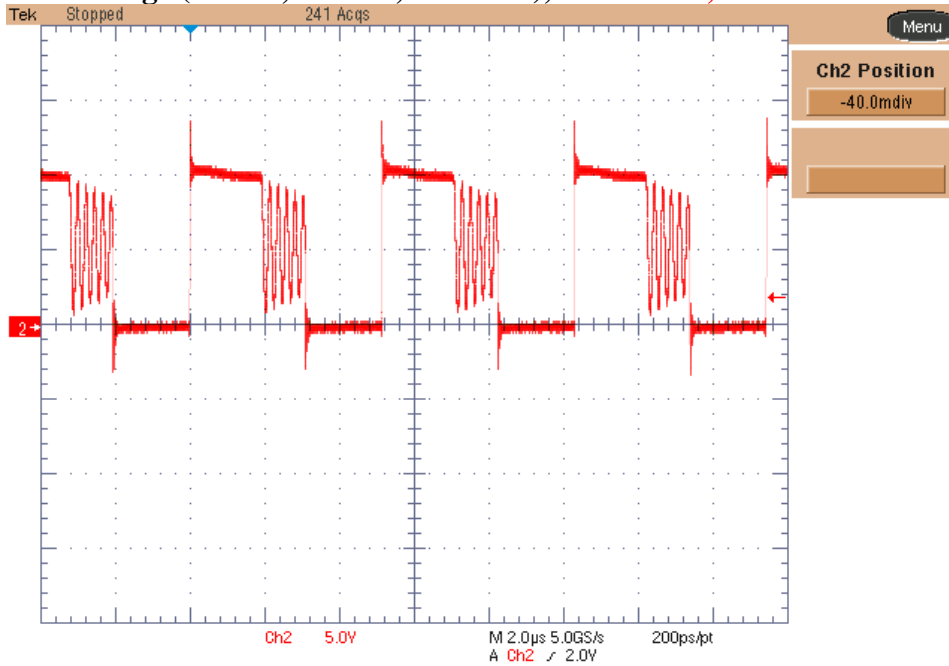
Ch4: Output Current (5A/div, DC coupled, no BWL)



4 Switching Node Waveform

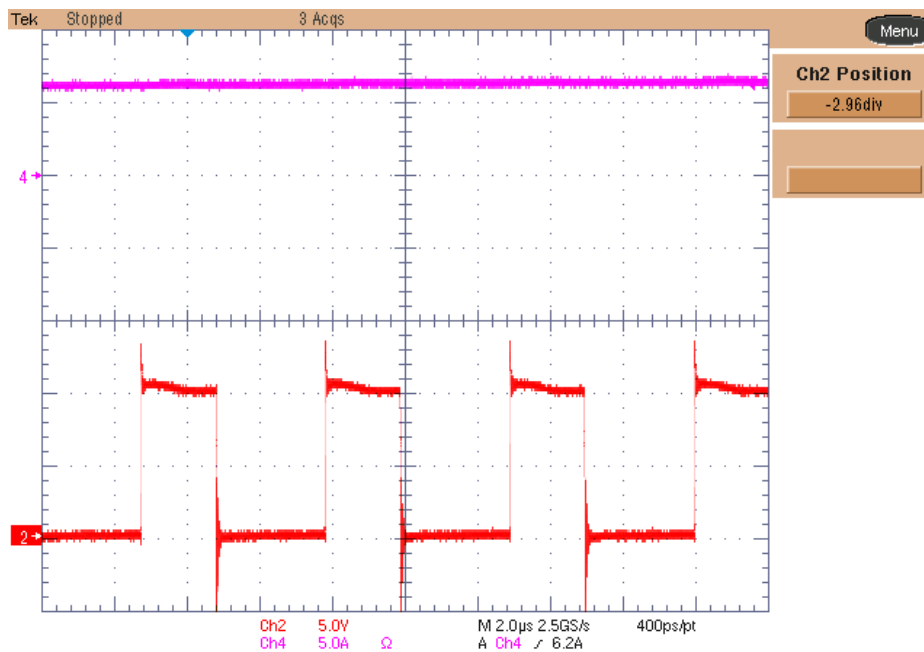
The images below show the peak voltage on drain of Q1 with 5.2Vin, 2A load and 3.5Vin, 7A load.

Ch2: Q1 drain Voltage (5V/div, 2us/div, No BWL), Vin = 5.2V, Iout = 2A.



Ch2: Q1 drain Voltage (5V/div, 2us/div, No BWL), Vin = 3.5V, Iout = 7A.

Ch4: Output Current (5A/div, No BWL).



5 Thermal Analysis

The thermal analysis of the converter shows the temperatures for each component, in the graph below. The converter has been placed horizontally on the bench without any forced convection. The input voltage was 4.5V, the load switched between 500mA and 7A (30msec ON, 630msec OFF); the ambient temperature 23C.

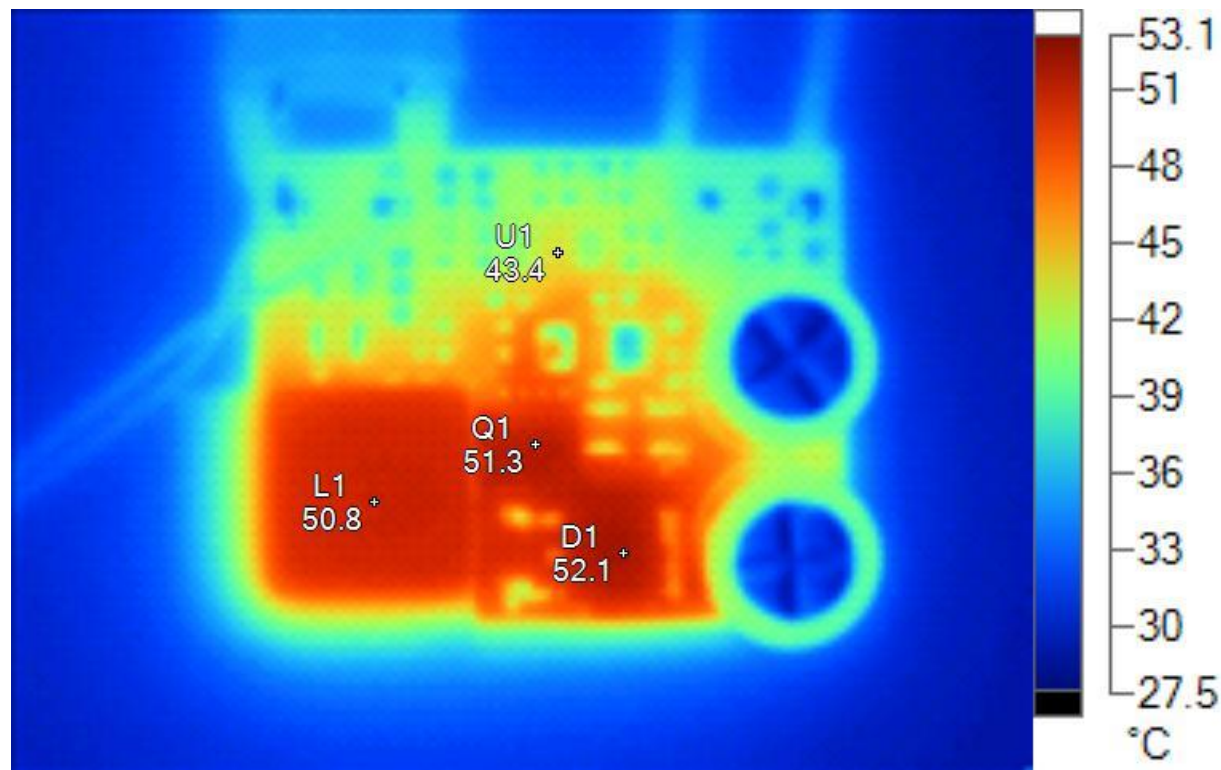


Image Info

Background temperature	20.0°C
Average Temperature	36.2°C
Image Range	28.5°C to 52.1°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	10/29/2013 1:04:40 PM

Main Image Markers

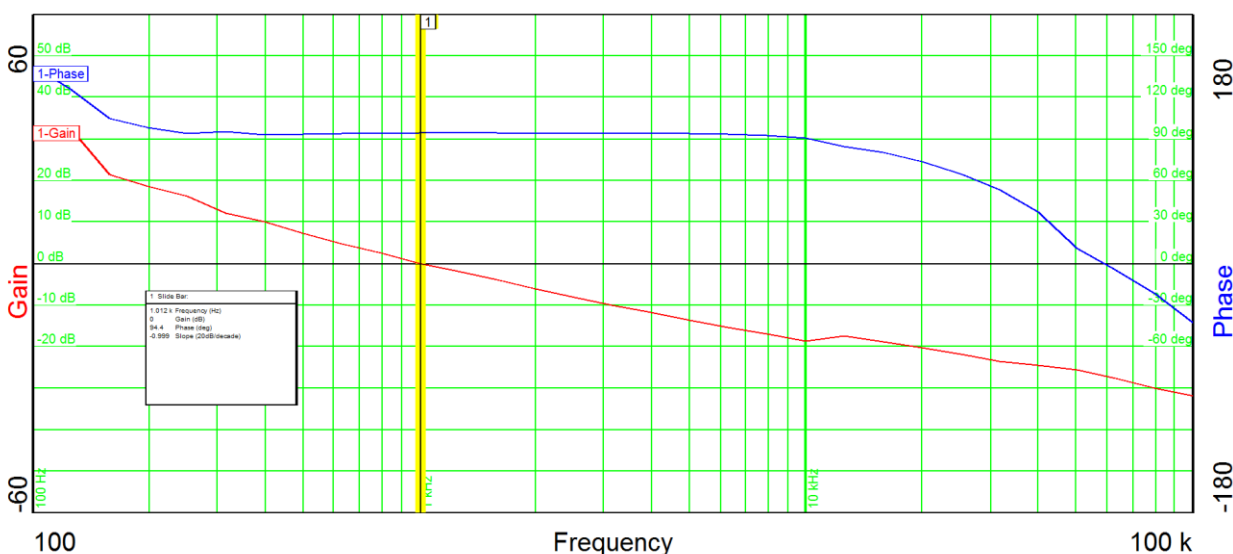
Name	Temperature
L1	50.8°C
D1	52.1°C
Q1	51.3°C
U1	43.4°C

6 Loop Analysis

The loop analysis on the converter shows results regarding phase margin and gain margin, as well as crossover frequency. The converter has been supplied @ 3.5V_{in}, and 2A load.

The measurement showed these results:

- 1) Phase margin = 94.4 deg.
- 2) Gain margin = 27.14 dB
- 3) Crossover frequency = 1 KHz



Even though the phase margin is very high and stays constant until 10KHz...20KHz, we have to consider that at this 2A load the converter runs in DCM mode, therefore showing a lower bandwidth and high phase margin. The real application will be a transient load of 7A for 30msec, which happens only for this short time. It is not possible to measure the loop at 7A load, because of a heavy overheating. At this high current the converter runs in CCM (see switch node waveform) and therefore we have to take into account the right half plane zero (RHPZ) which will destroy the phase margin very quickly if we choose a high bandwidth.

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3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.

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