TCK211
CCD Image Sensor
Evaluation Kit

SEPTEMBER 1994
SOCU005

TEXAS INSTRUMENTS

1 Introduction

The TCK211 demonstration kit is a one-board system used to evaluate the Texas Instruments TC211 small-area CCD image sensor. The kit consists of the CCD image sensor and a circuit board containing all support circuits necessary to operate the CCD image sensor. In addition, the kit includes a lens, faceplate, offset spacers, and a nonconductive foam doughnut used to shield the sensor from ambient light.

1.1 Formatting

The TC211 image area is configured into 165 horizontal lines each containing 192 pixels. The EIA RS-170 format requires 244 horizontal TV lines. Therefore, the TC211 lacks the required number of lines for standard RS-170. However, the TCK211 supplies an RS-170-compatible signal centered both horizontally and vertically on the monitor. This is accomplished by extending both horizontal and vertical blanking time.

2 Applicable Documents

This kit manual should be used in conjunction with the following data sheets:

– Small-Format CCD	TC211
– Sample-and-Hold Amplifier	TL1591
– Parallel Driver	TMS3473B

3 Construction

The CCD should be installed in the socket located in the back of the board with the dark-reference pixels on the right side. The three offset spacers are mounted to the back of the board with the white plastic screws. The left, top, and bottom holes are used. The nonconductive foam doughnut is then placed over the CCD. The faceplate is mounted to the spacers using the three metal screws provided. The 35-mm lens is then screwed into the faceplate. The user mounts the board on a tripod using the 1/4” 20 hole on the bottom of the faceplate.

4 Operating Instructions

The kit is factory adjusted and operational when received. This section lists 1) recommended equipment, 2) system interconnection diagrams, 3) basic operational instructions, which include signal voltage level requirements, test points, and reference designators for level adjustment potentiometers and, 4) options that are factory selected but that are easily modified by the user.

4.1 Recommended Equipment

– Oscilloscope
– NTSC monochrome monitor
– DC power supply (±15 V at 1 A)
– Test chart
– Tripod
– Strobe light

4.2 System Interconnection

The interconnection between the kit, the monitor, the dc power supplies, the test chart, and the strobe light is shown in Figure 1.

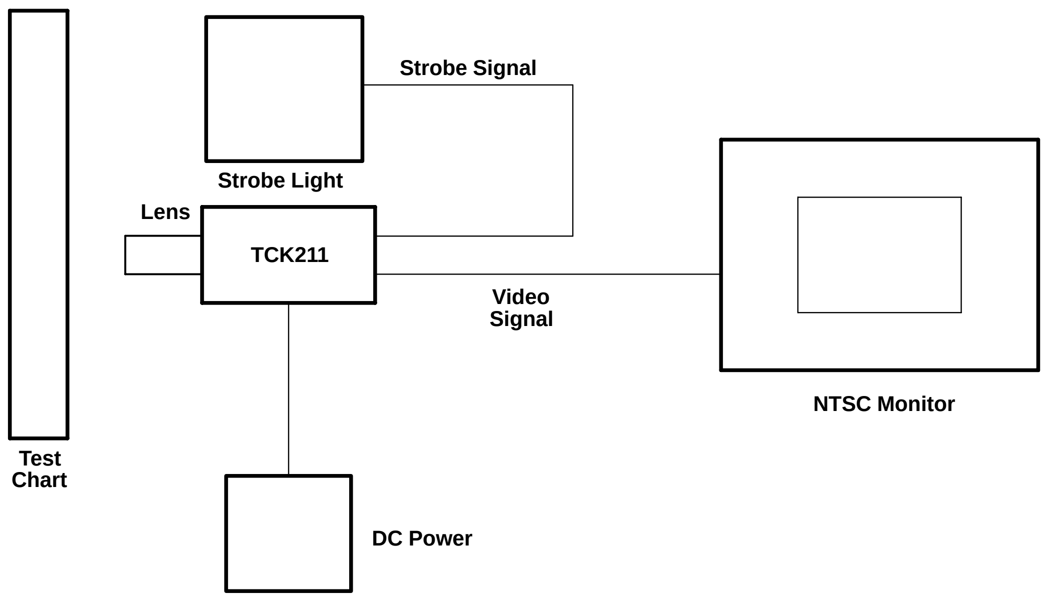

Figure 1. System Interconnection Diagram

4.3 Voltage Requirements

4.3.1 Power Supply Voltage

1) With the kit disconnected, adjust the power supplies to ±15 V.
2) Turn off the power supplies and connect the 3-wire power cable to the supplies — red to 15 V, black to ground, and blue to –15 V.
3) Turn on both supplies at the same time and observe the current. Make sure that it is approximately 350 mA for the 15-V supply and 100 mA for the –15-V supply. If the current is in excess of this, turn off the power immediately and check for proper connection and for short circuits.

4.3.2 Image Area Gate (IAG) Signal Levels

The following table specifies the approximate voltage levels, test points, and reference designators for level-adjustment potentiometers used to adjust the tri-level image area gate (IAG) clock. See Figure 2 for potentiometer location.

SIGNAL	REFERENCE DESIGNATORS	TEST POINT	APPROXIMATE VOLTAGE LEVEL
VP	R100	TP7	2 V
–VP	R102	TP7	–10 V
INLVL†	RV5	TP7	–5 V

† If the interlace mode is selected, INLVL should be adjusted to achieve maximum vertical resolution. If the noninterlace mode is chosen, INLVL should be brought down to the level of –VP.

4.3.3 Antiblooming Gate (ABG) Signal Levels

The following table specifies the approximate voltage levels, test points and reference designators for level-adjustment potentiometers that should be used to adjust the tri-level antiblooming gate (ABG) clock. See Figure 2 for potentiometer location.

SIGNAL	REFERENCE DESIGNATORS	TEST POINT	APPROXIMATE VOLTAGE LEVEL
VAB	R100	TP5	4 V
–VAB	R102	TP5	–7 V
ABLVL†	R105	TP5	–3 V

† Adjustment is necessary to maximize charge transfer efficiency.

4.3.4 Serial Register Gate (SRG) Signal Levels

The following table specifies the approximate voltage levels, test points, and reference designators for level-adjustment potentiometers that are used to adjust the tri-level serial register gate (SRG) clock. See Figure 2 for potentiometer location.

SIGNAL	REFERENCE DESIGNATORS	TEST POINT	APPROXIMATE VOLTAGE LEVEL
V_{SS}	R106	TP9	2 V
$-V_{SS}$	R108	TP9	–10 V
VSSLVL	R107	TP9	–4 V

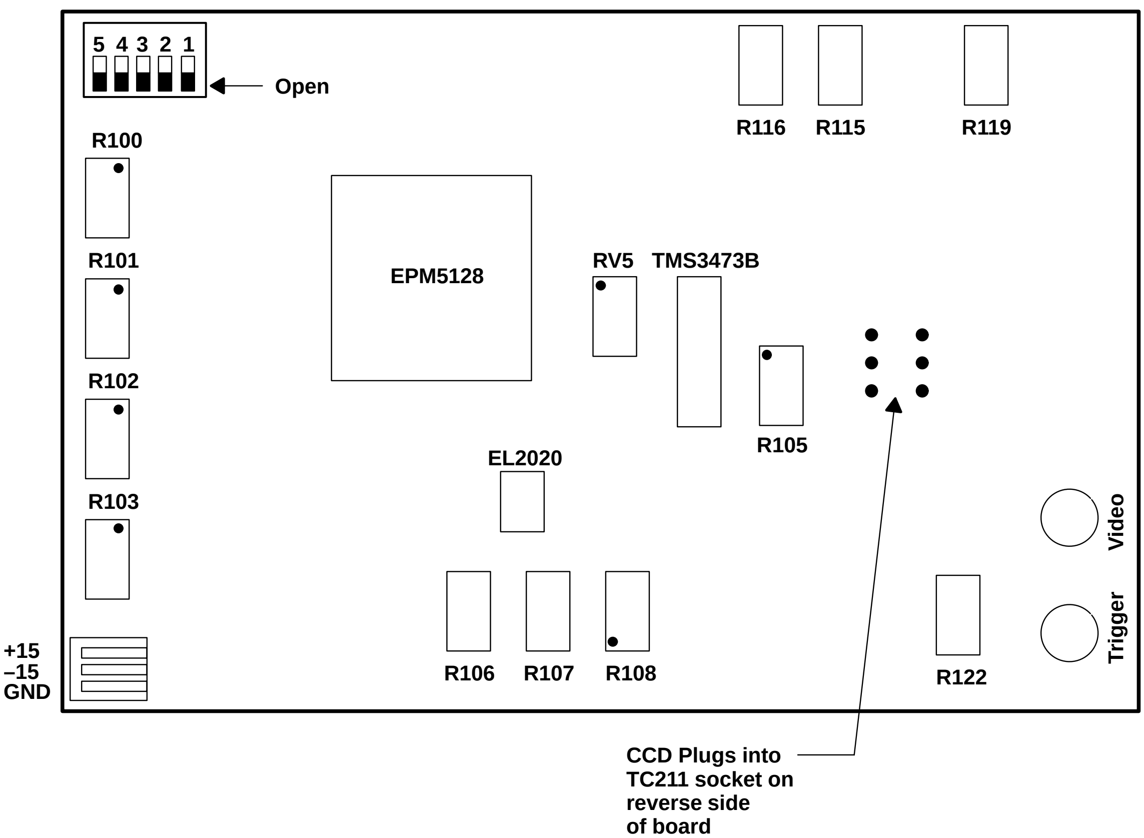

Figure 2. Component Location Diagram

4.4 Additional Potentiometer Adjustments and Options

4.4.1 Gain Adjust

Signal gain may be adjusted with R115. It will be factory adjusted to maximize gain without distortion.

4.4.2 DC Level Adjust

R116 controls dc level of the signal. It will be factory adjusted so that the dc level of the signal is at ground.

4.4.3 Delay Line Null Adjust

R119 is factory adjusted and fixed at the delay-line characteristic impedance of 200 Ω.

4.4.4 Composite Video Out

R122 controls the gain of composite video OUT. It is factory adjusted to ensure an EIA RS-170-compatible video signal at the output.

4.4.5 High Gain

In normal light settings, switch 1 of the five-pin dip switch should be open for normal gain. In low light levels, switch 1 can be closed to increase the gain by a factor of five. The kit will be factory selected for normal gain. Switch 1 is the only switch on the five-pin dip switch that should be changed. The other switches are used when evaluating the TC221, TC225 and TC227 CCD image sensors. See subsection 4.4.8.

4.4.6 Reflected Double Sampling

The delay line and the middle level of the serial register form the basis of the reflected double sampling circuit. This circuit is used for noise elimination. The delay line is easily removed, and the user can make noise measurement comparisons by measuring noise with and without the delay line.

4.4.7 Test Points

The following table lists the test points and signal descriptions of the TCK211.

TEST POINT	SIGNAL
TP0	Ground
TP1	V_{CC} (5 V)
TP2	Strobe trigger (hook on at BNC trigger connection)
TP3	Sync
TP4	Clamp
TP5	Antiblooming gate
TP7	Image area gate
TP9	Serial register gate
TP11	Signal with inverted gain (hook on at junction of R39 and R42)
TP13	Clamped signal
TP15	High-gain or unity-gain signal

4.4.8 Additional Devices

The kit is designed to evaluate three additional CCD sensors: the Texas Instruments TC221, TC225, and TC227. The board will need to be returned to the factory for modification, as additional components that control the antiblooming gate and signal processing are required. Switches 4 and 5 will be set to the appropriate positions for the image sensor selected. Finally, if the TC225 is selected, switches 2 and 3 will determine which lines of the TC225 will be flushed.

Note:

As the TC225 has 285 lines, it is not possible to image all of them in a 242-line field. Therefore, 45 lines of each field are flushed; switches two and three determine whether these are the top, middle or bottom 45 lines.

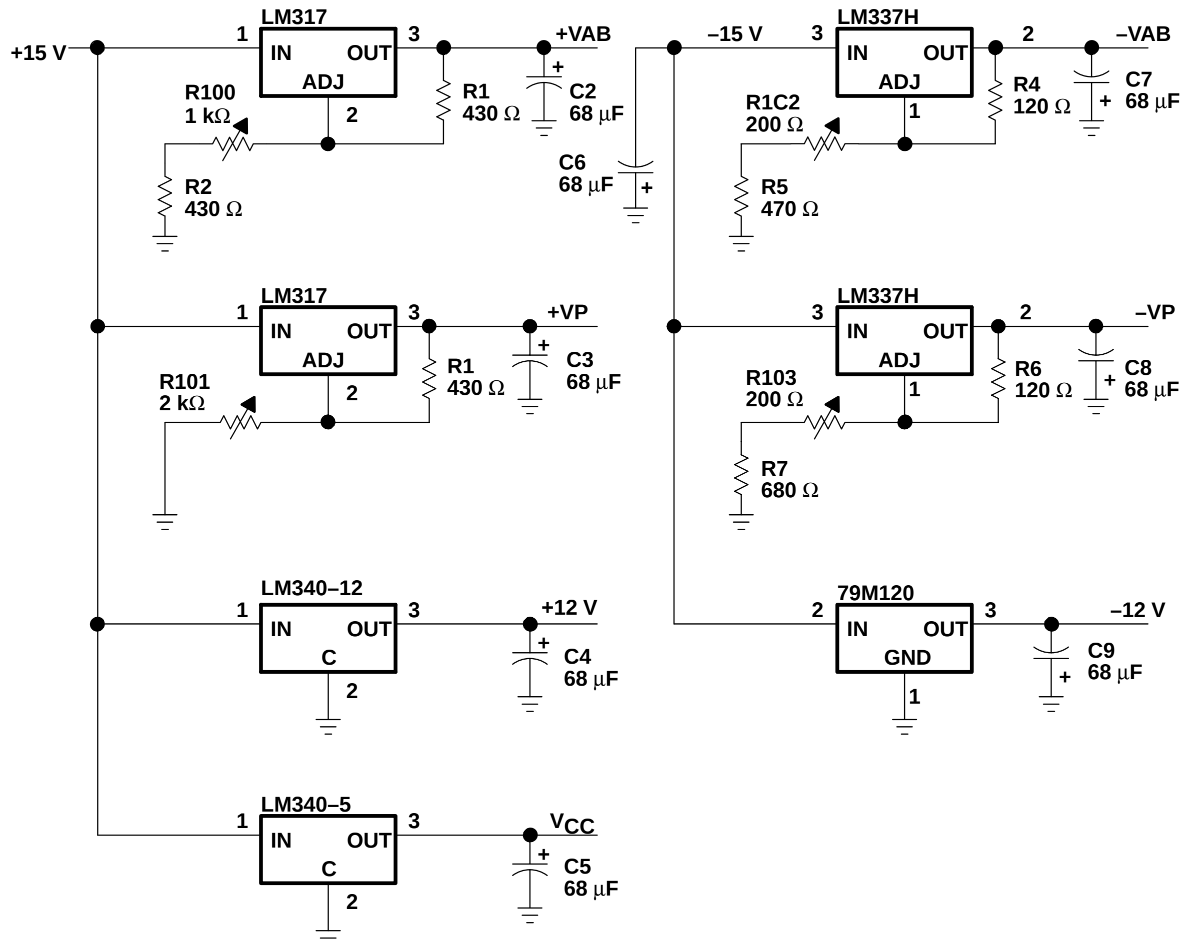

Figure 3. Small Imager Voltage Regulators

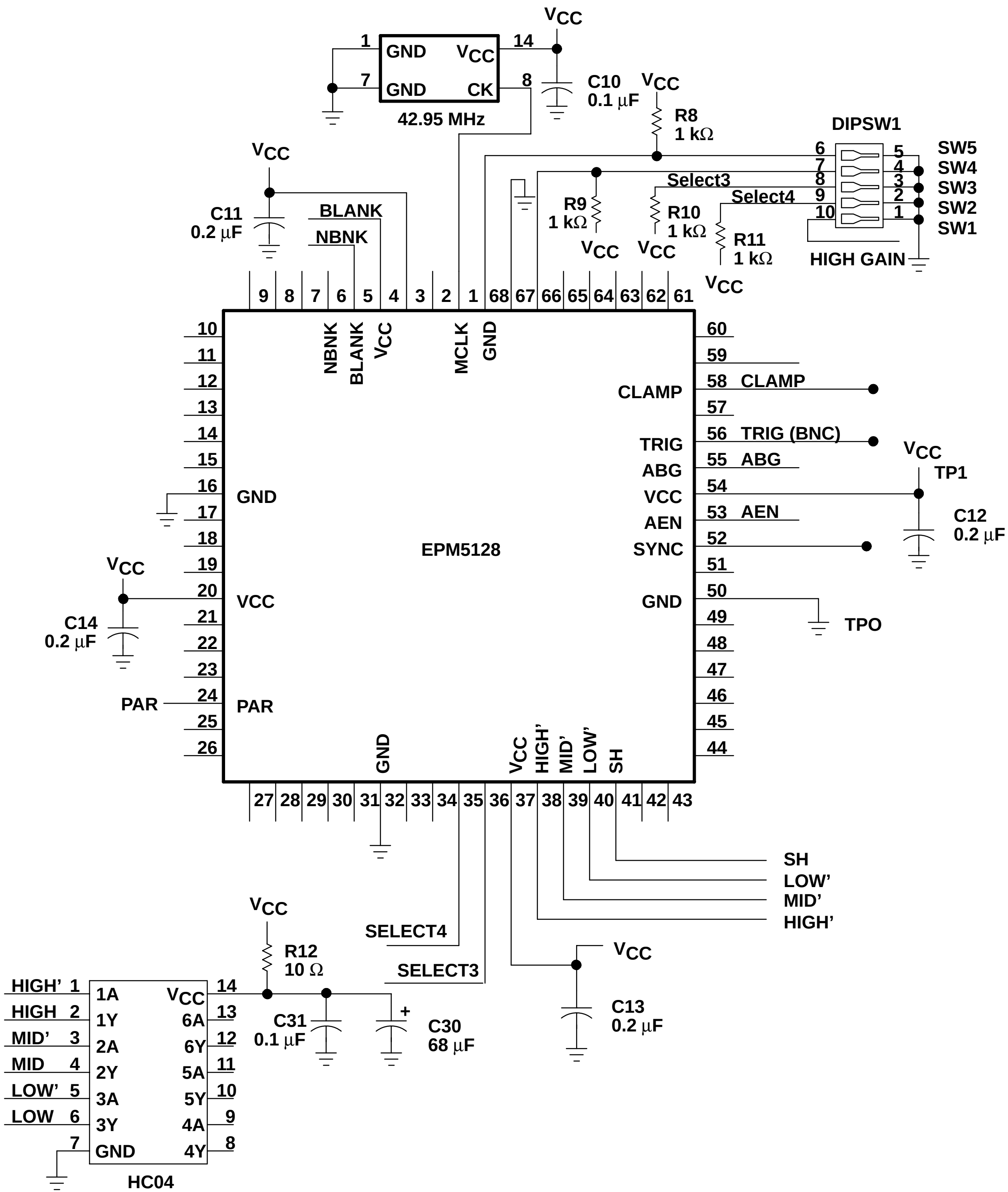

Figure 4.   Small Imager Timing and Drive Circuitry

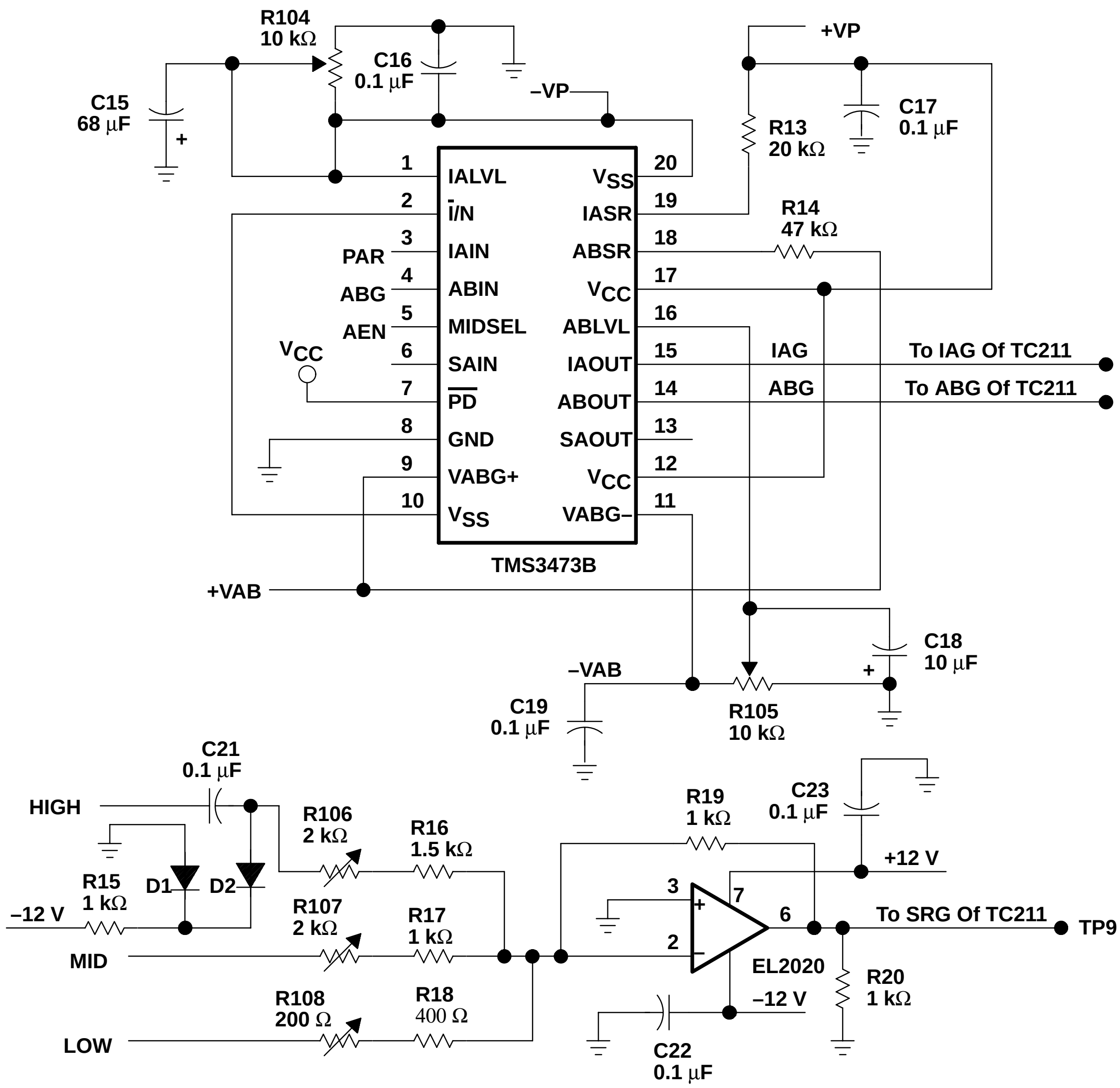

Figure 4. Small Imager Timing and Drive Circuitry (Continued)

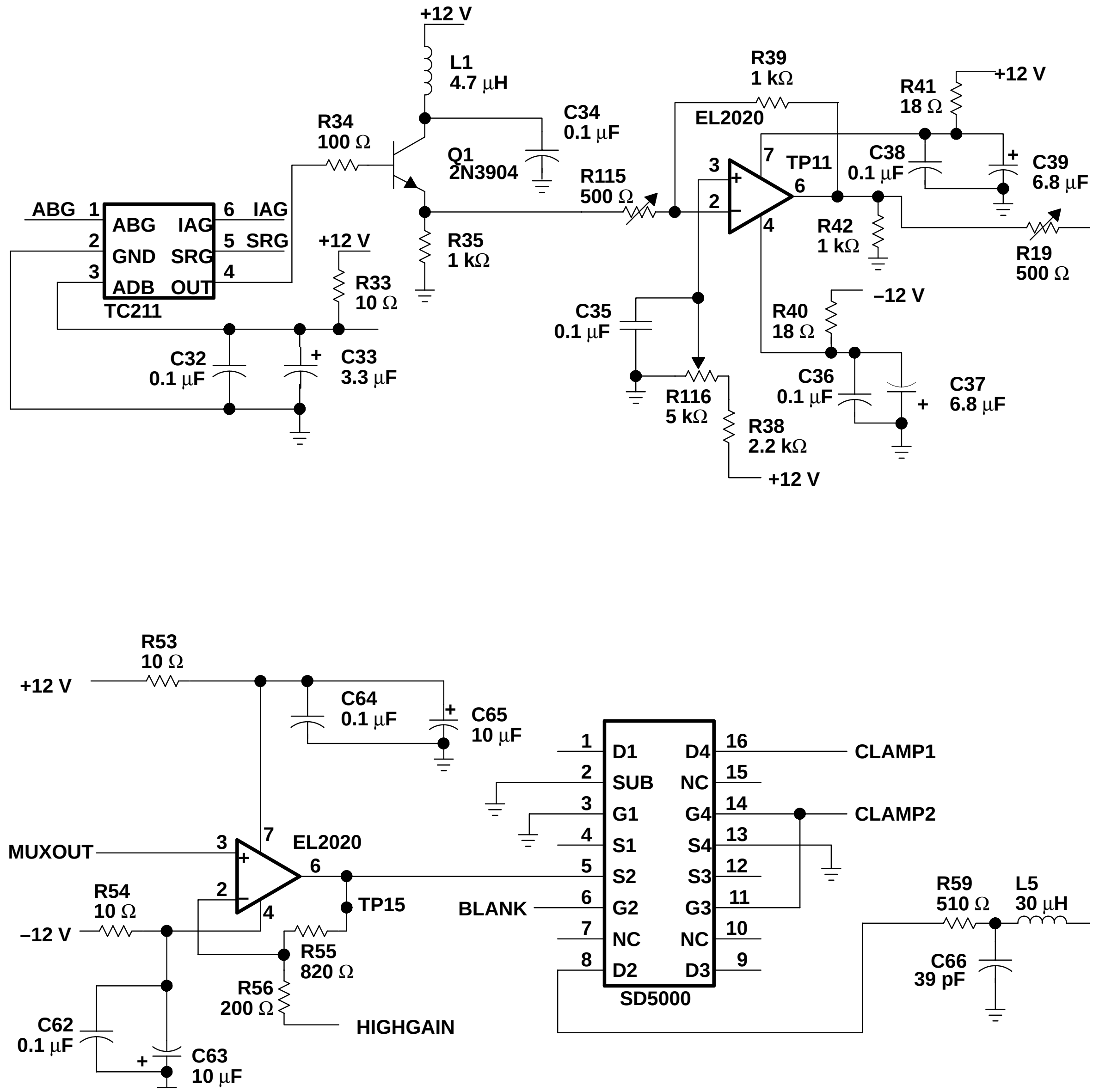

Figure 5. Small Imager Signal Processing

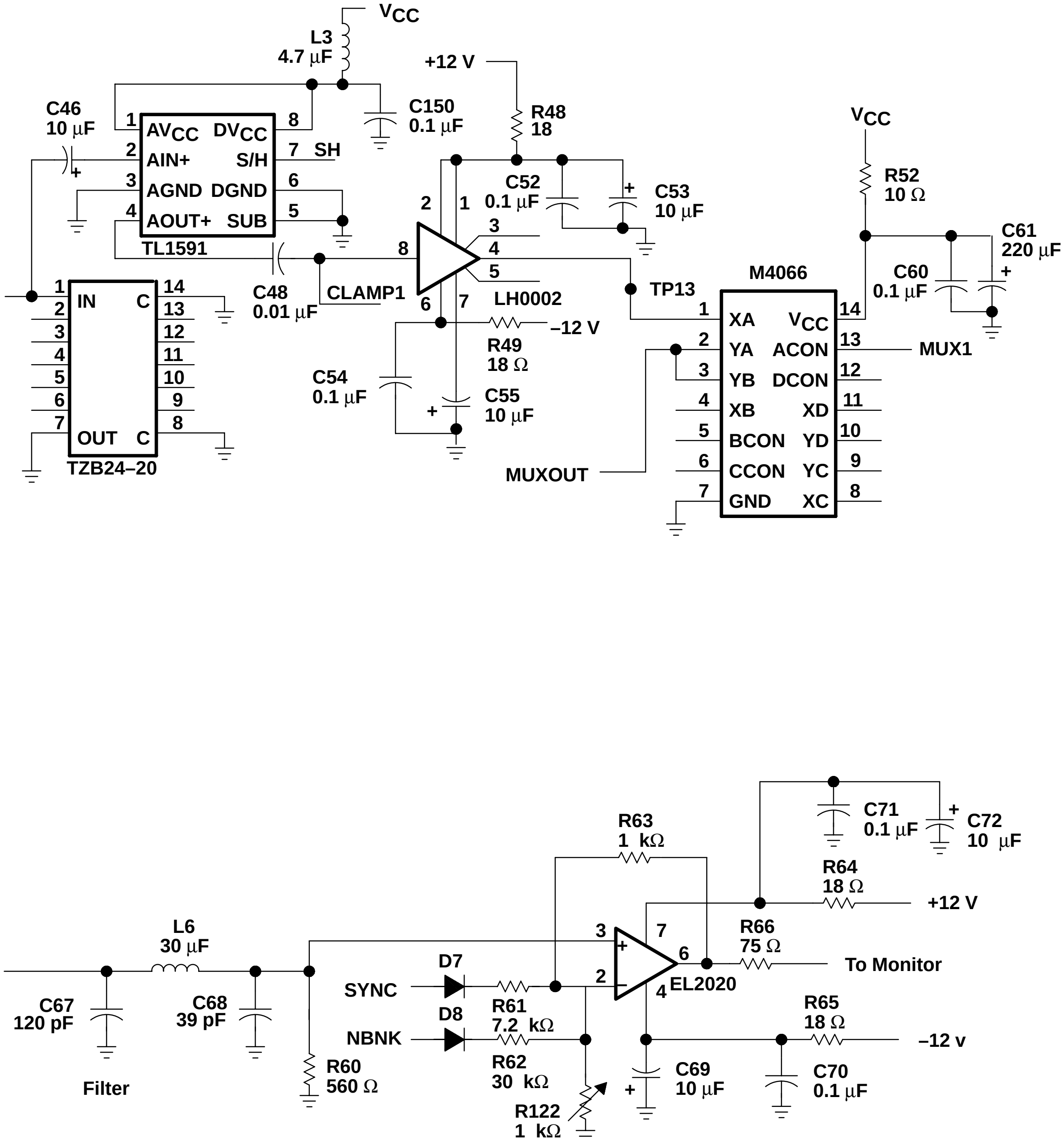

Figure 5. Small Imager Signal Processing (Continued)

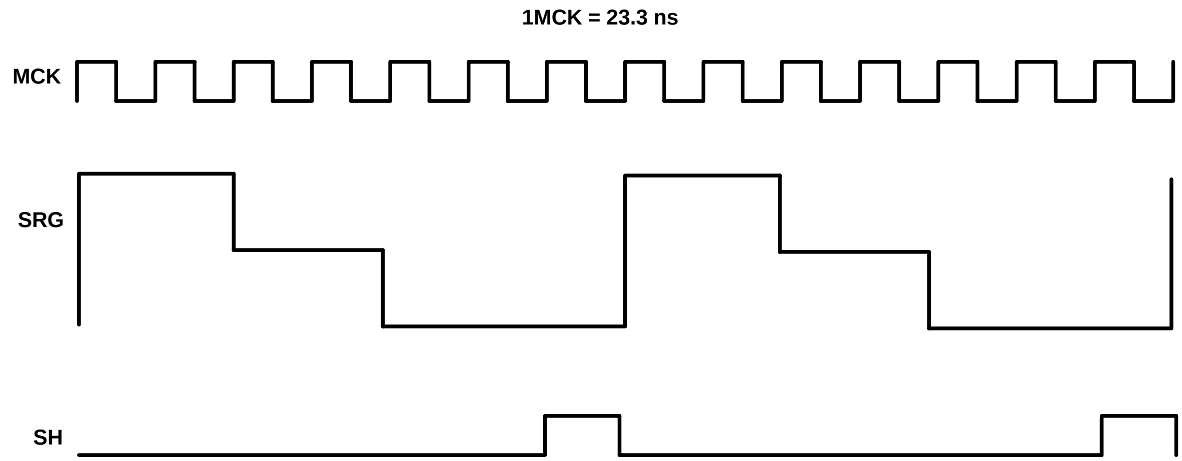

Figure 6. *Serial Register Timing*

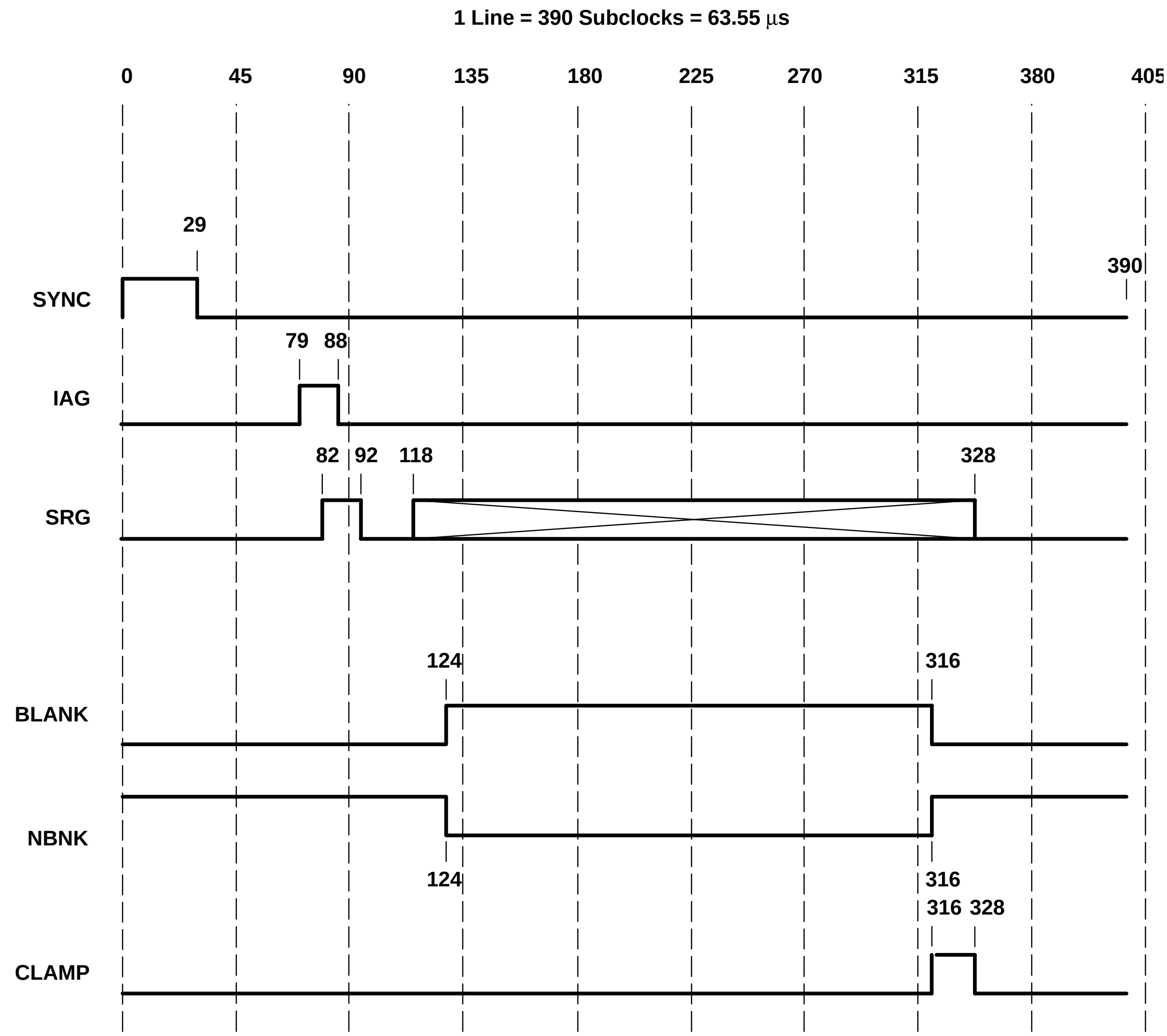

Figure 7. *Horizontal Timing*

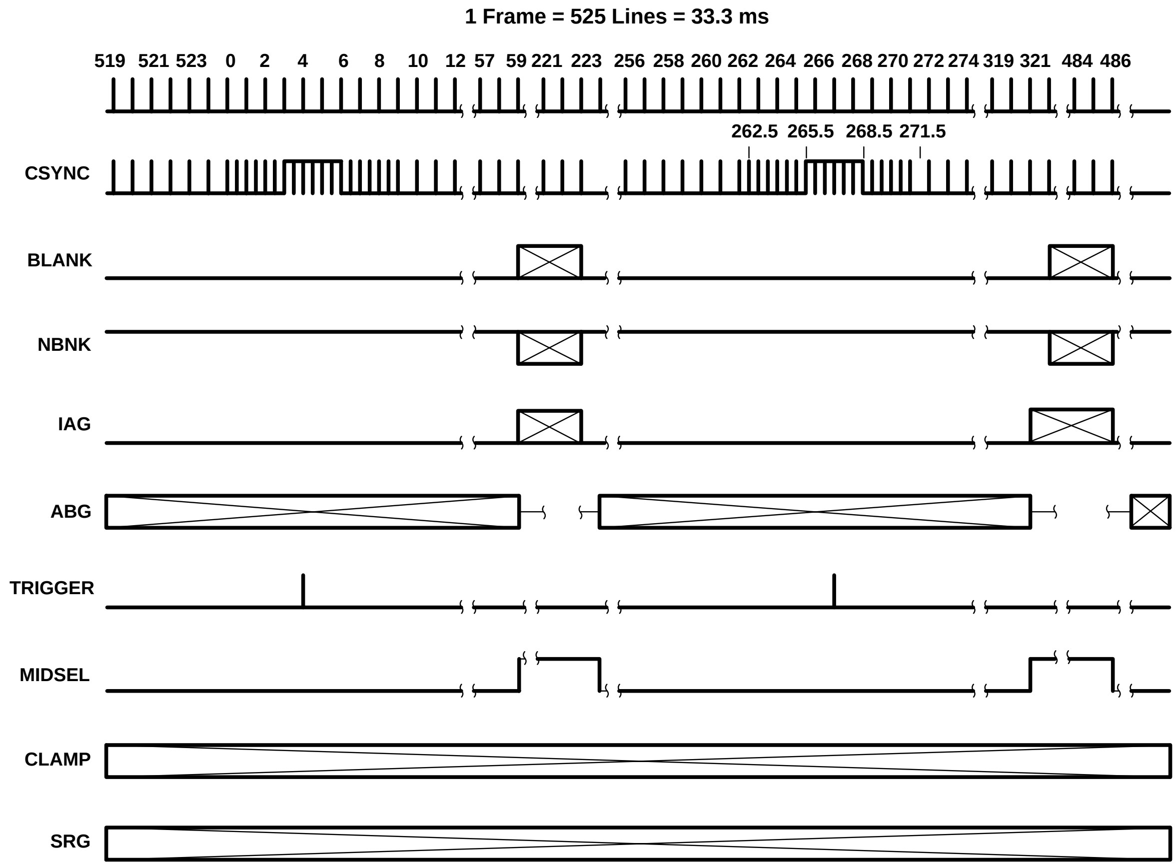

Figure 8. Vertical Timing

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