TMS470R1x External Clock Prescale (ECP) Reference Guide

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REVISION HISTORY

REVISION	DATE	NOTES
B	11/04	Removed author names; released to mass market.
A	9/02	Converted to a stand-alone book
*	2/00	*Pre-dates revision history*

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External Clock Prescaler (ECP)

The external clock prescaler (ECP) provides the TMS470R1x family of devices with an external output clock (ECLK). The ECP is multiplexed with a GIO pin.

1 Functional Description of the ECP Module

The ECP allows the device to output a continuous external clock on a general-purpose I/O pin (GIO). The external clock (ECLK) frequency is a user-programmable ratio of the interface clock (ICLK) frequency.

1.1 Overview

Table 1 contains a brief description of the ECP, lists applicable pins, and describes its significant features.

Table 1. ECP Module Overview

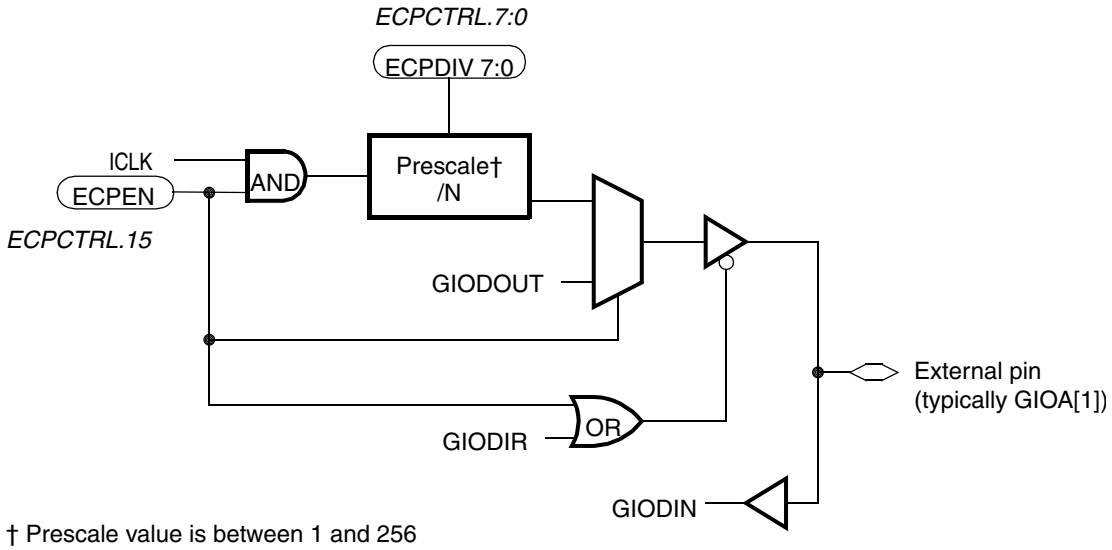
Description	The external clock prescaler provides the device with a free-running external clock that can be scaled from ICLK.
Pins	The ECP is multiplexed through a GIO pin (typically GIOA[1]). A control register is located in the GIO peripheral frame.
Features	The ECPEN bit enables/disables the ECLK output. The ECPDIV provides programmable prescale for generating ECLK from ICLK.

1.2 ECP Block Diagram

The ECP block diagram (see Figure 1) shows the overall functionality of the ECP module. The interface clock (ICLK) input is divided by the user-selected value programmed into the ECPCTRL register. The output of the divider is then multiplexed with the selected GIODOUT register. The output of the multiplexer is controlled by the ECP enable bit (ECPEN), and is output on the external I/O pin of the device.

$$ECLK = \frac{ICLK}{(ECPDIV + 1)}$$

Figure 1. External Clock Prescaler Block Diagram



† Prescale value is between 1 and 256

1.3 ECP Prescaler

The ECP prescaler generates the ECLK signal by dividing ICLK to a lower frequency; the prescale is implemented as a digital counter, programmable via the ECPCTRL register (ECPDIV.7:0). The prescale counts ICLK edges, and when the counter reaches the desired value programmed in ECPDIV.7:0, an ECLK edge is generated.

The prescale divider may be changed while the ECP module is enabled. However, in order to assure a smooth transition between output frequencies, the new prescale value does not take effect until the current ECLK period is complete.

The prescaler can be programmed with divider values ranging from a minimum of 1 to a maximum of 256. The divider values are programmed into the ECPDIV.7:0 bits in the ECPCTRL register (ECPCTRL.7:0). When the ECPDIV.7:0 bits are 0x07, the prescaler is set to divide by 8. This is the default state after reset.

Note: High Frequency Output May Generate EMI

High ECLK frequencies may result in electromagnetic interference (EMI).

1.4 ECP Enable

The ECPEN bit (ECPCTRL.15) controls the external I/O pin function of the device, as shown in Table 2.

Table 2. Settings for ECPEN

ECPEN	GIODIRx	External I/O Pin Function
0	0	GIO input
0	1	GIO output
1	x	ECLK output

You control the multiplexer output via the ECPEN bit in the ECPCTRL register (ECPCTRL.15). If the ECPEN bit is set, the multiplexer outputs ECLK on the external I/O pin of the device. If ECPEN is cleared, the multiplexer allows control of the external pin by the GIO control registers. See Chapter 4, *General-Purpose Input/Output*, of the *TMS470 Peripheral Module User Guide, Volume 1*, literature number SPNU166, for more information.

1.5 Standby and Halt Modes

When the device enters standby or halt mode, the ICLK input is disabled. Therefore, the ECLK output is also disabled. After waking up from low-power modes, the ECP returns to its previous state, and you do not need to reconfigure the ECPCTRL register after the ECP wakes up from standby or halt mode.

1.6 Suspend

When the ECP is in suspend mode, the ECP control register can still be modified. This allows you to modify the control register when a JTAG emulator/debugger tool is being used.

When the ECPCOS bit (ECPCTRL.14) is set, the ECP continues to output its ECLK if the ECPEN bit is set when the ECP is in suspend mode.

2 ECP Control Register (ECPCTRL)

This section describes the ECP control register. This register supports 16-bit and 32-bit write accesses.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x300	ECP EN	Reserved						ECP COS	ECPDIV.7:0							
	RW-0							RW-0	RW-0						RW-1	

RWP = Read in all modes, write in privilege mode only; *-n* = Value after reset

† The ECPCTRL register is located within the GIO peripheral frame. The physical address of the register is device specific. Please see the device-specific data sheet for the physical address of the ECPCTRL register.

Bit 15 **ECPEN.** ECP enable.

Any operation mode (read/write):

0 = ECLK output is disabled. GIO registers control the device I/O pin.
1 = ECLK output is enabled. ECLK output will be seen on the device I/O pin.

Bits 14:9 **Reserved.**

Reads are undefined and writes have no effect.

Bit 8 **ECPCOS.** ECP continue on suspend.

Any operation mode (read/write):

0 = ECLK output is disabled in suspend mode. ECLK output will not be seen on the I/O pin of the device.
1 = ECLK output is enabled in suspend mode. ECLK output will be seen on the I/O pin of the device.

Bits 7:0 **ECPDIV 7:0.** ECP divider value.

Any operation mode (read/write):

The value of the ECPDIV 7:0 bits determine the external clock (ECLK) output frequency as a ratio of the interface clock (ICLK), as shown in Equation 1.

Equation 1. External Clock Output

Where 0xFF $\geq$ *ECPDIV* $\geq$ 0x00

After reset, ECPDIV 7:0 = 0x07.