TMS470R1x Interrupt Expansion Module (IEM) Reference Guide

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REVISION HISTORY

REVISION	DATE	NOTES
A	9/02	Converted to a stand-alone book
*	6/01	*Initial version*

Contents

Interrupt Expansion Module (IEM)

This document describes the Interrupt Expansion Module (IEM). The IEM works with the Central Interrupt Module (CIM) to extend the TMS470R1Vx system to support up to 64 interrupt sources and provide programmable-interrupt priorities.

Topic **Page**

1 Overview

This document describes an extension to the basic CIM interrupt control capabilities for selected TMS470R1VX devices. The IEM is an optional extension to the TMS470R1VX system module. See the device-specific data sheet to verify if the IEM is included in your system module.

1.1 CIM Functionality

The 470R1Vx system includes a central interrupt module (CIM). This module controls and prioritizes interrupt requests originating from peripheral modules on a device. The CIM provides the following basic features:

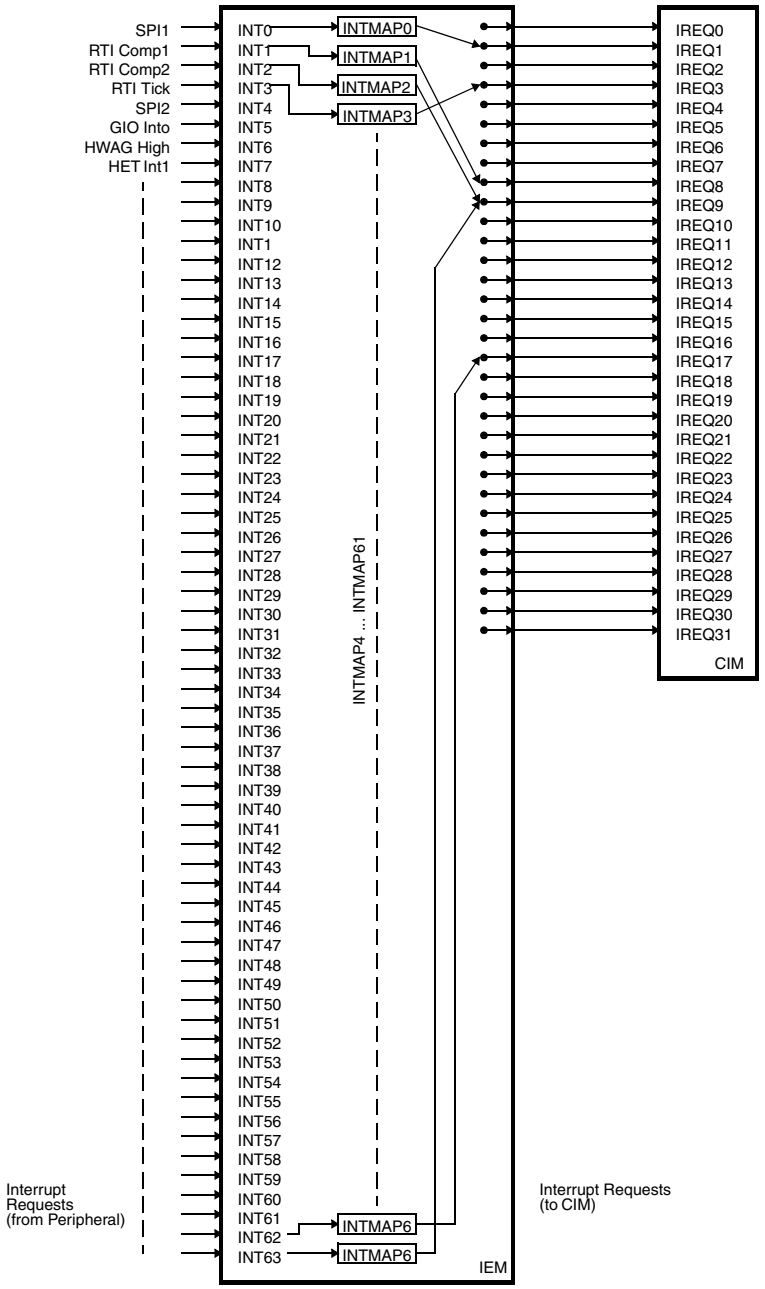
- 32 interrupt request inputs
- For each interrupt request:
  - Mask bit (enable/disable)
  - Level bit selects fast interrupt request (FIQ) or interrupt request (IRQ) level
  - Flag bit (read to determine if request pending)
- Three vector generators provide hardware assist for interrupt prioritizing and dispatch:
  - FIQIVEC provides hardware vector for all interrupts on the FIQ level.
  - IRQIVEC provides hardware vector for all interrupts on IRQ level.
  - CIMIVEC is a unified vector generator which returns either the value of FIQIVEC if the CPU is in the FIQ mode, or the value of IRQIVEC if the CPU is in the IRQ mode.
- Fixed priority scheme
  - CIM interrupt request 0 has highest priority.
  - CIM interrupt request 31 has lowest priority.

1.2 IEM Functionality

The IEM expands the number of interrupts in a 470R1VX system to 64. The programmability of the IEM allows software to control the interrupt priority or make the device backwards compatible with other 470 devices that lack the IEM. A block diagram of the IEM, shown in the default state following reset, is provided in Figure 1. In the reset state, the IEM is transparent for the first 32 interrupts in the system because they pass directly through the IEM to the first

32 CIM interrupt requests. Interrupts 31 through 63 share the CIM interrupt request 31 by default.

Figure 1. IEM in Default State



As illustrated in Figure 1, the IEM is used to map the interrupt requests from peripheral modules in the 470R1Vx system (INT[63:0]) to the CIM interrupt requests IREQ[31:0].

For each interrupt input, INT[n], there is a corresponding mapping register bit field INTMAP[4:0], which determines which CIM interrupt request the peripheral interrupt request maps to.

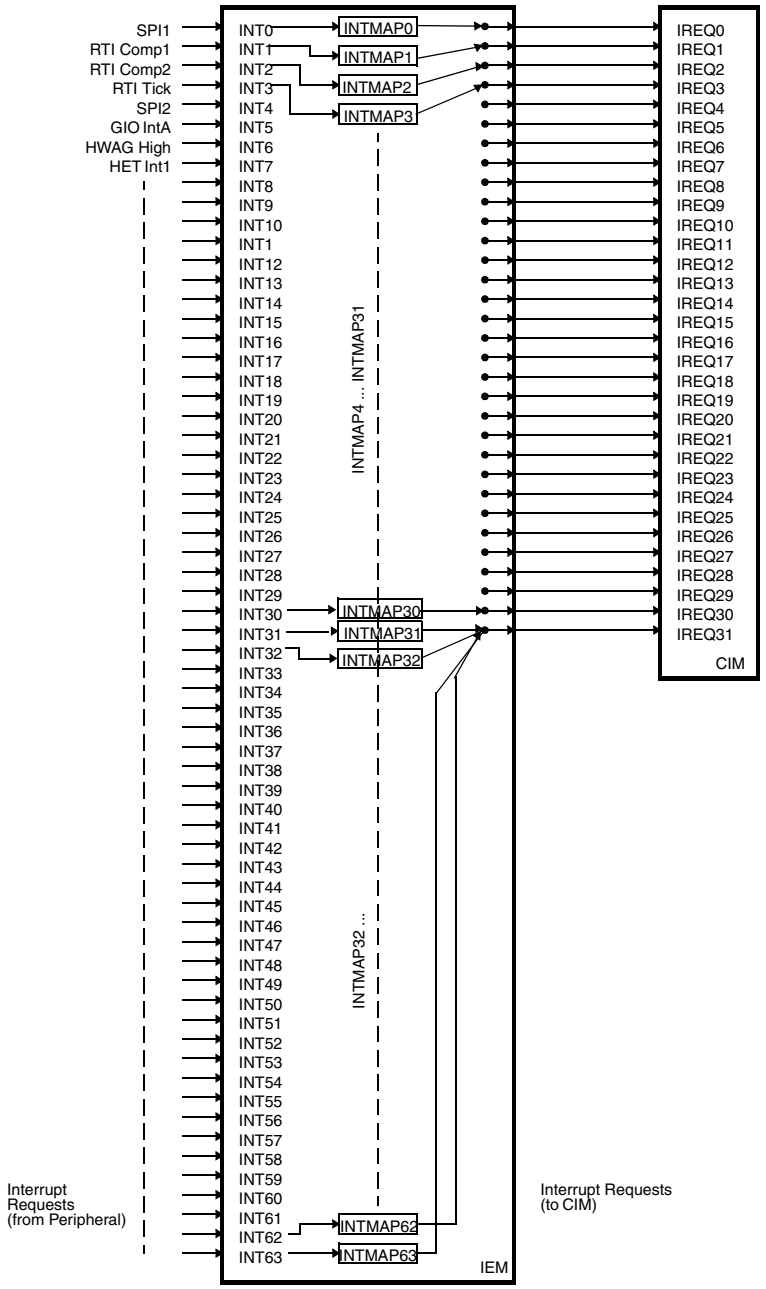
1.3 IEM Features

The IEM provides the following features:

- ❏ Accepts up to 64 interrupt requests from peripherals on a 470R1Vx device
- ❏ Maps each of the up to 64 interrupt requests to one of the 32 CIM interrupt channels
- ❏ Provides programmable-interrupt priority
- ❏ Default mapping compatible with SE470R1B11B device
- ❏ Mapping two or more interrupt requests to the same CIM channel results in interrupt sharing
- ❏ Transparent for channels 0-30 until programmed. See Figure 2.

Figure 2 provides a block diagram of the IEM partially reprogrammed. In this example, INTMAP0[4:0] has been reprogrammed to 0x01, INTMAP1[4:0] to 0x08, INTMAP2[4:0] to 0x09, INTMAP3[4:0] to 0x03, INTMAP62 to 0x11, and INTMAP63 to 0x09. Note that interrupts INT2 and INT63 both share the CIM interrupt request channel 9.

Figure 2. IEM in Partially Reprogrammed State



1.4 Interrupt Sharing

More than one peripheral interrupt request can be mapped to a single CIM interrupt request. In this case, the CIM interrupt request is shared among all of the peripherals mapped to it. If any peripheral asserts an interrupt request, it is registered by the CIM, which generates an interrupt to the 470R1Vx CPU if the interrupt request is enabled in the CIM.

Because the CIM interrupt request inputs are level sensitive, sharing a CIM interrupt request is a simple OR function. The interrupt request stays active until all interrupts sharing the CIM channel have been serviced.

For CIM channels that are shared, the IEMs INTPEND[0] and INTPEND[1] registers can be polled to determine which of the interrupts sharing a CIM channel generated the request.

2 IEM Control Registers

This section describes the IEM control register frame. The IEM control register frame is illustrated in Table 1.

For the interrupt-pending registers, the default state after reset depends upon whether the peripherals connected to the IEM assert an interrupt request during reset or not. This makes the default state of these bits after reset device dependent.

Table 1. IEM Control Registers

Address†	Mnemonic	Name	Description	Reset Value‡
0x00	INTPEND0	Interrupt Pending Register 0	Read Only - Returns pending interrupts INT[31:0]	Device dependent
0x04	INTPEND1	Interrupt Pending Register 1	Read Only - Returns pending interrupts INT[63:32]	Device dependent
0x08 - 0x1F	Reserved	N/A	Reserved for future expansion	N/A
0x20	INTCTRL0	Interrupt Control Register 0	Controls mapping of INT[3:0] to CIM channels	0x00010203
0x24	INTCTRL1	Interrupt Control Register 1	Controls mapping of INT[7:4] to CIM channels	0x04050607
0x28	INTCTRL2	Interrupt Control Register 2	Controls mapping of INT[11:8] to CIM channels	0x08090A0B
0x2C	INTCTRL3	Interrupt Control Register 3	Controls mapping of INT[15:12] to CIM channels	0x0C0D0E0F
0x30	INTCTRL4	Interrupt Control Register 4	Controls mapping of INT[19:16] to CIM channels	0x10111213
0x34	INTCTRL5	Interrupt Control Register 5	Controls mapping of INT[23:20] to CIM channels	0x14151617
0x38	INTCTRL6	Interrupt Control Register 6	Controls mapping of INT[27:24] to CIM channels	0x18191A1B
0x3C	INTCTRL7	Interrupt Control Register 7	Controls mapping of INT[31:28] to CIM channels	0x1C1D1E1F
0x40	INTCTRL8	Interrupt Control Register 8	Controls mapping of INT[35:32] to CIM Channels	0x1F1F1F1F
0x44	INTCTRL9	Interrupt Control Register 9	Controls mapping of INT[39:36] to CIM channels	0x1F1F1F1F
0x48	INTCTRL10	Interrupt Control Register 10	Controls mapping of INT[43:40] to CIM channels	0x1F1F1F1F
0x4C	INTCTRL11	Interrupt Control Register 11	Controls mapping of INT[47:44] to CIM channels	0x1F1F1F1F
0x50	INTCTRL12	Interrupt Control Register 12	Controls mapping of INT51:48] to CIM channels	0x1F1F1F1F
0x54	INTCTRL13	Interrupt Control Register 13	Controls mapping of INT[55:52] to CIM channels	0x1F1F1F1F
0x58	INTCTRL14	Interrupt Control Register 14	Controls mapping of INT[59:56] to CIM channels	0x1F1F1F1F
0x5C	INTCTRL15	Interrupt Control Register 15	Controls mapping of INT[63:60] to CIM channels	0x1F1F1F1F
0x60 - 0xFF	Reserved	N/A	Reserved for future expansion	N/A

† Addresses listed are offset address from the base of the IEM.

‡ For simplicity, the reset value listed in this column appears with reserved bits masked to zero. The CPU can read a different value after reset due to the indeterminate nature of the reserved bits.

2.1 IEM Interrupt Pending Register 0 (INTPEND 0)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x00	INT PEND 31	INT PEND 30	INT PEND 29	INT PEND 28	INT PEND 27	INT PEND 26	INT PEND 25	INT PEND 24	INT PEND 23	INT PEND 22	INT PEND 21	INT PEND 20	INT PEND 19	INT PEND 18	INT PEND 17	INT PEND 16
	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT PEND 15	INT PEND 14	INT PEND 13	INT PEND 12	INT PEND 11	INT PEND 10	INT PEND 9	INT PEND 8	INT PEND 7	INT PEND 6	INT PEND 5	INT PEND 4	INT PEND 3	INT PEND 2	INT PEND 1	INT PEND 0
	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:0 **INTPEND[31:0].** Interrupt Pending Status.

This register contains one bit INTPEND[n] for each IEM interrupt request input INT[n]. Each interrupt-pending bit reflects whether the peripheral interrupt request connected to the corresponding IEM interrupt request input is pending or not.

It is useful to read this register when multiple IEM interrupt request inputs are mapped to the same CIM interrupt request channel. In this case, the CIM produces a single vector for all peripherals sharing a particular CIM interrupt channel. Instead of polling the peripherals individually, the IEM can be polled to determine which of the peripherals sharing an interrupt line requires service.

For each bit INTPEND[n]:

INTPEND[n] = 1, the peripheral connected to INT[n] requests an interrupt.
INTPEND[n] = 0, the peripheral connected to INT[n] does not request an interrupt.

Note:

For simplicity, the reset value of this register is listed as undefined. In reality, it is device dependent and depends upon whether each peripheral connected to the IEM asserts or does not assert individual interrupt requests during reset.

2.2 IEM Interrupt Pending Register 1 (INTPEND 1)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x04	INT PEND 63	INT PEND 62	INT PEND 61	INT PEND 60	INT PEND 59	INT PEND 58	INT PEND 57	INT PEND 56	INT PEND 55	INT PEND 54	INT PEND 53	INT PEND 52	INT PEND 51	INT PEND 50	INT PEND 49	INT PEND 48
	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT PEND 47	INT PEND 46	INT PEND 45	INT PEND 44	INT PEND 43	INT PEND 42	INT PEND 41	INT PEND 40	INT PEND 39	INT PEND 38	INT PEND 37	INT PEND 36	INT PEND 35	INT PEND 34	INT PEND 33	INT PEND 32
	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U	R-U

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:0 **INTPEND[63:32].** Interrupt Pending Status.

This register contains one bit INTPEND[n] for each IEM interrupt request input INT[n]. Each interrupt-pending bit reflects whether the peripheral interrupt request connected to the corresponding IEM interrupt request input is pending or not.

It is useful to read this register when multiple IEM interrupt request inputs are mapped to the same CIM interrupt request channel. In this case, the CIM produces a single vector for all peripherals sharing a particular CIM interrupt channel. Instead of polling the peripherals individually, the IEM can be polled to determine which of the peripherals sharing an interrupt line need to be serviced.

For each bit INTPEND[n]:

INTPEND[n] = 1, the peripheral connected to INT[n] requests an interrupt.
INTPEND[n] = 0, the peripheral connected to INT[n] does not request an interrupt.

Note:

For simplicity, the reset value of this register is listed as undefined. In reality, it is device dependent and depends upon whether each peripheral connected to the IEM asserts or does not assert individual interrupt requests during reset.

2.3 IEM Interrupt Control Register 0 (INTCTRL 0)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x20	Reserved			INTMAP0[4:0]					Reserved			INTMAP1[4:0]				
	R-U			RWP-00000					R-U			RWP-00001				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP2[4:0]					Reserved			INTMAP3[4:0]				
	R-U			RWP-00010					R-U			RWP-00011				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP0[4:0].** IEM Interrupt Request INT0 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT0 maps to:

00000 Interrupt Request INT0 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT0 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT0 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 00000. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP1[4:0].** IEM Interrupt Request INT1 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT1 maps to:

00000 Interrupt Request INT1 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT1 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT1 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 0000. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP2[4:0].** IEM Interrupt Request INT2 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT2 maps to:

00000 Interrupt Request INT2 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT2 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT2 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 00010. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP3[4:0].** IEM Interrupt Request INT3 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT3 maps to:

00000 Interrupt Request INT3 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT3 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT3 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 00011. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.4 IEM Interrupt Control Register 1 (INTCTRL 1)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x24	Reserved			INTMAP4[4:0]					Reserved			INTMAP5[4:0]				
	R-U			RWP-00100					R-U			RWP-00101				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP6[4:0]					Reserved			INTMAP7[4:0]				
	R-U			RWP-00110					R-U			RWP-00111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP4[4:0].** IEM Interrupt Request INT4 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT4 maps to:

00000 Interrupt Request INT4 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT4 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT4 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 00100. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP5[4:0].** IEM Interrupt Request INT5 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT5 maps to:

00000 Interrupt Request INT5 maps to CIM Channel IREQ[0].
00001 Interrupt Request INT5 maps to CIM Channel IREQ[1]....
11111 Interrupt Request INT5maps to CIM Channel IREQ[31].

The default value of these bits after reset is 00101. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP6[4:0].** IEM Interrupt Request INT6 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT6 maps to:

00000 Interrupt Request INT6 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT6 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT6 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 00110. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP7[4:0].** IEM Interrupt Request INT7 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT7 maps to:

00000 Interrupt Request INT7 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT7 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT7 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 000111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.5 IEM Interrupt Control Register 2 (INTCTRL 2)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x28	Reserved			INTMAP8[4:0]					Reserved			INTMAP9[4:0]				
	R-U			RWP-01000					R-U			RWP-01001				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP10[4:0]					Reserved			INTMAP11[4:0]				
	R-U			RWP-01010					R-U			RWP-01011				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP8[4:0].** IEM Interrupt Request INT8 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT8 maps to:

00000 Interrupt Request INT8 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT8 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT8 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 01000. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP9[4:0].** IEM Interrupt Request INT9 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT9 maps to:

00000 Interrupt Request INT9 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT9 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT9 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 01001. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP10[4:0].** IEM Interrupt Request INT10 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT10 maps to:

00000 Interrupt Request INT10 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT10 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT10 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 01010. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP11[4:0].** IEM Interrupt Request INT11 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT11 maps to:

00000 Interrupt Request INT11 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT11 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT11 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 01011. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.6 IEM Interrupt Control Register 3 (INTCTRL 3)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x2C	Reserved			INTMAP12[4:0]					Reserved			INTMAP13[4:0]				
	R-U			RWP-01100					R-U			RWP-01101				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP14[4:0]					Reserved			INTMAP15[4:0]				
	R-U			RWP-01110					R-U			RWP-01111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP12[4:0].** IEM Interrupt Request INT12 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT12 maps to:

00000 Interrupt Request INT12 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT12 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT12 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 01100. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP13[4:0].** IEM Interrupt Request INT13 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT13 maps to:

00000 Interrupt Request INT13 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT13 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT13 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 01101. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP14[4:0].** IEM Interrupt Request INT14 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT14 maps to:

00000 Interrupt Request INT14 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT14 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT14 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 01110. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP15[4:0].** IEM Interrupt Request INT15 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT15 maps to:

00000 Interrupt Request INT15 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT15 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT15 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 01111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.7 IEM Interrupt Control Register 4 (INTCTRL 4)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x30	Reserved			INTMAP16[4:0]					Reserved			INTMAP17[4:0]				
	R-U			RWP-10000					R-U			RWP-10001				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP18[4:0]					Reserved			INTMAP19[4:0]				
	R-U			RWP-10010					R-U			RWP-10011				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP16[4:0].** IEM Interrupt Request INT16 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT16 maps to:

00000 Interrupt Request INT16 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT16 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT16 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 10000. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP17[4:0].** IEM Interrupt Request INT17 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT17 maps to:

00000 Interrupt Request INT17 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT17 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT17 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 10001. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP18[4:0].** IEM Interrupt Request INT18 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT18 maps to:

00000 Interrupt Request INT18 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT18 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT18 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 10010. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP19[4:0].** IEM Interrupt Request INT19 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT19 maps to:

00000 Interrupt Request INT19maps to CIM Channel IREQ[0]
00001 Interrupt Request INT19 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT19 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 10011. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.8 IEM Interrupt Control Register 5 (INTCTRL 5)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x34	Reserved			INTMAP20[4:0]					Reserved			INTMAP21[4:0]				
	R-U			RWP-10100					R-U			RWP-10101				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, -n = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP22[4:0]					Reserved			INTMAP23[4:0]				
	R-U			RWP-10110					R-U			RWP-10111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP20[4:0].** IEM Interrupt Request INT20 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT20 maps to:

00000	Interrupt Request INT20 maps to CIM Channel IREQ[0]
00001	Interrupt Request INT20 maps to CIM Channel IREQ[1]...
11111	Interrupt Request INT20 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 10100. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP21[4:0].** IEM Interrupt Request INT21 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT21 maps to:

00000	Interrupt Request INT21 maps to CIM Channel IREQ[0]
00001	Interrupt Request INT21 maps to CIM Channel IREQ[1]...
11111	Interrupt Request INT21 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 10101. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP22[4:0].** IEM Interrupt Request INT22 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT22 maps to:

00000 Interrupt Request INT22 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT22 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT22 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 10110. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP23[4:0].** IEM Interrupt Request INT23 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT23 maps to:

00000 Interrupt Request INT23 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT23 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT23 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 10111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.9 IEM Interrupt Control Register 6 (INTCTRL 6)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x38	Reserved			INTMAP24[4:0]					Reserved			INTMAP25[4:0]				
	R-U			RWP-11000					R-U			RWP-11001				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP26[4:0]					Reserved			INTMAP27[4:0]				
	R-U			RWP-11010					R-U			RWP-11011				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP24[4:0].** IEM Interrupt Request INT24 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT24 maps to:

00000 Interrupt Request INT24 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT24 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT24 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11000. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP25[4:0].** IEM Interrupt Request INT25 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT25 maps to:

00000 Interrupt Request INT25 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT25 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT25 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11001. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP26[4:0].** IEM Interrupt Request INT26 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT26 maps to:

00000 Interrupt Request INT26 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT26 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT26 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11010. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP27[4:0].** IEM Interrupt Request INT27 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT27 maps to:

00000 Interrupt Request INT27 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT27 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT27 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11011. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.10 IEM Interrupt Control Register 7 (INTCTRL 7)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x3C	Reserved			INTMAP28[4:0]					Reserved			INTMAP29[4:0]				
	R-U			RWP-11100					R-U			RWP-11101				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP30[4:0]					Reserved			INTMAP31[4:0]				
	R-U			RWP-11110					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP28[4:0].** IEM Interrupt Request INT28 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT28 maps to:

00000 Interrupt Request INT28 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT28 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT28 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11100. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP29[4:0].** IEM Interrupt Request INT29 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT29 maps to:

00000 Interrupt Request INT29 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT29 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT29 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11101. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP30[4:0].** IEM Interrupt Request INT30 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT30 maps to:

00000 Interrupt Request INT30 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT30 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT30 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11110. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP31[4:0].** IEM Interrupt Request INT31 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT31 maps to:

00000 Interrupt Request INT31 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT31 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT31 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.11 IEM Interrupt Control Register 8 (INTCTRL 8)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x40	Reserved			INTMAP32[4:0]					Reserved			INTMAP33[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP34[4:0]					Reserved			INTMAP35[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP32[4:0].** IEM Interrupt Request INT32 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT32 maps to:

00000 Interrupt Request INT32 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT32 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT32 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP33[4:0].** IEM Interrupt Request INT33 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT33 maps to:

00000 Interrupt Request INT33 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT33 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT33 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP34[4:0].** IEM Interrupt Request INT34 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT34 maps to:

00000 Interrupt Request INT34 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT34 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT34 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP35[4:0].** IEM Interrupt Request INT35 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT35 maps to:

00000 Interrupt Request INT35 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT35 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT35 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.12 IEM Interrupt Control Register 9 (INTCTRL 9)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x44	Reserved			INTMAP36[4:0]					Reserved			INTMAP37[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP38[4:0]					Reserved			INTMAP39[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP36[4:0].** IEM Interrupt Request INT36 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT36 maps to:

00000 Interrupt Request INT36 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT36 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT36 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP37[4:0].** IEM Interrupt Request INT37 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT37 maps to:

00000 Interrupt Request INT37 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT37 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT37 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP38[4:0].** IEM Interrupt Request INT38 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT38 maps to:

00000 Interrupt Request INT38 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT38 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT38 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP39[4:0].** IEM Interrupt Request INT39 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT39 maps to:

00000 Interrupt Request INT39 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT39 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT39 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.13 IEM Interrupt Control Register 10 (INTCTRL 10)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x48	Reserved			INTMAP40[4:0]					Reserved			INTMAP41[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP42[4:0]					Reserved			INTMAP43[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved;**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP40[4:0].** IEM Interrupt Request INT40 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT40 maps to:

00000 Interrupt Request INT40 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT40 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT40 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP41[4:0].** IEM Interrupt Request INT41 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT41 maps to:

00000 Interrupt Request INT41 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT41 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT41 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP42[4:0].** IEM Interrupt Request INT42 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT42 maps to:

00000 Interrupt Request INT42 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT42 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT42 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP43[4:0].** IEM Interrupt Request INT43 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT43 maps to:

00000 Interrupt Request INT43 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT43 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT43 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.14 IEM Interrupt Control Register 11 (INTCTRL 11)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x4C	Reserved			INTMAP44[4:0]					Reserved			INTMAP45[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP46[4:0]					Reserved			INTMAP47[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP44[4:0].** IEM Interrupt Request INT44 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT44 maps to:

00000	Interrupt Request INT44 maps to CIM Channel IREQ[0]
00001	Interrupt Request INT44 maps to CIM Channel IREQ[1]...
11111	Interrupt Request INT44 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP45[4:0].** IEM Interrupt Request INT45 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT45 maps to:

00000	Interrupt Request INT45 maps to CIM Channel IREQ[0]
00001	Interrupt Request INT45 maps to CIM Channel IREQ[1]...
11111	Interrupt Request INT45 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP46[4:0].** IEM Interrupt Request INT46 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT46 maps to:

00000 Interrupt Request INT46 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT46 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT46 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP47[4:0].** IEM Interrupt Request INT47 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT47 maps to:

00000 Interrupt Request INT47 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT47 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT47 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.15 IEM Interrupt Control Register 12 (INTCTRL12)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x50	Reserved			INTMAP48[4:0]					Reserved			INTMAP49[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP50[4:0]					Reserved			INTMAP51[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP48[4:0].** IEM Interrupt Request INT48 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT48 maps to:

00000 Interrupt Request INT48 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT48 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT48 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP49[4:0].** IEM Interrupt Request INT49 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT49 maps to:

00000 Interrupt Request INT49 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT49 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT49 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP50[4:0].** IEM Interrupt Request INT50 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT50 maps to:

00000 Interrupt Request INT50 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT50 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT50 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP51[4:0].** IEM Interrupt Request INT51 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT51 maps to:

00000 Interrupt Request INT51 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT51 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT51 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.16 IEM Interrupt Control Register 13 (INTCTRL 13)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x54	Reserved			INTMAP52[4:0]					Reserved			INTMAP53[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP54[4:0]					Reserved			INTMAP55[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP52[4:0].** IEM Interrupt Request INT52 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT52 maps to:

00000 Interrupt Request INT52 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT52 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT52 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP53[4:0].** IEM Interrupt Request INT53 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT53 maps to:

00000 Interrupt Request INT53 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT53 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT53 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP54[4:0].** IEM Interrupt Request INT54 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT54 maps to:

00000 Interrupt Request INT54 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT54 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT54 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP55[4:0].** IEM Interrupt Request INT55 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT55 maps to:

00000 Interrupt Request INT55 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT55 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT55 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.17 IEM Interrupt Control Register 14 (INTCTRL 14)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x58	Reserved			INTMAP56[4:0]					Reserved			INTMAP57[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP58[4:0]					Reserved			INTMAP59[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP56[4:0].** IEM Interrupt Request INT56 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT56 maps to:

00000 Interrupt Request INT56 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT56 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT56 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP57[4:0].** IEM Interrupt Request INT57 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT57 maps to:

00000 Interrupt Request INT57 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT57 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT57 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP58[4:0].** IEM Interrupt Request INT58 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT58 maps to:

00000 Interrupt Request INT58 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT58 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT58 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP59[4:0].** IEM Interrupt Request INT59 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT59 maps to:

00000 Interrupt Request INT59 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT59 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT59 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

2.18 IEM Interrupt Control Register 15 (INTCTRL 15)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x5C	Reserved			INTMAP60[4:0]					Reserved			INTMAP61[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			INTMAP62[4:0]					Reserved			INTMAP63[4:0]				
	R-U			RWP-11111					R-U			RWP-11111				

R = Read, W = Write, WP = Write from privilege mode only, S = Set, U = Undefined, *-n* = Value after reset

Bits 31:29 **Reserved .**

Reads are indeterminate; writes have no effect.

Bits 28:24 **INTMAP60[4:0].** IEM Interrupt Request INT60 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT60 maps to:

00000 Interrupt Request INT60 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT60 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT60 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 23:21 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 20:16 **INTMAP61[4:0].** IEM Interrupt Request INT61 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT61 maps to:

00000 Interrupt Request INT61 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT61 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT61 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 15:13 **Reserved.**

Reads are indeterminate; writes have no effect.

Bits 12:8 **INTMAP62[4:0].** IEM Interrupt Request INT62 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT62 maps to:

00000 Interrupt Request INT62 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT62 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT62 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.

Bits 7:5 **Reserved .**

Reads are indeterminate; writes have no effect.

Bits 4:0 **INTMAP63[4:0].** IEM Interrupt Request INT63 Mapping Control.

These bits determine which CIM channel the IEM Interrupt Request INT63 maps to:

00000 Interrupt Request INT63 maps to CIM Channel IREQ[0]
00001 Interrupt Request INT63 maps to CIM Channel IREQ[1]...
11111 Interrupt Request INT63 maps to CIM Channel IREQ[31]

The default value of these bits after reset is 11111. These bits can be written only while the CPU is in privilege mode. This register supports byte writes.