TMS470R1x Digital Watchdog Reference Guide

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Texas Instruments

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REVISION HISTORY

REVISION	DATE	NOTES
*	7/04	Initial version

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Digital Watchdog (DWD) Module

The digital watchdog (DWD) module monitors software operation and implements system reset functions upon CPU disruption. If the software enters into an improper loop, or if the CPU becomes temporarily disrupted, the DWD timer underflows to assert a system reset.

The DWD timer is an 25-bit resettable decrementing counter that provides a system reset when the watchdog counter expires. With its consistent performance, the watchdog increases the reliability of the CPU, thus ensuring system integrity.

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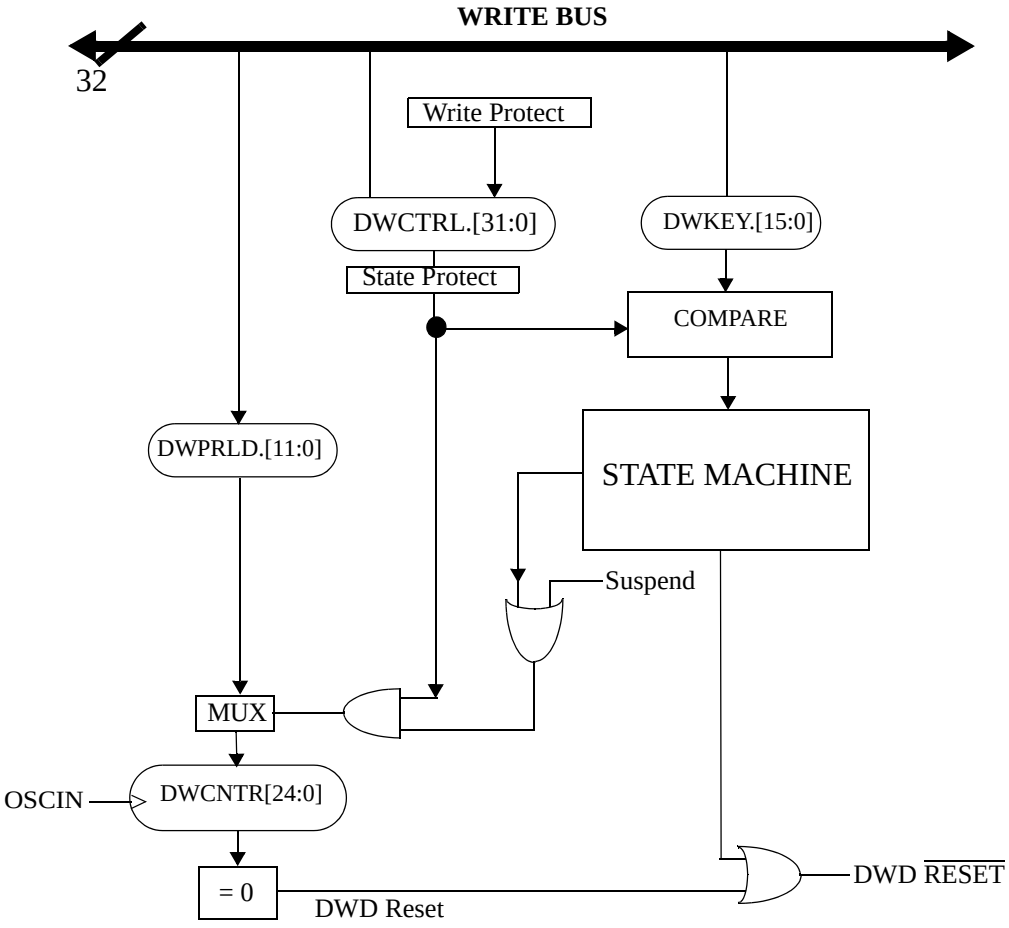
1 Features

See Figure 1 for a block diagram of the DWD module. The DWD module design includes the following features:

- ❏ 32-bit DWD enable located in the DWD control register (DWCTRL)
- ❏ 12-bit programmable preload value that provides a flexible watchdog expiration time (DWPRLD)
- ❏ 16-bit DWD key (DWKEY) register that reloads the DWD counter when the correct combination of values are written, and generates a system reset if an incorrect value is written to the DWKEY register
- ❏ 25-bit DWD counter that generates a system reset when the DWD counter expires

Figure 1. DWD Block Diagram



2 Operation

This section describes how to operate the DWD.

Note:

By default, when the device is initially powered, the DWD is disabled. Once enabled, the DWD counter cannot be disabled by software. Only a system RESET will disable the DWD counter.

System reset is the only point at which the DWEN bits are returned to their default values.

2.1 Configuration

The following sections explain how to set up, enable, and service the DWD.

2.1.1 Setting Up the DWD

You must first initialize the DWD preload register before the DWD will operate correctly. The DWD preload register is a 12-bit programmable register that provides the expiration time for the DWD counter.

Note:

Once the DWD has been enabled, the preload register cannot be written to by the CPU.

The expiration time is the time allotted for periodically servicing the DWD. The DWD counter expiration time is determined with the equation:

$t_{exp} = 2^{13} * (DWPRLD + 1) / OSCIN,$ *(EQ 1)*

where DWPRLD = 0,1,2,..,(2^{12} - 1) and t_{exp} is the counter expiration time.

The values for OSCIN are defined in the specific device datasheet. The preload value should be written only after a system reset or when the watchdog is serviced. After the preload value has been loaded into the DWPRLD register, the DWD counter must be enabled. This is accomplished by writing a key to the DWD control register (DWCTRL). Once enabled, the DWD counter begins decrementing. The resolution of the down-counter for the DWD counter, based on a minimum OSCIN of 4 MHz and a maximum of 20 MHz, is:

$0.41\ ms < (2^{13}/OSCIN) < 2.0\ ms$ *(EQ 2)*

The range of values for the DWD counter, based on a minimum OSCIN of 4 MHz and a maximum of 20 MHz, is:

$$1.68\ s < (2^{25} / OSCIN) < 8\ s \qquad (EQ\ 3)$$

2.1.2 Enabling the DWD

The robustness of the DWD is maintained by a 32-bit state machine. Activate the DWD counter by writing to the DWCTRL register. Any write, with the exception of 0x5312ACED, enables the DWD counter. This initial write can occur at any time during code execution. All write accesses made to this register after the DWD counter has been activated will have no effect. The DWD counter can only be disabled by a system reset.

TI's recommendation for enabling the DWD counter is to write 0xACED5312 into the DWCTRL register. This is the complement of the default value in the register (0x5312ACED). Writing 0xACED5312 provides further stability and robustness.

2.1.3 Servicing the DWD

The DWD counter is reloaded when the proper sequence is written to the DWKEY before the DWD counter expires. The watchdog counter is enabled to be reloaded when a value of 0xE51A is written to the DWKEY. Then when 0xA35C is written to the DWKEY register, the DWD counter is reloaded.

Any value written to the DWKEY other than 0xE51A or 0xA35C will cause a system reset (system reset exception status register bit 13). Any sequence of 0xE51A and 0xA35C can be written to the DWKEY register without causing a system reset. However, only a write of 0xE51A followed by a write of 0xA35C to the DWKEY reloads the DWD counter. Table 1 shows an example of a register sequence.

Table 1. Example DWKEY Register Sequence

Step	Value Written to WKEY	Result
1	0x0A35C	No action.
2	0x0A35C	No action.
3	0x0E51A	DWKEY is enabled for reloading by the next 0x0A35C.
4	0x0E51A	DWKEY is enabled for reloading by the next 0x0A35C.
5	0x0E51A	DWKEY is enabled for reloading by the next 0x0A35C.
6	0x0A35C	Watchdog is reloaded.
7	0x0A35C	No action.
8	0x0E51A	DWKEY is enabled for reloading by the next 0x0A35C.
9	0x0A35C	Watchdog is reloaded.
10	0x0E51A	DWKEY is enabled for reloading by the next 0x0A35C.
11	0x02332	System reset because of an improper key value written to DWKEY.

2.2 Debug Mode

When the device is in suspend and $\overline{\text{TRST}}$ is high, the counter stops decrementing. This situation provides more flexibility during software development and debugging.

2.3 Low Power Mode

When the system enters standby mode, the DWD counter remains active since it is clocked from OSCIN. However, in halt mode, the DWD counter is inactive since the clock source has been disabled. Therefore, the DWD will not generate a system reset in halt mode.

Note:

In standby mode, the DWD remains active. In halt mode, the DWD is inactive.

3 Register Description

Table 2 describes the registers for the DWD

Table 2. Register Description

Address	Mnemonic	Name	Description
0xFFFFFF60	DWCTRL	DWD Control Register	Enables the DWD counter
0xFFFFFF64	DWPRLD	DWD Preload Register	Contains the programmable preload value
0xFFFFFF68	DWKEY	DWD Key Register	Correct sequence written to this register resets the DWD counter
0xFFFFFF6C	DWCNTR	DWD Counter Register	Register displaying the current value of the DWD counter

4 Internal Registers

Figure 2 illustrates the internal register.

Figure 2. Internal Register Map

Address Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0	Page
Digital Watchdog (DWD) Registers																	
0xFFFFFF60 DWCTRL	DWEN.31:16																8
	DWEN.15:0																
0xFFFFFF64 DWPRLD	Reserved																9
	Reserved				DWPRLD.11:0												
0xFFFFFF68 DWKEY	Reserved																10
	DWKEY.15:0																
0xFFFFFF6C DWCNTR	Reserved							DWCNTR.24:16									11
	DWCNTR.15:0																

4.1 DWD Control (DWCTRL) Register

The DWD control register, shown in Figure 3 and described in Table 3, is used to enable the DWD counter.

Figure 3. DWD Control (DWCTRL) Register

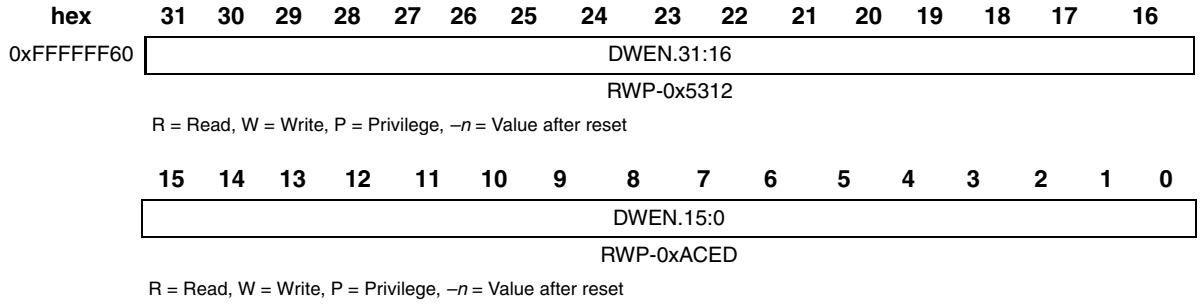


Table 3. DWD Control (DWCTRL) Register Field Descriptions

Bit	Name	Description
31–0	DWEN	DWD Enable User and privilege mode (read): 0x5312ACED = DWD counter is disabled Any other value = DWD counter is enabled Privilege mode (write): By default, the DWD counter is disabled. Any write other than 0x5312ACED to the DWCTRL register enables the counter. This initial write can occur at any time during code execution. Once the initial write has occurred, all other writes are ignored. TI recommends that the value 0xACED5312 be written to activate the counter.

4.2 DWD Preload (DWPRLD) Register

The DWD preload register, shown in Figure 4 and described in Table 4, is used to provide flexible watchdog expiration time.

Figure 4. DWD Preload (DWPRLD) Register

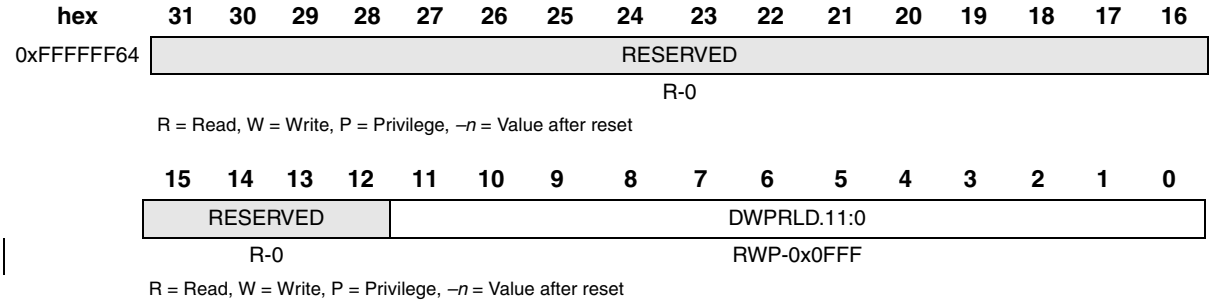


Table 4. DWD Preload (DWPRLD) Register Field Descriptions

Bit	Name	Description
15–12	Reserved	Reads are zero and writes have no effect.
11–0	DWPRLD	DWD Preloader User and privilege mode (read): This bit holds the current contents of the preload register. Privilege mode (write): The preload value must be written before enabling the DWD counter. **Note: The DWPRLD register does not support 8-bit writes.**

4.3 DWD Key (DWKEY) Register

The DWD key register, shown in Figure 5 and described in Table 5, is used to reset the DWD counter.

Figure 5. DWD Key (DWKEY) Register

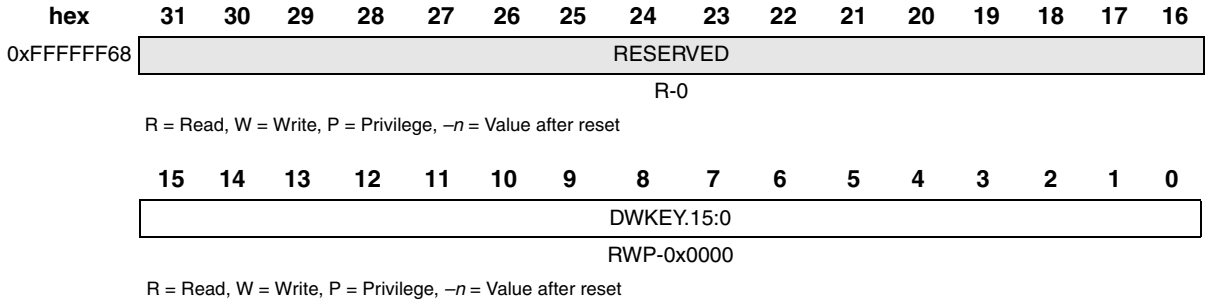


Table 5. DWD Key (DWKEY) Register Field Descriptions

Bit	Name	Description
31–16	Reserved	Reads are zero and writes have no effect.
15–0	DWKEY	DWD Key User and privilege mode (read): Reads are 0. Privilege mode (write): A write of 0xE51A followed by 0xA35C in two separate write operations defines the key sequence and reloads the DWD counter. Any value written to the DWKEY other than 0xE51A or 0xA35C will cause a system reset.

4.4 DWD Counter (DWCNT) Register

The DWD counter register, shown in Figure 6 and described in Table 6, is used to display the current value of the DWD counter.

Figure 6. DWD Counter (DWCNT) Register

Table 6. DWD Counter (DWCNT) Register Field Descriptions

Bit	Name	Description
31–25	Reserved	Reads are zero and writes have no effect.
24–0	DWCNT	DWD Counter User and privilege mode (read): This register, when expired, generates a system RESET. The counter will expire if the DWD key is not written within the calculated expiration time. However, each time the correct DWD key sequence is written, the counter is reloaded. Privilege mode (write): Writes have no effect.