



- **Fast Convergence**
- **Maximum Compensated Echo Path can be Set to 16, 32, or 64 msec**
- **Includes Tone Disabler (2100 Hz) and Comfort Noise Generator as Standalone eXpressDSP Objects Configurable by the User**
- **Robust Double-Talk Detector and Non-Linear Processor**
- **Direct Interface With PCM 8-kHz Sampled Data. Both Sample-By-Sample and Block-Based Processing Supported**
- **No Divergence During Double Talk and Narrow-Band Signals**
- **Passes ITU G.165 Tests 1–6 and ITU G.168 Tests 1, 2A, 2B, 2C, 3A, 3B, 3C, 4, and 5 (1997 Edition)**
- **eXpressDSP-Compliant Algorithm. Code is Reentrant, Supports Multithreading and Dynamic Memory Allocation. At the Same Time Allows Direct (Non-eXpressDSP) Interface to Enable Static Memory Allocation**
- **Can be Easily Ported to any Platform**

**description**

The SPIRIT Echo Canceller conforms to ITU–T G.165/G.168 recommendations. It cancels electrical line echoes caused by 2-to-4 wire conversion hybrids in telephone lines.

**resource requirements**

ALGORITHM	PEAK MIPS	PROGRAM MEMORY (KWORDS)	CONSTANT MEMORY (KWORDS)	DYNAMIC MEMORY (KWORDS)
16 msec echo path	5.9	2359	29	439 x Number of channels
32 msec echo path	8.5			823 x Number of channels
64 msec echo path	13.8			1591 x Number of channels

NOTE: The table shows peak MIPS for 80 sample block.

**availability**

The SPIRIT G.165/G.168 Echo Canceller is available in four forms:

- eXpressDSP-compliant object code for TMS320C54x
- Fully functional eXpressDSP evaluation object at extremely low price
- Portable C code
- Assembly code

The algorithm is supplied with test environment and integration example code.

Detailed product annotation and user guide documents describing testing procedures, interface and integration of this product, as well as PC-based and DSP-based (TI TMS320VC5406 EVM and TMS320VC5402 DSK) demos are available for evaluation upon request. To get additional information on CST software, go to [www.spiritdsp.com/CST](http://www.spiritdsp.com/CST).



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# TMS320C54CST

## G.165/G.168 ECHO CANCELLER ALGORITHM

SPRS181A – OCTOBER 2001 – REVISED MARCH 2003

### performance

FAR END SIGNAL LEVEL (REFERENCE SIGNAL LEVEL)	TIME TO ACHIEVE ACOM > 27 dB (CONVERGENCE SPEED TEST)	STEADY STATE RESIDUAL ECHO LEVEL (NONLINEAR PROCESSOR DISABLED)	ECHO SUPPRESSION	STEADY STATE RESIDUAL ECHO LEVEL (NONLINEAR PROCESSOR ENABLED)
<b>64 MSEC ECHO PATH DELAY</b>				
-30 dBm	<500 msec	-63 dBm	27 dB	<65 dBm
-20 dBm	<200 msec	-62 dBm	36 dB	<65 dBm
-10 dBm	<200 msec	-53 dBm	37 dB	<65 dBm
0 dBm	<200 msec	-42 dBm	36 dB	<51 dBm
<b>32 MSEC ECHO PATH DELAY</b>				
-30 dBm	<500 msec	-65 dBm	29 dB	<65 dBm
-20 dBm	<200 msec	-65 dBm	39 dB	<65 dBm
-10 dBm	<200 msec	-58 dBm	42 dB	<65 dBm
0 dBm	<200 msec	-36 dBm	30 dB	<51 dBm
<b>16 MSEC ECHO PATH DELAY</b>				
-30 dBm	<500 msec	-65 dBm	29 dB	<65 dBm
-20 dBm	<200 msec	-62 dBm	36 dB	<65 dBm
-10 dBm	<150 msec	-55 dBm	39 dB	<65 dBm
0 dBm	<150 msec	-35 dBm	30 dB	<51 dBm



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