

AM17x/AM18x ARM Microprocessor Enhanced Capture (eCAP) Module

User's Guide



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Read This First

About This Manual

Describes the enhanced capture (eCAP) module. The eCAP module is used in systems where accurate timing of external events is important.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
 - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
 - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DSP, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

[SPRUGU3](#) — ***AM1705 ARM Microprocessor System Reference Guide***. Describes the ARM subsystem, system memory, memory protection unit (MPU), device clocking, phase-locked loop controller (PLL), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

[SPRUGR6](#) — ***AM1707 ARM Microprocessor System Reference Guide***. Describes the ARM subsystem, system memory, memory protection unit (MPU), device clocking, phase-locked loop controller (PLL), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

[SPRUGU4](#) — ***AM1806 ARM Microprocessor System Reference Guide***. Describes the ARM subsystem, system memory, memory protection unit (MPU), device clocking, phase-locked loop controller (PLL), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

[SPRUGM9](#) — ***AM1808 ARM Microprocessor System Reference Guide***. Describes the ARM subsystem, system memory, memory protection unit (MPU), device clocking, phase-locked loop controller (PLL), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

[SPRUFU0](#) — ***AM17x/AM18x ARM Microprocessor Peripherals Overview Reference Guide***. Provides an overview and briefly describes the peripherals available on the AM17x/AM18x ARM Microprocessors.

Enhanced Capture (eCAP) Module

The enhanced capture (eCAP) module is essential in systems where accurate timing of external events is important.

1 Introduction

1.1 Purpose of the Peripheral

Uses for eCAP include:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

1.2 Features

The eCAP module includes the following features:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event time-stamps
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

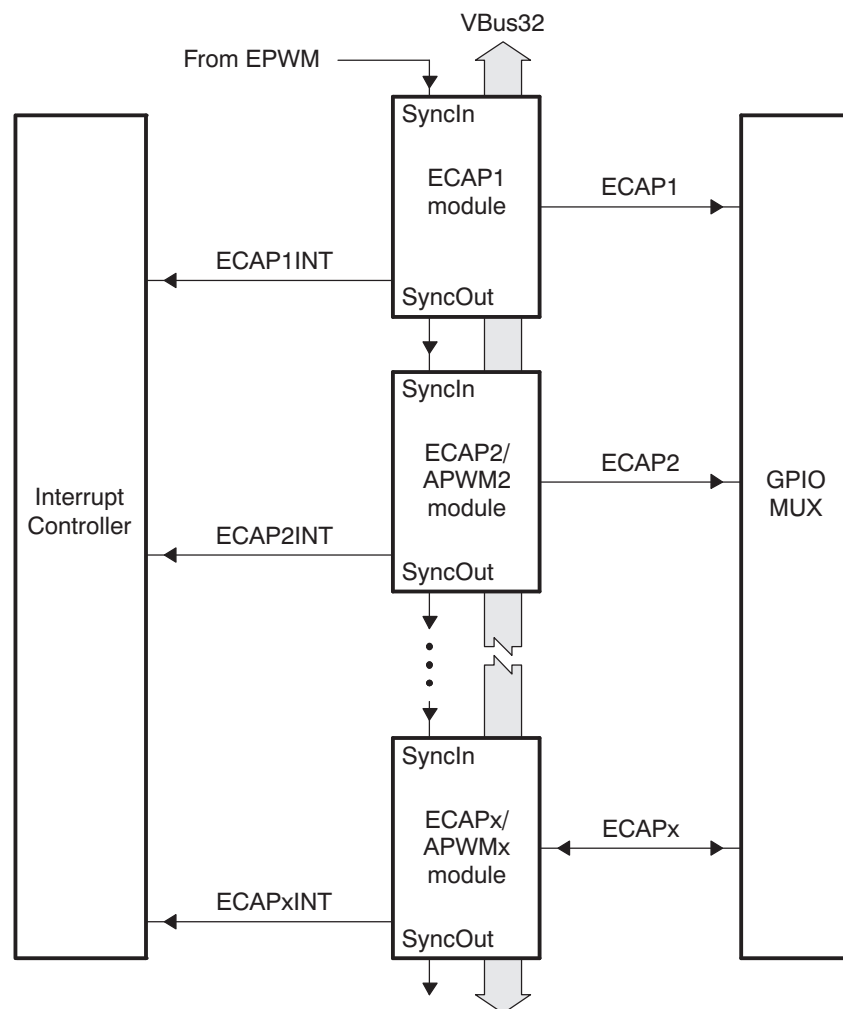
2 Architecture

The eCAP module represents one complete capture channel that can be instantiated multiple times depending on the target device. In the context of this guide, one eCAP channel has the following independent key resources:

- Dedicated input capture pin
- 32-bit time base counter
- 4 × 32-bit time-stamp capture registers (CAP1-CAP4)
- 4-stage sequencer (Modulo4 counter) that is synchronized to external events, ECAP pin rising/falling edges.
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Input capture signal prescaling (from 2-62)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Control for continuous time-stamp captures using a 4-deep circular buffer (CAP1-CAP4) scheme
- Interrupt capabilities on any of the 4 capture events

Multiple identical eCAP modules can be contained in a system as shown in [Figure 1](#). The number of modules is device-dependent and is based on target application needs. In this document, the letter x within a signal or module name is used to indicate a generic eCAP instance on a device.

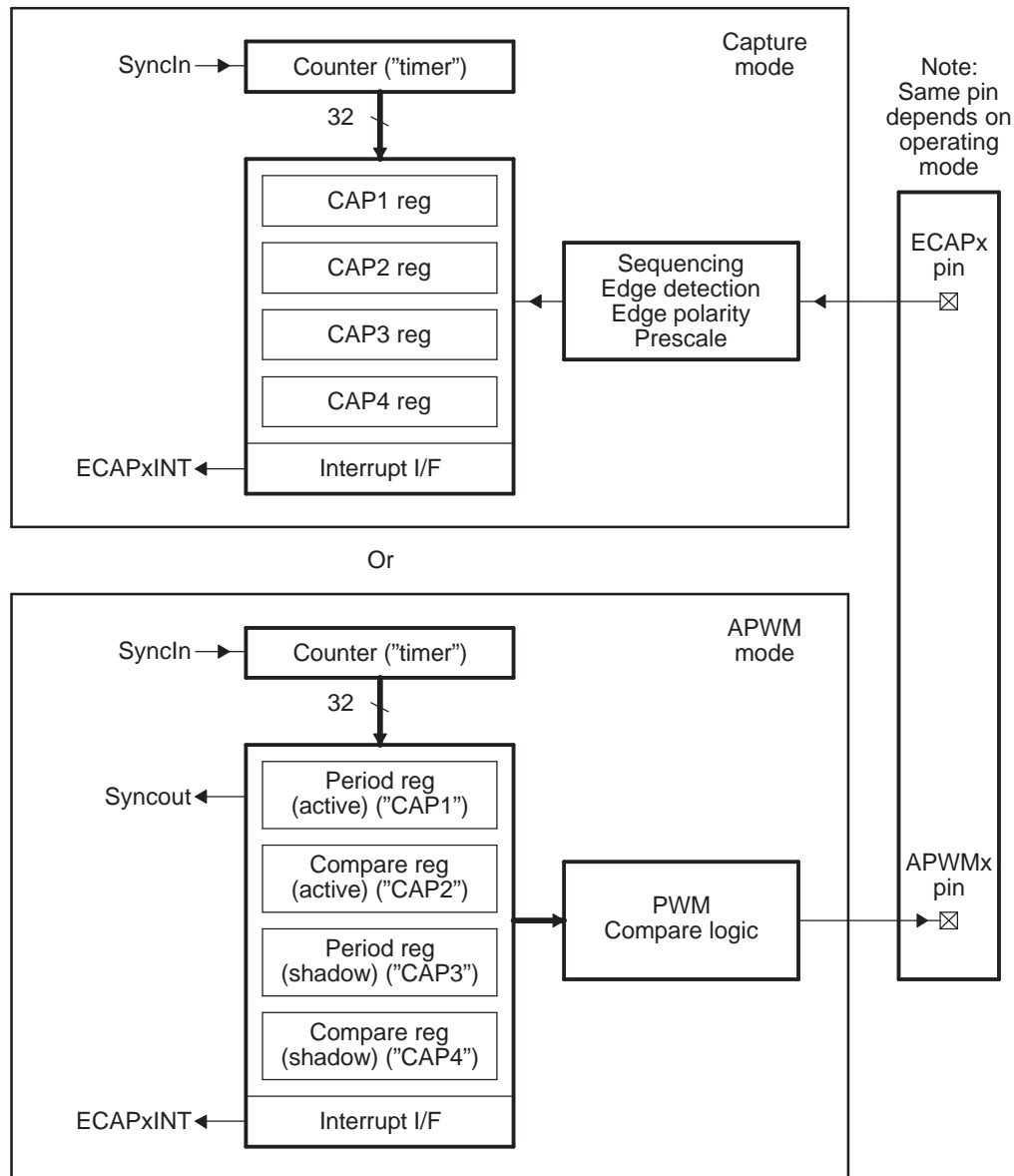
Figure 1. Multiple eCAP Modules



2.1 Capture and APWM Operating Mode

You can use the eCAP module resources to implement a single-channel PWM generator (with 32 bit capabilities) when it is not being used for input captures. The counter operates in count-up mode, providing a time-base for asymmetrical pulse width modulation (PWM) waveforms. The CAP1 and CAP2 registers become the active period and compare registers, respectively, while CAP3 and CAP4 registers become the period and capture shadow registers, respectively. Figure 2 is a high-level view of both the capture and auxiliary pulse-width modulator (APWM) modes of operation.

Figure 2. Capture and APWM Modes of Operation

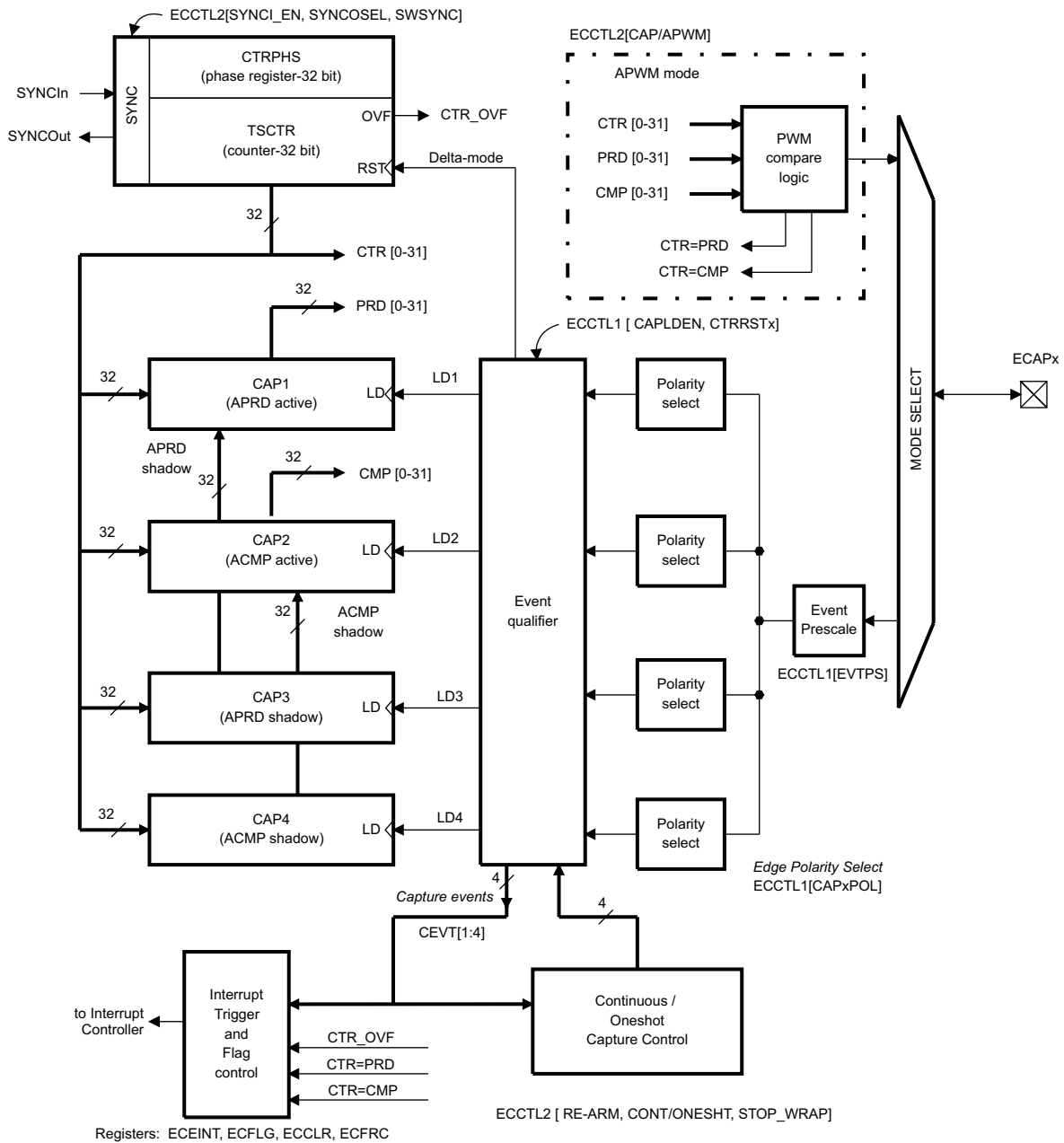


- (1) A single pin is shared between CAP and APWM functions. In capture mode, it is an input; in APWM mode, it is an output.
- (2) In APWM mode, writing any value to CAP1/CAP2 active registers also writes the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 invokes the shadow mode.

2.2 Capture Mode Description

Figure 3 shows the various components that implement the capture function.

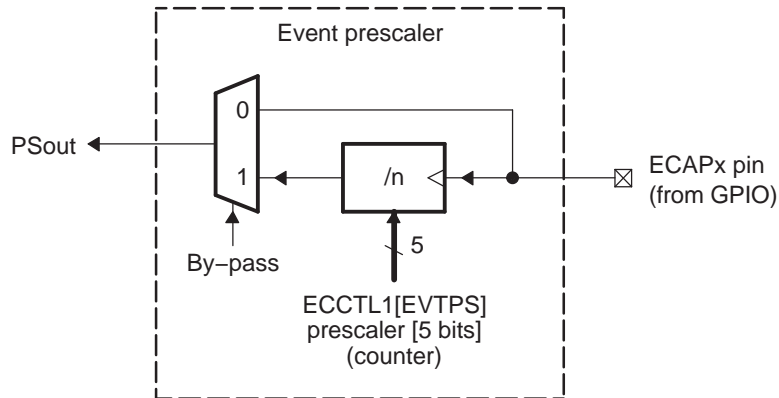
Figure 3. Capture Function Diagram



2.2.1 Event Prescaler

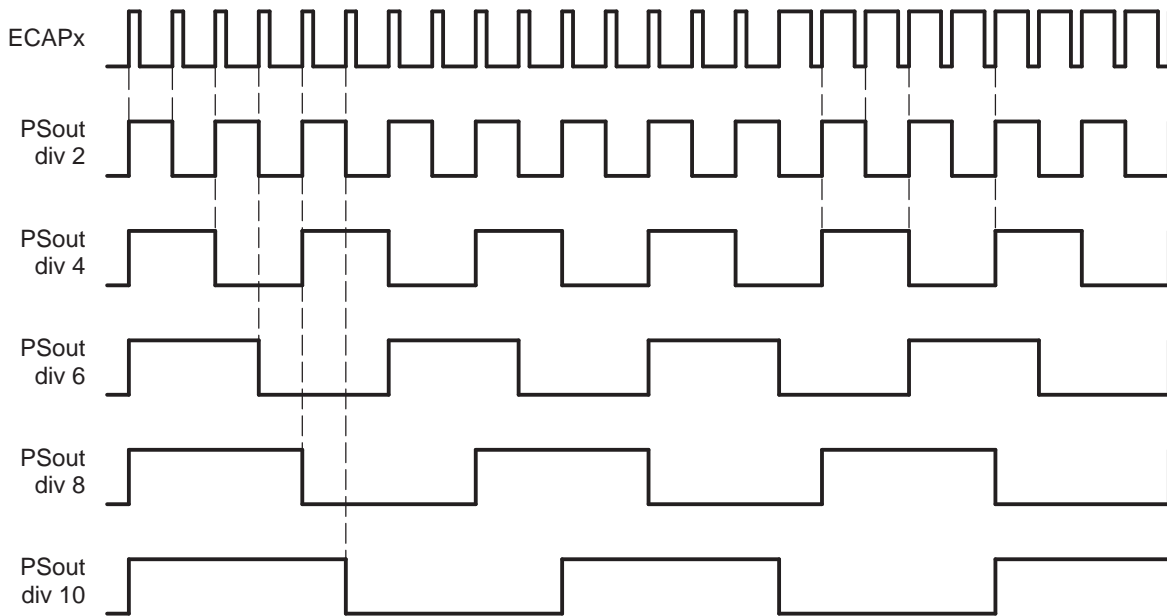
An input capture signal (pulse train) can be prescaled by $N = 2-62$ (in multiples of 2) or can bypass the prescaler. This is useful when very high frequency signals are used as inputs. Figure 4 shows a functional diagram and Figure 5 shows the operation of the prescale function.

Figure 4. Event Prescaler Control



- (1) When a prescale value of 1 is chosen (ECCTL1[13:9] = 0000) the input capture signal by-passes the prescale logic completely.

Figure 5. Prescale Function Waveforms



2.2.2 Edge Polarity Select and Qualifier

- Four independent edge polarity (rising edge/falling edge) selection multiplexers are used, one for each capture event.
- Each edge (up to 4) is event qualified by the Modulo4 sequencer.
- The edge event is gated to its respective CAP n register by the Mod4 counter. The CAP n register is loaded on the falling edge.

2.2.3 Continuous/One-Shot Control

- The Mod4 (2 bit) counter is incremented via edge qualified events (CEVT1-CEVT4).
- The Mod4 counter continues counting (0->1->2->3->0) and wraps around unless stopped.
- A 2-bit stop register is used to compare the Mod4 counter output, and when equal stops the Mod4 counter and inhibits further loads of the CAP1-CAP4 registers. This occurs during one-shot operation.

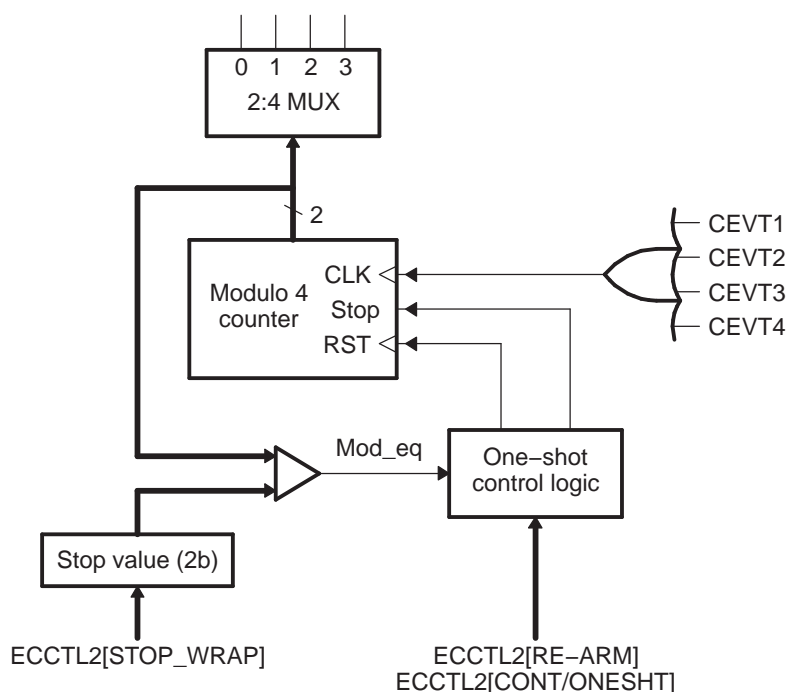
The continuous/one-shot block (Figure 6) controls the start/stop and reset (zero) functions of the Mod4 counter via a mono-shot type of action that can be triggered by the stop-value comparator and re-armed via software control.

Once armed, the eCAP module waits for 1-4 (defined by stop-value) capture events before freezing both the Mod4 counter and contents of CAP1-4 registers (time-stamps).

Re-arming prepares the eCAP module for another capture sequence. Also re-arming clears (to zero) the Mod4 counter and permits loading of CAP1-4 registers again, providing the CAPLDEN bit is set.

In continuous mode, the Mod4 counter continues to run (0->1->2->3->0, the one-shot action is ignored, and capture values continue to be written to CAP1-4 in a circular buffer sequence.

Figure 6. Continuous/One-shot Block Diagram



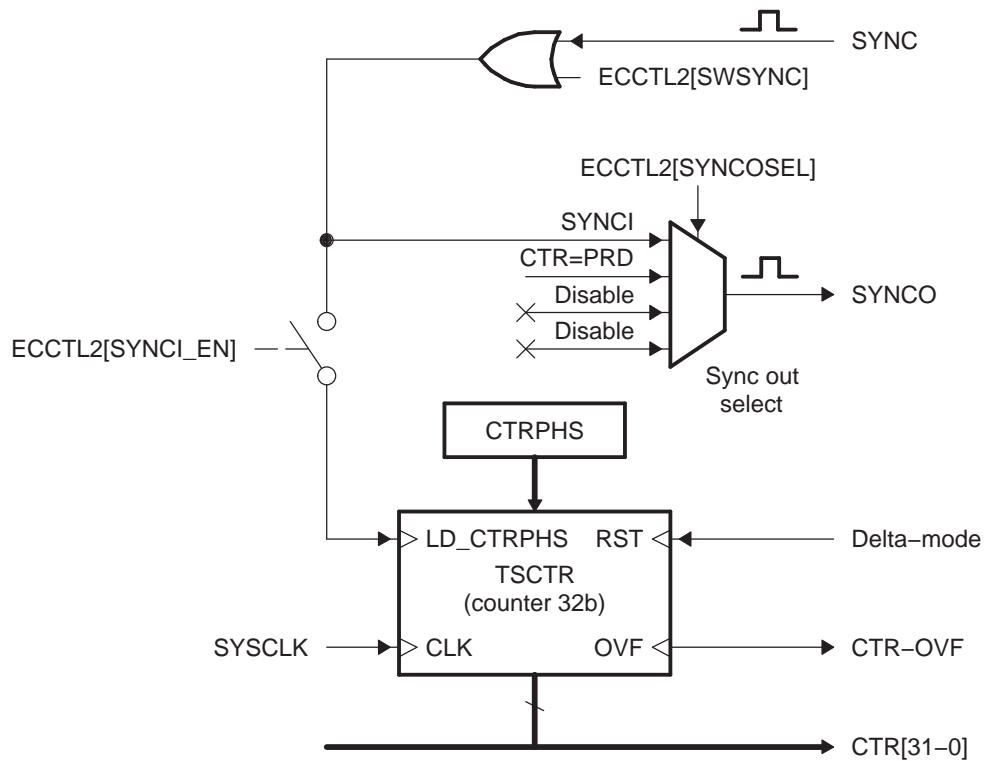
2.2.4 32-Bit Counter and Phase Control

This counter (Figure 7) provides the time-base for event captures, and is clocked via the system clock.

A phase register is provided to achieve synchronization with other counters, via a hardware and software forced sync. This is useful in APWM mode when a phase offset between modules is needed.

On any of the four event loads, an option to reset the 32-bit counter is given. This is useful for time difference capture. The 32-bit counter value is captured first, then it is reset to 0 by any of the LD1-LD4 signals.

Figure 7. Counter and Synchronization Block Diagram



2.2.5 CAP1-CAP4 Registers

These 32-bit registers are fed by the 32-bit counter timer bus, CTR[0-31] and are loaded (capture a time-stamp) when their respective LD inputs are strobed.

Loading of the capture registers can be inhibited via control bit CAPLDEN. During one-shot operation, this bit is cleared (loading is inhibited) automatically when a stop condition occurs, StopValue = Mod4.

CAP1 and CAP2 registers become the active period and compare registers, respectively, in APWM mode.

CAP3 and CAP4 registers become the respective shadow registers (APRD and ACMP) for CAP1 and CAP2 during APWM operation.

2.2.6 Interrupt Control

An Interrupt can be generated on capture events (CEVT1-CEVT4, CTROVF) or APWM events (CTR = PRD, CTR = CMP). See [Figure 8](#).

A counter overflow event (FFFF FFFFh->0000 0000h) is also provided as an interrupt source (CTROVF).

The capture events are edge and sequencer qualified (that is, ordered in time) by the polarity select and Mod4 gating, respectively.

One of these events can be selected as the interrupt source (from the eCAP n module) going to the interrupt controller.

Seven interrupt events (CEVT1, CEVT2, CEVT3, CEVT4, CNTOVF, CTR = PRD, CTR = CMP) can be generated. The interrupt enable register (ECEINT) is used to enable/disable individual interrupt event sources. The interrupt flag register (ECFLG) indicates if any interrupt event has been latched and contains the global interrupt flag bit (INT). An interrupt pulse is generated to the interrupt controller only if any of the interrupt events are enabled, the flag bit is 1, and the INT flag bit is 0. The interrupt service routine must clear the global interrupt flag bit and the serviced event via the interrupt clear register (ECCLR) before any other interrupt pulses are generated. You can force an interrupt event via the interrupt force register (ECFRC). This is useful for test purposes.

2.2.7 Shadow Load and Lockout Control

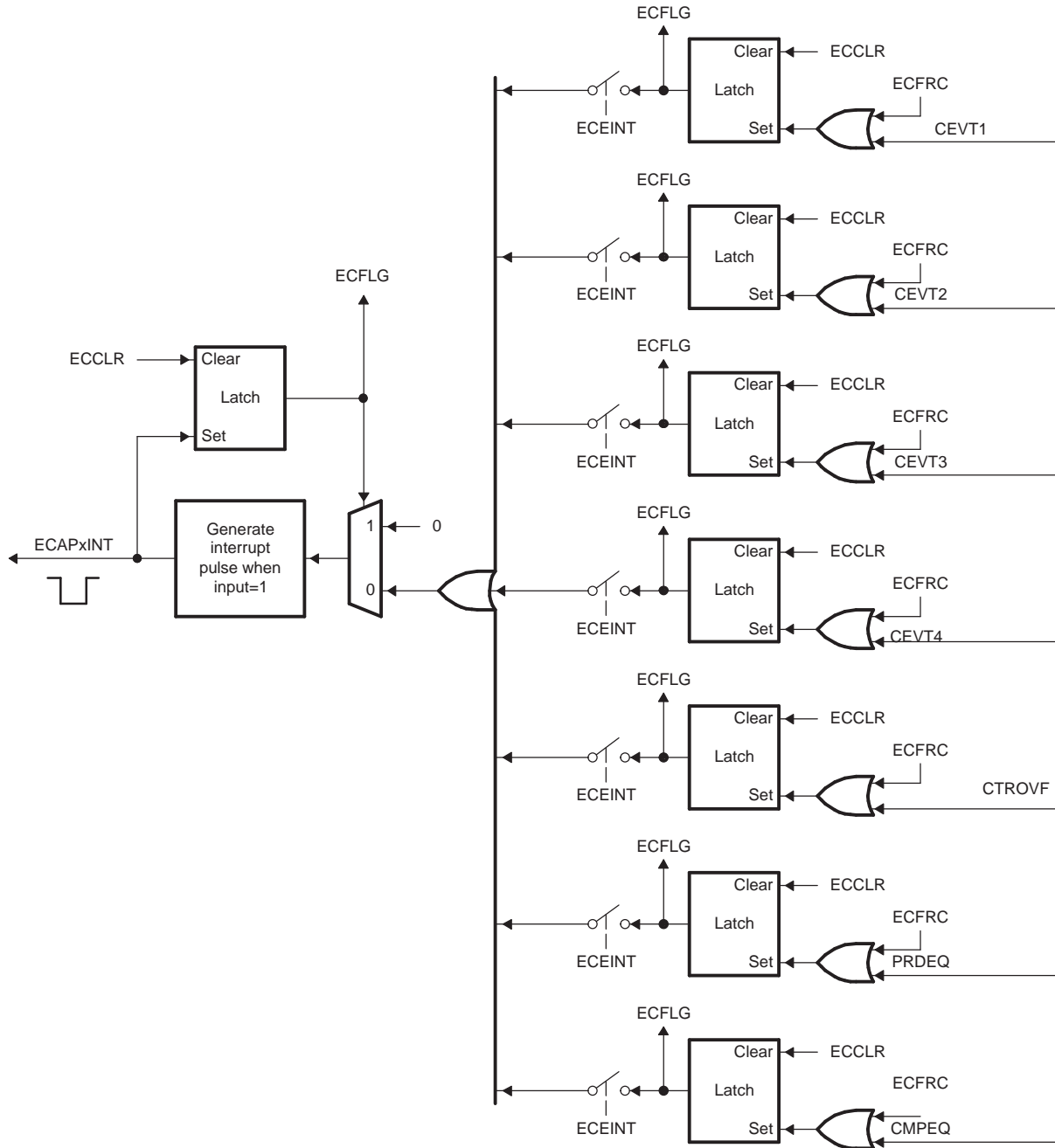
In capture mode, this logic inhibits (locks out) any shadow loading of CAP1 or CAP2 from APRD and ACMP registers, respectively.

In APWM mode, shadow loading is active and two choices are permitted:

- Immediate - APRD or ACMP are transferred to CAP1 or CAP2 immediately upon writing a new value.
- On period equal, CTR[31:0] = PRD[31:0]

NOTE: The CEVT1, CEVT2, CEVT3, CEVT4 flags are only active in capture mode (ECCTL2[CAP/APWM == 0]). The CTR = PRD, CTR = CMP flags are only valid in APWM mode (ECCTL2[CAP/APWM == 1]). CNTOVF flag is valid in both modes.

Figure 8. Interrupts in eCAP Module

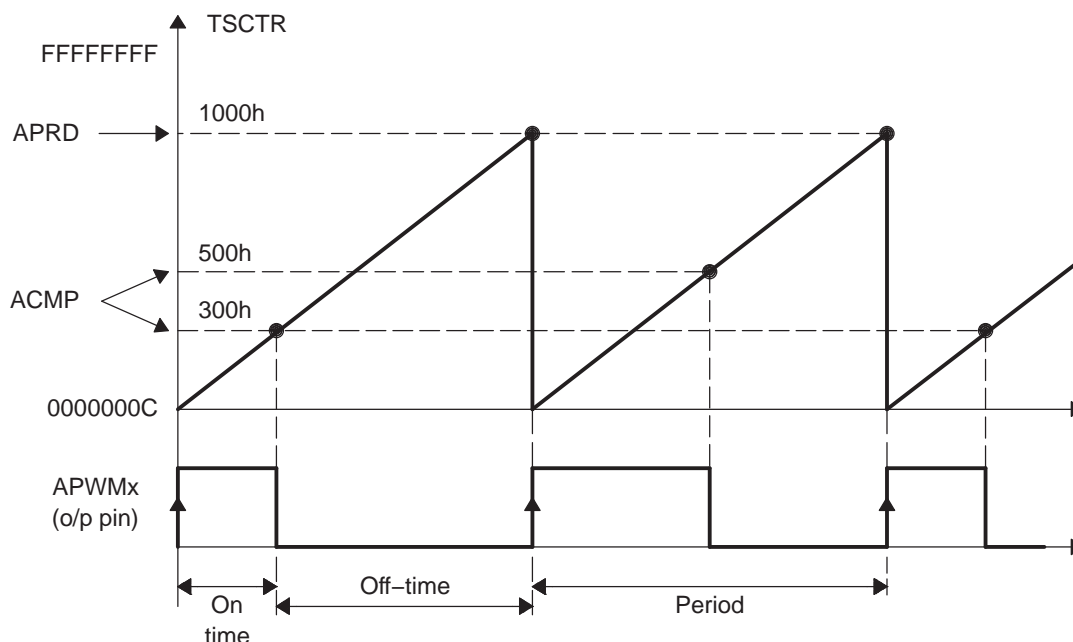


2.2.8 APWM Mode Operation

Main operating highlights of the APWM section:

- The time-stamp counter bus is made available for comparison via 2 digital (32-bit) comparators.
- When CAP1/2 registers are not used in capture mode, their contents can be used as Period and Compare values in APWM mode.
- Double buffering is achieved via shadow registers APRD and ACMP (CAP3/4). The shadow register contents are transferred over to CAP1/2 registers either immediately upon a write, or on a CTR = PRD trigger.
- In APWM mode, writing to CAP1/CAP2 active registers will also write the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 will invoke the shadow mode.
- During initialization, you must write to the active registers for both period and compare. This automatically copies the initial values into the shadow values. For subsequent compare updates, during run-time, you only need to use the shadow registers.

Figure 9. PWM Waveform Details Of APWM Mode Operation



The behavior of APWM active-high mode (APWMPOL == 0) is:

- CMP = 0x00000000, output low for duration of period (0% duty)
- CMP = 0x00000001, output high 1 cycle
- CMP = 0x00000002, output high 2 cycles
- CMP = PERIOD, output high except for 1 cycle (<100% duty)
- CMP = PERIOD+1, output high for complete period (100% duty)
- CMP > PERIOD+1, output high for complete period

The behavior of APWM active-low mode (APWMPOL == 1) is:

- CMP = 0x00000000, output high for duration of period (0% duty)
- CMP = 0x00000001, output low 1 cycle
- CMP = 0x00000002, output low 2 cycles
- CMP = PERIOD, output low except for 1 cycle (<100% duty)
- CMP = PERIOD+1, output low for complete period (100% duty)
- CMP > PERIOD+1, output low for complete period

3 Applications

The following sections will provide Applications examples and code snippets to show how to configure and operate the eCAP module. For clarity and ease of use, below are useful #defines which will help in the understanding of the examples.

```

// ECCTL1 ( ECAP Control Reg 1)
//=====
// CAPxPOL bits
#define EC_RISING 0x0
#define EC_FALLING 0x1

// CTRRSTx bits
#define EC_ABS_MODE 0x0
#define EC_DELTA_MODE 0x1

// PRESCALE bits
#define EC_BYPASS 0x0
#define EC_DIV1 0x0
#define EC_DIV2 0x1
#define EC_DIV4 0x2
#define EC_DIV6 0x3
#define EC_DIV8 0x4
#define EC_DIV10 0x5

// ECCTL2 ( ECAP Control Reg 2)
//=====
// CONT/ONESHOT bit
#define EC_CONTINUOUS 0x0
#define EC_ONESHOT 0x1

// STOPVALUE bit
#define EC_EVENT1 0x0
#define EC_EVENT2 0x1
#define EC_EVENT3 0x2
#define EC_EVENT4 0x3

// RE-ARM bit
#define EC_ARM 0x1

// TSCTRSTOP bit
#define EC_FREEZE 0x0
#define EC_RUN 0x1

// SYNCO_SEL bit
#define EC_SYNCIN 0x0
#define EC_CTR_PRD 0x1
#define EC_SYNCO_DIS 0x2

// CAP/APWM mode bit
#define EC_CAP_MODE 0x0
#define EC_APWM_MODE 0x1

// APWMPOL bit
#define EC_ACTV_HI 0x0
#define EC_ACTV_LO 0x1

// Generic
#define EC_DISABLE 0x0
#define EC_ENABLE 0x1
#define EC_FORCE 0x1

```

3.1 Absolute Time-Stamp Operation Rising Edge Trigger Example

Figure 10 shows an example of continuous capture operation (Mod4 counter wraps around). In this figure, TSCTR counts-up without resetting and capture events are qualified on the rising edge only, this gives period (and frequency) information.

On an event, the TSCTR contents (time-stamp) is first captured, then Mod4 counter is incremented to the next state. When the TSCTR reaches FFFF FFFFh (maximum value), it wraps around to 0000 0000h (not shown in Figure 10), if this occurs, the CTROVF (counter overflow) flag is set, and an interrupt (if enabled) occurs, CTROVF (counter overflow) Flag is set, and an Interrupt (if enabled) occurs. Captured time-stamps are valid at the point indicated by the diagram, after the 4th event, hence event CEVT4 can conveniently be used to trigger an interrupt and the CPU can read data from the CAP n registers.

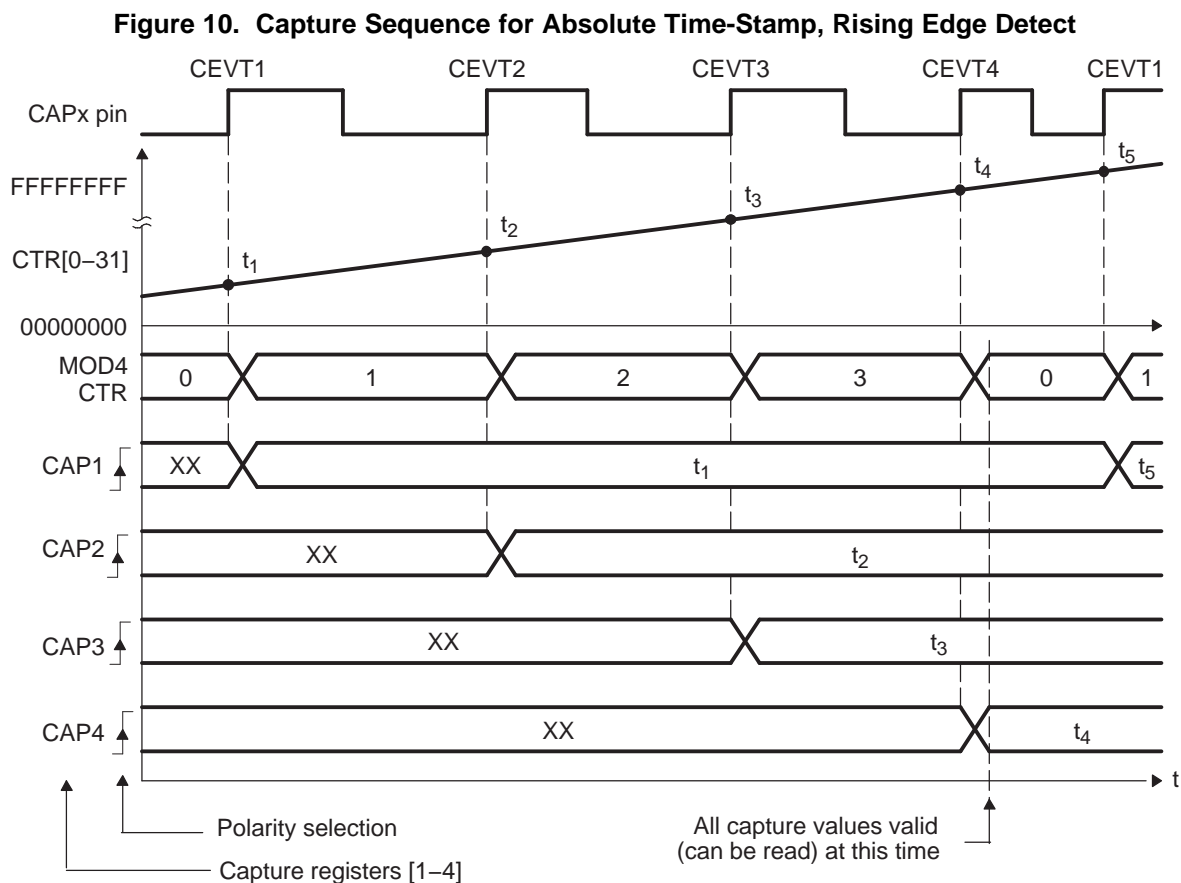


Table 1. ECAP Initialization for CAP Mode Absolute Time, Rising Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_RISING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_RISING
ECCTL1	CTRRST1	EC_ABS_MODE
ECCTL1	CTRRST2	EC_ABS_MODE
ECCTL1	CTRRST3	EC_ABS_MODE
ECCTL1	CTRRST4	EC_ABS_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCl_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Example 1. Code Snippet for CAP Mode Absolute Time, Rising Edge Trigger

```
// Code snippet for CAP mode Absolute Time, Rising edge trigger

// Run Time ( e.g. CEVT4 triggered ISR call)
//=====
TSt1 = ECAPxRegs.CAP1;      // Fetch Time-Stamp captured at t1
TSt2 = ECAPxRegs.CAP2;      // Fetch Time-Stamp captured at t2
TSt3 = ECAPxRegs.CAP3;      // Fetch Time-Stamp captured at t3
TSt4 = ECAPxRegs.CAP4;      // Fetch Time-Stamp captured at t4

Period1 = TSt2-TSt1;        // Calculate 1st period
Period2 = TSt3-TSt2;        // Calculate 2nd period
Period3 = TSt4-TSt3;        // Calculate 3rd period
```

3.2 Absolute Time-Stamp Operation Rising and Falling Edge Trigger Example

In Figure 11 the eCAP operating mode is almost the same as in the previous section except capture events are qualified as either rising or falling edge, this now gives both period and duty cycle information: Period1 = $t_3 - t_1$, Period2 = $t_5 - t_3$, ...etc. Duty Cycle1 (on-time %) = $(t_2 - t_1) / \text{Period1} \times 100\%$, etc. Duty Cycle1 (off-time %) = $(t_3 - t_2) / \text{Period1} \times 100\%$, etc.

Figure 11. Capture Sequence for Absolute Time-Stamp, Rising and Falling Edge Detect

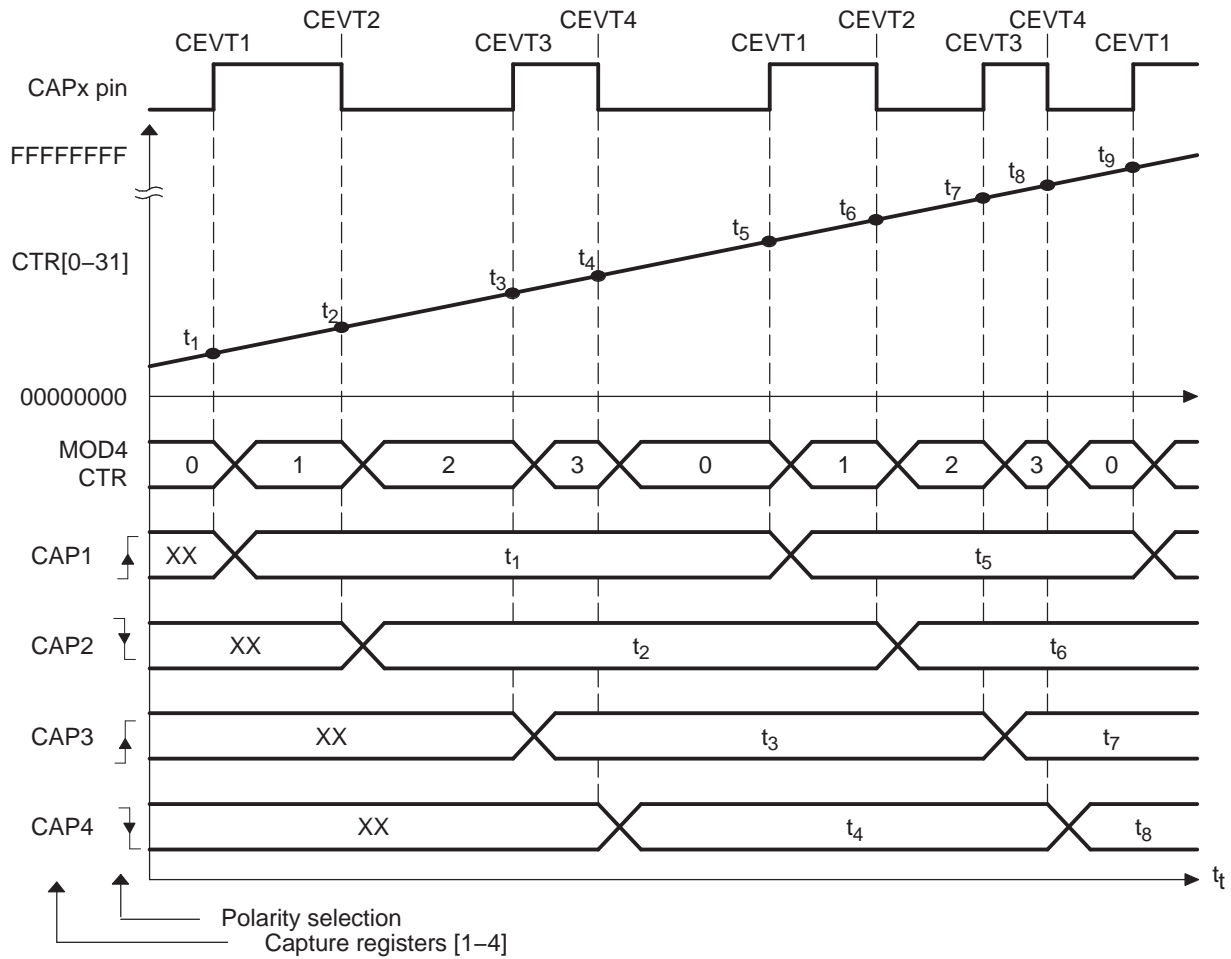


Table 2. ECAP Initialization for CAP Mode Absolute Time, Rising and Falling Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_FALLING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_FALLING
ECCTL1	CTRRST1	EC_ABS_MODE
ECCTL1	CTRRST2	EC_ABS_MODE
ECCTL1	CTRRST3	EC_ABS_MODE
ECCTL1	CTRRST4	EC_ABS_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCl_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Example 2. Code Snippet for CAP Mode Absolute Time, Rising and Falling Edge Trigger

```
// Code snippet for CAP mode Absolute Time, Rising & Falling edge triggers

// Run Time ( e.g. CEVT4 triggered ISR call)
//=====
TSt1 = ECAPxRegs.CAP1;      // Fetch Time-Stamp captured at t1
TSt2 = ECAPxRegs.CAP2;      // Fetch Time-Stamp captured at t2
TSt3 = ECAPxRegs.CAP3;      // Fetch Time-Stamp captured at t3
TSt4 = ECAPxRegs.CAP4;      // Fetch Time-Stamp captured at t4

Period1 = TSt3-TSt1;        // Calculate 1st period
DutyOnTime1 = TSt2-TSt1;    // Calculate On time
DutyOffTime1 = TSt3-TSt2;   // Calculate Off time
```

3.3 Time Difference (Delta) Operation Rising Edge Trigger Example

Figure 12 shows how the eCAP module can be used to collect Delta timing data from pulse train waveforms. Here Continuous Capture mode (TSCTR counts-up without resetting, and Mod4 counter wraps around) is used. In Delta-time mode, TSCTR is Reset back to Zero on every valid event. Here Capture events are qualified as Rising edge only. On an event, TSCTR contents (time-stamp) is captured first, and then TSCTR is reset to Zero. The Mod4 counter then increments to the next state. If TSCTR reaches FFFF FFFFh (maximum value), before the next event, it wraps around to 0000 0000h and continues, a CNTOVF (counter overflow) Flag is set, and an Interrupt (if enabled) occurs. The advantage of Delta-time Mode is that the CAPn contents directly give timing data without the need for CPU calculations: $Period1 = T_1$, $Period2 = T_2, \dots$ etc. As shown in Figure 12, the CEVT1 event is a good trigger point to read the timing data, T_1, T_2, T_3, T_4 are all valid here.

Figure 12. Capture Sequence for Delta Mode Time-Stamp, Rising Edge Detect

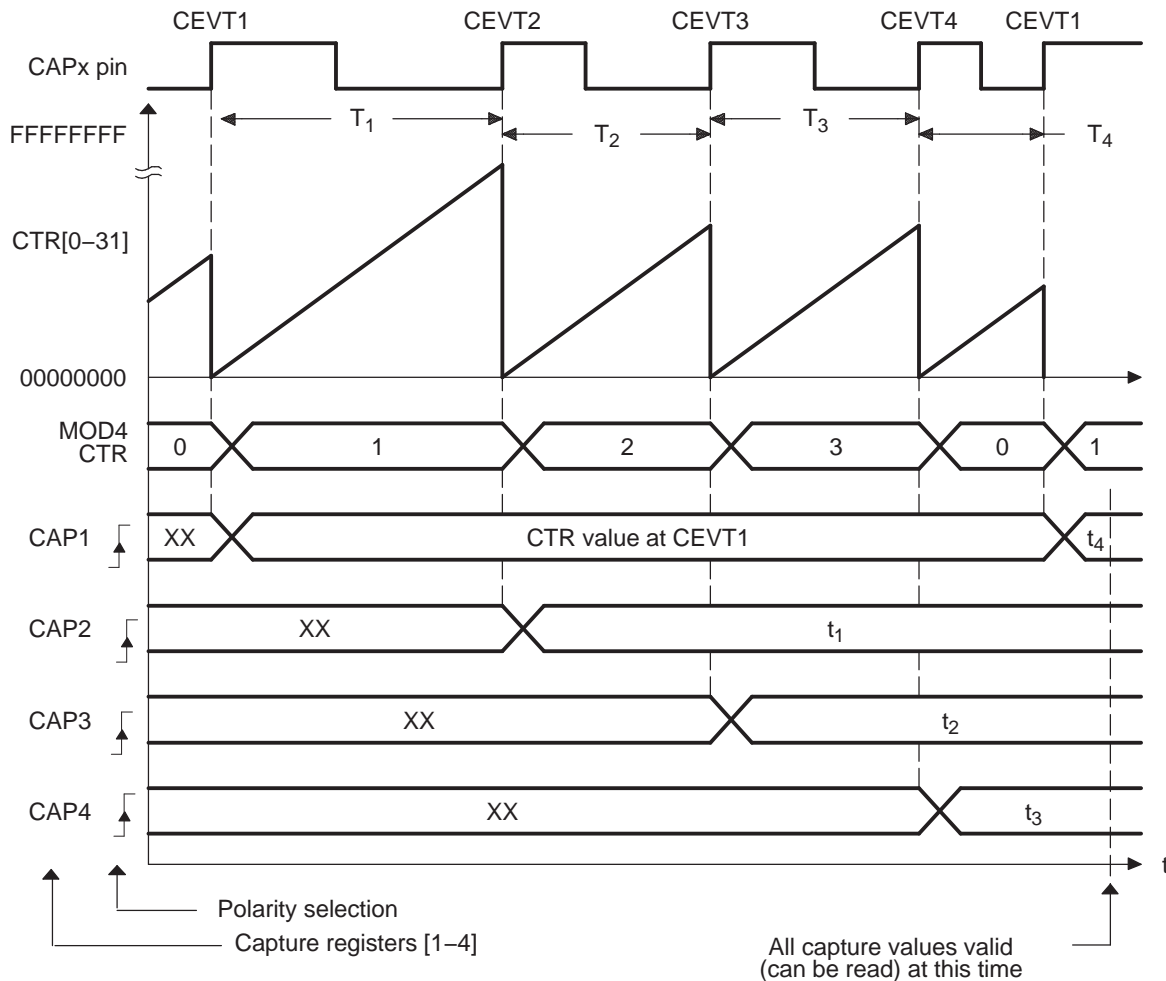


Table 3. ECAP Initialization for CAP Mode Delta Time, Rising Edge Trigger

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_RISING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_RISING
ECCTL1	CTRRST1	EC_DELTA_MODE
ECCTL1	CTRRST2	EC_DELTA_MODE
ECCTL1	CTRRST3	EC_DELTA_MODE
ECCTL1	CTRRST4	EC_DELTA_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCl_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Example 3. Code Snippet for CAP Mode Delta Time, Rising Edge Trigger

```
// Code snippet for CAP mode Delta Time, Rising edge trigger

// Run Time ( e.g. CEVT1 triggered ISR call)
//=====
// Note: here Time-stamp directly represents the Period value.
Period4 = ECAPxRegs.CAP1;    // Fetch Time-Stamp captured at T1
Period1 = ECAPxRegs.CAP2;    // Fetch Time-Stamp captured at T2
Period2 = ECAPxRegs.CAP3;    // Fetch Time-Stamp captured at T3
Period3 = ECAPxRegs.CAP4;    // Fetch Time-Stamp captured at T4
```

3.4 Time Difference (Delta) Operation Rising and Falling Edge Trigger Example

In Figure 13 the eCAP operating mode is almost the same as in previous section except Capture events are qualified as either Rising or Falling edge, this now gives both Period and Duty cycle information: Period1 = $T_1 + T_2$, Period2 = $T_3 + T_4$, ...etc Duty Cycle1 (on-time %) = $T_1 / \text{Period1} \times 100\%$, etc Duty Cycle1 (off-time %) = $T_2 / \text{Period1} \times 100\%$, etc

During initialization, you must write to the active registers for both period and compare. This will then automatically copy the init values into the shadow values. For subsequent compare updates, that is, during run-time, only the shadow registers must be used.

Figure 13. Capture Sequence for Delta Mode Time-Stamp, Rising and Falling Edge Detect

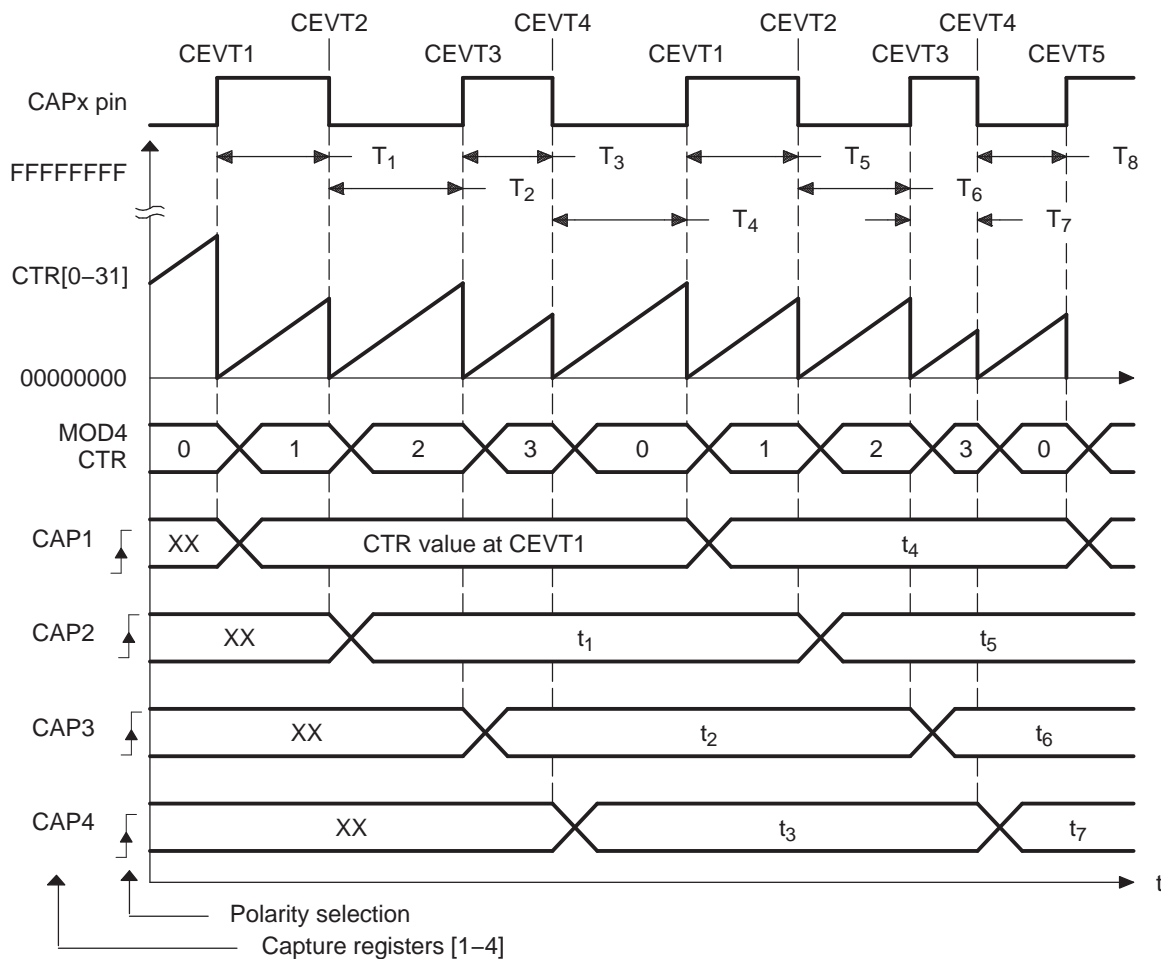


Table 4. ECAP Initialization for CAP Mode Delta Time, Rising and Falling Edge Triggers

Register	Bit	Value
ECCTL1	CAP1POL	EC_RISING
ECCTL1	CAP2POL	EC_FALLING
ECCTL1	CAP3POL	EC_RISING
ECCTL1	CAP4POL	EC_FALLING
ECCTL1	CTRRST1	EC_DELTA_MODE
ECCTL1	CTRRST2	EC_DELTA_MODE
ECCTL1	CTRRST3	EC_DELTA_MODE
ECCTL1	CTRRST4	EC_DELTA_MODE
ECCTL1	CAPLDEN	EC_ENABLE
ECCTL1	PRESCALE	EC_DIV1
ECCTL2	CAP_APWM	EC_CAP_MODE
ECCTL2	CONT_ONESHT	EC_CONTINUOUS
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	SYNCl_EN	EC_DISABLE
ECCTL2	TSCTRSTOP	EC_RUN

Example 4. Code Snippet for CAP Mode Delta Time, Rising and Falling Edge Triggers

```
// Code snippet for CAP mode Delta Time, Rising and Falling edge triggers

// Run Time ( e.g. CEVT1 triggered ISR call)
//=====
// Note: here Time-stamp directly represents the Duty cycle values.
DutyOnTime1 = ECAPxRegs.CAP2;    // Fetch Time-Stamp captured at T2
DutyOffTime1 = ECAPxRegs.CAP3;   // Fetch Time-Stamp captured at T3
DutyOnTime2 = ECAPxRegs.CAP4;    // Fetch Time-Stamp captured at T4
DutyOffTime2 = ECAPxRegs.CAP1;   // Fetch Time-Stamp captured at T1

Period1 = DutyOnTime1 + DutyOffTime1;
Period2 = DutyOnTime2 + DutyOffTime2;
```

3.5 Application of the APWM Mode

3.5.1 Simple PWM Generation (Independent Channel/s) Example

In this example, the eCAP module is configured to operate as a PWM generator. Here a very simple single channel PWM waveform is generated from output pin APWM n . The PWM polarity is active high, which means that the compare value (CAP2 reg is now a compare register) represents the on-time (high level) of the period. Alternatively, if the APWMPOL bit is configured for active low, then the compare value represents the off-time.

Figure 14. PWM Waveform Details of APWM Mode Operation

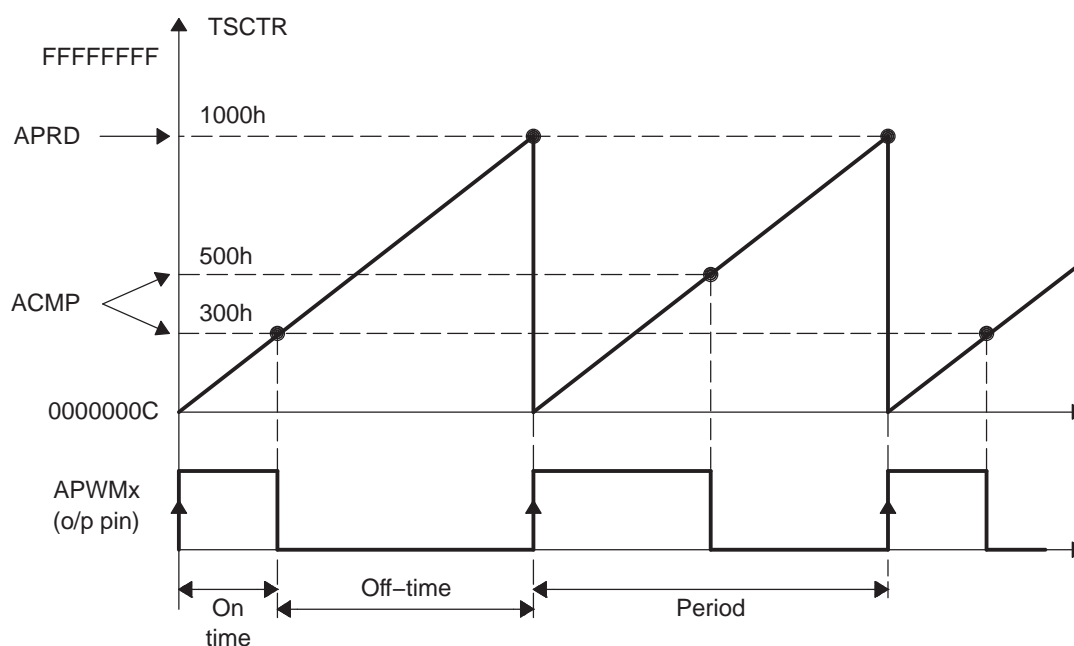


Table 5. ECAP Initialization for APWM Mode

Register	Bit	Value
CAP1	CAP1	0x1000
CTRPHS	CTRPHS	0x0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCL_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSTRSTOP	EC_RUN

Example 5. Code Snippet for APWM Mode

```

// Code snippet for APWM mode Example 1
// Run Time (Instant 1, e.g. ISR call)
//=====
ECAPxRegs.CAP2 = 0x300;      // Set Duty cycle i.e. compare value
// Run Time (Instant 2, e.g. another ISR call)
//=====
ECAPxRegs.CAP2 = 0x500;      // Set Duty cycle i.e. compare value

```

3.5.2 Multichannel PWM Generation with Synchronization Example

[Figure 15](#) takes advantage of the synchronization feature between eCAP modules. Here 4 independent PWM channels are required with different frequencies, but at integer multiples of each other to avoid "beat" frequencies. Hence one eCAP module is configured as the Master and the remaining 3 are Slaves all receiving their synch pulse (CTR = PRD) from the master. Note the Master is chosen to have the lower frequency ($F_1 = 1/20,000$) requirement. Here Slave2 Freq = $2 \times F_1$, Slave3 Freq = $4 \times F_1$ and Slave4 Freq = $5 \times F_1$. Note here values are in decimal notation. Also, only the APWM1 output waveform is shown.

Figure 15. Multichannel PWM Example Using 4 eCAP Modules

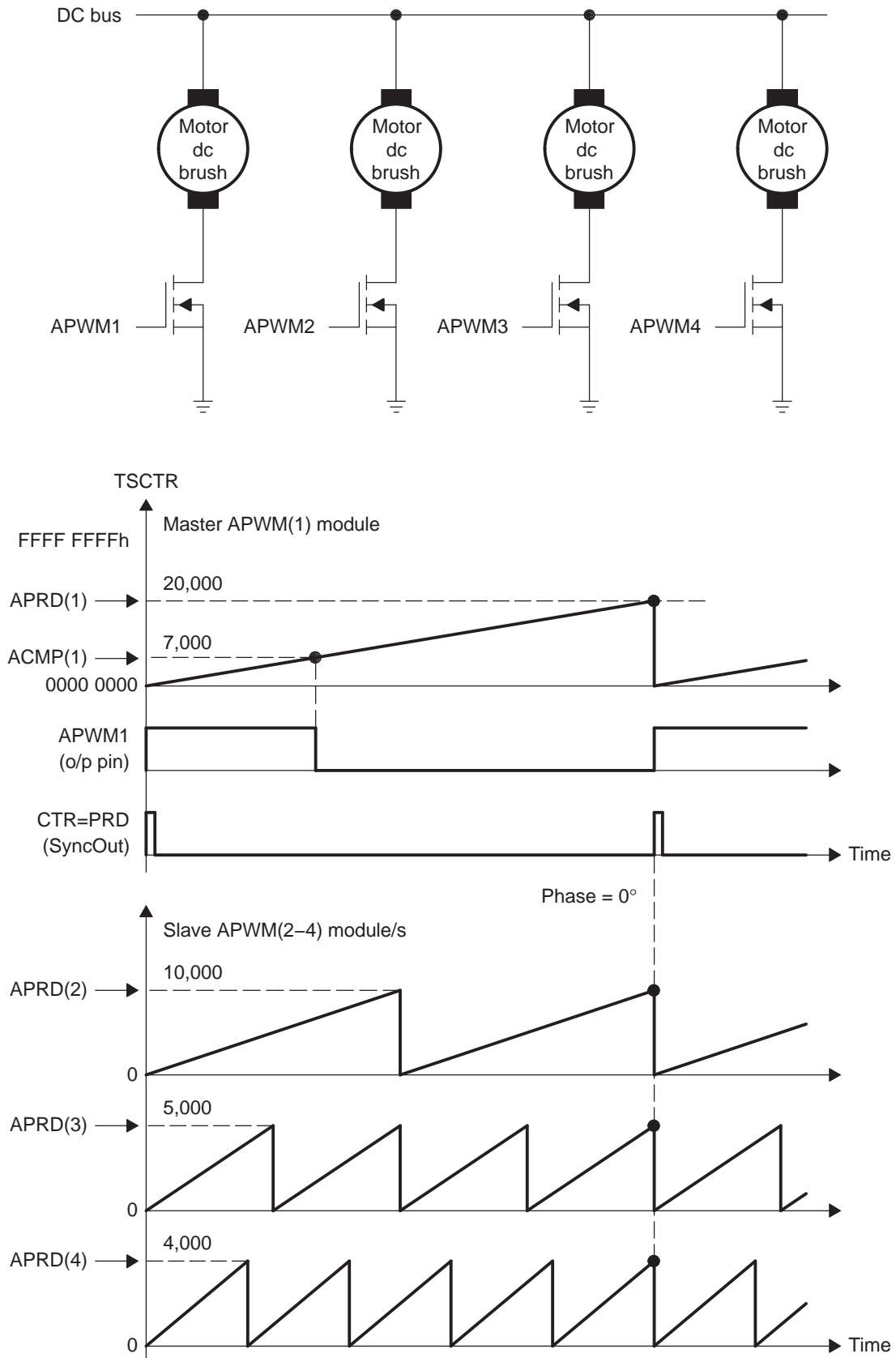


Table 6. ECAP1 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	20000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCl_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_CTR_PRD
ECCTL2	TSTRSTOP	EC_RUN

Table 7. ECAP2 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	10000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCl_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSTRSTOP	EC_RUN

Table 8. ECAP3 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	5000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCl_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCI
ECCTL2	TSTRSTOP	EC_RUN

Table 9. ECAP4 Initialization for Multichannel PWM Generation with Synchronization

Register	Bit	Value
CAP1	CAP1	4000
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCl_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSTRSTOP	EC_RUN

Example 6. Code Snippet for Multichannel PWM Generation with Synchronization

```

// Code snippet for APWM mode Example 2

// Run Time (Note: Example execution of one run-time instant)
//=====
ECAP1Regs.CAP2 = 7000;    // Set Duty cycle i.e., compare value = 7000
ECAP2Regs.CAP2 = 2000;    // Set Duty cycle i.e., compare value = 2000
ECAP3Regs.CAP2 = 550;     // Set Duty cycle i.e., compare value = 550
ECAP4Regs.CAP2 = 6500;    // Set Duty cycle i.e., compare value = 6500
  
```

3.5.3 Multichannel PWM Generation with Phase Control Example

In [Figure 16](#), the Phase control feature of the APWM mode is used to control a 3 phase Interleaved DC/DC converter topology. This topology requires each phase to be off-set by 120° from each other. Hence if “Leg” 1 (controlled by APWM1) is the reference Leg (or phase), that is, 0°, then Leg 2 need 120° off-set and Leg 3 needs 240° off-set. The waveforms in [Figure 16](#) show the timing relationship between each of the phases (Legs). Note eCAP1 module is the Master and issues a sync out pulse to the slaves (modules 2, 3) whenever TSCTR = Period value.

Figure 16. Multiphase (channel) Interleaved PWM Example Using 3 eCAP Modules

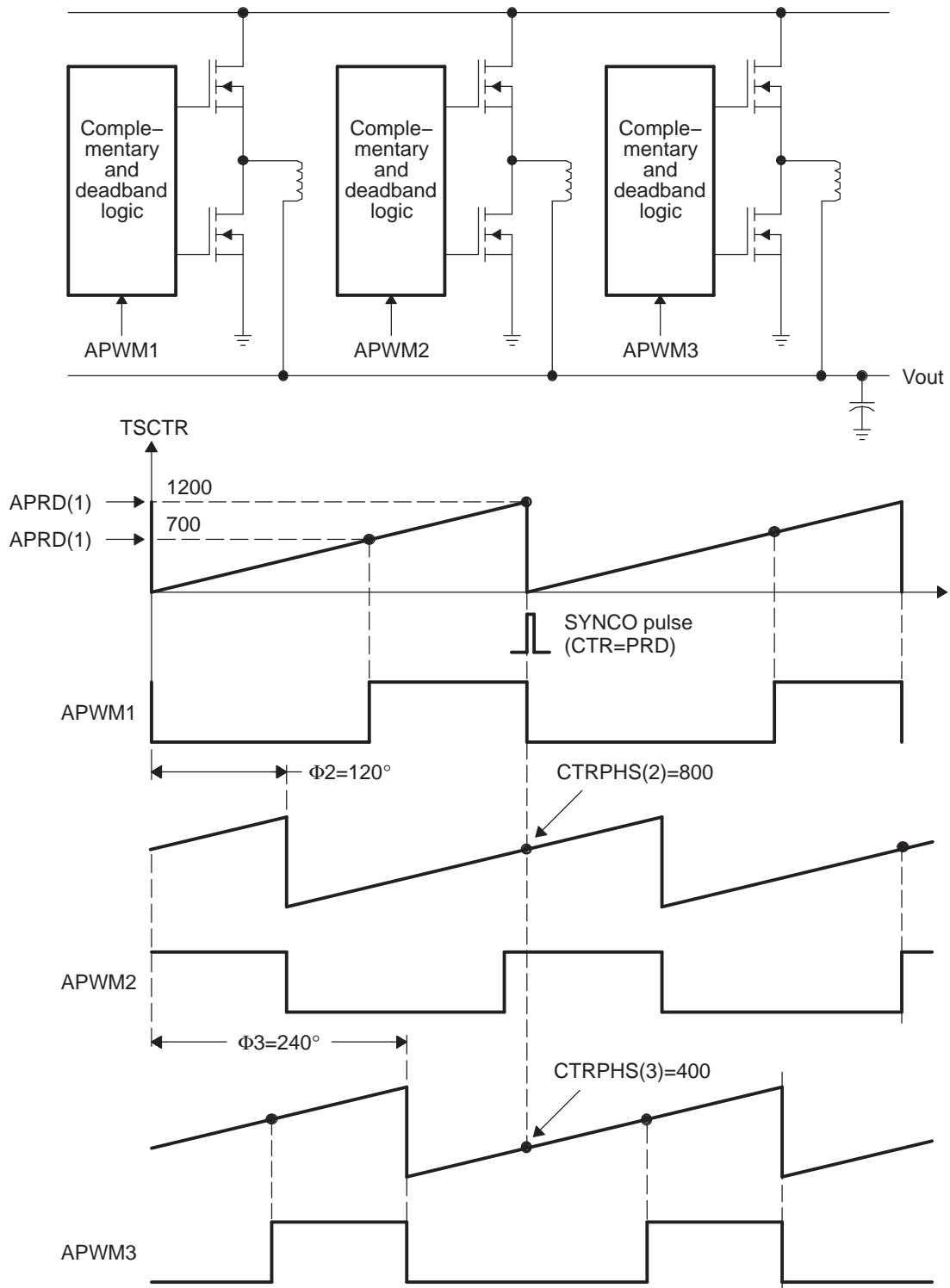


Table 10. ECAP1 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	0
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCl_EN	EC_DISABLE
ECCTL2	SYNCO_SEL	EC_CTR_PRD
ECCTL2	TSTRSTOP	EC_RUN

Table 11. ECAP2 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	800
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCl_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCl
ECCTL2	TSTRSTOP	EC_RUN

Table 12. ECAP3 Initialization for Multichannel PWM Generation with Phase Control

Register	Bit	Value
CAP1	CAP1	1200
CTRPHS	CTRPHS	400
ECCTL2	CAP_APWM	EC_APWM_MODE
ECCTL2	APWMPOL	EC_ACTV_HI
ECCTL2	SYNCl_EN	EC_ENABLE
ECCTL2	SYNCO_SEL	EC_SYNCO_DIS
ECCTL2	TSTRSTOP	EC_RUN

Example 7. Code Snippet for Multichannel PWM Generation with Phase Control

```
// Code snippet for APWM mode Example 3

// Run Time (Note: Example execution of one run-time instant)
//=====
// All phases are set to the same duty cycle
ECAP1Regs.CAP2 = 700;    // Set Duty cycle i.e. compare value = 700
ECAP2Regs.CAP2 = 700;    // Set Duty cycle i.e. compare value = 700
ECAP3Regs.CAP2 = 700;    // Set Duty cycle i.e. compare value = 700
```


4 Registers

[Table 13](#) shows the eCAP module control and status register set. All 32-bit registers are aligned on even address boundaries and are organized in little-endian mode. The 16 least-significant bits of a 32-bit register are located on lowest address (even address).

NOTE: In APWM mode, writing to CAP1/CAP2 active registers also writes the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 invokes the shadow mode.

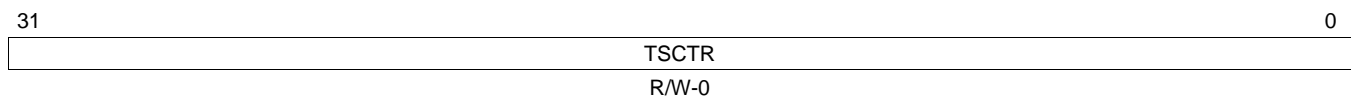
Table 13. Control and Status Register Set

Offset	Acronym	Description	Size (x16)	Section
0h	TSCTR	Time-Stamp Counter Register	2	Section 4.1
4h	CTRPHS	Counter Phase Offset Value Register	2	Section 4.2
8h	CAP1	Capture 1 Register	2	Section 4.3
Ch	CAP2	Capture 2 Register	2	Section 4.4
10h	CAP3	Capture 3 Register	2	Section 4.5
14h	CAP4	Capture 4 Register	2	Section 4.6
28h	ECCTL1	Capture Control Register 1	1	Section 4.7
2Ah	ECCTL2	Capture Control Register 2	1	Section 4.8
2Ch	ECEINT	Capture Interrupt Enable Register	1	Section 4.9
2Eh	ECFLG	Capture Interrupt Flag Register	1	Section 4.10
30h	ECCLR	Capture Interrupt Clear Register	1	Section 4.11
32h	ECFRC	Capture Interrupt Force Register	1	Section 4.12
5Ch	REVID	Revision ID Register	2	Section 4.13

4.1 Time-Stamp Counter Register (TSCTR)

The time-stamp counter register (TSCTR) is shown in [Figure 17](#) and described in [Table 14](#).

Figure 17. Time-Stamp Counter Register (TSCTR)



LEGEND: R/W = Read/Write; -n = value after reset

Table 14. Time-Stamp Counter Register (TSCTR) Field Descriptions

Bit	Field	Value	Description
31-0	TSCTR	0-FFFF FFFFh	Active 32-bit counter register that is used as the capture time-base

4.2 Counter Phase Control Register (CTRPHS)

The counter phase control register (CTRPHS) is shown in [Figure 18](#) and described in [Table 15](#).

Figure 18. Counter Phase Control Register (CTRPHS)

31	0
CTRPHS	
R/W-0	

LEGEND: R/W = Read/Write; -n = value after reset

Table 15. Counter Phase Control Register (CTRPHS) Field Descriptions

Bit	Field	Value	Description
31-0	CTRPHS	0-FFFF FFFFh	Counter phase value register that can be programmed for phase lag/lead. This register shadows TSCTR and is loaded into TSCTR upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases.

4.3 Capture 1 Register (CAP1)

The capture 1 register (CAP1) is shown in [Figure 19](#) and described in [Table 16](#).

Figure 19. Capture 1 Register (CAP1)

31	0
CAP1	
R/W-0	

LEGEND: R/W = Read/Write; -n = value after reset

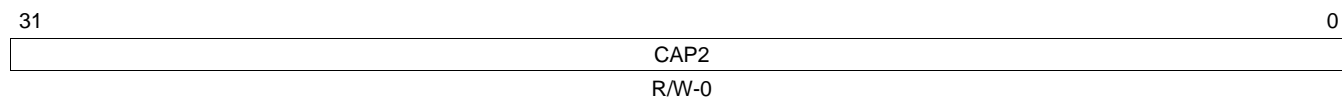
Table 16. Capture 1 Register (CAP1) Field Descriptions

Bit	Field	Value	Description
31-0	CAP1	0-FFFF FFFFh	This register can be loaded (written) by: <ul style="list-style-type: none"> • Time-Stamp (i.e., counter value) during a capture event • Software - may be useful for test purposes • APRD active register when used in APWM mode

4.4 Capture 2 Register (CAP2)

The capture 2 register (CAP2) is shown in [Figure 20](#) and described in [Table 17](#).

Figure 20. Capture 2 Register (CAP2)



LEGEND: R/W = Read/Write; -n = value after reset

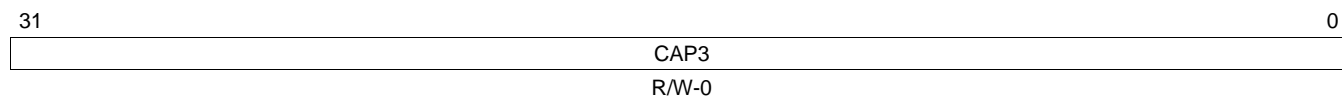
Table 17. Capture 2 Register (CAP2) Field Descriptions

Bit	Field	Value	Description
31-0	CAP2	0-FFFF FFFFh	This register can be loaded (written) by: <ul style="list-style-type: none"> • Time-Stamp (i.e., counter value) during a capture event • Software - may be useful for test purposes • ACMP active register when used in APWM mode

4.5 Capture 3 Register (CAP3)

The capture 3 register (CAP3) is shown in [Figure 21](#) and described in [Table 18](#).

Figure 21. Capture 3 Register (CAP3)



LEGEND: R/W = Read/Write; -n = value after reset

Table 18. Capture 3 Register (CAP3) Field Descriptions

Bit	Field	Value	Description
31-0	CAP3	0-FFFF FFFFh	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the period shadow (APRD) register. You update the PWM period value through this register. In this mode, CAP3 shadows CAP1.

4.6 Capture 4 Register (CAP4)

The capture 4 register (CAP4) is shown in [Figure 22](#) and described in [Table 19](#).

Figure 22. Capture 4 Register (CAP4)

31	CAP4	0
R/W-0		

LEGEND: R/W = Read/Write; -n = value after reset

Table 19. Capture 4 Register (CAP4) Field Descriptions

Bit	Field	Value	Description
31-0	CAP4	0-FFFF FFFFh	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the compare shadow (ACMP) register. You update the PWM compare value through this register. In this mode, CAP4 shadows CAP2.

4.7 ECAP Control Register 1 (ECCTL1)

The ECAP control register 1 (ECCTL1) is shown in [Figure 23](#) and described in [Table 20](#).

Figure 23. ECAP Control Register 1 (ECCTL1)

15	14	13	9	8			
FREE/SOFT		PRESCALE			CAPLDEN		
R/W-0		R/W-0			R/W-0		
7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Table 20. ECAP Control Register 1 (ECCTL1) Field Descriptions

Bit	Field	Value	Description
15-14	FREE/SOFT	0-3h 0 1h 2h-3h	Emulation Control TSCTR counter stops immediately on emulation suspend TSCTR counter runs until = 0 TSCTR counter is unaffected by emulation suspend (Run Free)
13-9	PRESCALE	0-1Fh 0 1 2h 3h 4h 5h ... 1Eh 1Fh	Event Filter prescale select Divide by 1 (i.e., no prescale, by-pass the prescaler) Divide by 2 Divide by 4 Divide by 6 Divide by 8 Divide by 10 ... Divide by 60 Divide by 62
8	CAPLDEN	0 1	Enable Loading of CAP1-4 registers on a capture event Disable CAP1-4 register loads at capture event time. Enable CAP1-4 register loads at capture event time.

Table 20. ECAP Control Register 1 (ECCTL1) Field Descriptions (continued)

Bit	Field	Value	Description
7	CTRRST4	0	Counter Reset on Capture Event 4 <i>Do not</i> reset counter on Capture Event 4 (absolute time stamp operation)
		1	Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	0	Capture Event 4 Polarity select Capture Event 4 triggered on a rising edge (RE)
		1	Capture Event 4 triggered on a falling edge (FE)
5	CTRRST3	0	Counter Reset on Capture Event 3 <i>Do not</i> reset counter on Capture Event 3 (absolute time stamp)
		1	Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	0	Capture Event 3 Polarity select Capture Event 3 triggered on a rising edge (RE)
		1	Capture Event 3 triggered on a falling edge (FE)
3	CTRRST2	0	Counter Reset on Capture Event 2 <i>Do not</i> reset counter on Capture Event 2 (absolute time stamp)
		1	Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	0	Capture Event 2 Polarity select Capture Event 2 triggered on a rising edge (RE)
		1	Capture Event 2 triggered on a falling edge (FE)
1	CTRRST1	0	Counter Reset on Capture Event 1 <i>Do not</i> reset counter on Capture Event 1 (absolute time stamp)
		1	Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	0	Capture Event 1 Polarity select Capture Event 1 triggered on a rising edge (RE)
		1	Capture Event 1 triggered on a falling edge (FE)

4.8 ECAP Control Register 2 (ECCTL2)

The ECAP control register 2 (ECCTL2) is shown in [Figure 24](#) and described in [Table 21](#).

Figure 24. ECAP Control Register 2 (ECCTL2)

15	Reserved				11	10	9	8
				R-0	R/W-0		R/W-0	R/W-0
7	6	5	4	3	2	1	0	
SYNCO_SEL		SYNCI_EN	TSCTRSTOP	REARM	STOP_WRAP		CONT/ONESHT	
R/W-0		R/W-0	R/W-0	R/W-0	R/W-1		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. ECAP Control Register 2 (ECCTL2) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10	APWMPOL	0 1	APWM output polarity select. This is applicable only in APWM operating mode 0 Output is active high (Compare value defines high time) 1 Output is active low (Compare value defines low time)
9	CAP/APWM	0 1	CAP/APWM operating mode select 0 ECAP module operates in capture mode. This mode forces the following configuration: <ul style="list-style-type: none"> Inhibits TSCTR resets via CTR = PRD event Inhibits shadow loads on CAP1 and 2 registers Permits user to enable CAP1-4 register load ECAPn/APWMn pin operates as a capture input 1 ECAP module operates in APWM mode. This mode forces the following configuration: <ul style="list-style-type: none"> Resets TSCTR on CTR = PRD event (period boundary) Permits shadow loading on CAP1 and 2 registers Disables loading of time-stamps into CAP1-4 registers ECAPn/APWMn pin operates as a APWM output
8	SWSYNC	0 1	Software-forced Counter (TSCTR) Synchronizing. This provides a convenient software method to synchronize some or all ECAP time bases. In APWM mode, the synchronizing can also be done via the CTR = PRD event. 0 Writing a zero has no effect. Reading always returns a zero 1 Writing a one forces a TSCTR shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0,0. After writing a 1, this bit returns to a zero. Note: Selection CTR = PRD is meaningful only in APWM mode; however, you can choose it in CAP mode if you find doing so useful.
7-6	SYNCO_SEL	0-3h 0 1h 2h 3h	Sync-Out Select 0 Select sync-in event to be the sync-out signal (pass through) 1h Select CTR = PRD event to be the sync-out signal 2h Disable sync out signal 3h Disable sync out signal
5	SYNCI_EN	0 1	Counter (TSCTR) Sync-In select mode 0 Disable sync-in option 1 Enable counter (TSCTR) to be loaded from CTRPHS register upon either a SYNCI signal or a S/W force event.
4	TSCTRSTOP	0 1	Time Stamp (TSCTR) Counter Stop (freeze) Control 0 TSCTR stopped 1 TSCTR free-running

Table 21. ECAP Control Register 2 (ECCTL2) Field Descriptions (continued)

Bit	Field	Value	Description
3	RE-ARM	0 1	One-Shot Re-Arming Control, that is, wait for stop trigger. Note: The re-arm function is valid in one shot or continuous mode. Has no effect (reading always returns a 0) Arms the one-shot sequence as follows: 1) Resets the Mod4 counter to zero 2) Unfreezes the Mod4 counter 3) Enables capture register loads
2-1	STOP_WRAP	0-3h 0 1h 2h 3h	Stop value for one-shot mode. This is the number (between 1-4) of captures allowed to occur before the CAP(1-4) registers are frozen, that is, capture sequence is stopped. Wrap value for continuous mode. This is the number (between 1-4) of the capture register in which the circular buffer wraps around and starts again. Stop after Capture Event 1 in one-shot mode. Wrap after Capture Event 1 in continuous mode. Stop after Capture Event 2 in one-shot mode. Wrap after Capture Event 2 in continuous mode. Stop after Capture Event 3 in one-shot mode. Wrap after Capture Event 3 in continuous mode. Stop after Capture Event 4 in one-shot mode. Wrap after Capture Event 4 in continuous mode. Notes: STOP_WRAP is compared to Mod4 counter and, when equal, 2 actions occur: <ul style="list-style-type: none"> • Mod4 counter is stopped (frozen) • Capture register loads are inhibited In one-shot mode, further interrupt events are blocked until re-armed.
0	CONT/ONESHT	0 1	Continuous or one-shot mode control (applicable only in capture mode) Operate in continuous mode Operate in one-shot mode

4.9 ECAP Interrupt Enable Register (ECEINT)

The ECAP interrupt enable register (ECEINT) is shown in [Figure 25](#) and described in [Table 22](#).

The interrupt enable bits (CEVT_n) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ECCLR registers.

The proper procedure for configuring peripheral modes and interrupts is:

1. Disable global interrupts
2. Stop eCAP counter
3. Disable eCAP interrupts
4. Configure peripheral registers
5. Clear spurious eCAP interrupt flags
6. Enable eCAP interrupts
7. Start eCAP counter
8. Enable global interrupts

Figure 25. ECAP Interrupt Enable Register (ECEINT)

15							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
CTR=CMP	CTR=PRD	CTROVF	CEVT4	CEVT3	CEVT2	CETV1	Reserved
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. ECAP Interrupt Enable Register (ECEINT) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7	CTR=CMP	0 1	Counter Equal Compare Interrupt Enable Disable Compare Equal as an Interrupt source Enable Compare Equal as an Interrupt source
6	CTR=PRD	0 1	Counter Equal Period Interrupt Enable Disable Period Equal as an Interrupt source Enable Period Equal as an Interrupt source
5	CTROVF	0 1	Counter Overflow Interrupt Enable Disable counter Overflow as an Interrupt source Enable counter Overflow as an Interrupt source
4	CEVT4	0 1	Capture Event 4 Interrupt Enable Disable Capture Event 4 as an Interrupt source Enable Capture Event 4 as an Interrupt source
3	CEVT3	0 1	Capture Event 3 Interrupt Enable Disable Capture Event 3 as an Interrupt source Enable Capture Event 3 as an Interrupt source
2	CEVT2	0 1	Capture Event 2 Interrupt Enable Disable Capture Event 2 as an Interrupt source Enable Capture Event 2 as an Interrupt source
1	CEVT1	0 1	Capture Event 1 Interrupt Enable Disable Capture Event 1 as an Interrupt source Enable Capture Event 1 as an Interrupt source
0	Reserved	0	Reserved

4.10 ECAP Interrupt Flag Register (ECFLG)

The ECAP interrupt flag register (ECFLG) is shown in [Figure 26](#) and described in [Table 23](#).

Figure 26. ECAP Interrupt Flag Register (ECFLG)

Reserved							
R-0							
7	6	5	4	3	2	1	0
CTR=CMP	CTR=PRD	CTROVF	CEVT4	CETV3	CEVT2	CETV1	INT
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R = Read only; -n = value after reset

Table 23. ECAP Interrupt Flag Register (ECFLG) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7	CTR=CMP	0	Compare Equal Compare Status Flag. This flag is only active in APWM mode. Indicates no event occurred
		1	Indicates the counter (TSCTR) reached the compare register value (ACMP)
6	CTR=PRD	0	Counter Equal Period Status Flag. This flag is only active in APWM mode. Indicates no event occurred
		1	Indicates the counter (TSCTR) reached the period register value (APRD) and was reset.
5	CTROVF	0	Counter Overflow Status Flag. This flag is active in CAP and APWM mode. Indicates no event occurred.
		1	Indicates the counter (TSCTR) has made the transition from 0xFFFFFFFF to 0x00000000
4	CEVT4	0	Capture Event 4 Status Flag This flag is only active in CAP mode. Indicates no event occurred
		1	Indicates the fourth event occurred at ECAP _n pin
3	CEVT3	0	Capture Event 3 Status Flag. This flag is active only in CAP mode. Indicates no event occurred.
		1	Indicates the third event occurred at ECAP _n pin.
2	CEVT2	0	Capture Event 2 Status Flag. This flag is only active in CAP mode. Indicates no event occurred.
		1	Indicates the second event occurred at ECAP _n pin.
1	CEVT1	0	Capture Event 1 Status Flag. This flag is only active in CAP mode. Indicates no event occurred.
		1	Indicates the first event occurred at ECAP _n pin.
0	INT	0	Global Interrupt Status Flag Indicates no interrupt generated.
		1	Indicates that an interrupt was generated.

4.11 ECAP Interrupt Clear Register (ECCLR)

The ECAP interrupt clear register (ECCLR) is shown in [Figure 27](#) and described in [Table 24](#).

Figure 27. ECAP Interrupt Clear Register (ECCLR)

Reserved							
R-0							
7	6	5	4	3	2	1	0
CTR=CMP	CTR=PRD	CTROVF	CEVT4	CETV3	CETV2	CETV1	INT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. ECAP Interrupt Clear Register (ECCLR) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7	CTR=CMP	0 1	Counter Equal Compare Status Flag Writing a 0 has no effect. Always reads back a 0 Writing a 1 clears the CTR=CMP flag condition
6	CTR=PRD	0 1	Counter Equal Period Status Flag Writing a 0 has no effect. Always reads back a 0 Writing a 1 clears the CTR=PRD flag condition
5	CTROVF	0 1	Counter Overflow Status Flag Writing a 0 has no effect. Always reads back a 0 Writing a 1 clears the CTROVF flag condition
4	CEVT4	0 1	Capture Event 4 Status Flag Writing a 0 has no effect. Always reads back a 0. Writing a 1 clears the CEVT3 flag condition.
3	CEVT3	0 1	Capture Event 3 Status Flag Writing a 0 has no effect. Always reads back a 0. Writing a 1 clears the CEVT3 flag condition.
2	CEVT2	0 0	Capture Event 2 Status Flag Writing a 0 has no effect. Always reads back a 0. Writing a 1 clears the CEVT2 flag condition.
1	CEVT1	0 1	Capture Event 1 Status Flag Writing a 0 has no effect. Always reads back a 0. Writing a 1 clears the CEVT1 flag condition.
0	INT	0 1	Global Interrupt Clear Flag Writing a 0 has no effect. Always reads back a 0. Writing a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1.

4.12 ECAP Interrupt Forcing Register (ECFRC)

The ECAP interrupt forcing register (ECFRC) is shown in [Figure 28](#) and described in [Table 25](#).

Figure 28. ECAP Interrupt Forcing Register (ECFRC)

15	14	13	12	11	10	9	8
Reserved							
R-0							
7	6	5	4	3	2	1	0
CTR=CMP	CTR=PRD	CTROVF	CEVT4	CETV3	CETV2	CETV1	Reserved
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

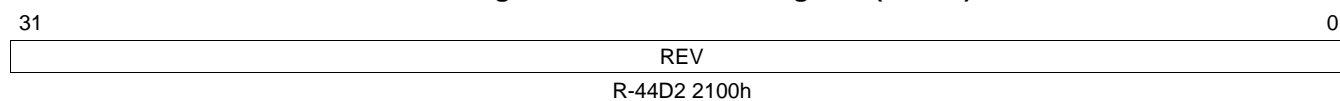
Table 25. ECAP Interrupt Forcing Register (ECFRC) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7	CTR=CMP	0 1	Force Counter Equal Compare Interrupt No effect. Always reads back a 0. Writing a 1 sets the CTR=CMP flag bit.
6	CTR=PRD	0 1	Force Counter Equal Period Interrupt No effect. Always reads back a 0. Writing a 1 sets the CTR=PRD flag bit.
5	CTROVF	0 1	Force Counter Overflow No effect. Always reads back a 0. Writing a 1 to this bit sets the CTROVF flag bit.
4	CEVT4	0 1	Force Capture Event 4 No effect. Always reads back a 0. Writing a 1 sets the CEVT4 flag bit
3	CEVT3	0 1	Force Capture Event 3 No effect. Always reads back a 0. Writing a 1 sets the CEVT3 flag bit
2	CEVT2	0 1	Force Capture Event 2 No effect. Always reads back a 0. Writing a 1 sets the CEVT2 flag bit.
1	CEVT1	0 1	Force Capture Event 1 No effect. Always reads back a 0. Writing a 1 sets the CEVT1 flag bit.
0	Reserved	0	Reserved

4.13 Revision ID Register (REVID)

The revision ID register (REVID) is shown in [Figure 29](#) and described in [Table 26](#).

Figure 29. Revision ID Register (REVID)



LEGEND: R = Read only; -n = value after reset

Table 26. Revision ID Register (REVID) Field Descriptions

Bit	Field	Value	Description
31-0	REV	44D2 2100h	Revision ID.

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