

# EVM User's Guide: HSEC180ADAPEVM-AM2

## AM261x SOM to HSEC Adapter Board



### Description

This evaluation module is a 180-pin High Speed Edge Card (HSEC) adapter for TI AM261x System-On-Module (SOM) platforms, allowing for SOM-based platforms to have backwards compatibility with Sitara/C2000 HSEC-based EVMs. The HSEC180ADAPEVM-AM2 connects 180 pins from the SOM board to HSEC pins for use with legacy Sitara/C2000 HSEC Docking Stations, such as the [TMDSHSECDOCK-AM263](#) and [TMDSHSECDOCK](#).

### Get Started

1. Order the AM261x SOM to HSEC Adapter Board ([HSEC180ADAPEVM-AM2](#))
2. Order the AM261 controlSOM Evaluation Board ([AM261-SOM-EVM](#))
3. Order the XDS110 emulation board ([XDS110ISO-EVM](#))
4. Order the HSEC Docking Station hardware. For a board comparison, see [Table 2-1](#)
  - a. AM26x HSEC Docking Station ([TMDSHSECDOCK-AM263](#))
  - b. C2000 HSEC Docking Station ([TMDSHSECDOCK](#))

5. Download the latest [Code Composer Studio™](#) Integrated Development Environment (IDE) and the [AM261x MCU PLUS Software Development Kit \(SDK\)](#)
6. Read the Setup chapter ([Section 2.2](#)) in this User's Guide to get started

### Features

- Standard 180-pin HSEC interface
- Compatibility with XDS110ISO-EVM for emulation
- 2x DP83869 10/100/1000-Mbps Ethernet PHY with 2x RJ-45 Ethernet jacks
- 1x Ethernet Add-on Board Connector compatible with:
  - DP83826-EVM-AM2 Industrial Ethernet add-on board
  - DP83TG720-EVM-AM2 Automotive Ethernet add-on board
- USB 2.0 Interface with Micro-AB port
- Fast Serial Interface (FSI) Header
- ADC filtering and ESD protection for dedicated analog HSEC pins
- OSPI Memory expansion board connector
- MCAN and LIN Transceiver connectivity when used with [TMDSHSECDOCK-AM263](#)



# 1 Evaluation Module Overview

## 1.1 Introduction

The HSEC180ADAPEVM-AM2 is a SOM to HSEC adapter board that is used to expand the IO and evaluation capabilities of the AM261x controlSOM EVM (AM261-SOM-EVM). The SOM to HSEC adapter board allows interfaces not present on the AM261x controlSOM to be evaluated using a compatible HSEC docking station for powering the system and prototyping using the IO headers and on-board hardware of the HSEC docking station.

The SOM to HSEC adapter allows on-board interfacing with Ethernet, USB 2.0, FSI, JTAG, and off-board interfacing with GPIO pins, MCAN, and LIN using the TMDSHSECDOCK-AM263. By utilizing all three boards in the AM261x controlSOM system (AM261-SOM-EVM + HSEC180ADAPEVM-AM2 + TMDSHSECDOCK-AM263), a customer can create and evaluate complex applications built around the AM261x Microcontroller.

The 180-pin Edge connector is intended to provide a well-filtered, robust design capable of working in most environments. The pinout of the 180-pin HSEC hardware is designed to be nearly identical to the existing AM263x and AM263Px controlCARD EVMs ([TMDSCNCD263](#) and [TMDSCNCD263P](#)).

Included in this User's Guide are the hardware details of the SOM to HSEC adapter board and explanations of the functions of the on-board peripherals, locations of jumpers and connectors, and configurations of switches on the PCB. Also included in this guide are instructions on how to start developing software applications using the AM261x controlSOM, SOM to HSEC adapter board, and HSEC docking station.

### **Preface: Read This First**

#### **1.1.1 Sitara MCU+ Academy**

Texas Instruments offers the [MCU+ Academy](#) as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

#### **1.1.2 Important Usage Notes**

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##### **Note**

External power supply or power accessory requirements:

- Compatible HSEC Docking Station
    - TMDSHSECDOCK-AM263
    - TMDSHSECDOCK
  - HSEC Docking Station Power Supply
    - Nominal output voltage: 5-VDC
    - Max output current: 3000mA
    - Efficiency Level V
- 

##### **Note**

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE.

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## 1.2 Kit Contents

The following items are included in the HSEC180ADAPEVM-AM2 kit:

- HSEC180ADAPEVM-AM2 PCB
- Quick Start Guide

## 1.3 Specification

The HSEC180ADAPEVM-AM2 is designed to expand on the capabilities of the AM261x controlSOM EVM, allowing a user to explore the full functionality of AM261x microcontrollers. The SOM to HSEC adapter board can be treated as a good reference design for the AM261x interfaces, but is not intended to be a complete

customer design. Full compliance to safety, EMI/EMC, and other regulations are left to the designer of the AM261x system.

### 1.3.1 Component Identification

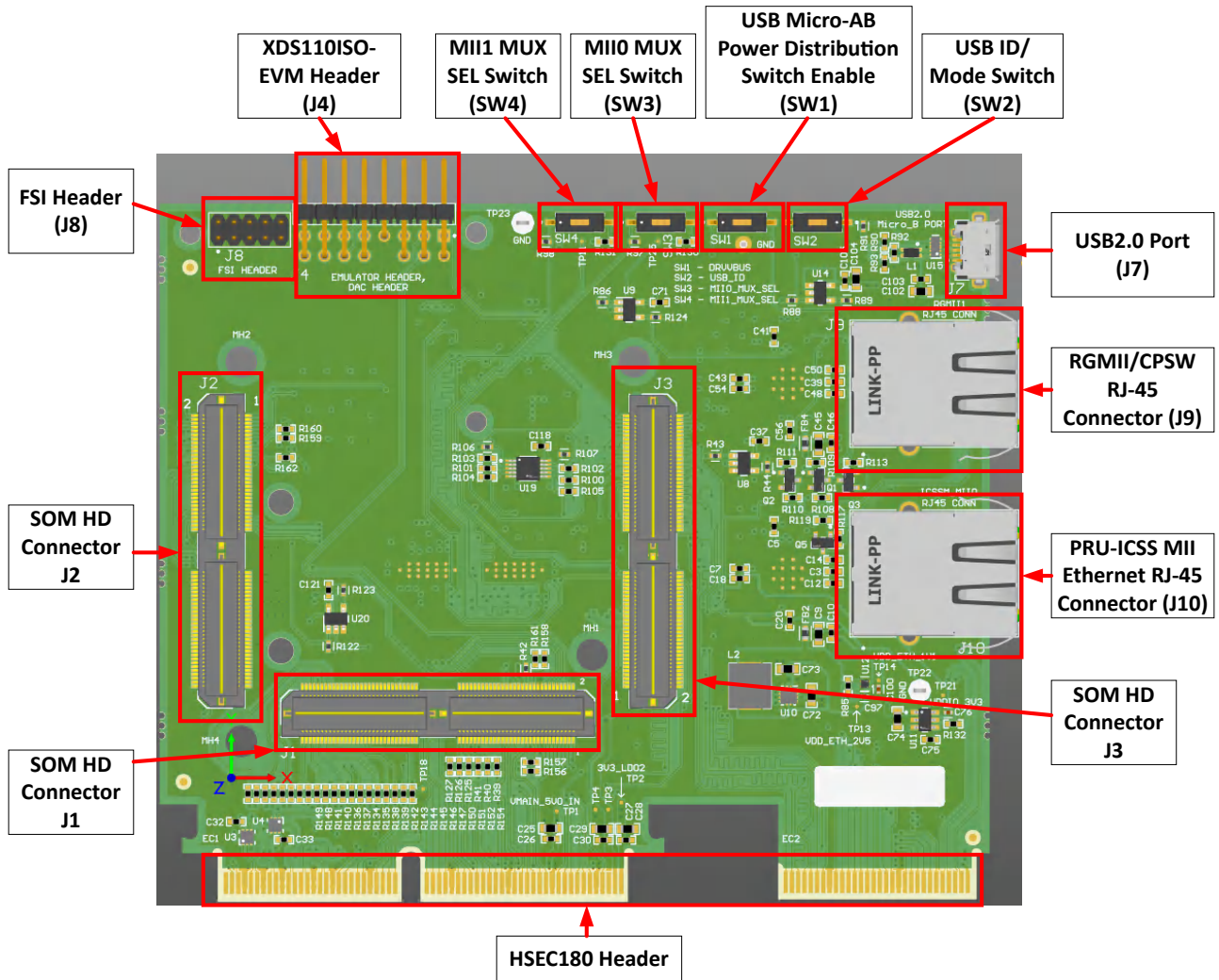


Figure 1-1. HSEC180ADAPEVM-AM2 Top

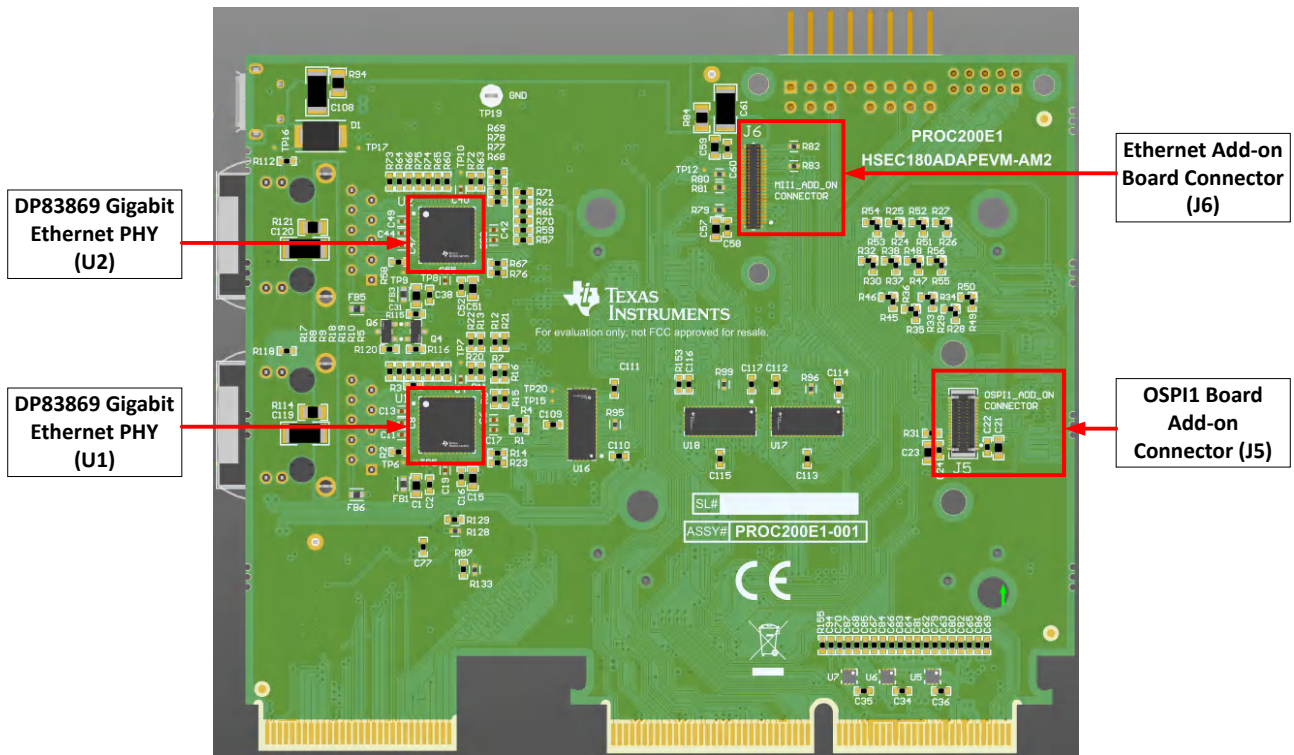


Figure 1-2. HSEC180ADAEVM-AM2 Bottom

### 1.3.2 Functional Block Diagram

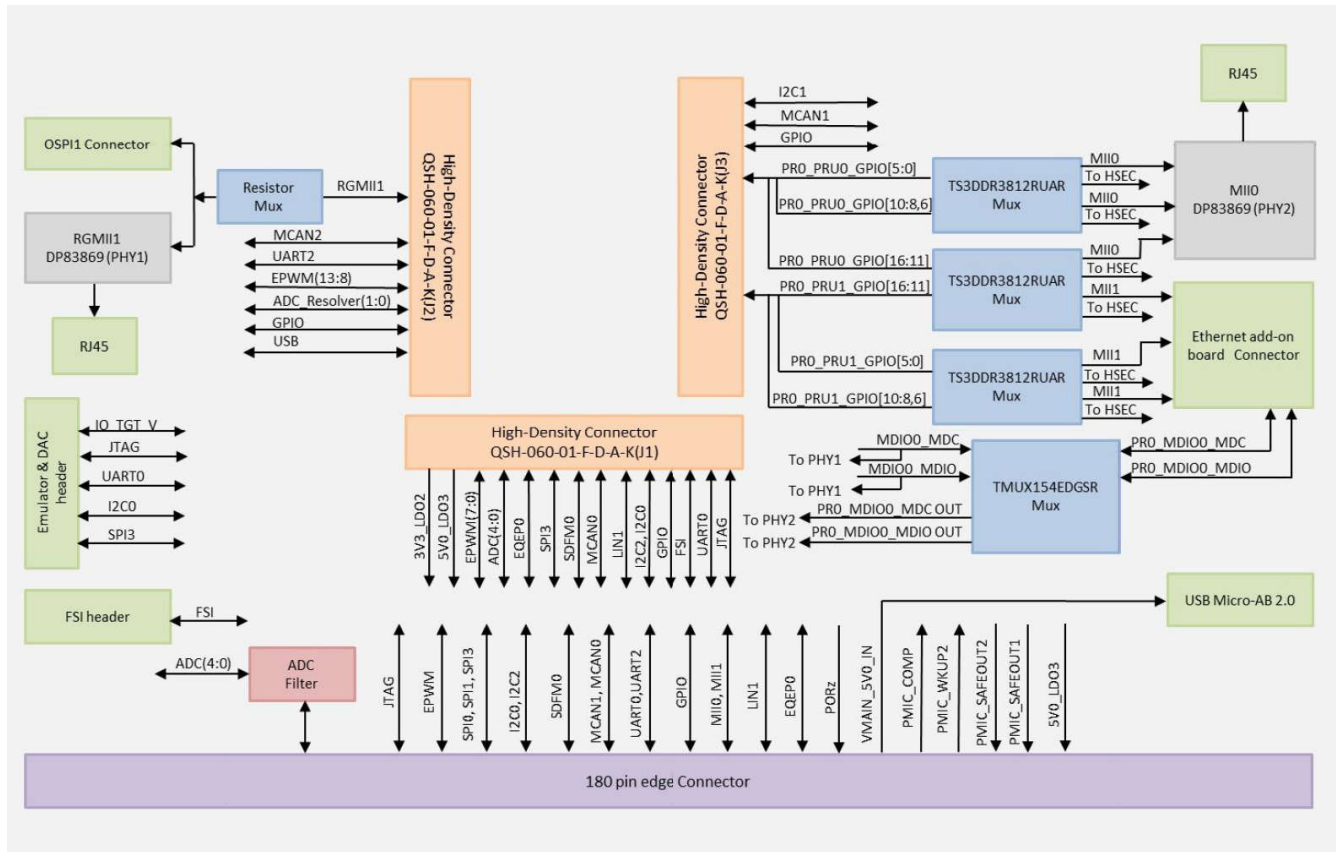


Figure 1-3. HSEC180ADAPEVM-AM2 Functional Block Diagram

### 1.4 Device Information

The AM261x Sitara Arm® Microcontrollers are part of Sitara AM26x real-time MCU families designed to meet the complex real-time processing needs of next generation industrial and automotive embedded products. With scalable Arm® Cortex-R5F performance and an extensive set of peripherals, AM261x device is designed for a broad range of applications while offering safety features and optimized peripherals for real time control.

Key features and benefits:

- Peripherals supporting system level connectivity such as Gigabit Ethernet, USB, OSPI/QSPI, CAN, UARTs, SPI and GPIOs.
- Granular firewalls managed by Hardware Security Manager (HSM) enable developers to implement stringent security minded system design requirements.
- Up to two R5F cores in cluster with 256KB of shared Tightly Coupled Memory (TCM) per core along with 1.5MB of shared SRAM, greatly reducing the need for external memory.

## 2 Hardware

### 2.1 Additional Images

### 2.2 Setup

The AM261x SOM to HSEC adapter board supports **controlSOM Configuration 2: controlCARD Backward Compatibility Configuration**. Power for the system is provided to the SOM to HSEC adapter + controlSOM system through an HSEC dock (TMDSHSECDOCK-AM263 or TMDSHSECDOCK). An emulation debug probe such as the XDS110ISO-EVM is required to provide debug connectivity to the MCU on the controlSOM. The controlSOM, XDS110 debug probe, and HSEC dock are sold separately.

TMDSHSECDOCK-AM263 and TMDSHSECDOCK are HSEC docking stations are required to use the HSEC180ADAPEVM-AM2, and provide the power supply to the overall controlSOM system. Both HSEC docking stations enable rapid prototyping and enhances the development capability of the AM261x controlSOM. The TMDSHSECDOCK-AM263 contains hardware to enable AM26x MCU-specific features that allow various peripherals not enabled on-board the controlSOM to be interfaced with, whereas the TMDSHSECDOCK only enables access to the IOs pinned out to the SOM HD connectors. [Table 2-1](#) compares the features of each docking station.

**Table 2-1. AM26x controlCARD HSEC Dock Comparison**

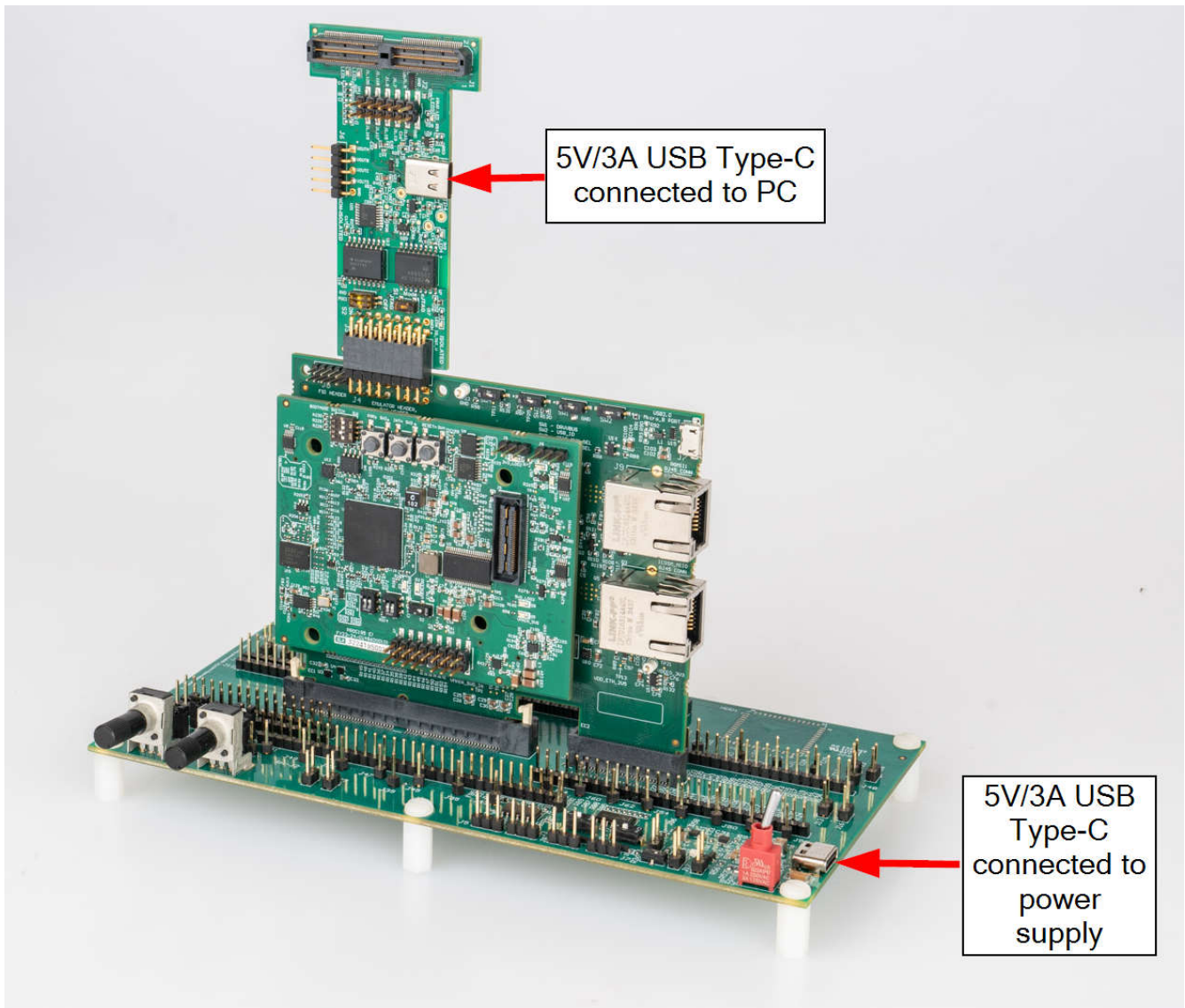
Feature	TMDSHSECDOCK	TMDSHSECDOCK-AM263
USB Type-C power input	✓	✓
GPIO breakout headers	✓	✓
Breadboard area for customizable routing and prototyping	✓	
2-channel MCAN Transceiver		✓
2-channel LIN Transceiver		✓
MIPI-60 debug header		✓
14-pin JTAG header	✓	✓
ADC input signal conditioning		✓

In this configuration, Code Composer Studio™ connects to the SOM to HSEC adapter board via JTAG and enables software development. The XDS110 debug-probe also enumerates a virtual COM port (VCP) for communication with the MCU via UART.

Follow these steps to enable this configuration:

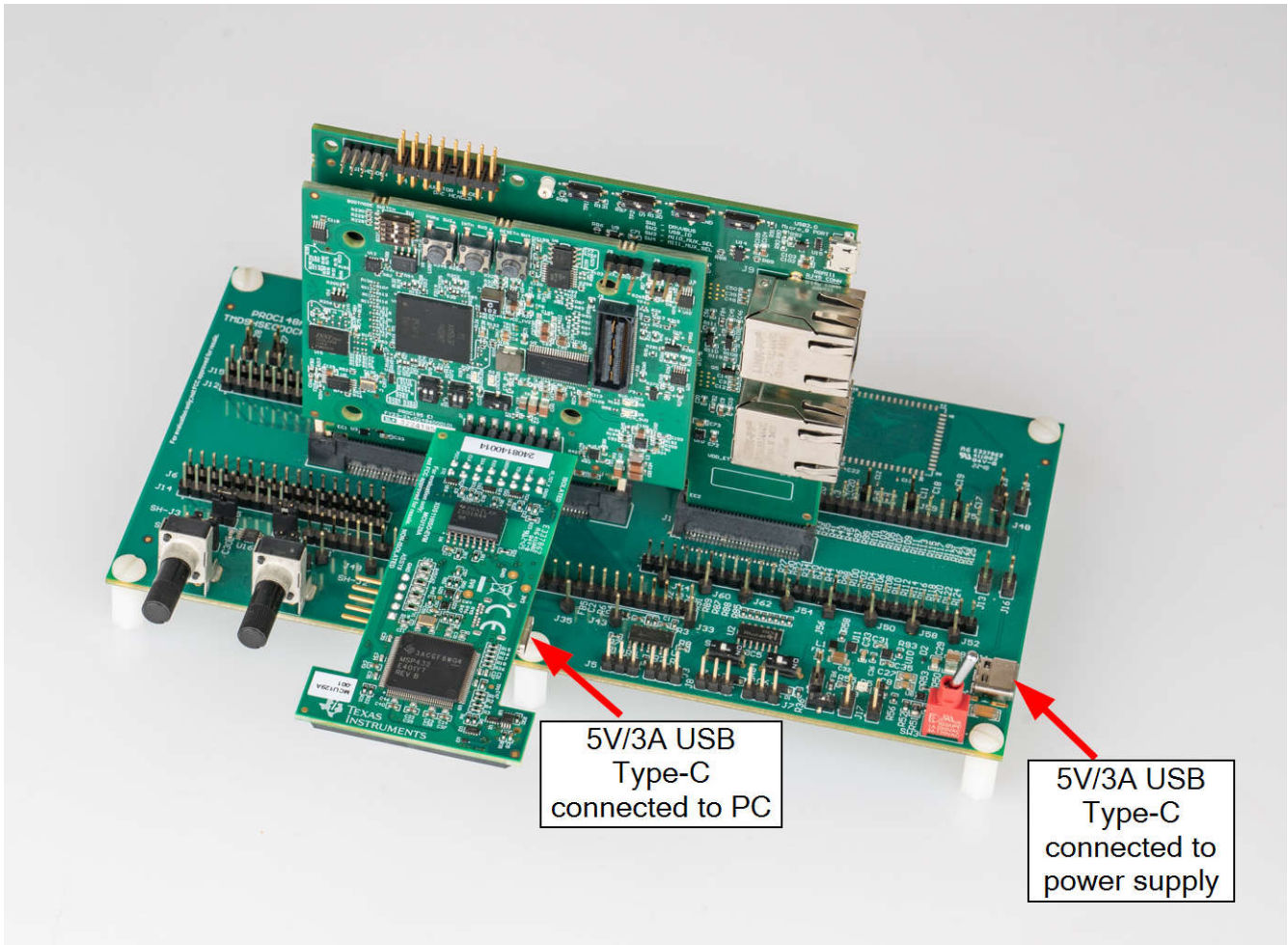
1. The following equipment is required:
  - a. AM261x controlSOM (AM261-SOM-EVM)
  - b. AM261x HSEC180 adapter board (HSEC180ADAPEVM-AM2)
  - c. AM26x controlCARD compatible baseboard/HSEC180 docking station (TMDSHSECDOCK-AM263 or TMDSHSECDOCK)
  - d. XDS110 isolated debug probe (XDS110ISO-EVM)
  - e. 2 USB Type-C cables
  - f. (Optional) DC 5V power supply if using TMDSHSECDOCK
2. Verify the switch settings are correct on each EVM.
  - a. AM261-SOM-EVM:
    - i. Use SW1 to select the desired boot mode (see *Boot Mode Selection* in the [AM261-SOM-EVM User Guide](#))
    - ii. Use S1, S2, S4 to select the desired ADC voltage reference mode (if applicable for the application) (see *ADC and DAC* in the [AM261-SOM-EVM User Guide](#))
  - b. XDS110ISO-EVM:

- i. S1 selects JTAG mode – set to JTAG mode.
  - ii. S2 enables UART/SPI connection – set to ON mode.
3. Attach the controlSOM to the SOM to HSEC180 adapter board
4. Ensure the controlSOM is correctly oriented. The J1 header on the controlSOM should connect with the J1 header on the HSEC180 adapter board.
5. Insert the HSEC180 adapter board into the HSEC docking station
6. Connect the XDS110ISO-EVM into the connector J4 of the HSEC-180 adapter board ([Figure 2-1](#)) OR J7 ([Figure 2-2](#)) of the controlSOM.
7. Connect the USB cable into connector J5 on the XDS110 isolated debug probe. The XDS110 isolated probe is powered on
8. Connect a USB cable into the connector on the HSEC docking station.
9. HSEC Dock Power
  - a. If using TMDSHSECDOCK-AM263 - Flip SW3 to the ON position
  - b. If using TMDSHSECDOCK - Flip S1 to the USB-ON position
10. Verify the power status LEDs (D5, D6, D7) on the controlSOM are turned on.
11. The controlSOM is ready for use. Follow the steps in [Software](#) to get started developing software.



**Figure 2-1. AM26x controlCARD Backward Compatibility Configuration - XDS110ISO connected to HSEC180ADAPEVM-AM2 J4**





**Figure 2-2. AM26x controlCARD Backward Compatibility Configuration - XDS110ISO connected to controlSOM J7**

### 2.3 Power Requirements

The SOM to HSEC adapter board receives power from the HSEC docking station through the 5V input pins on the HSEC header. The 5V input is passed to the controlSOM through the SOM HD Connectors to supply the PMIC on the controlSOM. The PMIC generates the 3.3V IO supply to power the on-board hardware of the HSEC180ADAPEVM-AM2, as well as the on-board supplies for the Ethernet PHYs.

2.3.1 Power Tree

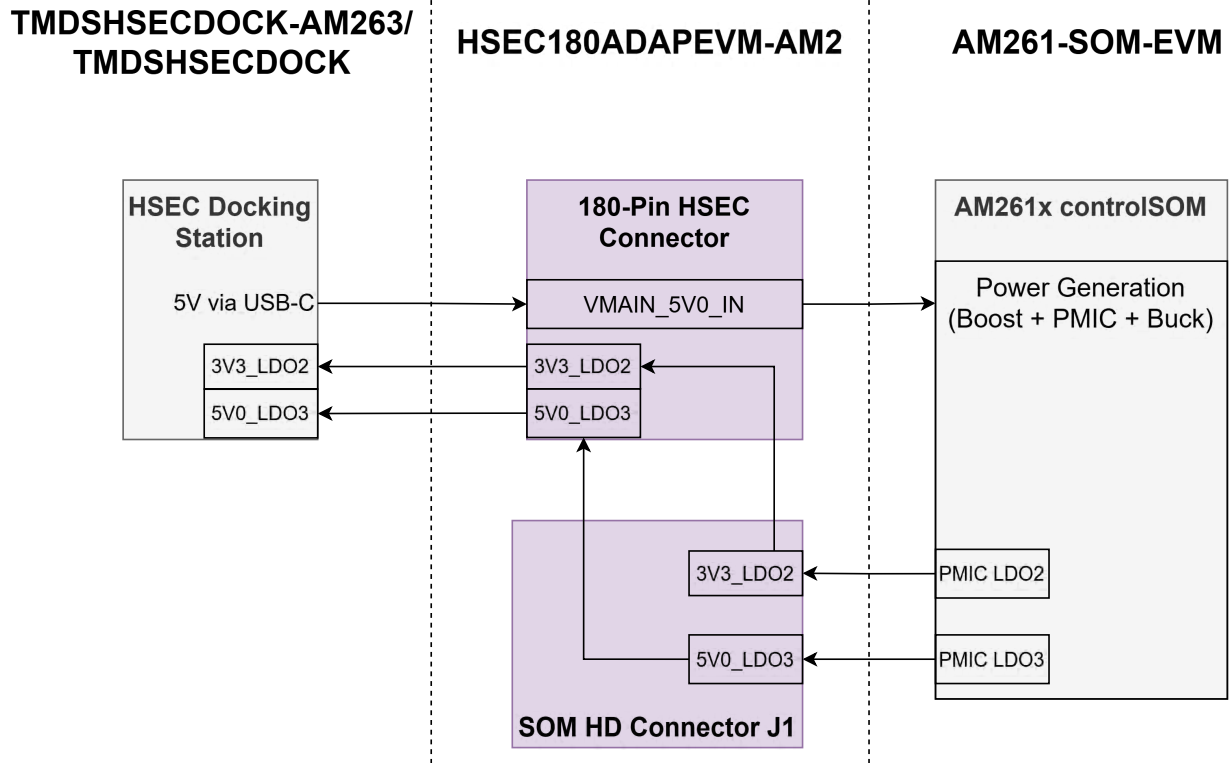
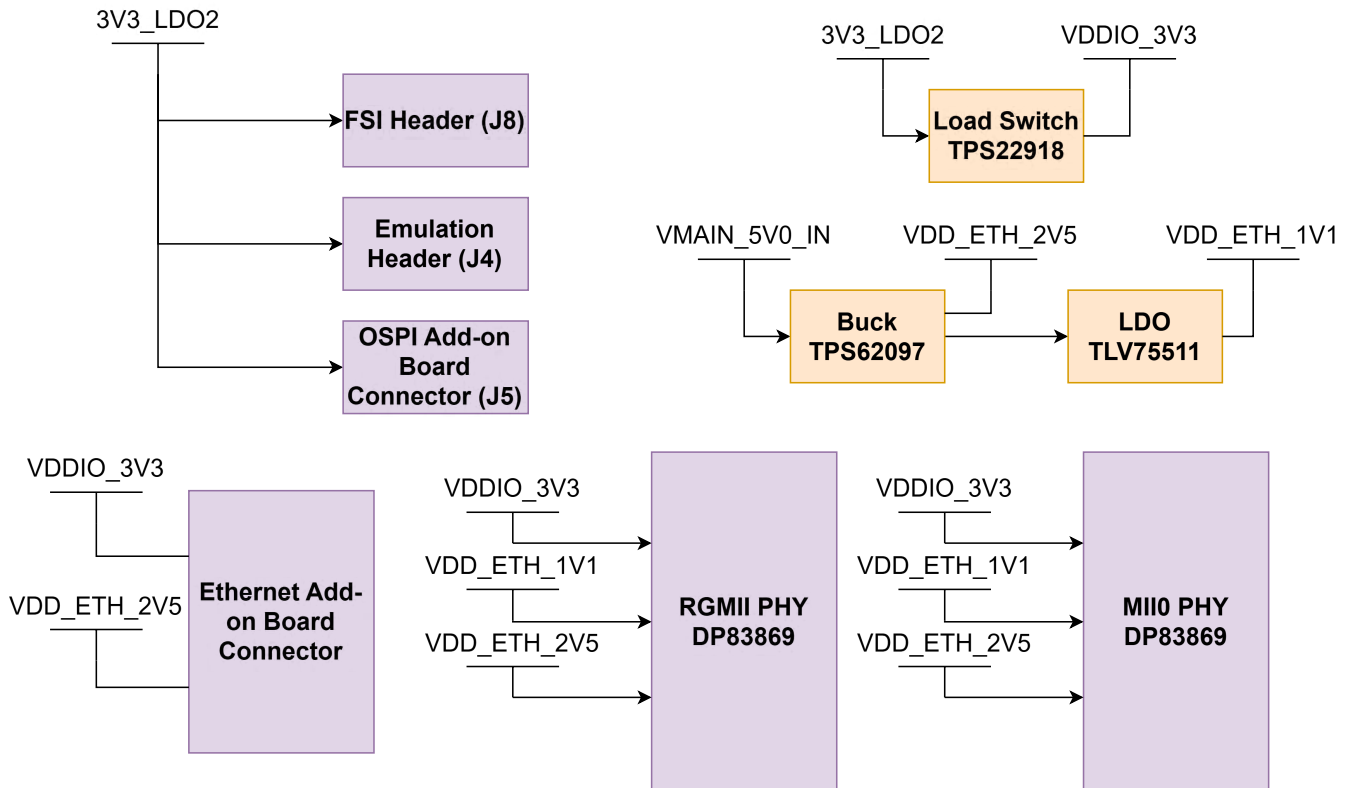


Figure 2-3. HSEC180ADAPEVM-AM2 Power Tree



### 2.3.2 Power Sequence

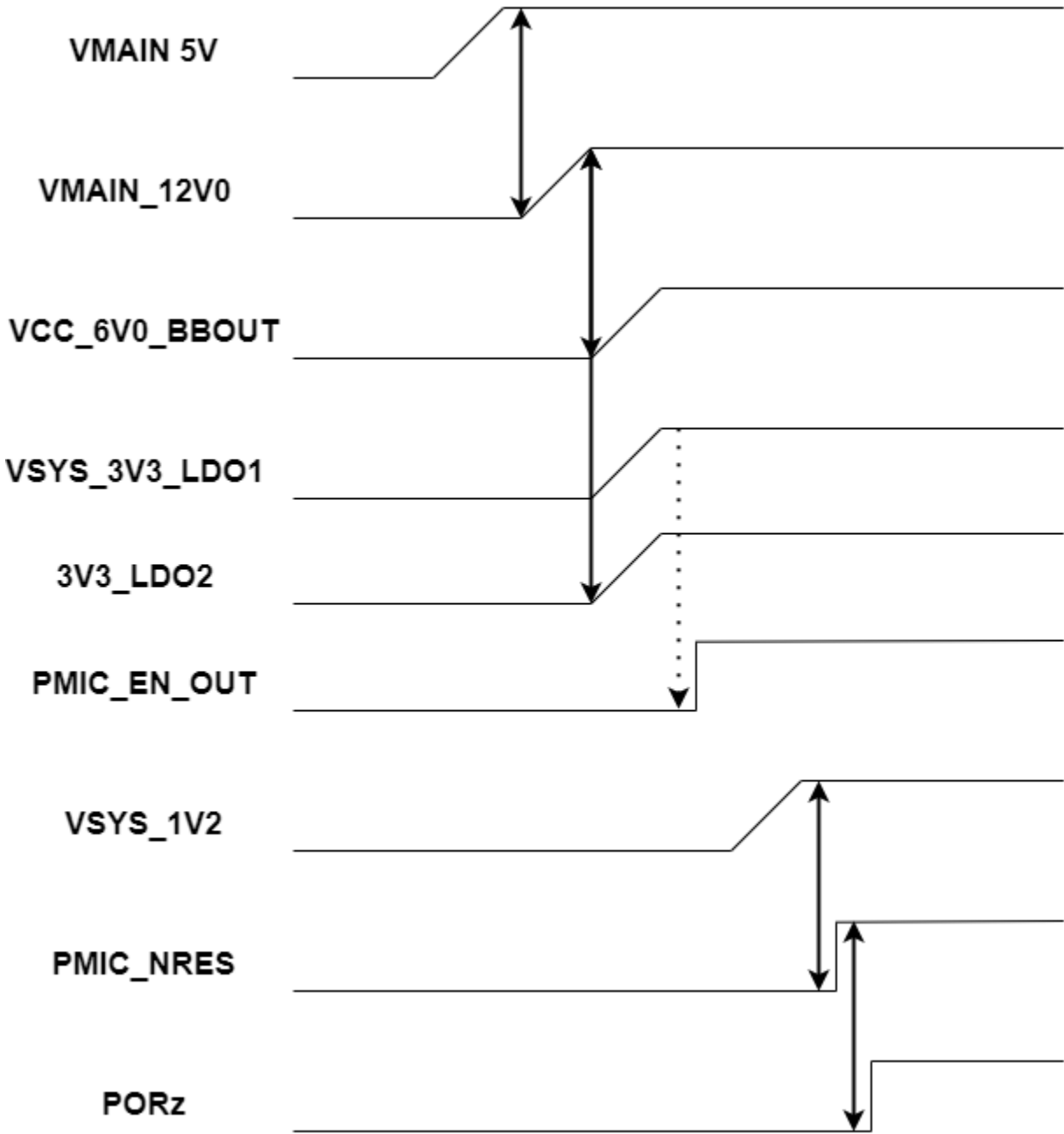


Figure 2-4. AM261-SOM-EVM Power Sequence

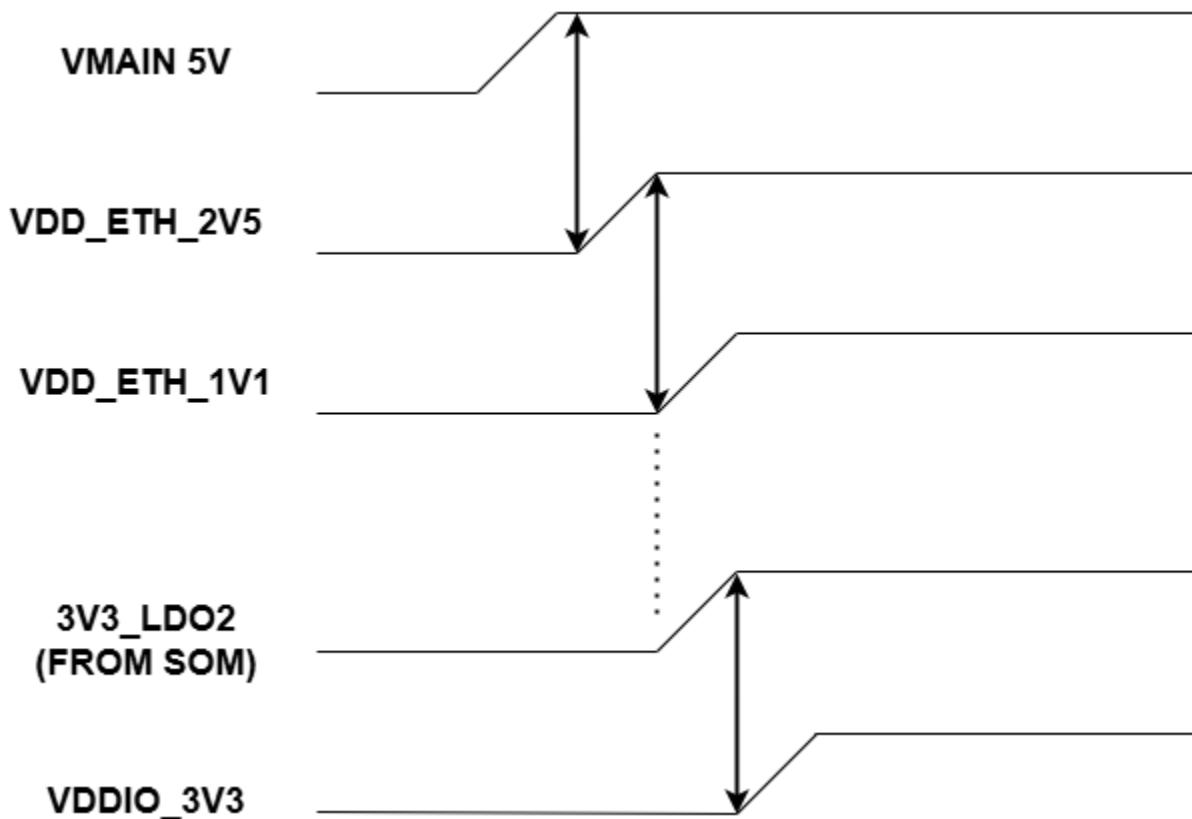


Figure 2-5. HSEC180ADAPEVM-AM2 Power Sequence

## 2.4 Header Information

### 2.4.1 Baseboard Headers (J1, J2, J3)

The HSEC180ADAPEVM-AM2 SOM HD Connector pinout conforms to the C2000/Sitara MCU controlSOM standard. Three baseboard headers, J1, J2, and J3, are supported for interfacing with the AM261x controlSOM EVM. Refer to the HSEC180ADAPEVM-AM2 design files for a complete pinout of these headers.

J1, J2, J3 header information:

- Part number: QSH-060-01-L-D-A
- Manufacturer: Samtec
- Maximum insertion cycles: 100

## 2.4.2 HSEC Pinout

The 180-pin High Speed Edge Connector (HSEC) connects to an HSEC docking station. This interface provides power to the SOM to HSEC adapter board and controlSOM through the SOM HD connectors. In addition, the HSEC pins bring out analog and digital IO from the controlSOM and allow access to prototyping using these interfaces, such as SPI, I2C, UART, FSI, EQEP, PRU-ICSS, EPWM, and ADC.

[Table 2-2](#) details the HSEC pinout. The pinout can also be found in the HSEC180ADAPEVM-AM2 design files package in the *PROC195E1(001)\_SOM\_to\_AM26x-HSEC.pdf* file.

**Table 2-2. HSEC Pinout - AM261-SOM-EVM Rev E1**

Pin #	SOM HD Pin	Package Signal Name	Muxed Signal Options	Muxed Signal Options	Signal Package Name	SOM HD Pin	Pin #
1		-	-		-		2
3	J1.24	TMS	TMS		-		4
5	J1.22	TCK	TCK		TDO	J1.21	6
7		GND	GND		TDI	J1.19	8
9	J1.119	ADC0_AIN0 / DAC_OUT	ADC0_AIN0 / DAC_OUT		GND		10
11	J1.117	ADC0_AIN1 / DAC_OUT	ADC0_AIN1 / DAC_OUT		ADC1_AIN0	J1.116	12
13		GND	GND		ADC1_AIN1	J1.114	14
15	J1.120	ADC0_AIN2	ADC0_AIN2		GND		16
17	J1.118	ADC0_AIN3	ADC0_AIN3		ADC1_AIN2	J1.111	18
19		GND	GND		ADC1_AIN3	J1.109	20
21	J1.115	ADC0_AIN4	ADC0_AIN4		GND		22
23	J1.113	ADC0_AIN5	ADC0_AIN5		ADC1_AIN4	J1.112	24
25	J1.107	ADC2_AIN0	ADC2_AIN0		ADC1_AIN5	J1.110	26
27	J1.105	ADC2_AIN1	ADC2_AIN1		ADC_CAL0	J1.92	28
29		GND	GND		-		30
31	J1.108	ADC2_AIN2	ADC2_AIN0		-		32
33	J1.106	ADC2_AIN3			-		34
35		GND	GND		-		36
37	J1.103	ADC2_AIN4	ADC2_AIN2		GND		38
39	J1.101	ADC2_AIN5	ADC2_AIN3		-		40
41		-	-		-		42
43	J1.87	ADC_VREFLO_G0_G1_G2			-		44
45	J1.85	ADC_VREFHI_G0_G1			GND		46
47		GND	GND		VMAIN_5V0_IN		48

**Table 2-2. HSEC Pinout - AM261-SOM-EVM Rev E1 (continued)**

Pin #	SOM HD Pin	Package Signal Name	Muxed Signal Options	Muxed Signal Options	Signal Package Name	SOM HD Pin	Pin #
49	J1.15	EPWM0_A	EPWM0_A / PR1_PRU0_GPIO5 / GPMC0_A3 / GPIO43	EPWM2_A / PR1_PRU0_GPIO3 / GPMC0_A1 / GPIO47 / EPWM2_A	EPWM2_A	J1.7	50
51	J1.13	EPWM0_B	EPWM0_B / PR1_PRU0_GPIO8 / GPMC0_A6 / GPIO44	EPWM2_B 0 / PR1_PRU0_GPIO16 / PR1_PRU0_GPIO7 / GPMC0_A14 / GPIO48 / EPWM2_B	EPWM2_B	J1.5	52
53	J1.11	EPWM1_A	EPWM1_A / PR1_PRU0_GPIO6 / GPMC0_A4 / GPIO45	EPWM3_A / PR1_PRU0_GPIO15 / GPMC0_A13 / GPIO49 / EPWM3_A	EPWM3_A	J1.3	54
55	J1.9	EPWM1_B	EPWM1_B / PR1_PRU0_GPIO4 / GPMC0_A2 / GPIO46	EPWM3_B / PR1_PRU0_GPIO11 / GPMC0_A9 / GPIO50 / EPWM6_A	EPWM3_B	J1.1	56
57	J1.16	EPWM4_A	EPWM4_A / PR1_PRU0_GPIO12 / GPMC0_A10 / GPIO51	EPWM6_A / PR1_PRU1_GPIO8 / CLKOUT0 / GPMC0_AD8 / GPIO55 / EPWM3_B	EPWM6_A	J1.8	58
59	J1.14	EPWM4_B	EPWM4_B / PR1_PRU0_GPIO13 / GPMC0_A11 / GPIO52	EPWM6_B / PR1_PRU1_GPIO6 / UART2_RTSn / GPMC0_A20 / GPIO56 / EPWM6_B	EPWM6_B	J1.6	60
61	J1.12	EPWM5_A	EPWM5_A / PR1_PRU0_GPIO14 / GPMC0_A12 / GPIO53	EPWM7_A / PR1_PRU1_GPIO4 / OSPI0_CSn1 / OSPI1_CSn1 / GPMC0_AD4 / GPIO57 / EPWM7_A	EPWM7_A	J1.4	62
63	J1.10	EPWM5_B	EPWM5_B / PR1_PRU1_GPIO5 / OSPI0_RESET_OUT0 / GPMC0_AD5 / GPIO54 / EPWM8_B	EPWM7_B / PR1_PRU1_GPIO3 / OSPI1_D1 / OSPI0_D1 / GPMC0_AD3 / GPIO58 / EPWM5_B	EPWM7_B	J1.2	64
65		GND	GND	-	-		66
67	J2.30	SPI0_D1	SPI0_D1 / PR1_PRU0_GPIO1 / MMC0_D1 / UART3_RTSn / GPMC0_A16 / FSITX0_DATA1 / GPIO14 / ADC_ETCH_XBAROUT3 / XBAROUT3	PR0_PRU1_GPIO19 / UART3_RXD / PR0_IEP0_EDC_SYNC_OUT0 / GPMC0_A19 / GPIO119 / TRC_CLK / EQEP1_A / XBAROUT13	EQEP1_A	J3.68	68
69	J2.32	SPI0_D0	SPI0_D0 / PR1_PRU0_GPIO0 / MMC0_D0 / UART3_CTSn / GPMC0_BE1n / FSITX0_DATA0 / GPIO13 / ADC_ETCH_XBAROUT_2 / XBAROUT2 / SOP3	PR0_PRU1_GPIO18 / UART3_TXD / PR0_IEP0_EDIO_DATA_IN_OUT31 / GPMC0_A17 / GPIO120 / TRC_CTL / EQEP1_B / XBAROUT14	EQEP1_B	J3.66	70
71	J2.34	SPI0_CLK	SPI0_CLK / PR1_PRU0_GPIO9 / MMC0_CMD / UART3_TXD / FSITX0_CLK / GPMC0_A7 / GPIO12 / ADC_ETCH_XBAROUT1 / XBAROUT1 / SOP2	CLKOUT1 / PR1_PRU0_GPIO7 / UART2_RTSn / PSM_CLKOUT / PR1_UART0_CTSn / GPMC0_A5 / GPIO122 / SDFM0_CLK0 / EQEP1_STROBE	EQEP1_STROBE	J1.54	72
73	J2.36	SPI0_CS0	SPI0_CS0 / PR1_PRU0_GPIO2 / MMC0_CLK / UART3_RXD / GPMC0_A0 / GPIO11 / ADC_ETCH_XBAROUT0 / XBAROUT0	EXT_REFCLK0 / SAFETY_ERRORn / USB0_DRVVBUS / PR0_IEP0_EDIO_DATA_IN_OUT30 / GPMC0_A18 / GPIO121 / EQEP1_INDEX / XBAROUT15 / DTB_OUT_14	EQEP1_INDEX	J1.70	74
75	J1.59	SPI1_D0	SPI1_D0 / EPWM8_A / MMC0_WP / UART5_TXD / OSPI0_ECC_FAIL / PR1_PRU1_GPIO16 / FSIRX0_DATA0 / GPIO17 / GPMC0_DIR / ADC_ETCH_XBAROUT6 / XBAROUT3	LIN1_RXD / OSPI0_ECC_FAIL / SPI2_CS0 / PR1_PRU1_GPIO6 / OSPI1_ECC_FAIL / UART1_RXD / GPMC0_AD6 / GPIO19 / OSPI0_RESET_OUT1 / XBAROUT5 / EPWM6_B	LIN1_RXD	J1.37	76

**Table 2-2. HSEC Pinout - AM261-SOM-EVM Rev E1 (continued)**

Pin #	SOM HD Pin	Package Signal Name	Muxed Signal Options	Muxed Signal Options	Signal Package Name	SOM HD Pin	Pin #
77	J1.57	SPI1_D1	SPI1_D1 / EPWM8_B / MMC0_CD / UART5_RXD / OSPI0_RESET_OUT0 / PR1_PRU1_GPIO15 / FSIRX0_DATA1 / GPIO18 / GPMC0_WPn / ADC_ETCH_XBAROUT7 / XBAROUT4	LIN1_TXD / OSPI0_RESET_OUT0 / SPI2_CLK / PR1_PRU1_GPIO8 / OSPI1_RESET_OUT0 / UART1_TXD / GPMC0_AD8 / GPIO20 / XBAROUT6 / EPWM6_A	LIN1_TXD	J1.35	78
79	J1.55	SPI1_CLK	SPI1_CLK / EPWM7_B / MMC0_D3 / UART4_RXD / PR1_PRU1_GPIO3 / FSIRX0_CLK / GPIO16 / GPMC0_OEn_REn / ADC_ETCH_XBAROUT5	MMC0_CLK / UART0_RXD / LIN0_RXD / MCAN0_RX / PR1_MDIO0_MDIO / GPIO77 / SDFM1_CLK0	MCAN0_RX	J1.38	80
81	J3.57	SPI1_CS0	SPI1_CS0 / EPWM7_A / MMC0_D2 / UART4_TXD / PR1_PRU1_GPIO4 / GPIO15 / GPMC0_WAIT0 / ADC_ETCH_XBAROUT4 / XBAROUT1	MMC0_CMD / UART0_TXD / LIN0_TXD / MCAN0_TX / PR1_MDIO0_MDC / GPIO78 / SDFM1_D0	MCAN0_TX	J1.36	82
83		GND	GND		VMAIN_5V0_IN		84
85	J1.63	I2C2_SDA	MMC0_CD / UART0_CTSn / I2C2_SDA / GPIO84 / SDFM1_D3	UART0_RXD / LIN0_RXD / GPIO27 / XBAROUT4 / DTB_INOUT_6	UART0_RXD	J1.33	86
87	J1.61	I2C2_SCL	MMC0_WP / UART0_RTSn / I2C2_SCL / PR1_PRU0_GPIO2 / GPIO83 / SDFM1_CLK3	UART0_TXD / LIN0_TXD / GPIO28 / XBAROUT5 / DTB_INOUT_7	UART0_TXD	J1.31	88
89	J3.99	PR0_MDIO0_MDIO	PR0_MDIO0_MDIO / LIN0_RXD / MCAN0_RX / GPIO85 / XBAROUT14	PR0_MDIO0_MDC / LIN0_TXD / MCAN0_TX / GPIO86 / XBAROUT15 / DTB_OUT_11	PR0_MDIO0_MDC	J3.97	90
91	J1.60	SDFM0_D0	PR0_ECAP0_APWM_OUT / PR1_PRU1_GPIO10 / UART2_CTSn / PR1_ECAP0_APWM_OUT / PR1_UART0_RTSn . GPMC0_AD10 / GPIO123 / SDFM0_D0	I2C0_SDA / GPIO134 / SDFM1_CLK2	I2C0_SDA	J1.25	92
93	J1.23	I2C0_SCL	I2C0_SCL / GPIO135 / SDFM1_CLK3	MMC0_D0 / UART2_RXD / I2C1_SCL / MCAN1_RX / PR1_PRU0_GPIO10 / GPIO79 / SDFM1_CLK1	MCAN1_RX	J3.56	94
95	J3.54	MCAN1_TX	MMC0_D1 / MCAN1_TX / PR1_PRU0_GPIO10 / GPIO79 / SDFM1_CLK1	MMC0_D2 / UART2_TXD / I2C1_SDA / PR1_PRU0_GPIO0 / GPIO81 / SDFM1_CLK2	I2C1_SDA	J3.72	96
97		GND	GND		VMAIN_5V0_IN		98
99	J1.58	SDFM0_D1	PR0_PRU1_GPIO17 / PR1_PRU1_GPIO13 / UART2_RXD / PR0_IEP0_EDIO_DATA_IN_OUT30 / PR1_UART0_TXD / UART5_CTSn / GPMC0_AD13 / GPIO125 / SDFM0_D1	SPI2_D0 / PR1_PRU1_GPIO18 / UART4_RTSn / PR1_IEP0_EDC_SYNC_OUT0 / I2C1_SDA / MCAN1_RX / GPMC0_OEn_REn / GPIO130 / EQEP0_A / SDFM1_CLK0	EQEP0_A	J1.71	100
101	J1.72	SDFM0_CLK1	PR0_PRU1_GPIO7 / CPTS0_TS_SYNC / PR1_PRU0_GPIO10 / PR0_IEP0_EDC_SYNC_OUT1 / PR1_UART0_RXD / GPMC0_A8 / GPIO124 / SDFM0_CLK1 / SDFM1_D0 / UART2_TXD / UART5_RTSn	SPI2_CS0 / PR1_PRU0_GPIO19 / UART4_CTSn / PR1_IEP0_EDIO_DATA_IN_OUT31 / I2C1_SCL / MCAN1_TX / GPMC0_CS0 / GPIO131 / EQEP0_B / SDFM1_D0	EQEP0_B	J1.69	102
103	J1.56	SDFM0_D2	UART2_CTSn / PR1_MDIO0_MDC / SPI3_CS1 / UART5_RXD / GPMC0_BE0n_CLE / GPIO127 / SDFM0_D2 / ADC_EXTCH_XBAROUT0	I2C2_SDA / PR1_PRU0_GPIO20 / UART4_TXD / PR1_IEP0_EDIO_DATA_IN_OUT30 / GPMC0_A15 / GPIO132 / EQEP0_STROBE / SDFM1_CLK1 / ADC_EXTCH_XBAROUT2	EQEP0_STROBE	J1.67	104

**Table 2-2. HSEC Pinout - AM261-SOM-EVM Rev E1 (continued)**

Pin #	SOM HD Pin	Package Signal Name	Muxed Signal Options	Muxed Signal Options	Signal Package Name	SOM HD Pin	Pin #
105	J1.73	SDFM0_CLK2	UART1_CTSn / PR1_MDIO0_MDIO / SPI2_CS1 / PR1_IEP0_EDC_SYNC_OUT1 / UART5_CTSn / UART5_TXD / GPMC0_CLKLB / GPIO126 / SDFM0_CLK2 / SDFM1_D1 / ADC_EXTCH_XBAROUT8	I2C2_SCL / PR1_PRU1_GPIO7 / UART4_RXD / GPMC0_AD7 / GPIO133 / EQEP0_INDEX / SDFM1_D1 / ADC_EXTCH_XBAROUT3	EQEP0_INDEX	J1.65	106
107	J1.50	SDFM0_D3	SPI2_CLK / PR1_PRU1_GPIO17 / UART5_TXD / GPMC0_WEn / GPIO129 / SDFM0_D3 / ADC_EXTCH_XBAROUT1	PR0_PRU0_GPIO5 / UART3_RTSn / RMII2_RX_ER / MII2_RX_ER / GPIO87 / TRC_CTL / ADC_EXTCH_XBAROUT4 / XBAROUT6	PR0_PRU0_GPIO5	J3.111	108
109	J1.46	-	-	PR0_PRU0_GPIO9 / PR1_PRU0_GPIO9 / PR0_IEP0_EDC_SYNC_OUT1 / PR0_UART0_CTSn / MII2_COL	PR0_PRU0_GPIO9	J3.105	110
111		GND	GND	VMAIN_5V0_IN	VMAIN_5V0_IN		112
113	J3.29	PMIC_SAFE_OUT2	PMIC_SAFE_OUT2	PMIC_WKUP2	PMIC_WKUP2	J1.30	114
115		NC	NC	-	-		116
117	J1.34	VSS_5V0_LDO3	VCC_5V0	-	-		118
119	J1.28	3V3_LDO2	3V3_LDO2	PORz	PORz	J1.29	120
121	J3.109	PR0_PRU0_GPIO10	PR0_PRU0_GPIO10 / UART3_CTSn / RMII2_CRS_DV / PR0_UART0_RTSn / MII2_CRS / GPIO89	PR0_PRU0_GPIO8 / I2C0_SDA / GPIO90	PR0_PRU0_GPIO8	J3.87	122
123	J.100	PR0_PRU0_GPIO6	PR0_PRU0_GPIO6 / I2C0_SCL / RMII2_REF_CLK / RGMII2_RXC / MII2_RXCLK / GPIO91	PR0_PRU0_GPIO4 / UART3_RXD / RGMII2_RX_CTL / MII2_RXDV / GPIO92 / TRC_CLK / ADC_EXTCH_XBAROUT5 / XBAROUT7	PR0_PRU0_GPIO4	J3.113	124
125	J3.102	PR0_PRU0_GPIO0	PR0_PRU0_GPIO0 / PR1_PRU0_GPIO0 / RMII2_RXD0 / RGMII2_RD0 / MII2_RXD0 / GPIO93 / TRC_DATA0 / ADC_EXTCH_XBAROUT6 / XBAROUT8	PR0_PRU0_GPIO1 / PR1_PRU0_GPIO1 / RMII2_RXD1 / RGMII2_RD1 / MII2_RXD1 / GPIO94 / TRC_DATA1 / ADC_EXTCH_XBAROUT7 / XBAROUT11	PR0_PRU0_GPIO1	J3.104	126
127	J3.106	PR0_PRU0_GPIO2	PR0_PRU0_GPIO2 / PR1_PRU0_GPIO2 / RGMII2_RD2 / MII2_RXD2 / GPIO95 / TRC_DATA2 / ADC_EXTCH_XBAROUT8 / XBAROUT12	PR0_PRU0_GPIO3 / UART3_TXD / RGMII2_RD3 / MII2_RXD3 / GPIO96 / TRC_DATA3 / ADC_EXTCH_XBAROUT9 / XBAROUT13 / DTB_INOUT_0	PR0_PRU0_GPIO3	J3.108	128
129	J3.112	PR0_PRU0_GPIO16	PR0_PRU0_GPIO16 / RGMII2_TXC / MII2_TXCLK / GPIO97	PR0_PRU0_GPIO15 / RMII2_TX_EN / RGMII2_TX_CTL / MII2_TX_EN / GPIO98	PR0_PRU0_GPIO15	J3.115	130
131	J3.114	PR0_PRU0_GPIO11	PR0_PRU0_GPIO11 / RMII2_TXD0 / RGMII2_TD0 / MII2_TXD0 / GPIO99	PR0_PRU0_GPIO12 / RMII2_TXD1 / RGMII2_TD1 / MII2_TXD1 / GPIO100	PR0_PRU0_GPIO12	J3.116	132
133	J3.118	PR0_PRU0_GPIO13	PR0_PRU0_GPIO13 / RGMII2_TD2 / MII2_TXD2 / GPIO101	PR0_PRU0_GPIO14 / RGMII2_TD3 / MII2_TXD3 / GPIO102	PR0_PRU0_GPIO14	J3.120	134
135		GND	GND	-	-		136



**Table 2-2. HSEC Pinout - AM261-SOM-EVM Rev E1 (continued)**

Pin #	SOM HD Pin	Package Signal Name	Muxed Signal Options	Muxed Signal Options	Signal Package Name	SOM HD Pin	Pin #
137	J3.95	PR0_PRU1_GPIO5	PR0_PRU1_GPIO5 / RMII1_RX_ER / MII1_RX_ER / GPIO103 / TRC_DATA0 / ADC_EXTCH_XBAROUT6	PR0_PRU1_GPIO9 / PR0_UART0_RXD / PR0_IEP0_EDIO_DATA_IN_OUT31 / MII1_COL / GPMC0_A21 / GPIO104 / TRC_DATA1 / ADC_EXTCH_XBAROUT7	PR0_PRU1_GPIO9	J3.85	138
139	J3.83	PR0_PRU1_GPIO10	PR0_PRU1_GPIO10 / PR0_UART0_TXD / RMII1_CRS_DV / PR0_IEP0_EDIO_DATA_IN_OUT30 / MII1_CRS / GPMC0_A20 / GPIO105 / TRC_DATA2	PR0_PRU1_GPIO8 / GPIO106 / TRC_DATA3	PR0_PRU1_GPIO8	J3.89	140
141	J3.76	PR0_PRU1_GPIO6	PR0_PRU1_GPIO6 / MCAN0_RX / RMII1_REF_CLK / RGMII1_RXC / MII1_RXCLK / GPIO107 / TRC_DATA4 / DTB_INOUT_4	PR0_PRU1_GPIO4 / MCAN0_TX / RGMII1_RX_CTL / MII1_RXDV / GPIO108 / TRC_DATA5 / DTB_OUT_9	PR0_PRU1_GPIO4	J3.93	142
143	J3.78	PR0_PRU1_GPIO0	PR0_PRU1_GPIO0 / MCAN1_RX / RMII1_RXD0 / RGMII1_RD0 / MII1_RXD0 / GPIO109 / TRC_DATA6	PR0_PRU1_GPIO1 / MCAN1_TX / RMII1_RXD1 / RGMII1_RD1 / MII1_RXD1 / GPIO110 / TRC_DATA7 / DTB_OUT_13	PR0_PRU1_GPIO1	J3.80	144
145	J3.82	PR0_PRU1_GPIO2	PR0_PRU1_GPIO2 / RGMII1_RD2 / MII1_RXD2 / GPIO111 / TRC_DATA8	PR0_PRU1_GPIO3 / RGMII1_RD3 / MII1_RXD3 / GPIO112 / TRC_DATA9	PR0_PRU1_GPIO3	J3.84	146
147	J3.88	PR0_PRU1_GPIO16	PR0_PRU1_GPIO16 / RGMII1_TXC / MII1_TXCLK / GPIO113 / TRC_DATA10	PR0_PRU1_GPIO15 / RMII1_TX_EN / RGMII1_TX_CTL / MII1_TX_EN / GPIO114 / TRC_DATA11	PR0_PRU1_GPIO15	J3.91	148
149	J3.90	PR0_PRU1_GPIO11	PR0_PRU1_GPIO11 / RMII1_TXD0 / RGMII1_TD0 / MII1_TXD0 / GPIO115 / TRC_DATA12	PR0_PRU1_GPIO12 / RMII1_TXD1 / RGMII1_TD1 / MII1_TXD1 / GPIO116 / TRC_DATA13	PR0_PRU1_GPIO12	J3.92	150
151	J3.94	PR0_PRU1_GPIO13	PR0_PRU1_GPIO13 / RGMII1_TD2 / MII1_TXD2 / GPIO117 / TRC_DATA14 / XBAROUT11	PR0_PRU1_GPIO14 / RGMII1_TD3 / MII1_TXD3 / GPIO118 / TRC_DATA15 / XBAROUT12	PR0_PRU1_GPIO14	J3.96	152
153	J2.23	GPIO136	UART1_RTSn / SPI0_CS1 / LIN0_RXD / UART3_RXD / GPIO136 / SDFM1_D2		GPIO68	J2.57	154
155	J2.21	GPIO137	UART2_RTSn / EQEP1_INDEX / LIN0_TXD / UART3_TXD / GPIO137 / SDFM1_D3	PR1_PRU0_GPIO0 / OSPI0_D5 / UART3_CTSn / GPIO67	GPIO67	J2.59	156
157		GND	GND	VMAIN_5V0_IN	VMAIN_5V0_IN		158
159	J2.58	EPWM8_B	EPWM8_B / PR1_PRU1_GPIO15 / OSPI1_CLK / MCAN0_TX / OSPI0_CLK / GPMC0_AD15 / GPIO60 / UART4_RXD / EPWM9_B	PR1_PRU0_GPIO9 / OSPI0_D1 / UART1_DTRn / UART3_CTSn / OSPI1_D1 / OSPI0_ECC_FAIL / GPIO70	GPIO70	J2.53	160
161	J2.60	EPWM8_A	EPWM8_A / PR1_PRU1_GPIO16 / OSPI1_D0 / MCAN0_RX / PR0_PRU1_GPIO7 / OSPI0_D0 / GPMC0_CSn1 / GPIO59 / UART4_TXD / EPWM8_A	PR1_PRU0_GPIO2 / OSPI0_D3 / UART1_RIn / GPIO69	GPIO69	J2.55	162
163	J2.54	EPWM9_B	EPWM9_B / LIN1_RXD / OSPI0_CSn0 / UART1_RTSn / OSPI1_CSn0 / GPIO62	UART0_RTSn / I2C2_SCL / SPI3_D0 / PR1_PRU1_GPIO19 / PR1_PRU0_GPIO17 / UART3_RXD / GPMC0_WAIT1 / GPIO25 / XBAROUT9 / DTB_OUT_8	UART0_RTSn	J1.45	164

**Table 2-2. HSEC Pinout - AM261-SOM-EVM Rev E1 (continued)**

Pin #	SOM HD Pin	Package Signal Name	Muxed Signal Options	Muxed Signal Options	Signal Package Name	SOM HD Pin	Pin #
165	J2.56	EPWM9_A	EPWM9_A / LIN1_TXD / OSPI0_RESET_OUT0 / SPI2_CLK / UART1_TXD / OSPI1_RESET_OUT0 / GPIO61 / EPWM9_A	UART0_CTSn / I2C2_SDA / SPI3_D1 / SPI0_CS1 / PR1_PRU0_GPIO7 / UART3_TXD / GPIO26 / XBAROUT10	UART0_CTSn	J1.43	166
167	J2.50	GPIO64	LIN0_TXD / UART2_RTSn / OSPI0_RESET_OUT0 / I2C0_SCL / UART4_TXD / GPIO64	I2C1_SDA / SPI3_CLK / PR1_PRU0_GPIO18 / GPMC0_OEn_REn / GPIO24 / XBAROUT8	I2C1_SDA	J1.41	168
169	J2.52	GPIO63	LIN0_RXD / UART1_CTSn / I2C0_SDA / UART2_TXD / GPIO63 / EPWM7_B	I2C1_SCL / SPI3_CS0 / PR1_PRU0_GPIO17 / GPMC0_WEn / GPIO23 / XBAROUT7	I2C1_SCL	J1.39	170
171	J3.33	PMIC_COMP2_IN+	PMIC_COMP2_IN+	-	-	-	172
173	J3.31	PMIC_COMP2_IN-	PMIC_COMP2_IN-	-	-	-	174
175	J3.37	PMIC_COMP1_IN+	PMIC_COMP1_IN+	-	-	-	176
177	J3.35	PMIC_COMP1_IN-	PMIC_COMP1_IN-	PMIC_SAFE_OUT1	PMIC_SAFE_OUT1	J1.32	178
179		GND	GND	VMAIN_5V0_IN	VMAIN_5V0_IN		180

### 2.4.3 XDS Debug Header (J4)

The XDS debug header (J4) provides debug access to the AM261-SOM-EVM. The XDS debug header is compatible with the [XDS110ISO-EVM](#). [Table 2-3](#) provides a pinout of the J4 header.

#### CAUTION

The XDS debug header (J4) is only compatible with the [XDS110ISO-EVM](#). Do not plug in any other debug probe directly into this header. See [Section 2.9](#) for information on using other debug probes with the controlSOM.

**Table 2-3. XDS Debug Header (J4) Pinout**

EVM Connection	Function	Pin	Pin	Function	EVM Connection
VSYS_3V3_LDO1	IO_TGT_V	1	2	GND	GND
TMS	MCU_TMS	3	4	MCU_TCK	TCK
TDI	MCU_TDI	5	6	MCU_TDO	TDO
GND	GND	7	8	KEY	NC
UART0_RXD	MCU_SCI_RX	9	10	MCU_SCI_TX	UART0_TXD
I2C0_SDA	EE_I2CSDA	11	12	EE_I2CSCL	I2C0_SCL
SPI3_CLK	DAC_SPI_SCLK	13	14	DAC_SPI_PICO	SPI3_D0
SPI3_D1	DAC_SPI_POCI	15	16	DAC_SPI_PTE	SPI3_CS0

### 2.4.4 FSI Header

The HSEC180ADAPEVM-AM2 has a 10-pin Fast Serial Interface (FSI) header for interfacing with the AM261x FSI peripheral. The pinout is shown in [Table 2-4](#) below.

**Table 2-4. FSI Header (J8) Pinout**

EVM Connection	Pin	Pin	EVM Connection
FSIRX0_DATA0	1	2	FSIRX0_DATA1
FSIRX0_CLK	3	4	GND
FSITX0_DATA0	5	6	FSITX0_DATA1
FSITX0_CLK	7	8	GND
-	9	10	3V3_LDO2

For more information on the FSI implementation, see [Section 2.8.3](#).

### 2.4.5 OSPI Expansion Connector

The HSEC180ADAPEVM-AM2 has a 30-pin high density connector for connecting an external OSPI memory to interface with the OSPI1 peripheral on the AM261x MCU. The pinout is detailed in [Table 2-5](#) below:

**Table 2-5. OSPI Expansion Connector (J5)**

EVM Connection	Pin	Pin	EVM Connection
GND	1	2	3V3_LDO2
3V3_LDO2	3	4	GND
OSPI1_RESET_OUT0	5	6	OSPI1_ECC_FAIL
OSPI1_CSn0	7	8	OSPI1_CSn1
GND	9	10	OSPI1_CLK
GND	11	12	OSPI1_DQS

**Table 2-5. OSPI Expansion Connector (J5) (continued)**

EVM Connection	Pin	Pin	EVM Connection
GND	13	14	OSPI1_D0
OSPI1_D1	15	16	OSPI1_D2
OSPI1_D3	17	18	GND
OSPI1_D4	19	20	OSPI1_D5
OSPI1_D6	21	22	OSPI1_D7
GND	23	24	-
-	25	26	-
-	27	28	-
-	29	30	-

For more information, see [Section 2.8.4](#).

### 2.4.6 Ethernet Add-on Board Connector

The HSEC180ADAPEVM-AM2 has a 48-pin high-density shielded connector ([DF40GB-48DP-0.4V\(58\)](#)) for connecting a supported TI Ethernet Add-on Board, such as the [DP83826-EVM-AM2](#).

The PR0\_PRU1 instance of the AM261x PRU-ICSS core is routed to the Ethernet add-on board Connector to be used as MII Ethernet. The connector pinout is standard across TI EVMs that support Ethernet add-on boards, and is detailed in [Table 2-6](#) below.

**Table 2-6. DF40GB Header Pinout**

Pin #	AM261x EVM Connection	Ethernet Add-on Board Standard	Description	Description	Ethernet Add-on Board Standard	AM261x EVM Connection	Pin #
1	GND	GND	Ground	PMIC External Voltage Monitor	EXT_VMON	EXT_VMON2	2
3	ICSSM_MII_TXD0	TX_CLK	Transmit Clock	2.5V supply	VDD_2V5	VDD_ETH_2V5	4
5	GND	GND	Ground	2.5V supply	VDD_2V5	VDD_ETH_2V5	6
7	ICSSM_MII_TXD0	TX_D0	Transmit Data 0	Ground	GND	GND	8
9	ICSSM_MII_TXD1	TX_D1	Transmit Data 1	Interrupt To Ethernet PHY	PWDN/INTn	MII1_INTn (GPIO119)	10
11	ICSSM_MII_TXD2	TX_D2	Transmit Data 2	Reset input to Ethernet PHY	RESETn	MII0/MII1_RST	12
13	ICSSM_MII_TXD3	TX_D3	Transmit Data 3	Collision Detected	COL	ICSSM_MII1_COLL	14
15	GND	GND	Ground	Ground	GND	GND	16
17	GND	GND	Ground	Ground	GND	GND	18
19	ICSSM_MII1_RXCLK	RX_CLK	Receive Clock	MDIO Clock	MDIO_MDC	PR0_MDIO0_MD C	20
21	GND	GND	Ground	MDIO Data	MDIO_MDIO	PR0_MDIO0_MDI O	22
23	ICSSM_MII1_RXD0	RX_D0	Receive Data 0	Ground	GND	GND	24
25	ICSSM_MII1_RXD1	RX_D1	Receive Data 1	Inhibit	INH	GND	26
27	ICSSM_MII1_RXD2	RX_D2	Receive Data 2	PRUx Reference Clock	REF_CLK	PHY1_25MHZ_C LK	28
29	ICSSM_MII1_RXD3	RX_D3	Receive Data 3	Carrier Sense	CRS	ICSSM_MII1_CR S	30
31	GND	GND	Ground	Ground	GND	GND	32

**Table 2-6. DF40GB Header Pinout (continued)**

Pin #	AM261x EVM Connection	Ethernet Add-on Board Standard	Description	Description	Ethernet Add-on Board Standard	AM261x EVM Connection	Pin #
33	GND	GND	Ground	Ground	GND	GND	34
35	ICSSM_MII1_TX EN	TXEN	Transmit Enable	Board Connection Detect	BRD_CONN_DE T	3V3_LDO2	36
37	MII_EEPROM_A2	EEPROM_A2	EEPROM I2C Address bit [2]	IEEE 1588 SFD	1588_SFD	TP12	38
39	ICSSM_MII1_RX ER	RX_ER	Receive Data Error	I2C Clock	I2C_SCL	I2C0_SCL	40
41	GND	GND	Ground	I2C Data	I2C_SDA	I2C0_SDA	42
43	ICSSM_MII1_RX LINK	RX_LINK	Receive Indicator	IO Voltage Supply	VDDIO	VDDIO_3V3	44
45	ICSSM_MII1_RX DV	RXDV	Receive Data Valid	IO Voltage Supply	VDDIO	VDDIO_3V3	46
47	MII1_EEPROM_A0	EEPROM_A0	EEPROM I2C Address bit [0]	Audio Bit Clock	GPIO_2/CLKOUT	-	48

For more information, see [Section 2.8.5.2.2](#).

## 2.5 Reset

The Power-On-Reset net from the AM261x controlSOM, driven by the on-SOM push button or the AM261x SoC PORz signal is routed through SOM HD connector J1 and is tied to the reset logic for the following peripherals:

- HSEC connector
- OSPI Expansion connector reset
- PHY1 reset
- PHY2 reset
- Ethernet add-on board connector reset

PORz is ANDed with each target peripheral's dedicated reset signal to drive the reset logic for each device.

- MDIO0\_MDIO - pinmuxed with the OSPI1\_RESET\_OUT0 signal from the AM261x SoC, routed through SOM HD connector J2 and passed through a resistor mux.

### Note

The resistor to route OSPI1\_RESET\_OUT0 to the OSPI Expansion Connector is DNI by default, and must be populated for the reset signal to route to the OSPI Expansion Connector.

- RGMII1\_RST - AM261x controlSOM IO Expander output, input to reset logic for the RGMII1 PHY (PHY1)
- MII\_RST# - AM261x controlSOM IO Expander output, input to reset logic for the MII0 PHY (PHY1) and Ethernet add-on Board Connector

[Figure 2-6](#) shows the reset architecture of the HSEC180ADAPEVM-AM2.

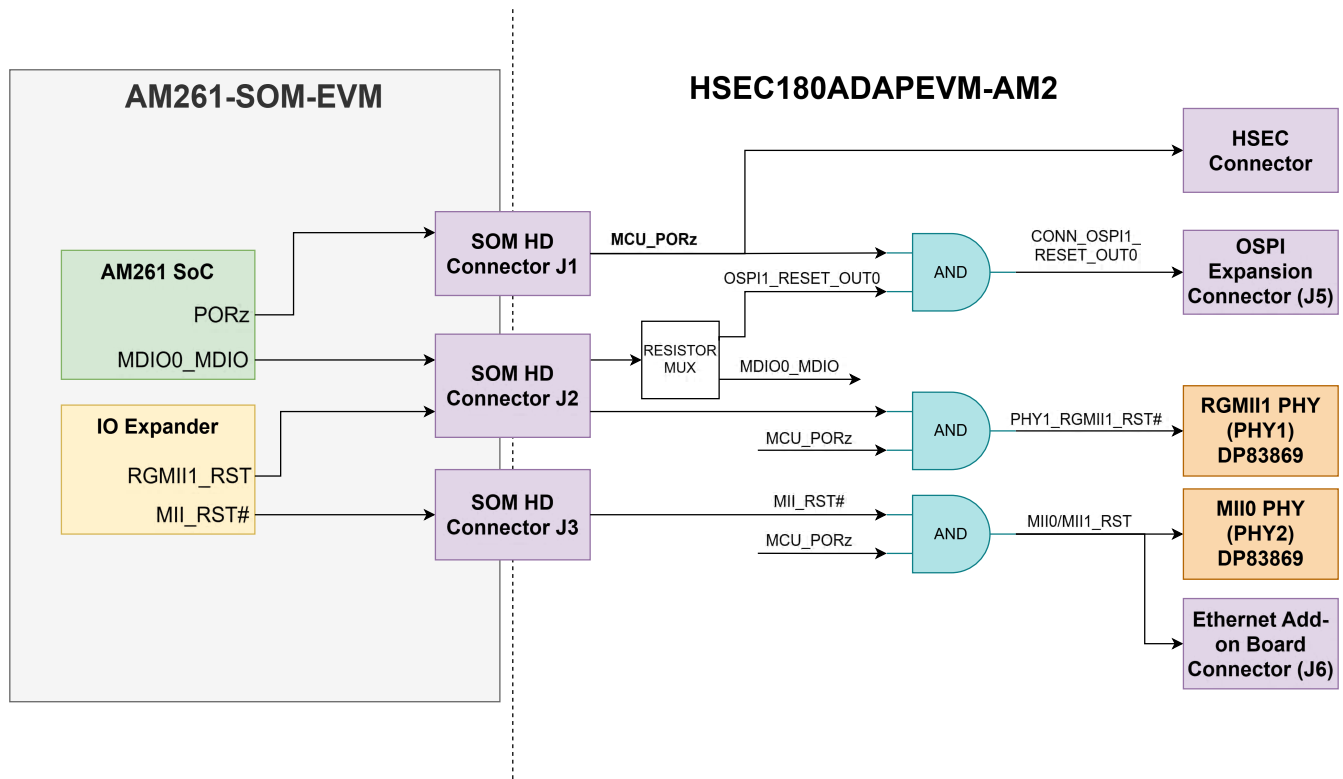


Figure 2-6. HSEC180ADAPEVM-AM2 Reset Architecture

## 2.6 Clock

The Ethernet peripheral clocking scheme is sourced from the clock buffer IC on the AM261x controlSOM. Three 25MHz clock outputs from the clock buffer are routed through the SOM HD connectors to their target on the HSEC180ADAPEVM-AM2. The RGMII PHY, MII0 PHY, and Ethernet add-on board connector each have their own independent 25MHz clock lines. [Figure 2-7](#) details the clock tree on the HSEC180ADAPEVM-AM2.

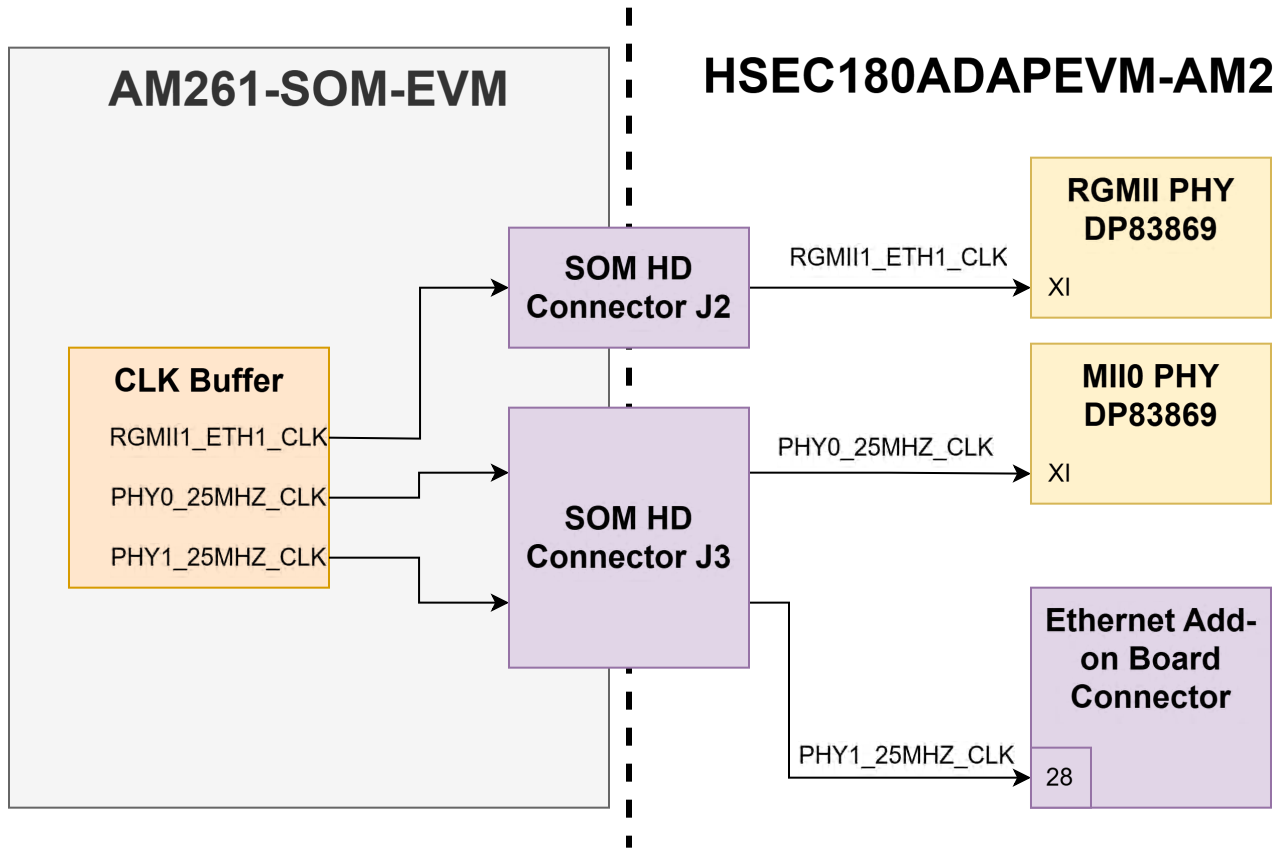


Figure 2-7. HSEC180ADAPEVM-AM2 Clock Tree

## 2.7 GPIO Mapping

Table 2-7. GPIO Mapping Table - Rev E1

GPIO	GPIO Description	Pin Name	Functionality	Net Name	Active Status	SOM HD Connector Pin	Baseboard/Adapter Board Usage
GPIO66	Reset to OSPI flash device	GPIO66	Reset	OSPI0_RESET_OUTn	LOW		
GPIO138	Resistor option between GPIO and PMIC_DIAG_OUT	CLKOUT0	GPIO	MCU_GPIO138	PREFERABLE	J1-74	Default PMIC_DIAG_OUT. Remove R84 and populate R138 to use as GPIO.
GPIO65	Error signal from OSPI flash device	GPIO65	Error Signal	OSPI0_ECS	LOW		
GPIO1	USER_LED1	OSPI0_CSn1	GPIO	MCU_GPIO1	PREFERABLE	J1-52	Default USER_LED_OUT. Remove R140 and populate R237 to use as GPIO.
GPIO82	Select line for I2C1/MCAN1 Mux, terminated to SOM HD Connector	MMC0_D3	Mux Select	MCU_GPIO82	PREFERABLE	J1-48	GPIO. Left floating on HSEC180ADAPEVM-AM2
GPIO73	Terminated to SOM HD Connector	PR1_PRU1_GPIO2	GPIO	MCU_GPIO73	PREFERABLE	J1-75	Interrupt signal for MII0 on HSEC180ADAPEVM-AM2
GPIO119	Terminated to SOM HD Connector	PR0_PRU1_GPIO19	GPIO	MCU_GPIO119	PREFERABLE	J3-66	Interrupt signal for MII1 on HSEC180ADAPEVM-AM2
GPIO128	SoC interrupt signal from push button SW3	SDFM0_CLK3	Interrupt	MCU_INTn	LOW		
GPIO126	Terminated to SOM HD Connector	SDFM0_CLK2	GPIO	MCU_GPIO126	PREFERABLE	J1-73	GPIO
GPIO71	Terminated to SOM HD Connector	PR1_PRU1_GPIO0	Interrupt	RGMI11_INTn	LOW	J2-7	Interrupt signal for RGMI11 on HSEC180ADAPEVM-AM2
GPIO37	Terminated to SOM HD Connector	RGMI11_TD0	GPIO	RGMI11_TD0	PREFERABLE	J2-8	RGMI11 Transmit Data 0 on HSEC180ADAPEVM-AM2
GPIO121	Resistor option between SOM HD Connector and PMIC_INTn	EXT_REFCLK0	GPIO	MCU_GPIO121	PREFERABLE	J1-70	Default PMIC_INTn. Remove R311 and populate R312 to use as GPIO.
GPIO124	Resistor option between USER_LED0 and SOM HD Connector	SDFM0_CLK1	GPIO	MCU_GPIO124	PREFERABLE	J1-72	Default USER_LED0. Remove R215 and populate R214 to use as GPIO.
GPIO74	Terminated to SOM HD Connector	PR1_PRU1_GPIO9	GPIO	MCU_GPIO74	PREFERABLE	J2-25	MDIO & MDC MUX select line on HSEC180ADAPEVM-AM2
GPIO21	Connection for USB_DRVVBUS	LIN2_RXD	GPIO	AM26x_UART2_RXD	PREFERABLE	J2-26	USB_DRVVBUS
GPIO22	Connection for USB0_VBUS_OC	LIN2_TXD	GPIO	AM26x_UART2_TXD	LOW	J2-28	USB0_VBUS_OC
<b>IO Expander</b>							
	Select line for PMIC SPI MUX/ DEMUX (U24)	P0	Mux Select	PMIC_SPI1/ FSIRX0_MUX_SEL	PREFERABLE		



**Table 2-7. GPIO Mapping Table - Rev E1 (continued)**

GPIO	GPIO Description	Pin Name	Functionality	Net Name	Active Status	SOM HD Connector Pin	Baseboard/Adapter Board Usage
	Select line for ADC0_AIN0/ DAC_OUT MUX (U20)	P1	Mux Select	ADC0_AIN0/ DAC_OUT_MUX_SE L	PREFERABLE		
	MII Reset	P2	Reset	MII_RST#	LOW	J3-101	Reset signal for MII0 and MII1 on HSEC180ADAPEVM-AM2
	RGMII1 Reset	P3	Reset	RGMII1_RST	LOW	J2-11	Reset signal for RGMII1 on HSEC180ADAPEVM-AM2
	Select line for SPI0-FSI MUX/ DEMUX (U13)	P4	Mux Select	SPI0/ FSITX0_MUX_SEL	PREFERABLE		
	Select line for SPI3 MUX/DEMUX (U18)	P5	Mux Select	SPI3_MUX_SEL	PREFERABLE		
	Select line for HSEC180ADAPEVM- AM2 MII0 Mux	P6	Mux Select	IOEXP_OUT_P6	PREFERABLE	J2-5	MII0 Mux select line on HSEC180ADAPEVM-AM2
	Select line for HSEC180ADAPEVM- AM2 MII1 Mux	P7	Mux Select	IOEXP_OUT_P7	PREFERABLE	J2-9	MII1 Mux select line on HSEC180ADAPEVM-AM2

## 2.8 Interfaces

### 2.8.1 USB

The HSEC180ADAPEVM-AM2 has one USB2.0 interface connected to the USB0 peripheral on the AM261x MCU. On the AM261x controlSOM, the USB signals are routed from the MCU to the SOM HD Connector J2.

On the SOM to HSEC adapter board, the USB0\_DM and USB0\_DP nets are routed to a common mode choke to reduce noise on the high-speed USB signal bus. The nets are passed through a TPD4E02B04 ESD protection diode, and are terminated at a Micro-USB receptacle. Figure 2-8 details the USB implementation on the HSEC180ADAPEVM-AM2.

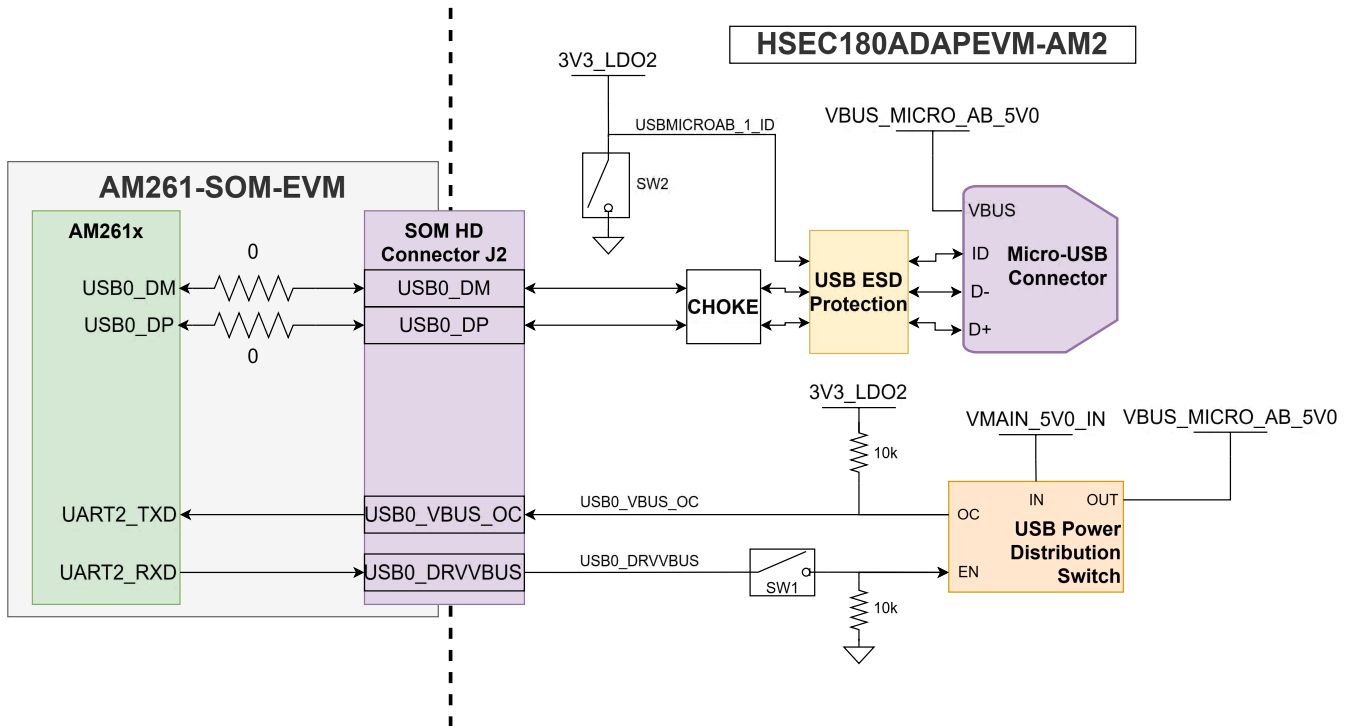


Figure 2-8. HSEC180ADAPEVM-AM2 USB Interface

The USB mode of operation is controlled using a set of DIP switches - SW1 and SW2. The setting of the DIP switches determines the USB mode of operation, and is detailed in Table 2-8 below.

Table 2-8. USB Mode Switch Settings

SW1 (USB0_DRVVBUS)	SW2 (USBMICROAB_ID)	USB Mode
OFF / RIGHT (TPS2051B disabled)	ON / RIGHT (3V3)	Device Mode
ON / LEFT (TPS2051B enabled)	OFF / LEFT (GND)	Host Mode

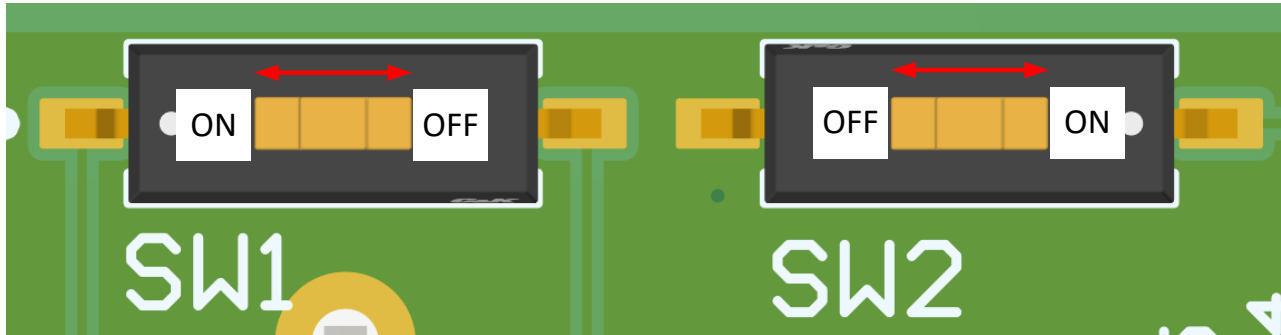


Figure 2-9. SW1/SW2 Positions

### USB Device Mode

When using the AM261x device in USB device mode, the VBUS pin of the Micro-USB receptacle is used to detect when voltage has been applied to or removed from the USB connector. Software running on the AM261x manages the internal USB PHY according to the presence of 5V or 0V on the VBUS pin.

### USB Host Mode

When using the AM261x device in USB Host mode, 5V on the VBUS pin of the Micro-USB receptacle is required. On the HSEC180ADAPEVM-AM2, this supply is generated using a TPS2051B USB Power Distribution switch which sources the main 5V system input from the HSEC connector and supplies a separate 5V input for the USB bus. As shown in Table 2-8 above, SW1 must be set to ON to enable the TPS2051B USB Power Distribution switch, and SW2 must be OFF to indicate that the device is set to USB Host mode. SW1 controls the state of the USB0\_DRVVBUS net, which is connected to a dedicated USB0\_DRVVBUS pin on the AM261x MCU and drives the enable pin on the TPS2051B. The OC pin of the TPS2051B is an active low, open-drain output that occurs when an overcurrent or overtemperature shutdown condition is detected. The USB0\_VBUS\_OC net is connected to the UART2\_TXD pin on the AM261x MCU and is configured as a GPIO for this use case.

### 2.8.2 UART

One instance of the UART peripheral is routed from the SOM HD Connector J1 to the Emulation header (J4) and the HSEC connector.

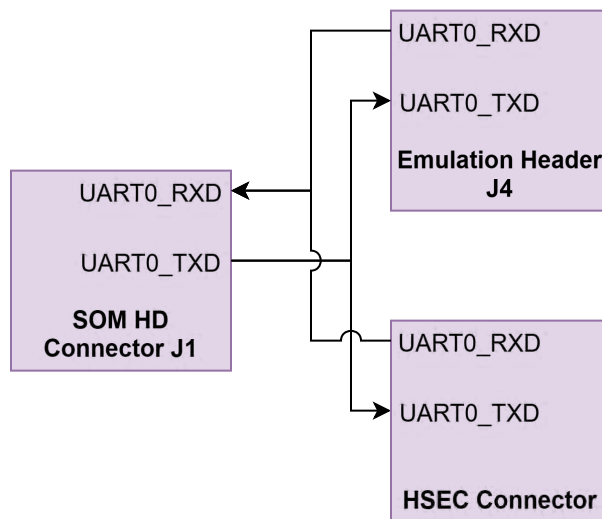


Figure 2-10. HSEC180ADAPEVM-AM2 UART Interface

The XDS110ISO-EVM uses its on-board XDS110 emulator as a USB2.0 to UART bridge for terminal access. The UART0 transmit and receive signals of the AM261x SoC are mapped to SOM HD Connector J1 to connect to the XDS110ISO-EVM via J4 when mated to the HSEC180ADAPEVM-AM2.

### 2.8.3 FSI

The AM261x SOM to HSEC adapter provides a 10-pin header for interfacing with the AM261x MCU Fast Serial Interface (FSI) peripheral. The interface has two lines of data and a clock line for both the receive and transmit signals.

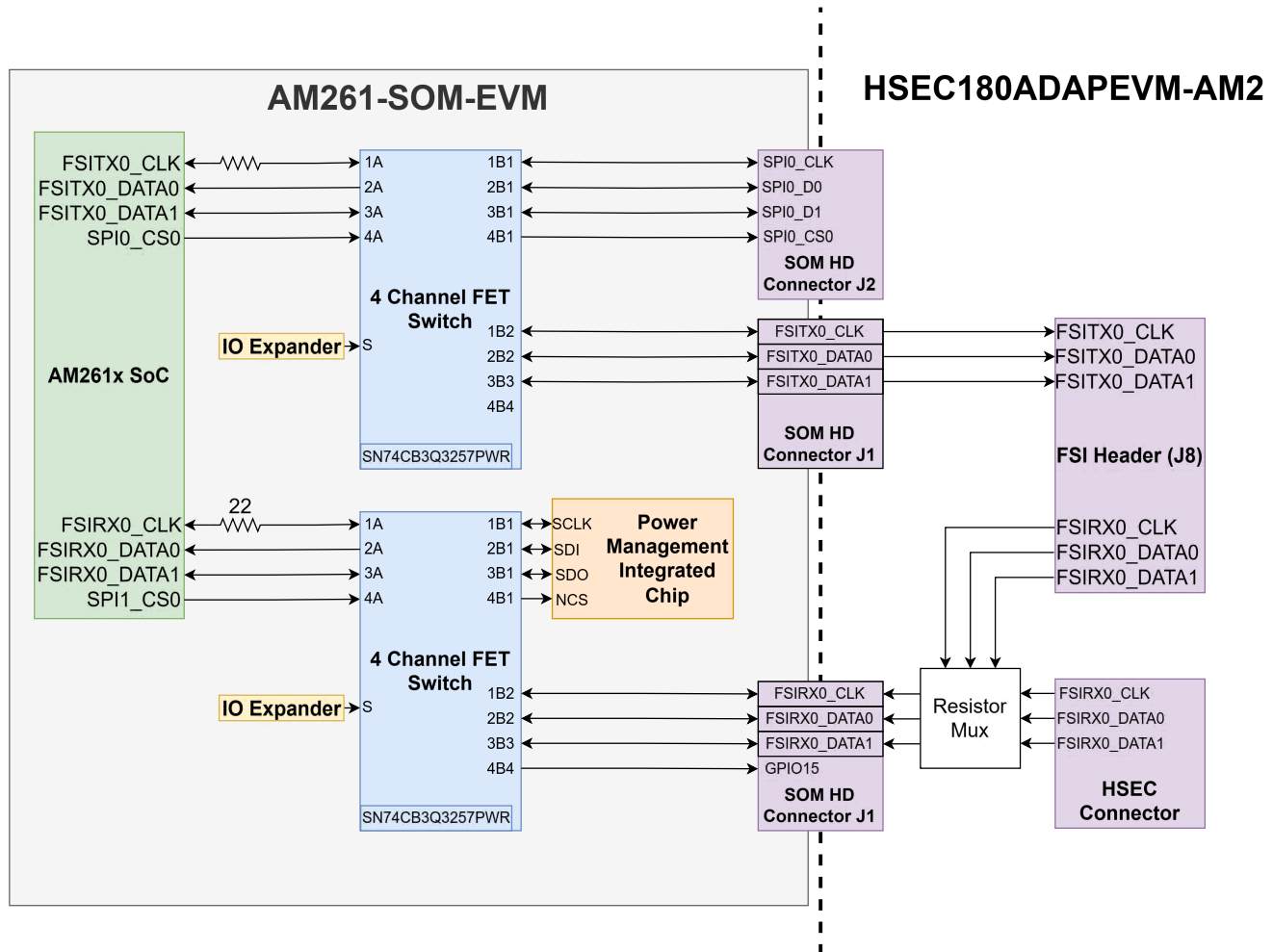


Figure 2-11. HSEC180ADAPEVM-AM2 FSI Interface

The FSIRX signals are passed through a resistor mux, routing the FSIRX signals to either the dedicated FSI header (J8) or the HSEC connector. The FSITX signals are directly connected to the dedicated FSI header (J8)

#### Note

On the AM261x controlSOM, FSI TX signals go through a 4-bit 1:2 signal routing mux. There is a pull-down resistor on the select line of the mux, which does not route FSI as the default selection. To use FSI, the SPI0/FSITX0\_MUX\_SEL GPIO from the IO expander must be configured as a logic high output. In addition, the FSI RX signals go through a separate 4-bit 1:2 signal routing mux. There is a pull-down resistor on the select line of the mux, which does not route FSI as the default selection. To use FSI, the PMIC\_SPI1/FSIRX0\_MUX\_SEL GPIO from the IO expander must also be configured as a logic high output.

### 2.8.4 OSPI

The OSPI1 instance of the AM261x OSPI peripheral is routed to a 30-pin high density connector on the HSEC180ADAPEVM-AM2. Compatible OSPI add-on boards can be connected to the SOM to HSEC adapter board for interfacing with the AM261x MCU on the AM261x controlSOM.

Figure 2-12 shows the connections between the RGMII1 signals routed from the SOM HD connectors, the resistor muxing scheme, and connection to the OSPI expansion header. The OSPI1 reset logic is determined by the output of an AND gate with inputs PORz and OSPI1\_RESET\_OUT0.

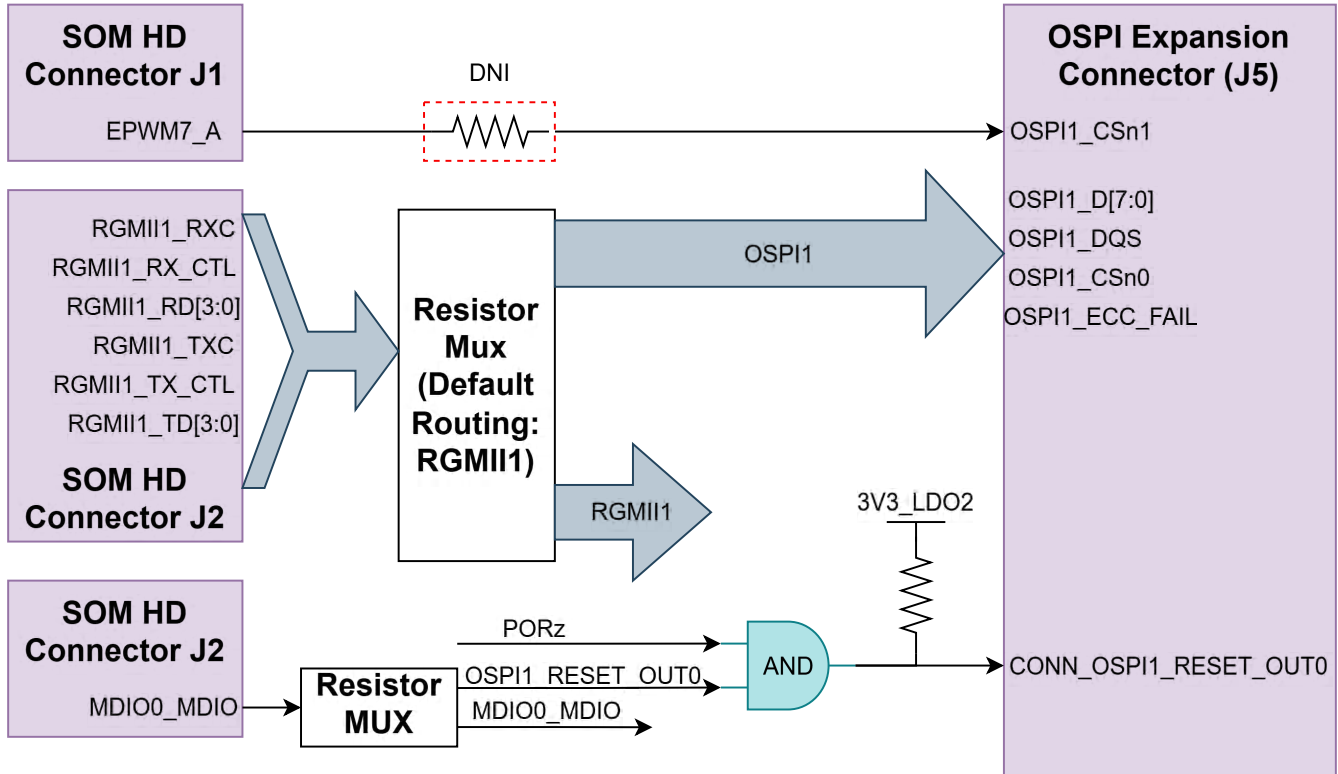


Figure 2-12. HSEC180ADAPEVM-AM2 OSPI Interface

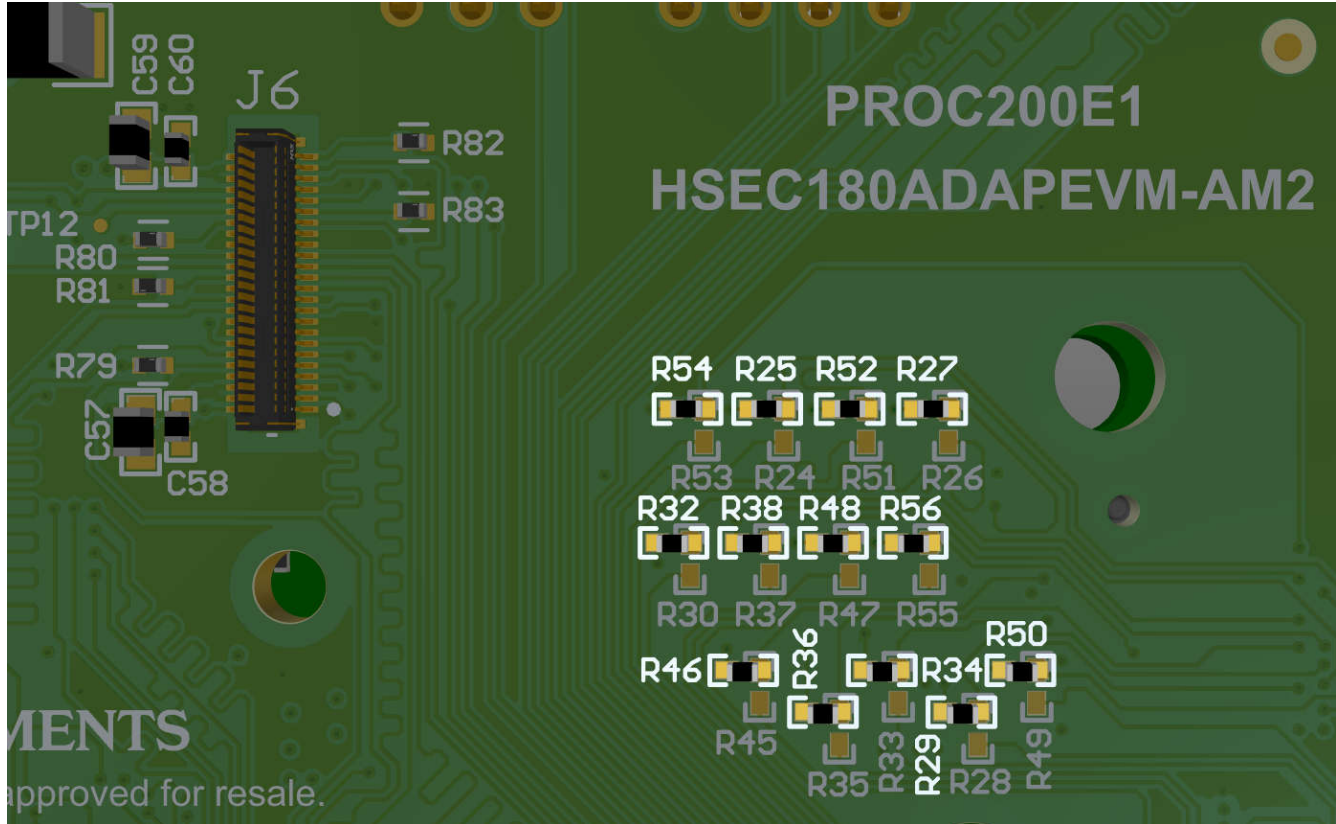
The majority of the OSPI1 signals are pinmuxed with the RGMII signals on the AM261x MCU. The OSPI1\_CSn1 signal is pinmuxed with EPWM7\_A. In order to enable OSPI1 and route the OSPI1 nets to the OSPI Expansion connector, the following resistor modifications must be made:

Table 2-9. OSPI1 Resistor Mods

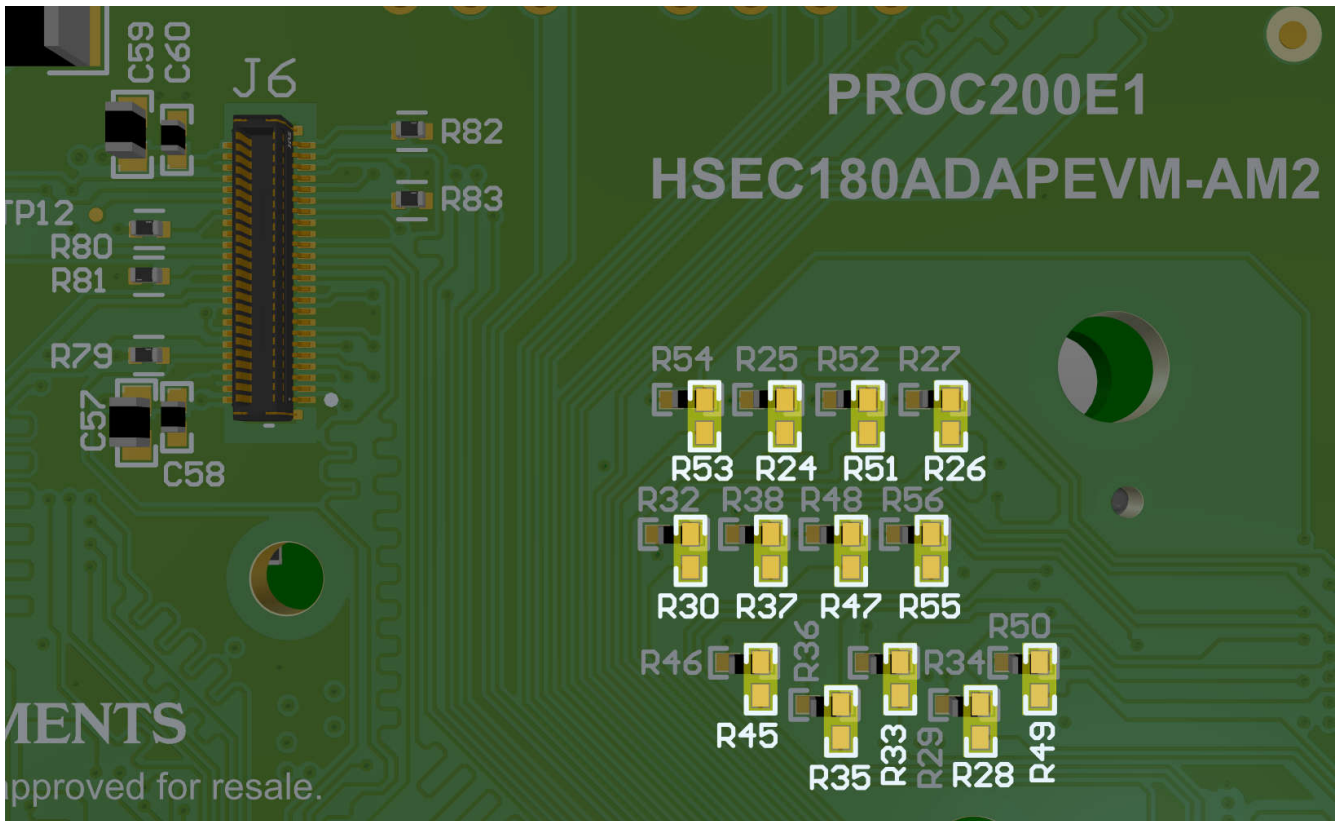
AM261x Signal	Pinmuxed OSPI1 Signal	DNI Resistor	Populate Resistor
RGMII1_RXC	OSPI1_CLK	R25	R24
RGMII1_RX_CTL	OSPI1_D0	R27	R26
RGMII1_RD0	OSPI1_D1	R29	R28
RGMII1_RD1	OSPI1_D2	R32	R30
RGMII1_RD2	OSPI1_D3	R34	R33
RGMII1_RD3	OSPI1_D4	R36	R35
RGMII1_TXC	OSPI1_D5	R38	R37
RGMII1_TX_CTL	OSPI1_D6	R46	R45
RGMII1_TD0	OSPI1_D7	R48	R47
RGMII1_TD1	OSPI1_CSn0	R50	R49
RGMII1_TD2	OSPI1_DQS	R52	R51

**Table 2-9. OSPI1 Resistor Mods (continued)**

AM261x Signal	Pinmuxed OSPI1 Signal	DNI Resistor	Populate Resistor
RGMII1_TD3	OSPI1_ECC_FAIL	R54	R53
MDIO0_MDIO	OSPI1_RESET_OUT0	R56	R55
EPWM7_A	OSPI1_CSn1 <sup>1</sup>	-	R31



**Figure 2-13. OSPI1 - DNI Resistors**



**Figure 2-14. OSPI1 - Install Resistors**

## 2.8.5 Ethernet

### 2.8.5.1 RGMII

One port of RGMII signals is routed from the AM261x controlSOM to the HSEC180ADAPEVM-AM2 to a 48-pin DP83869 gigabit Ethernet PHY, and terminated at a RJ45 connector.

The DP83869 PHY is configured to advertise 1Gb operation. The RJ45 connector is used for 10/100/1000 Mbps Ethernet connectivity with integrated magnets and LEDs for link and activity indication.





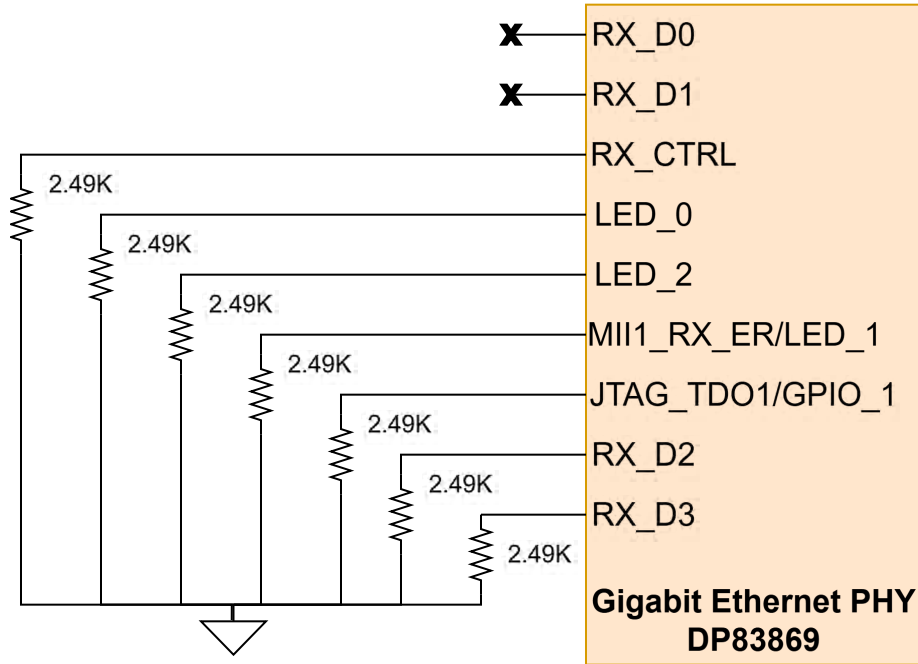


Figure 2-16. DP83869 RGMII1 PHY Strapping Resistors

Table 2-10. DP83869 RGMII1 Gigabit Ethernet PHY Strapping Resistors

Functional Pin	Default Mode	Mode on HSEC180ADAPEVM-AM2	Function
RX_D0	0	0	PHY address: 0000
RX_D1	0	0	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
LED_0	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port mirroring disabled

### RJ45 Connector LED Indications

The RJ45 receptacle connected to the DP83869 PHY contains two bi-color LEDs that are used to indicate link and activity.

Table 2-11. CPSW/RGMII1 RJ45 Receptacle LED Indication

RJ45 LED	Color	Indication
Right LED	GREEN	Ethernet PHY power established
	YELLOW	Transmit or Receive activity
Left LED	GREEN	Link OK
	YELLOW	1000BT link is up

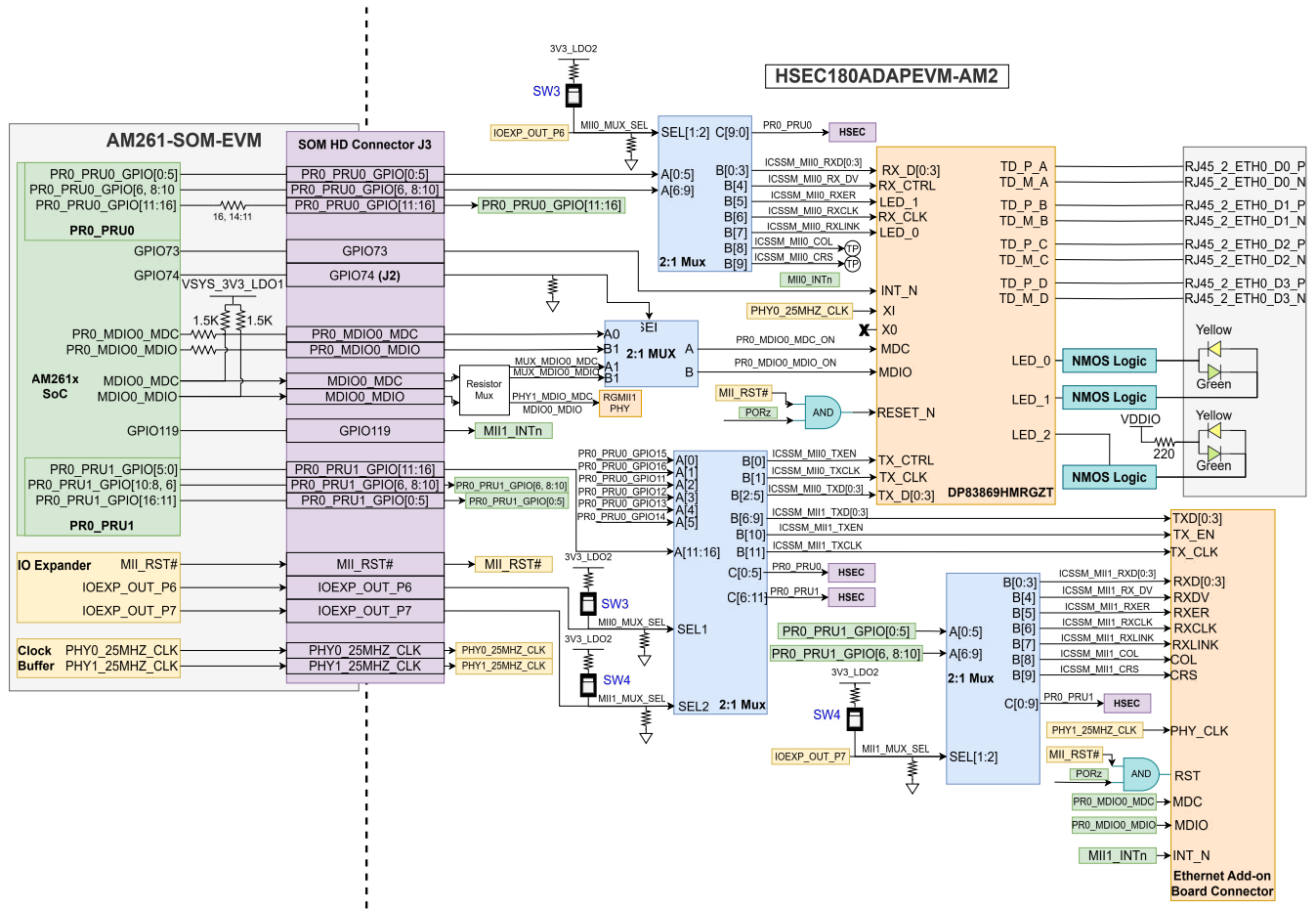
### 2.8.5.2 PRU-ICSS

The AM261x controlSOM routes two instances of the AM261x MCU on-die programmable real-time unit and industrial communication subsystem (PRU-ICSS) to the SOM HD connectors. On the HSEC180ADAPEVM-AM2,

there are two external Ethernet ports - one on-board gigabit Ethernet PHY transceiver (DP83869), and one Ethernet add-on board connector. The gigabit Ethernet PHY is connected to the PR0\_PRU0 core of the PRU-ICSS, and the Ethernet add-on board interface is connected to the PR0\_PRU1 core of the PRU-ICSS. [Table 2-12](#) details the protocols supported at each Ethernet port interface:

**Table 2-12. PRU-ICSS Ethernet Protocols**

AM261x PRU-ICSS Core	On-board Peripheral / Speed	External Interface	Supported Protocols
PR0_PRU0	<ul style="list-style-type: none"> <li>DP83869 gigabit PHY</li> <li>10/100/1000 Mbps</li> </ul>	RJ45	<ul style="list-style-type: none"> <li>PRU-ICSS RGMII/MII</li> <li>CPSW RGMII/MII</li> </ul>
PR0_PRU1	<ul style="list-style-type: none"> <li>Ethernet add-on board connector</li> <li>10/100/1000 Mbps</li> </ul>	Ethernet add-on board	<ul style="list-style-type: none"> <li>PRU-ICSS RGMII/MII</li> </ul>



**Figure 2-17. HSEC180ADAPEVM-AM2 PRU-ICSS Ethernet Implementation**

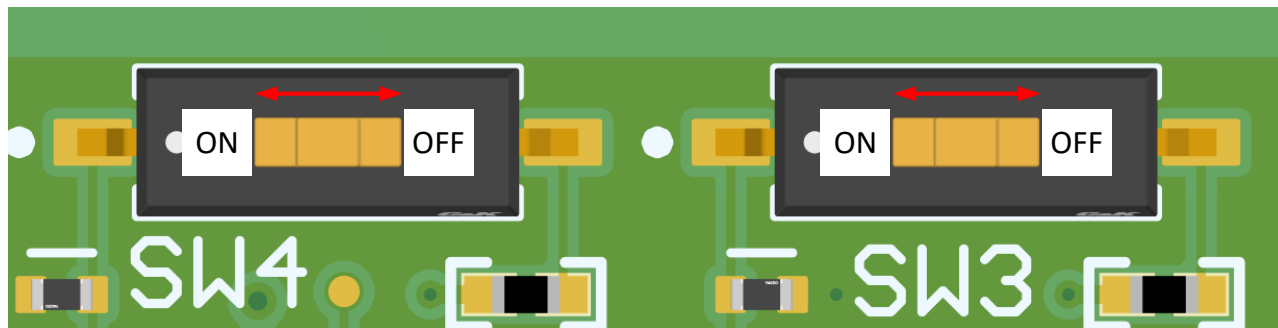
The Ethernet data signals of the DP83869 PHY are terminated to a RJ45 connector. The RJ45 connector supports Ethernet speeds of 10/100/1000 Mbps connectivity and has integrated magnets and LEDs for link and activity indication.

There are a series of multiplexers on the paths of the PRU-ICSS nets from the SOM HD connectors to their external interfaces. 3 high-speed, 12-channel switches (TS3DDR3812) control the routing of the PR<sub>x</sub> PRU<sub>x</sub> GPIO<sub>x</sub> signals to either the Ethernet interfaces or to the HSEC connector. The select lines for the muxes are software controlled by two output signals configured by the on-SOM IO Expander, or hardware controlled by the on-board switches (SW3 and SW4) on the HSEC180ADAPEVM-AM2. An additional mux selects which set of MDIO signals is routed to the DP83869 PHY, and is dependent on which protocol is being

used on the DP83869 - CPSW RGMII or PRU MII. The select line of this mux is controlled by AM261x GPIO74, which is routed from the MCU to the HSEC180ADAPEVM-AM2 through SOM HD connector J2. [Table 2-13](#) shows the mux configurations. [Figure 2-18](#) shows the mux select switches.

**Table 2-13. PRU-ICSS Signal Routing**

AM261x PRU-ICSS Core	Destination	Protocol	MII0_MUX_SEL (SW3)	MII1_MUX_SEL (SW4)	MDIO/MDC MUX SEL
			Controlled by controlSOM IO Expander OR on-board DIP Switches		Controlled by AM261x GPIO74
PR0_PRU0	DP83869 PHY	CPSW RGMII2	LOW / RIGHT (default)	LOW / RIGHT (default)	HIGH (AM261x SoC MDIO0 signals)
	DP83869 PHY	PRU MII0	LOW / RIGHT (default)	LOW / RIGHT (default)	LOW (default) (PRU MDIO0 signals)
	HSEC	CPSW RGMII	HIGH / LEFT	HIGH / LEFT	HIGH (AM261x SoC MDIO0 signals)
	HSEC	PRU MII0	HIGH / LEFT	HIGH / LEFT	LOW (default) (PRU MDIO0 signals)
PR0_PRU1	Ethernet Add-on Board Connector	PRU MII1	LOW / RIGHT (default)	LOW / RIGHT (default)	X
	HSEC	PRU MII1	HIGH / LEFT	HIGH / LEFT	X



**Figure 2-18. SW3/SW4 Positions**

### 2.8.5.2.1 On-Board PHY

The on-board DP83869 gigabit Ethernet PHY has the following hardware connections, shown in [Figure 2-19](#) and detailed in [Table 2-14](#).

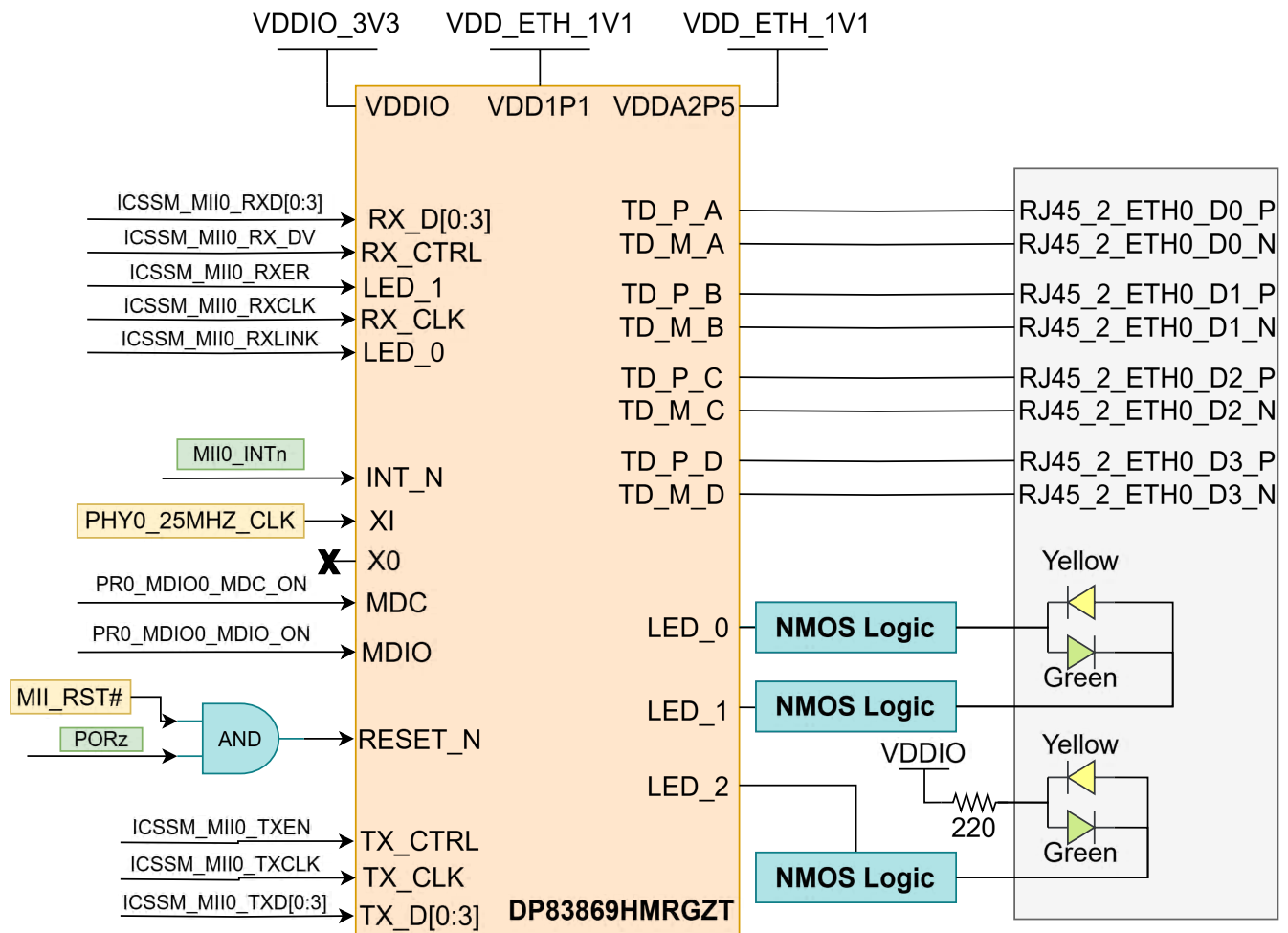


Figure 2-19. HSEC180ADAPEVM-AM2 On-Board PRU-ICSS PHY

Table 2-14. DP83869 Hardware Connections

DP83869 Pin	AM261x / controlSOM Pin Source	HSEC180ADAPEVM Net	Notes
RX_D[0:3]	PR0_PRU0_GPIO[0:3]	ICSSM_MII0_RXD[0:3]	
RX_CTRL/RX_DV	PR0_PRU0_GPIO4	ICSSM_MII0_RX_DV	
LED1/RX_ER	PR0_PRU0_GPIO5	ICSSM_MII0_RXER	
RX_CLK	PR0_PRU0_GPIO6	ICSSM_MII0_RXCLK	
LED_0	PR0_PRU0_GPIO8	ICSSM_MII0_RXLINK	
TX_CTRL/TX_EN	PR0_PRU0_GPIO15	ICSSM_MII0_TXEN	
TX_CLK	PR0_PRU0_GPIO16	ICSSM_MII0_TXCLK	
TX_D[0:3]	PR0_PRU0_GPIO[11:14]	ICSSM_MII0_TXD[0:3]	
MDC	Output of MDIO/MDC Mux	PR0_MDIO0_MDC_ON	See Table 2-13
MDIO	Output of MDIO/MDC Mux	PR0_MDIO0_MDIO_ON	See Table 2-13.
INT_N	GPIO73	MII0_INTn	
XI	PHY0_25MHZ_CLK	PHY0_25MHZ_CLK	Output of Clock Buffer IC on AM261x controlSOM

Table 2-14. DP83869 Hardware Connections (continued)

DP83869 Pin	AM261x / controlSOM Pin Source	HSEC180ADAPEVM Net	Notes
RESET_N	Output of MII_RST# AND PORz	MII0/MII1_RST	MII_RST# net sourced from IO Expander on AM261x controlSOM

The DP83869 PHY requires three separate power sources. VDDIO (3.3V) is the output of the on-board load switch, which uses the 3.3V system IO voltage as its input. The other two PHY power inputs - VDD1P1 and VDDA2P5 - are generated from on-board LDOs. For more on the system power, see [Section 2.3](#).

### Strapping Resistors

The DP83869 Ethernet PHY uses several functional pins as strap options to place the PHY into specific modes of operation. Each functional pin has a default mode that is driven by an internal pull resistor.

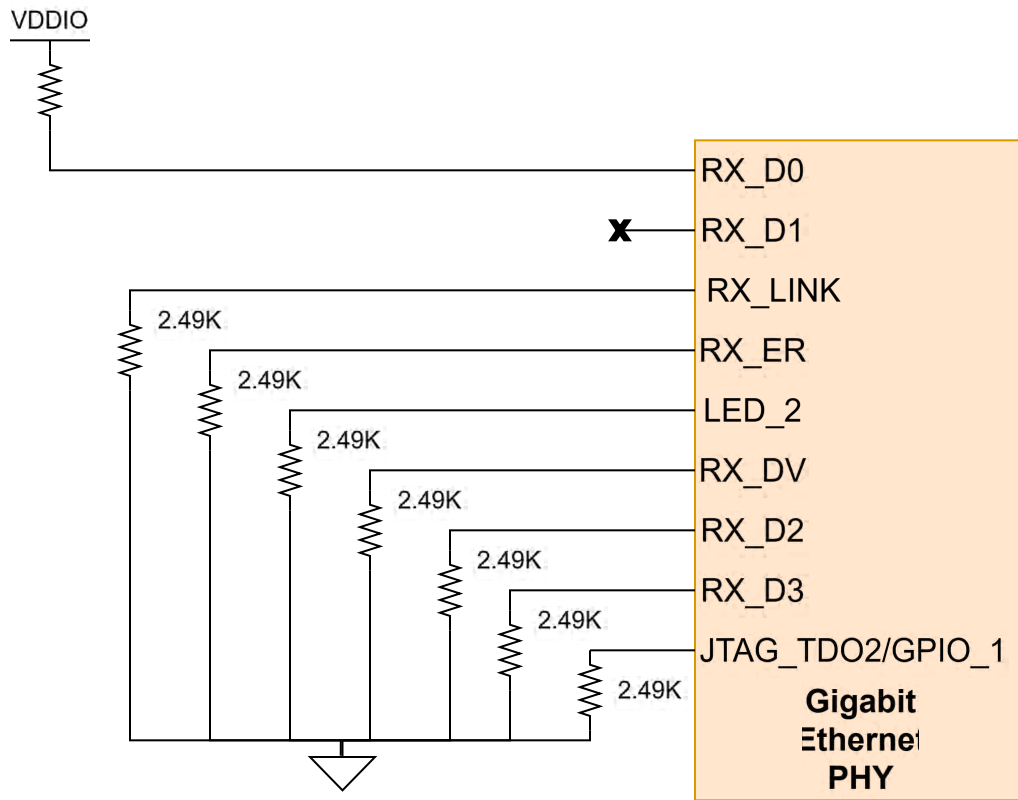


Figure 2-20. DP83869 PHY Strapping Resistors

Table 2-15. PR0\_PRU0 ICSS Gigabit Ethernet PHY Strapping Resistors

Functional Pin	Default Mode	Mode on HSEC180ADAPEVM-AM2	Function
RX_D0	0	3	PHY address: 0011
RX_D1	0	0	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	

**Table 2-15. PR0\_PRU0 ICSS Gigabit Ethernet PHY Strapping Resistors (continued)**

Functional Pin	Default Mode	Mode on HSEC180ADAPEVM-AM2	Function
LED_0	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port mirroring disabled

### RJ45 Connector LED Indications

The RJ45 receptacle connected to the DP83869 PHY contains two bi-color LEDs that are used to indicate link and activity.

**Table 2-16. PR0\_PRU0 ICSS RJ45 Receptacle LED Indication**

RJ45 LED	Color	Indication
Right LED	GREEN	Ethernet PHY power established
	YELLOW	Transmit or Receive activity
Left LED	GREEN	Link OK
	YELLOW	1000BT link is up

#### 2.8.5.2.2 Ethernet Add-on Board

There is one Ethernet Add-on Board Connector on the HSEC180ADAPEVM-AM2 for connecting compatible TI Ethernet Add-on Boards. The primary Ethernet Add-on Board for this EVM system is the [DP83826-EVM-AM2](#). Visit the tool page for more information.

To connect the HSEC180ADAPEVM-AM2 to the Ethernet add-on board, attach the receptacle on the bottom side of the add-on board to J6 on the HSEC180ADAPEVM-AM2. Use the screws and spacers included in the Ethernet add-on board kit to securely mount the two boards together. The connected board assembly is shown in [Figure 2-21](#).

**Figure 2-21. HSEC180ADAPEVM-AM2 + Ethernet Add-on Board Connection**

The AM261x PR0\_PRU1 core is connected to the Ethernet Add-on Board Connector. The full pinout details of the connector can be found in [Section 2.4.6](#). The hardware connections between the AM261x controlSOM + HSEC180ADAPEVM-AM2 system and the connector are shown in [Figure 2-22](#) and detailed in [Table 2-17](#) below:

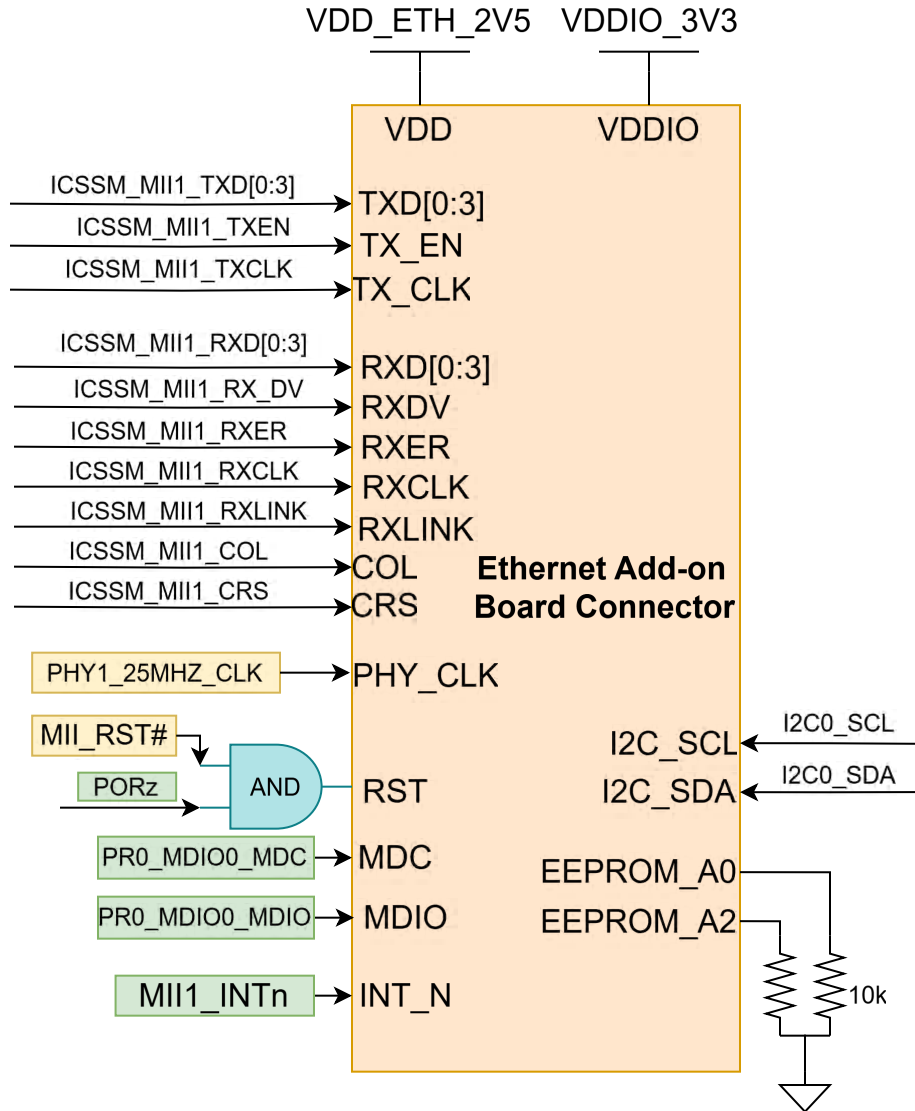


Figure 2-22. HSEC180ADAPEVM-AM2 Ethernet Add-on Board Interface

Table 2-17. Ethernet Add-on Board Hardware Connections

Ethernet Add-on Board Pin	AM261x / controlSOM Pin Source	HSEC180ADAPEVM Net	Notes
RX_D[0:3]	PR0_PRU1_GPIO[0:3]	ICSSM_MII1_RXD[0:3]	
RXDV	PR0_PRU1_GPIO4	ICSSM_MII1_RX_DV	
RX_ER	PR0_PRU1_GPIO5	ICSSM_MII1_RXER	
RX_CLK	PR0_PRU1_GPIO6	ICSSM_MII1_RXCLK	
RX_LINK	PR0_PRU1_GPIO8	ICSSM_MII1_RXLINK	
TXEN	PR0_PRU1_GPIO15	ICSSM_MII1_TXEN	
TX_CLK	PR0_PRU1_GPIO16	ICSSM_MII1_TXCLK	
TX_D[0:3]	PR0_PRU1_GPIO[11:14]	ICSSM_MII1_TXD[0:3]	

**Table 2-17. Ethernet Add-on Board Hardware Connections (continued)**

Ethernet Add-on Board Pin	AM261x / controlSOM Pin Source	HSEC180ADAPEVM Net	Notes
MDC	PR0_MDIO0_MDC	PR0_MDIO0_MDC	
MDIO	PR0_MDIO0_MDIO	PR0_MDIO0_MDIO	
INT_N	GPIO119	MII1_INTn	
REF_CLK	PHY1_25MHZ_CLK	PHY1_25MHZ_CLK	Output of Clock Buffer IC on AM261x controlSOM
RESET_N	Output of MII_RST# AND PORz	MII0/MII1_RST	MII_RST# net sourced from IO Expander on AM261x controlSOM

The I2C address of the Ethernet Add-on Board EEPROM is determined by on-board pull resistors that connect to the address pins of an EEPROM on a Ethernet Add-on Board when connected to the HSEC180ADAPEVM-AM2. These address pins also drive a FET network on the Ethernet Add-on Board that determine the PHY's address. All Ethernet add-on boards in the TI Ethernet Add-on Board Ecosystem follow the same addressing convention. Because the HSEC180ADAPEVM-AM2 only has a single connector, the CONNECTOR\_0 addressing is followed:

**Table 2-18. CONNECTOR\_0 I2C / PHY Addressing Scheme**

Connector_#	EEPROM_A2 (connector pin 37)		EEPROM_A1		EEPROM_A0 (connector pin 47)		I2C Address	PHY Address
	Pull	A2	Pull	A1	Pull	A0		
CONNECTOR_0	GND	0	VDDIO	1	GND	0	0x52	Ethernet add-on board dependent

The PHY address is dependent on which Ethernet add-on board is being used, since different PHYs have different address configurations. To determine the PHY address for a specific Ethernet Add-on Board, see the Add-on Board's User Guide and find the *Multi-Connector Addressing* section in the document.

### 2.8.6 I2C

Two instances of the AM261x I2C peripheral are routed from the SOM HD connectors to various target devices/destinations on the HSEC180ADAPEVM-AM2.



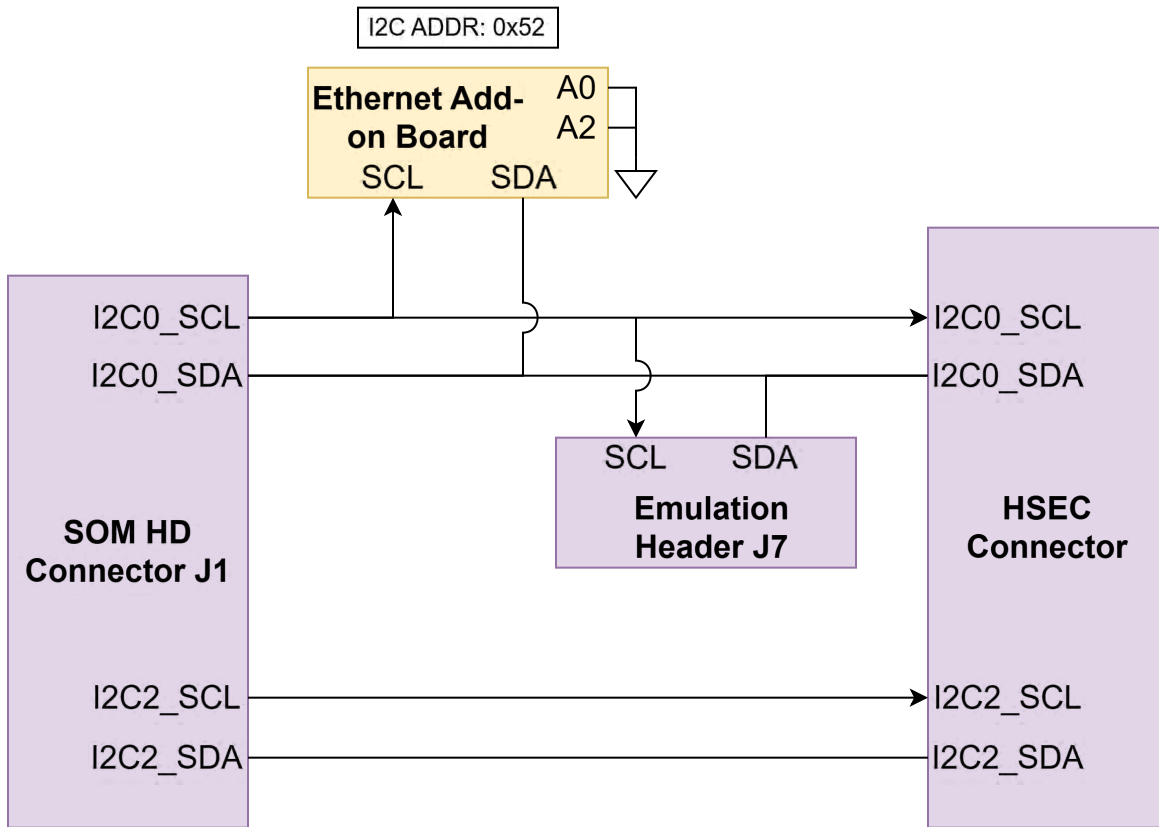


Figure 2-23. HSEC180ADAPEVM-AM2 I2C Interface

Table 2-19 details the I2C peripheral connections.

Table 2-19. I2C Devices and Destinations

Target	I2C Instance	Description	I2C Address
HSEC Connector	I2C0	HSEC Connector pins 92 (SDA), 93 (SCL)	
	I2C2	HSEC Connector pins 85 (SDA), 87 (SCL)	
Emulation Header (J4)	I2C0	Allows XDS110 device on XDS110ISO-EVM to read Board ID EEPROM on AM261x controlSOM	
Ethernet Add-on Board Connector	I2C0	Ethernet Add-on Board EEPROM connection	0x52

### 2.8.7 SPI

Two instances of SPI are routed to the HSEC180ADAPEVM-AM2 from the AM261x controlSOM through SOM HD connector J2 (SPI0) and J1 (SPI3).

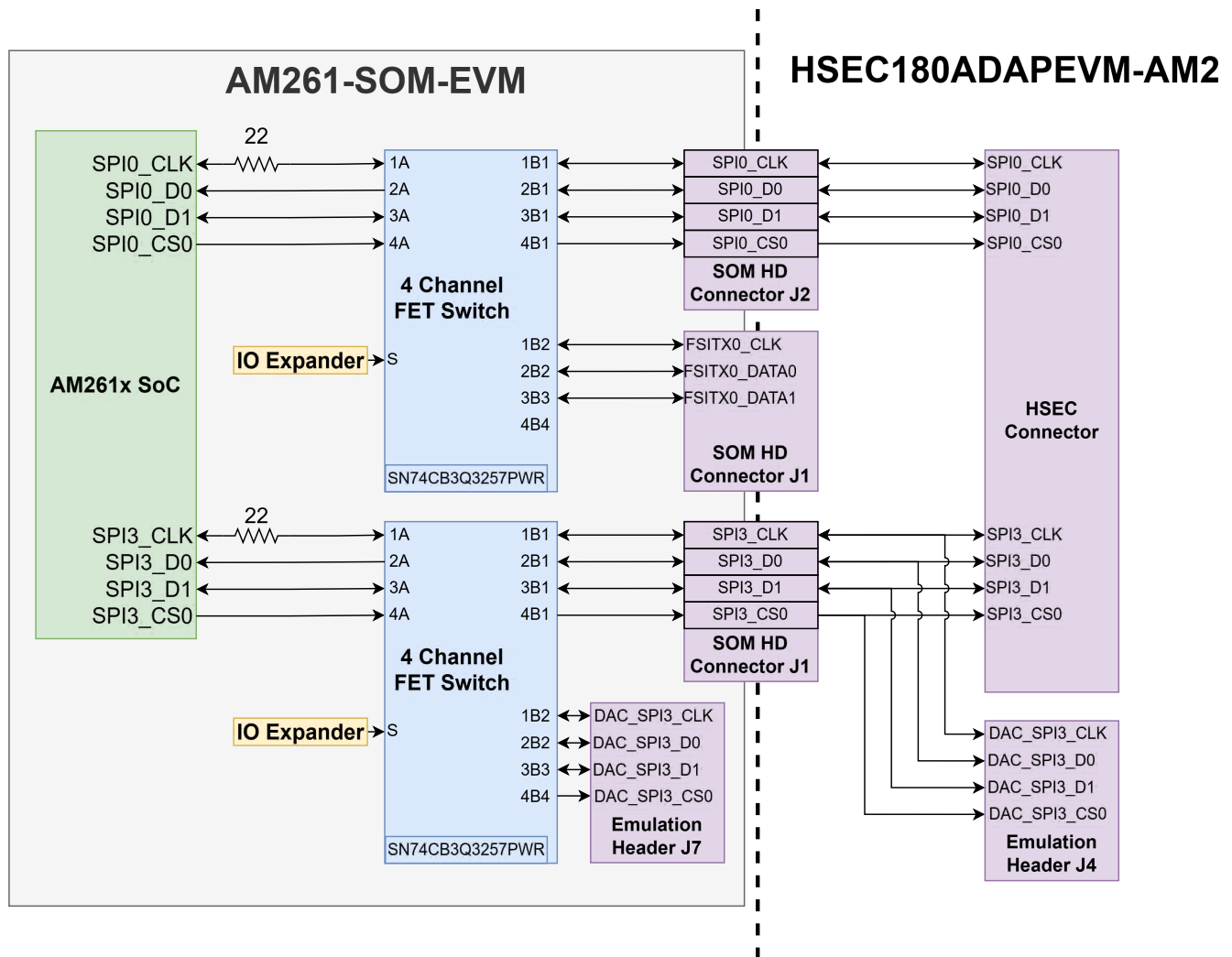


Figure 2-24. HSEC180ADAPEVM-AM2 SPI Interface

SPI0 is directly connected to the HSEC connector.

SPI3 is routed to both the HSEC connector and the Emulation Header (J4).

### 2.8.8 TMDSHSECDOCK-AM263 Peripherals

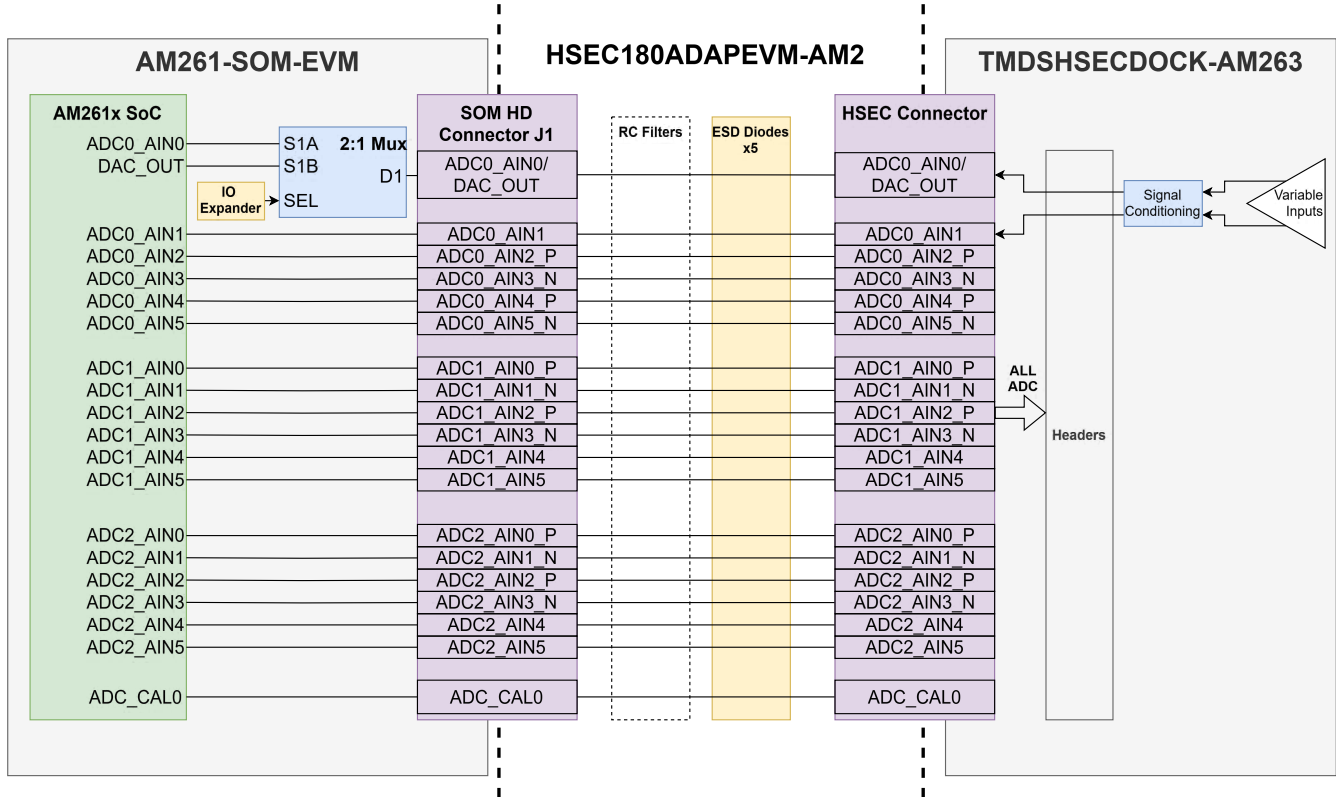
There are several peripherals routed from the AM261x MCU on the AM261x controlSOM, through the SOM HD connectors to the HSEC180ADAPEVM-AM2, and passed to the HSEC connector for use on the TMDSHSECDOCK-AM263. The TMDSHSECDOCK-AM263 has AM26x MCU feature-specific on board hardware for interfacing with the following peripherals:

- ADC
- MCAN
- LIN
- JTAG
- GPIO

The following sections in this User's Guide will detail the integration of the HSEC180ADAPEVM-AM2 between the AM261x controlSOM and the AM26x HSEC Dock. For specific information on the implementation of the hardware on the TMDSHSECDOCK-AM263, consult the [TMDSHSECDOCK-AM263 User's Guide](#).

### 2.8.8.1 ADC/DAC

18 ADC signal channels (3 ADC instances x 5 input channels) are routed from the AM261x controlSOM to the HSEC180ADAPEVM-AM2 via SOM HD Connector J1. On the HSEC180ADAPEVM-AM2, the channels are routed through RC filtering and ESD diodes before terminating at the HSEC connector. When docked with a TMDSHSECDOCK-AM263, the ADC channels can be interfaced with on the 100-mil headers on the AM26x Docking Station.



**Figure 2-25. HSEC180ADAPEVM-AM2 + TMDSHSECDOCK-AM263 ADC Interface**

On the TMDSHSECDOCK-AM263, a pair of potentiometers and op-amps provide variable inputs and signal conditioning for ADC0\_AIN0 and ADC0\_AIN1. For more information on the implementation, see the ADC section in the TMDSHSECDOCK-AM263 User's Guide.

### 2.8.8.2 MCAN

Two instances of the AM261x MCAN peripheral are routed from the AM261x controlSOM through the SOM HD connectors to the HSEC180ADAPEVM-AM2. On the SOM to HSEC adapter board, the signals are routed directly to the HSEC connector. When docking the controlSOM + SOM to HSEC adapter with the TMDSHSECDOCK-AM263, the HSEC pins with the MCAN0 and MCAN1 signals connect to a 2-channel MCAN PHY (TCAN1046) on the AM26x HSEC docking station.

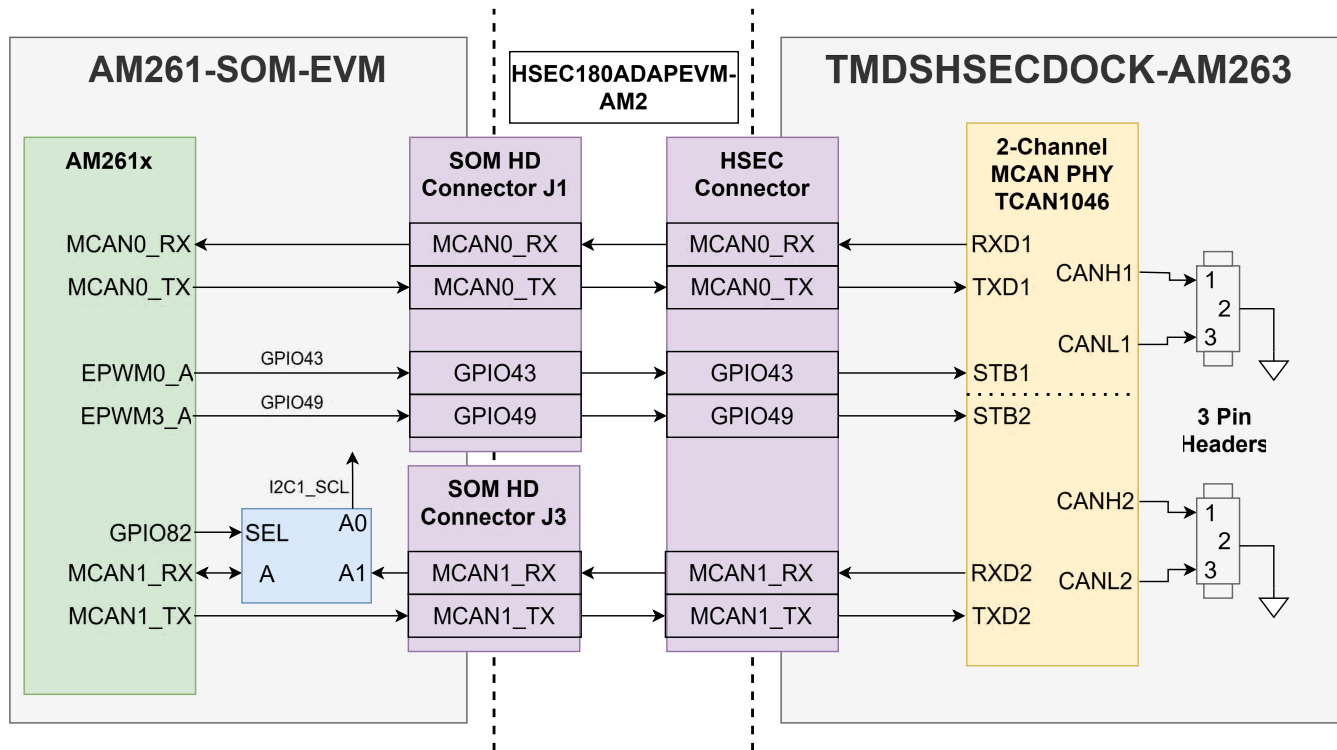


Figure 2-26. HSEC180ADAPEVM-AM2 + TMDSHSECDOCK-AM263 MCAN Interface

GPIO43 (EPWM0\_A) and GPIO49 (EPWM3\_A) are used as standby control signals for each channel of the TCAN1046, and are appropriately routed to the correct HSEC pin to connect to the STB[2:1] pins of the TCAN1046 on the AM26x HSEC docking station.

From the MCAN PHY, The low and high level CAN bus I/O lines for each channel are terminated to a three pin header.

For more information on the implementation of the TCAN1046 on the TMDSHSECDOCK-AM263, see the the MCAN section in the TMDSHSECDOCK-AM263 User's Guide.

### 2.8.8.3 LIN1

One instance of the AM261x Local Interconnect Network (LIN) peripheral is routed from the AM261x controlSOM to the HSEC180ADAPEVM-AM2 via SOM HD Connector J1. The LIN1 RXD/TXD signals are directly routed to the HSEC connector. When docking with the TMDSHSECDOCK-AM263, these HSEC pins connect to a TLIN2022A 2-channel LIN transceiver. **Only one of the two channels of the TLIN2022A is enabled for LIN communication when using the AM261x controlSOM + HSEC180ADAPEVM-AM2.** The LIN bus of LIN1 is connected to the second pin of a 3-pin header on the AM26x HSEC Docking Station.

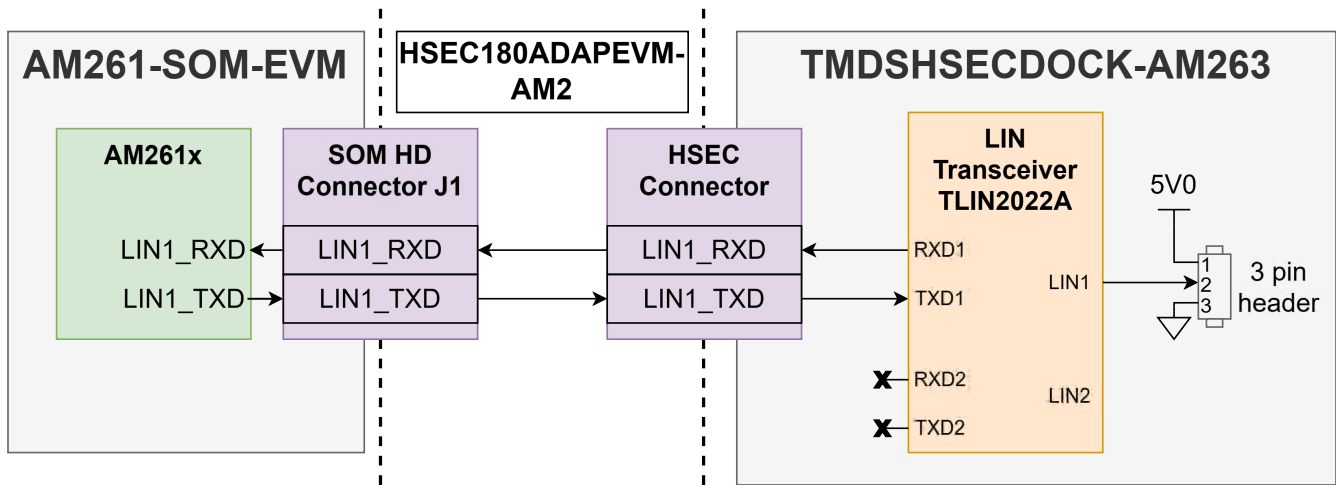


Figure 2-27. HSEC180ADAPEVM-AM2 + TMDSHSECDOCK-AM263 LIN Interface

### 2.8.8.4 JTAG

The JTAG signals (TDO, TDI, TMS, TCK) are routed from the AM261x controlSOM through the SOM HD Connector J1 to the HSEC180ADAPEVM-AM2. On the HSEC180ADAPEVM-AM2, the JTAG nets are routed to an emulation header (J4) and the HSEC Connector. When docked with the TMDSHSECDOCK-AM263, the JTAG signals can be accessed at the AM26x Docking Station MIPI-60 header or TI 14-pin JTAG header.

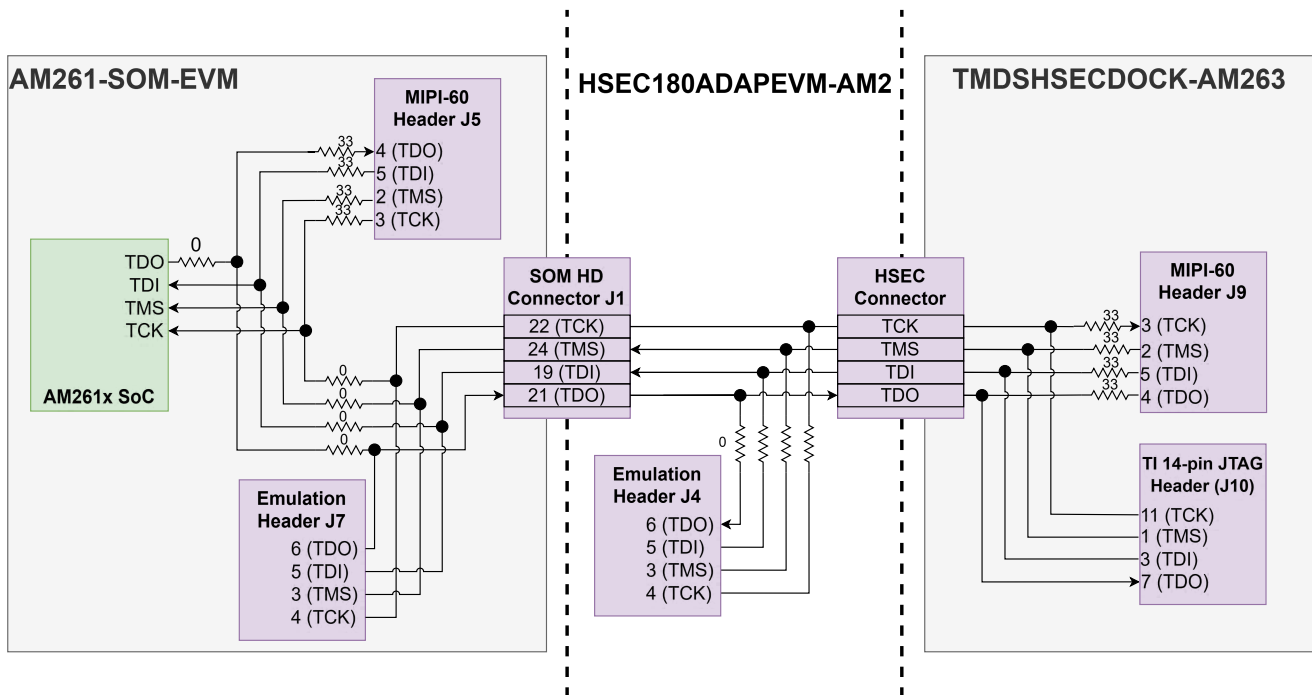


Figure 2-28. HSEC180ADAPEVM-AM2 + TMDSHSECDOCK-AM263 JTAG Interface

### 2.8.8.5 GPIO

All digital IO from the AM261x controlSOM routed to the HSEC connector on the HSEC180ADAPEVM-AM2 can be interfaced with as GPIO signals on standard 100-mil headers when docked with the TMDSHSECDOCK-AM263. For pinmux information, see [Table 2-2](#).

## 2.9 Debug Information

## 2.10 Test Points

The AM261x SOM to HSEC adapter includes multiple test points to aid in hardware debug. [Table 2-20](#) includes a list of the test points available on the HSEC180ADAPEVM-AM2.

**Table 2-20. HSEC180ADAPEVM-AM2 Test Points**

Test Point Designator	Test Point Net Name	Description
TP1	VMAIN_5V0_IN	System 5V input
TP2	3V3_LDO2	System 3.3V I/O supply. AM261x controlSOM PMIC LDO2 output
TP3	5V0_LDO3	AM261x controlSOM PMIC 5V LDO3 output
TP4	GND	GND
TP5	VDDA2_1V8	DP83869 (U1) PHY 1.8V supply input for three-supply mode
TP6	PHY2_RBIAS	DP83869 (U1) PHY bias resistor pin
TP7	PHY2_CLKOUT	DP83869 (U1) PHY output clock
TP8	VDDA1_1V8	DP83869 (U2) PHY 1.8V supply input for three-supply mode
TP9	PHY1_RBIAS	DP83869 (U2) PHY bias resistor pin
TP10	PHY1_CLKOUT	DP83869 (U2) PHY output clock
TP11	EXT_VMON2	AM261x controlSOM PMIC external voltage monitor for Ethernet add-on board connector
TP12	1588_SFD	IEEE 1588 SFD
TP13	VDD_ETH_2V5	2.5V Ethernet PHY power supply output
TP14	VDD_ETH_1V1	1.1V Ethernet PHY power supply output
TP15	ICSSM_MII0_COL	MII0 collision detected
TP16	VBUS_MICRO_AB_5V0	USB micro-AB power distribution switch 5V output
TP17	GND	GND
TP18	AM26x_VREFH1	1.8V analog voltage reference
TP19	GND	GND
TP20	ICSSM_MII0_CRS	MII0 carrier sense
TP21	VDDIO_3V3	3.3V load switch output
TP22	GND	GND
TP23	GND	GND
TP25	MCU_PORz	AM261x power-on-reset

## 2.11 Assembly Instructions

## 2.12 Best Practices

### Electrostatic Discharge (ESD) Compliance

Components installed on the product are sensitive to electrostatic discharge (ESD). TI recommends this product be used in ESD controlled environment. This includes a temperature or humidity controlled environment to limit the buildup of ESD. TI recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

### Assumed Operating Conditions

This kit is assumed to run at standard room conditions. Standard ambient temperature and pressure (SATP) with moderate-to-low humidity is assumed.

### 3 Software

The AM261x MCU+ Software Development Kit ([MCU-PLUS-SDK-AM261X](#)) is a unified software platform for embedded processors providing easy setup and fast out-of-the-box access to examples, benchmarks and demonstrations. This software accelerates application development schedules by eliminating creating basic system software functions from scratch.

The [AM261x MCU+ Academy](#) provides a [Getting Started Guide](#) for first-time software development using the AM261-SOM-EVM. Follow the steps in this guide to begin development.

## 4 Hardware Design Files

The HSEC180ADAPEVM-AM2 hardware design files can be downloaded from the [EVM Tool Page](#), or by clicking this link.



## **5 Additional Information**

### **5.1 Trademarks**

All trademarks are the property of their respective owners.

## 6 References

In addition to this document, the following references are available for download at

- [AM2612 Microcontroller Product Page](#)
- [AM261x Data Sheet](#)
- [AM261x Technical Reference Manual](#)
- [AM261x Register Addendum](#)
- [XDS110ISO-EVM](#) XDS110 isolated plug-in evaluation module for C2000 and Sitara™ controlSOMs
- [TMDSHSECDOCK](#) C2000™ HSEC180 baseboard docking station
- [TMDSHSECDOCK-AM263](#) AM26x HSEC180 dock and breakout board

### 6.1 Other TI Components Used in This Design

This EVM uses various other TI components. A consolidated list of these components with links to their TI Product Pages is shown below.

- [DP83869HM](#) gigabit Ethernet PHY transceiver
- [TPD4E001](#) Quad 1.5-pF, 5.5-V, ±8-kV ESD protection diode with 1-nA max leakage & VCC pin for USB 2.0
- [SN74AHC1G09](#) 1-ch, 2-input AND gate with open-drain outputs
- [TPS62097](#) 2-A Step Down Converter with Selectable Switching Frequency
- [TPS22918](#) 5.5-V, 2-A, 52-mΩ load switch
- [TLV755P](#) 500mA high-PSRR low-IQ low-dropout voltage regulator with enable
- [TPS2051B](#) 0.5A loading, 2.7-5.5V, 70mΩ USB power switch
- [TPD4E02B04](#) Quad 0.25-pF, ±3.6-V, ±12-kV ESD protection diode for USB 3.0, HDMI 2.0 & High Speed Signals
- [TS3DDR3812](#) 3.3-V, 2:1 (SPDT), 12-channel switch
- [TMUX154E](#) 7.5-pF on-state capacitance, 3.3-V, 2:1 (SPDT), 2-channel analog switch

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial Release

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