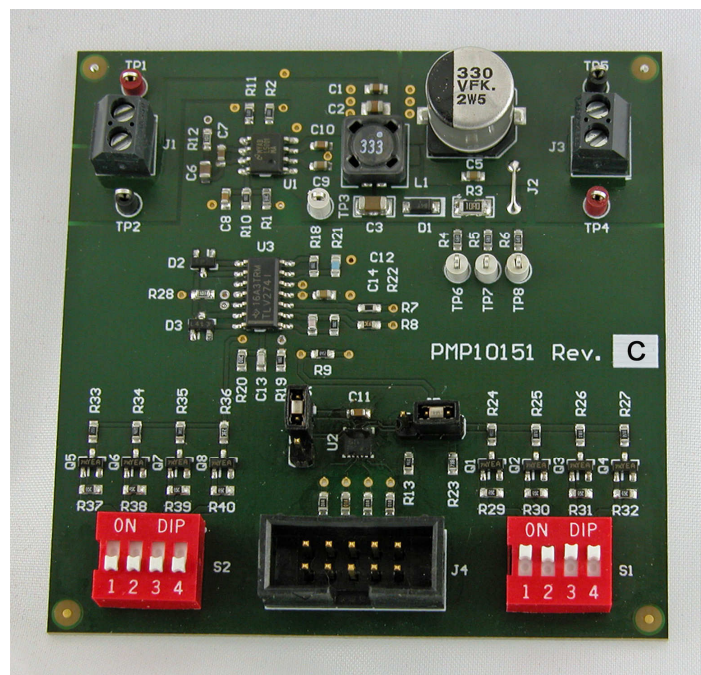


## Sepic with Adjustable Output Voltage and Input Current Limit

- Input 10 .. 14V DC
- Output 20 .. 25V @ 70 .. 135mA
- Devices LM5001, LM10011, TLV274, LP2980-5.0
- Free-running switching frequency of 1000 kHz
- The converter provides a non-isolated output with an adjustable range of 20 .. 25V. The output voltage can be changed by either by a programmable DAC (LM10011) or by a discrete VID interface. It provides also the functionality to limit the charge current of the output capacitor to 70 .. 135mA, which is set by a VID interface. This function limits practically the input current of the converter, if large pulsed loads need to be supported. These loads discharge the output capacitor and therefore the current for recharging it can be limited.



## 1 Startup

The startup waveform at 12V input and no load on the output is shown in Figure 1.

Channel C1: **12V Input voltage**  
5V/div, 20ms/div

Channel C2: **25V Output voltage**  
5V/div, 20ms/div

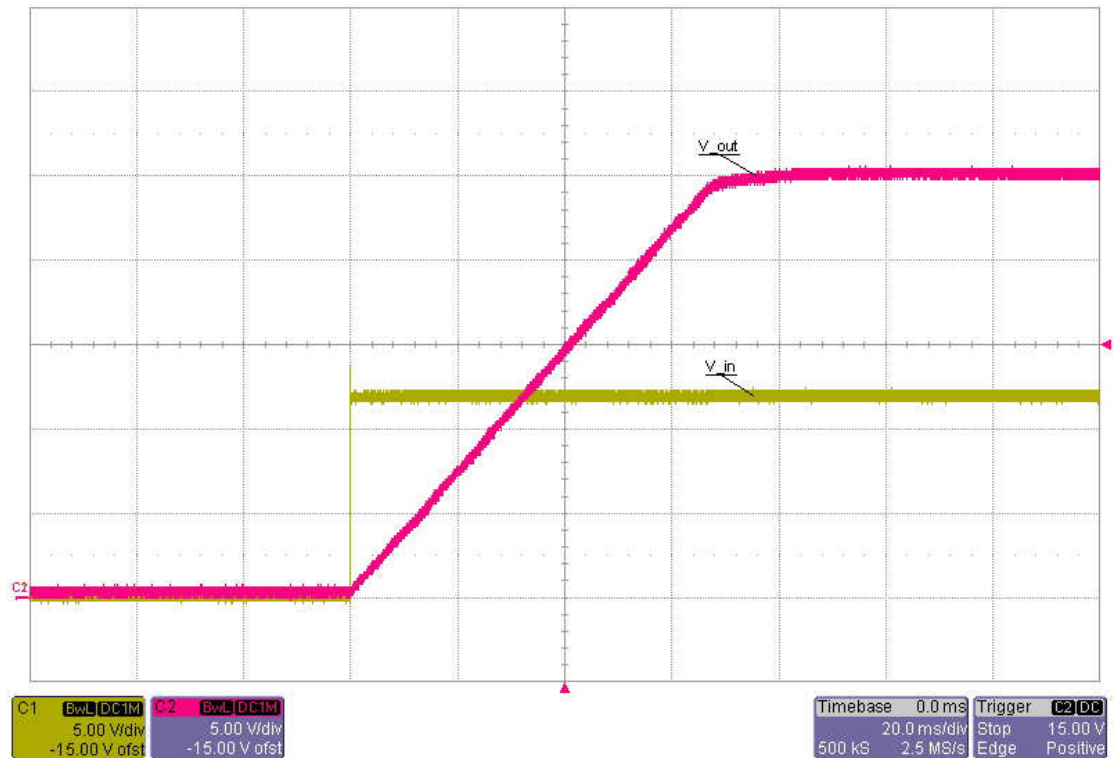


Figure 1

## 2 Shutdown

The shutdown waveform at 12V input, 25V output and 120mA load is shown in Figure 2. The converter is regulating the output voltage

Channel C1: **12V Input voltage**  
5V/div, 50ms/div

Channel C2: **25V Output voltage**  
2V/div, 50ms/div

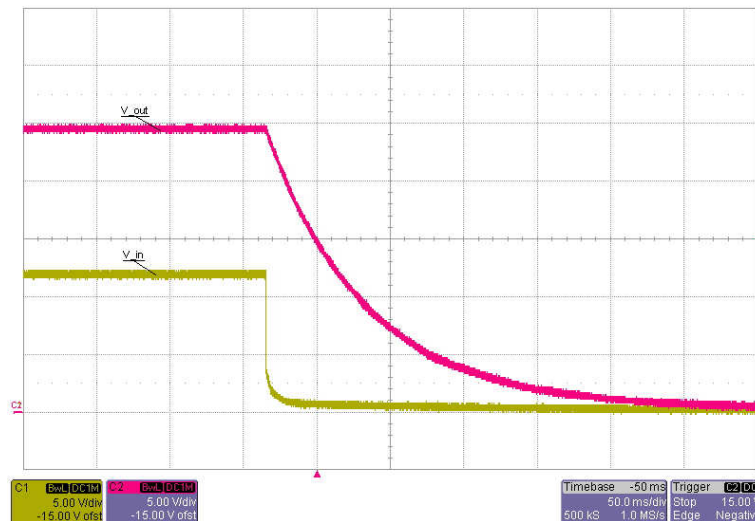


Figure 2

The shutdown waveform at 12V input, 20V output and 135mA load is shown in Figure 3. The converter is regulating the output current

Channel C1: **12V Input voltage**  
5V/div, 50ms/div

Channel C2: **20V Output voltage**  
5V/div, 50ms/div

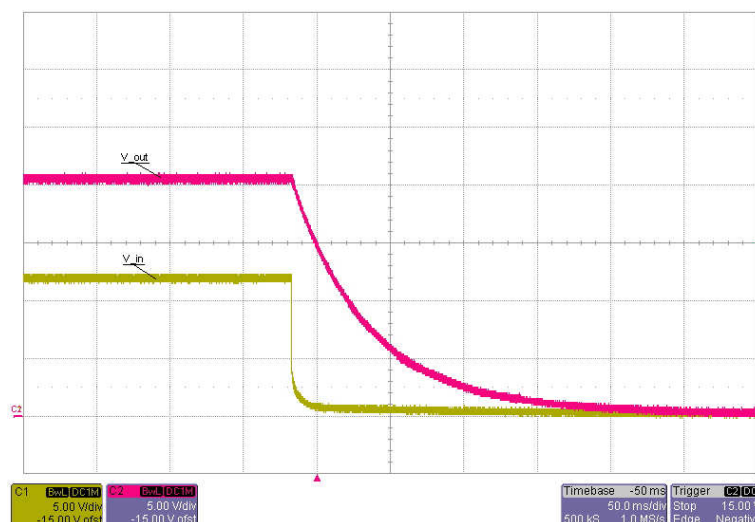


Figure 3

### 3 Efficiency and Load Regulation

The efficiency and load regulation are shown in Figure 4 and Figure 5.  
The output voltage was set to 25V and the converter regulated the output voltage.

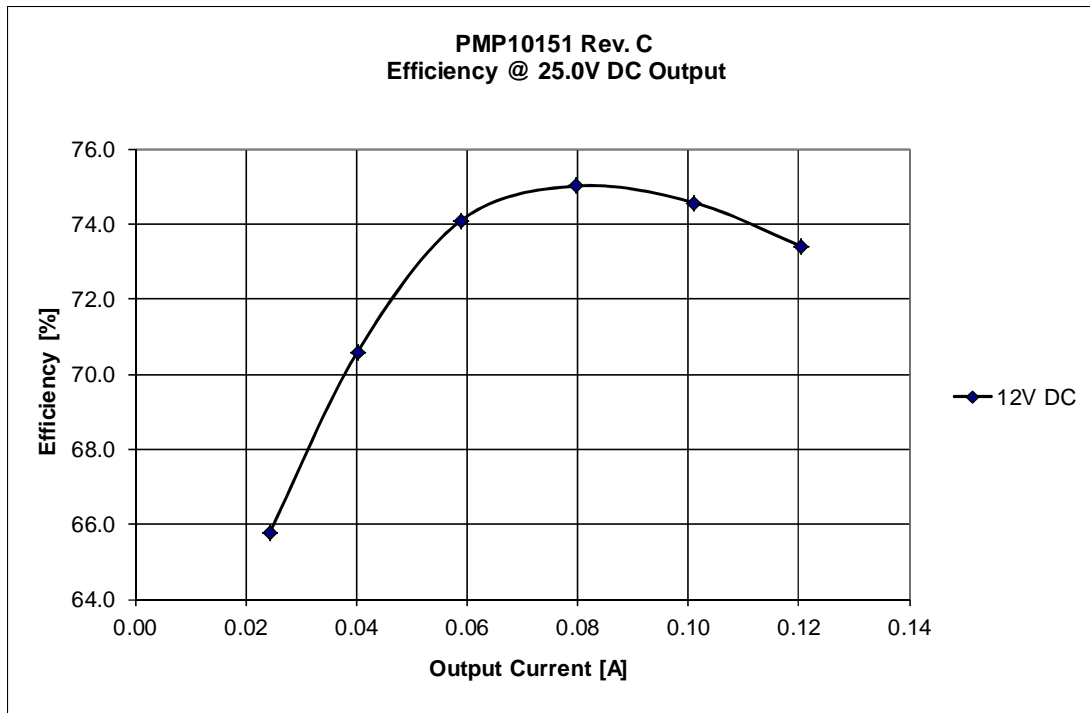


Figure 4

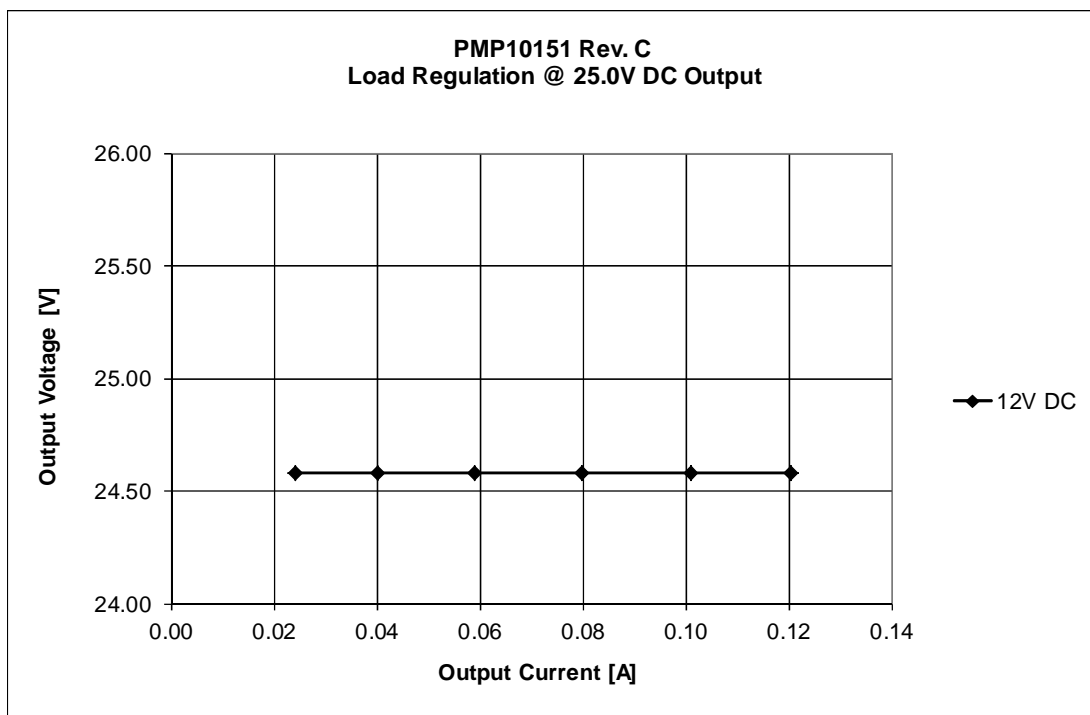


Figure 5

## 4 Frequency Response

Figure 6 shows the loop response at 12V input and 120mA load.  
The output voltage was set to 25V and the converter regulated the output voltage.

### Voltage regulation

89 deg phase margin, 60 Hz bandwidth, enough gain margin

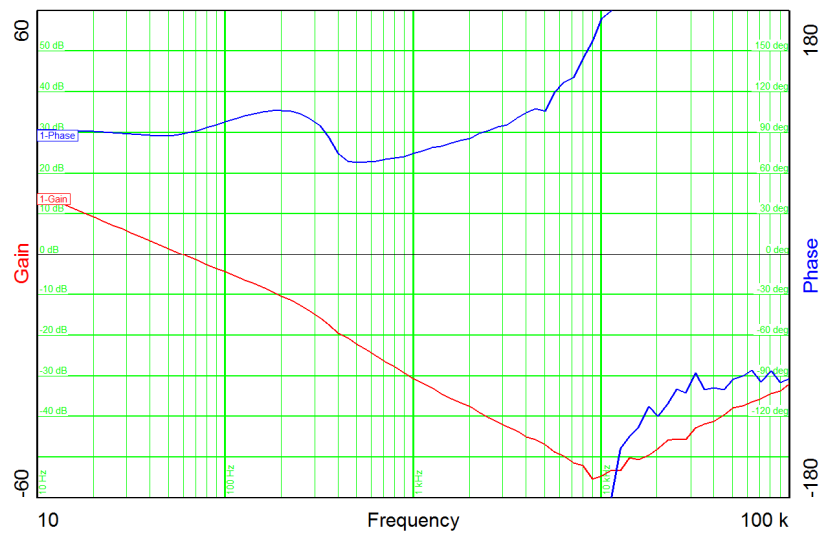


Figure 6

Figure 7 shows the loop response at 12V input and 135mA load.  
The output voltage was set to 25V and the converter regulated the output current.

### Current regulation

85 deg phase margin, 8.7 kHz bandwidth, -17 dB gain margin

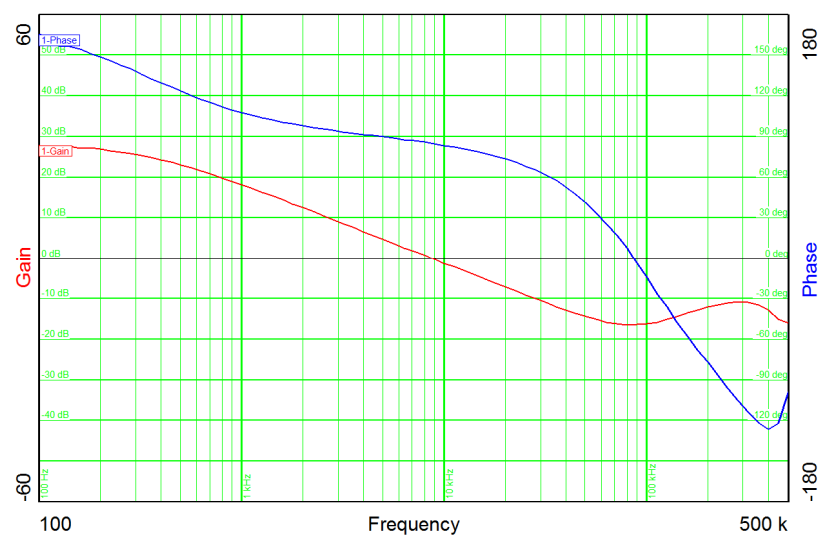


Figure 7

## 5 Switching Node

The drain-source voltage on the switching node at 12V input is shown in Figure 8. The image was captured with 120mA load and the output voltage was set to 25V.

Channel C2: **Drain-source voltage**, -1.0V minimum voltage, 51.1V maximum voltage  
10V/div, 500ns/div

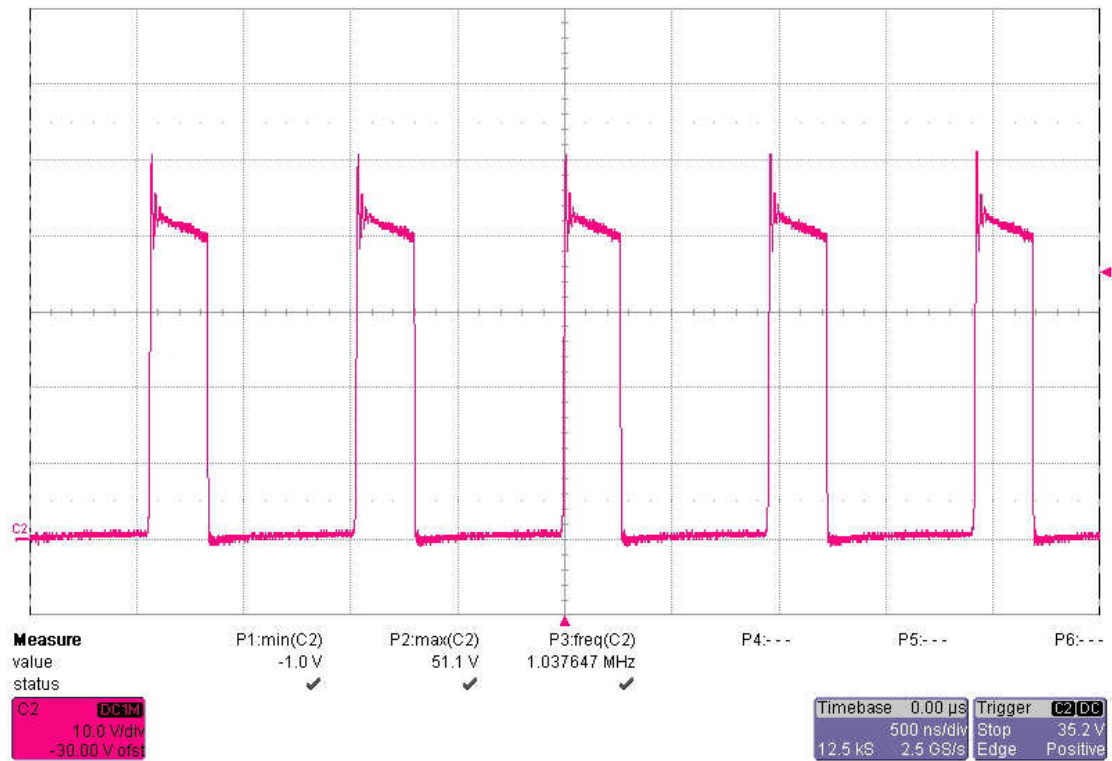


Figure 8

## 6 Output Ripple Voltage

The output ripple voltage at 12V input is shown in Figure 9.

The image was captured with 120mA load and the output voltage was set to 25V.

Channel C2: **Output voltage @ 12V input**, 230mV peak-peak (0.9%)  
50mV/div, 1us/div, AC coupled

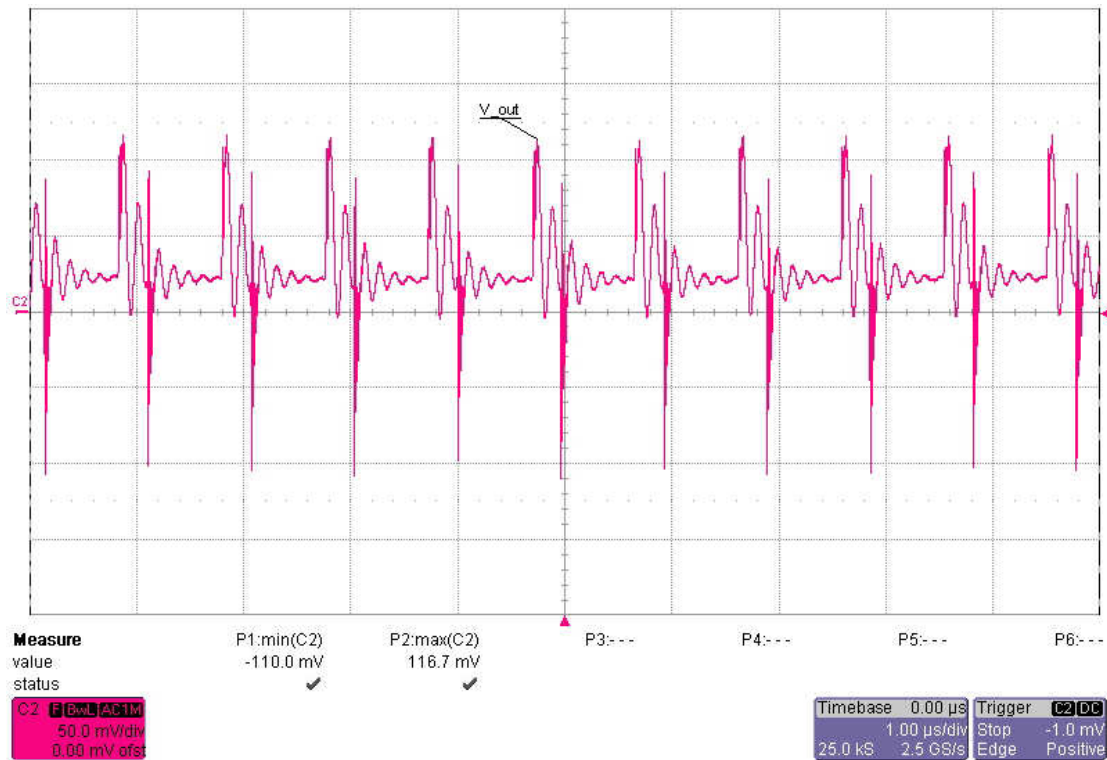
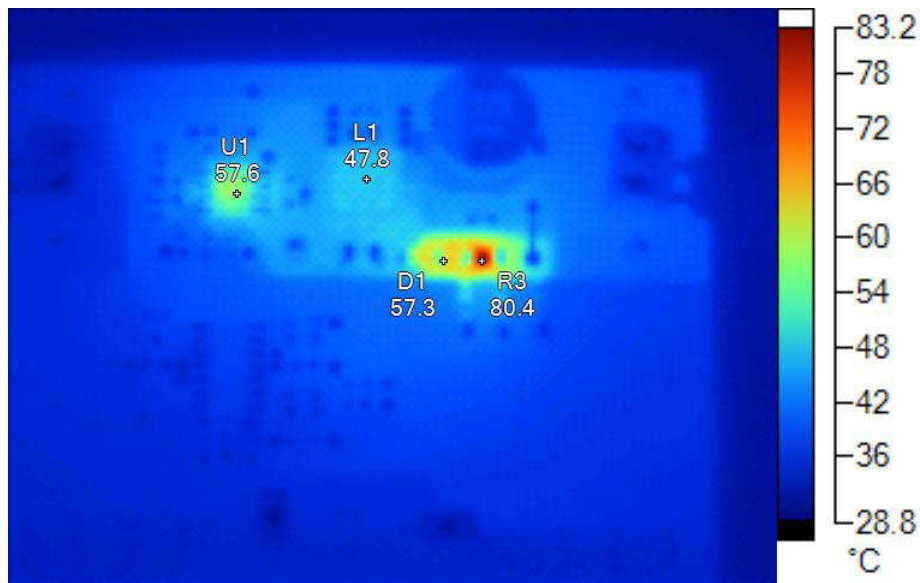


Figure 9

## 7 Thermal Measurement

Figure 10 shows the thermal image at an ambient temperature of 21 °C with an input voltage of 12V and 130mA load.

The converter delivered 130mA continuously, which is not the normal operation mode. Usually, only pulsed loads with a low duty cycle have to be supplied. With these pulsed load the thermal stress will be much lower.



**Figure 10**

### Markers

Label	Temperature	Emissivity	Background
U1	57.6 °C	0.95	21.0 °C
L1	47.8 °C	0.95	21.0 °C
D1	57.3 °C	0.95	21.0 °C
R3	80.4 °C	0.95	21.0 °C



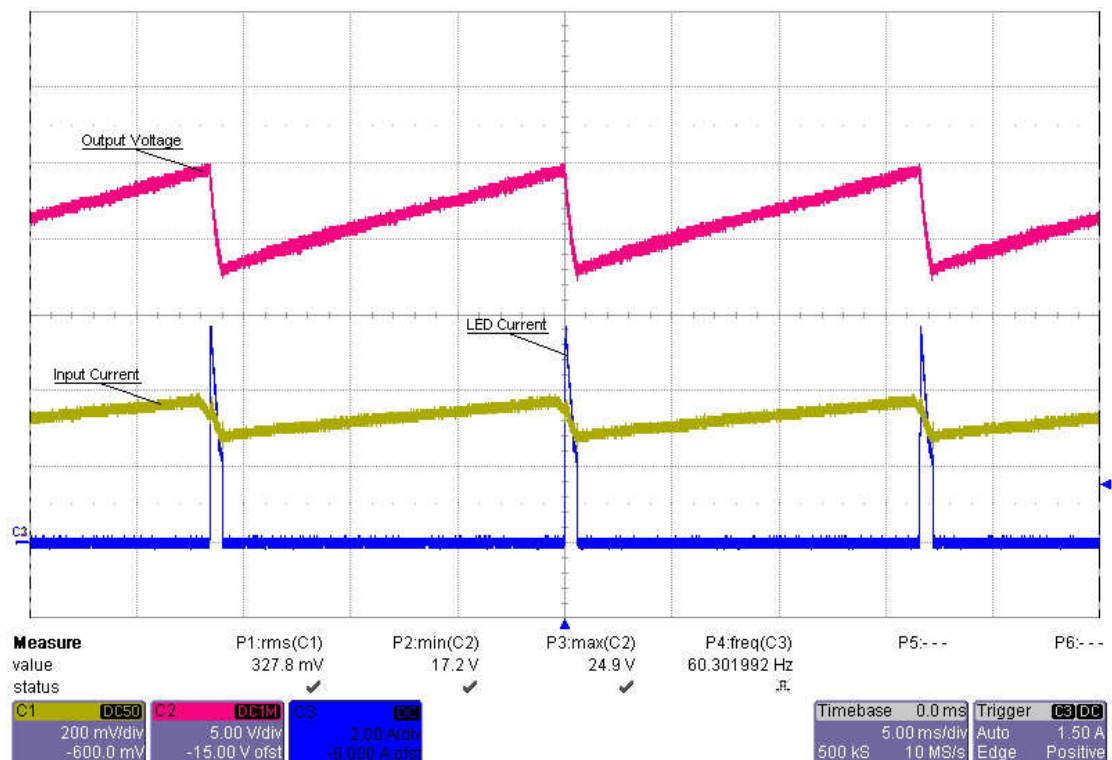
## 8 Pulsed Load

The normal operation is supplying a pulsed load with 3.0A peak for 600 us and a frequency of 60 Hz. These high peak currents are provided by the large output capacitance which is discharged for several volts.

As the input current of the converter is limited, the additional current control limits the charge current of the capacitor to an adjustable value (135mA nominal).

As the performance of the electronic load is limited, the exact pulsed load couldn't be simulated. Nevertheless the circuit shows proper regulation of the output voltage and current limitation.

- Channel C1: **Input current**  
200mA/div, 5ms/div
- Channel C2: **Output voltage**  
5V/div, 5ms/div
- Channel C3: **Pulsed load**  
2A/div, 5ms/div



**Figure 11**

Channel C1: **Capacitor/diode current**  
200mA/div, 5ms/div

Channel C2: **Output voltage**  
5V/div, 5ms/div

Channel C1: **Pulsed load**  
2A/div, 5ms/div

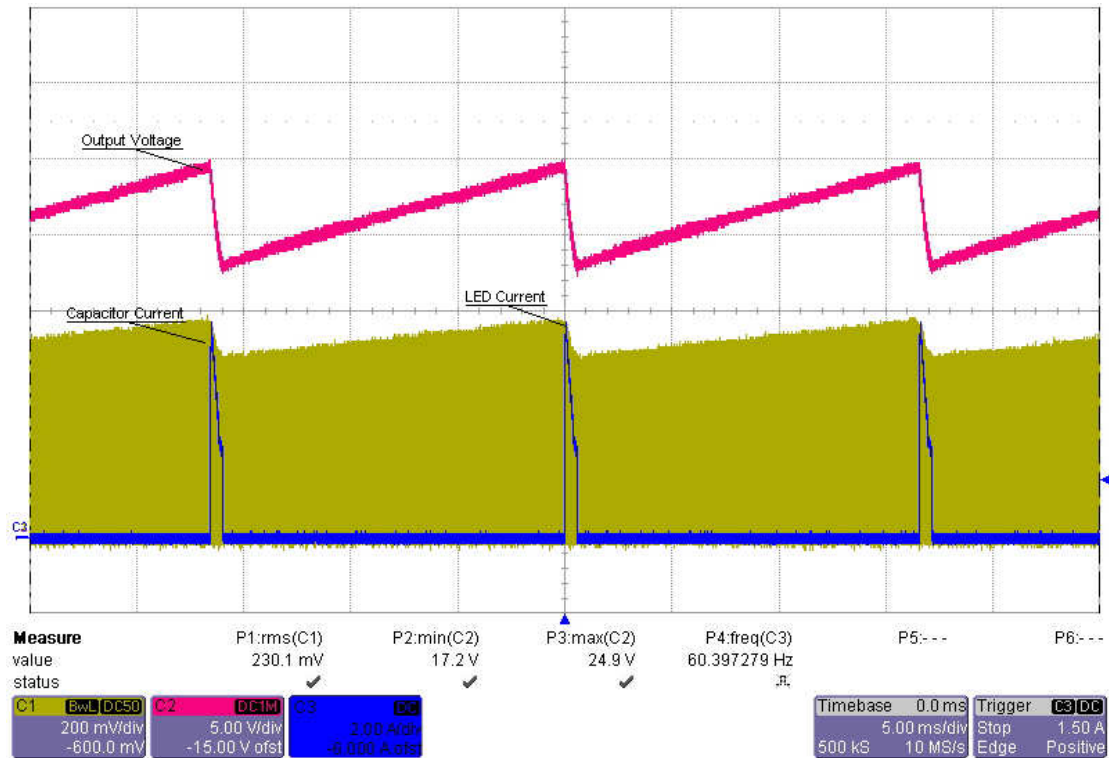


Figure 12

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