A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V (Part One of Two)

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A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V
BY: Robert C. Taft and Maria Rosaria Tursi, Data Conversion Systems

Abstract A 100-MS/s 8-b CMOS analog-to-digital converter (ADC) designed for very low supply voltage and power dissipation is presented. This single-ended-input ADC is based on the unified two-step subranging architecture, which processes the coarse and fine decisions in identical signal paths to maximize their matching. However, to minimize power and area, the coarse-to-fine overlap correction has been aggressively reduced to only one LSB. The ADC incorporates five established design techniques to maximize performance: bottom-plate sampling, distributed sampling, auto-zeroing, interpolation, and interleaving. Very low voltage operation required for a general purpose ADC was obtained with four additional and new circuit techniques. These are a dual-gain first-stage amplifier, differential T-gate boosting, a supply independent delay generator, and a digital delay-locked-loop controlled output driver. For a clock rate of 100 MS/s, 7.0 (7.3) effective bits for a 50 MHz (10 MHz) input are maintained from 3.8 V down to 2.2 V. At 2.2 V, this 100-MS/s converter dissipates 75 mW plus 9 mW for the reference ladder. For a typical supply of 2.7 V, it consumes just 1 mW per MS/s over the 10 160-MS/s clock frequency range. Differential nonlinearity below 0.5 LSB is maintained from 2.7 V down to 2.2 V, and it degrades only slightly to 0.8 LSB at 3.8-V supply. The converter is implemented in a 0.35-mm CMOS process, with double-poly capacitors and no low-threshold devices.

Index TermsAnalog-to-digital converters, CMOS analog integrated circuits, Nyquist converters, subranging A/D converters, switched capacitor circuits, two-step A/D converters.

I. INTRODUCTION

High-Speed Nyquist analog-to-digital converters (ADCs) play a decisive role in the overall performance of many imaging, video, and digital communications systems, and have been successfully developed using a number of different architectures. Flash was the earliest of such architectures [1]. A resistor ladder with 2^N 1 taps provides the reference voltages, which are directly compared to the input voltage by 2^N 1 comparators. This 2^N 1 wide "thermometer code" is encoded, usually in binary or gray code, to obtain an N-bit digital word which represents the input voltage relative to the reference voltages of the reference ladder. Fig. 1 shows the schematic for a simplified N = 2 bit example, where the input voltage lies between reference voltages V_{R3} and V_{R2} . Three trends have affected monolithic Nyquist (in which inputs frequencies near half the conversion clock frequency need to be accurately digitized) ADCs. The first trend is an increase in the input frequency F_{IN} and hence required conversion rate F_{CLK}. The second is an increase in resolution or number of bits N, as communication and video systems evolve and become more sophisticated. The third and more recent trend is to design ADCs in aggressive CMOS technologies, with their corresponding reduction in power-supply voltage. This latter trend resulted in part from process consolidation, in which specialized analog processes were avoided due to the high cost of low-volume manufacturing. ADC designs in aggressive CMOS technologies enable the ultimate goal of integrating almost all of the analog functionality together with the digital cores.

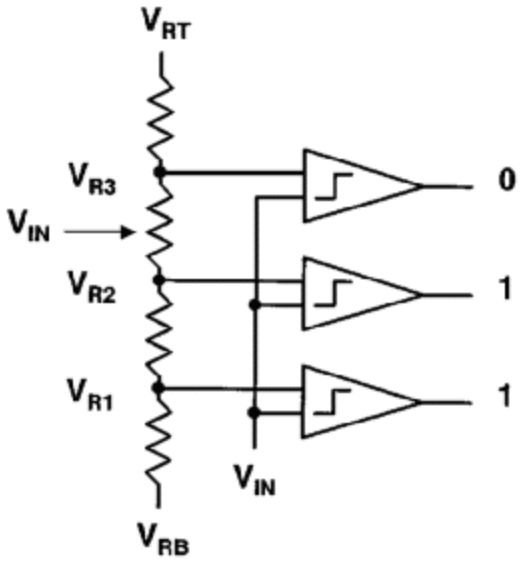

Fig. 1. Schematic for a 2-b flash converter, which uses a resistor ladder to subdivide end-point reference voltages V_{RT} and V_{RB}. The comparators output thermometer code "0, 1, 1," corresponds to a V_{IN} between voltage taps V_{R3} and V_{R2}. Note that there is no over-range indication; the binary encoded output is "10."

II. SELECTING A LOW-VOLTAGE ADC ARCHITECTURE

The choice of ADC architecture was motivated primarily by the third trend: Designing in an aggressive CMOS tech-nology, with its corresponding reductions in power-supply voltage. Classical 1.5-b-per-stage pipeline architectures require high-gain and high-bandwidth amplifiers [2], whose realization will become increasingly difficult with reductions in power-supply voltage and increasing speed. The highly parallel flash architecture lends itself to easily implemented low-voltage circuit blocks. Amplifiers preceding the comparators, used to reduce the referred-to-input comparator offsets, do not require large gain, so they can have a high bandwidth. However, the largest drawback of flash with respect to pipeline architectures is the exponential growth in the number of comparators to 2^N for increasing resolution, N. This growth in number of comparators translates directly to an exponential growth in power, area, and input capacitance of the flash converter. Two distinct enhancements to the flash architecture address this limitation, two-step subranging [3] and folding [4]. In two-step subranging, the most significant bits (MSBs) are obtained first using $2^{N/2}$ comparators. These MSBs are then used to subtract the coarse content of the input signal to create a residue, so that the least significant bits (LSBs) can be obtained, again with $2^{N/2}$ comparators. The total number of comparators required is only $2 * 2^{N/2}$, nearly the square root of 2^N the flash requirement. This gives a commensurate saving in power, area, and input capacitance.

In folding, the residue for evaluating the LSBs, which is evaluated explicitly in the two-step method, is evaluated without *a priori* knowledge of the MSBs using collector cross-connected differential bipolar pairs. Thus, the MSBs and LSBs can be evaluated simultaneously. Although this technique has been successfully migrated from bipolar to CMOS, using nMOS differential pairs [5], the residue generation using drain cross-connected differential nMOS pairs generates analog signals much higher in frequency than the input signal. This necessitates a sample-and-hold amplifier at the front end for good Nyquist performance, and may limit the folding architectures for very high conversion speeds. For these latter reasons, folding was not pursued as the basis for this low-voltage ADC design.

III. UNIFIED SUBRANGING ARCHITECTURE

In implementing the (two-step) subranging ADC architecture, the same reference ladder provides both the MSBs "coarse" and LSBs "fine" reference voltages. A 4-b converter example starting with the flash conversion of Fig. 1

is shown in Fig. 2, where the 2-b LSBs are evaluated by comparing V_{IN} to the appropriate segment of the reference ladder. This requires an analog MUX between the four possible resistor segments and the comparator bank. The MSBs, obtained previously as in Fig. 1, control this MUX, select the appropriate resistor segment, and are then added to the LSBs to obtain the complete digital output code.

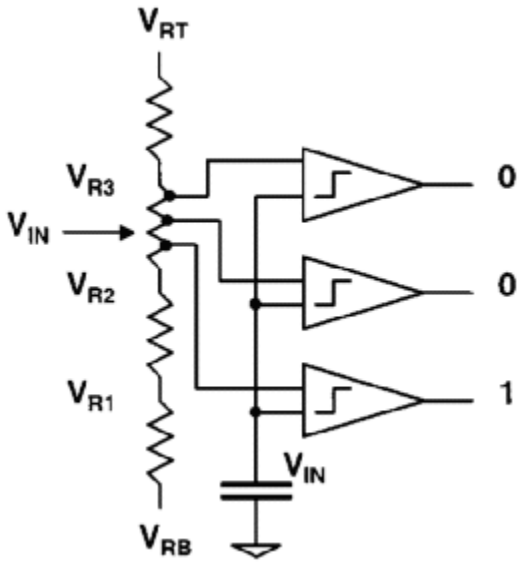

Fig. 2. Schematic for the second comparison of a 4-b subranging converter, showing the evaluation of the two LSBs. The two MSBs "10" were obtained as shown in Fig. 1. The MSBs are not subtracted from V_{IN} . Rather, the input voltage V_{IN} is held, and the comparator reference inputs are switched onto the appropriate segment of the reference ladder. The binary representation of the LSBs is "01," which together with the MSBs "10" forms the 4-b digital output code "1001."

A concern with this approach is the need for matching between the MSBs and LSBs conversion. For inputs near the re-sistor segment boundary, a small mismatch results in the MSBs conversion selecting the incorrect resistor segment for the LSBs evaluation. Most subranging converters address this problem by extending the range of the LSBs segment beyond the MSBs seg-ment boundary by several LSBs, , in both directions. In case of a mismatch, the LSBs result is then taken as the definitive answer, and the MSBs result is either incremented or decremented one digit. This "error correction" requires a wider analog MUX bus for generating the fine reference voltages and significantly more comparators, $2^{N/2} + 2 * k$.

To address the MSBs to LSBs matching concern, Hosotani s [6] "unified" architecture was used. The same analog channel evaluates both the MSBs and LSBs, so that the input signal need not be sampled and routed to two different comparator banks, resulting in inherently good matching. One fully unified channel can sample V_{IN} and autonomously process all bits, making this architecture well suited to interleaving. Despite using a unified architecture, Hosotani uses $k = 3$ additional fine references in the analog MUX, requiring a total of 21 comparators. To avoid this extra circuitry and power, no extra fine codes outside of the range imposed by the coarse-compare are examined. Seventeen comparators ($k = 1$) are used, which is no more overhead than that required for over/underflow indication. Only one LSB of MSBs-to-LSBs mismatch correction is obtained implicitly by using the output of comparators 1 and 17, which also generate the over-range indication.

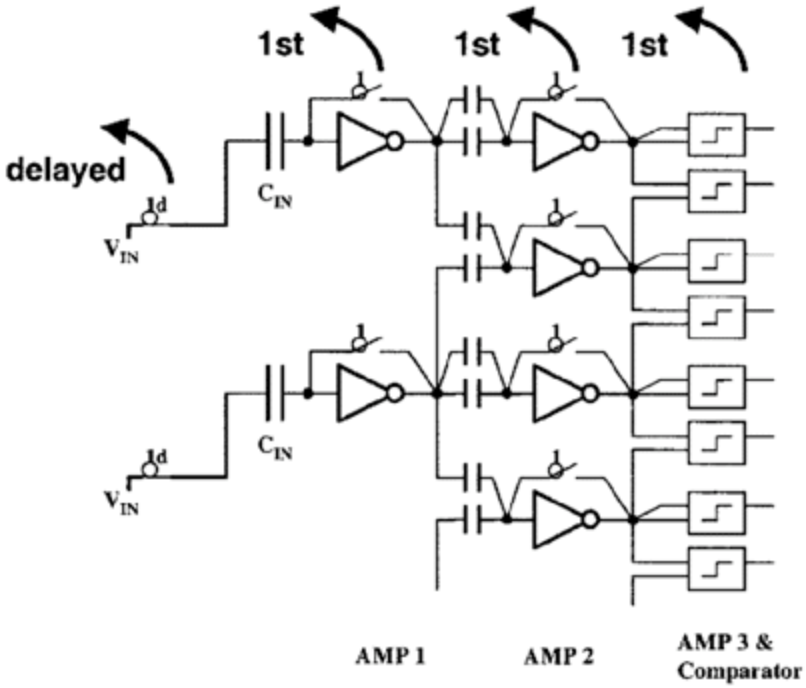

Fig. 3. Phase 1 distributed "bottom-plate" sampling, in which the sampling switch at the virtual ground of amplifier 1 is opened before opening the T-gate to V_{IN} , to avoid signal-dependent charge injection. Since the sampling switches around amplifiers 1, 2, and 3 are all opened simultaneously, the architecture is auto-zeroing: C_{IN} stores V_{IN} , whereas the input capacitors of amplifier 2 store the offset voltage of amplifier 1, and the input capacitors of amplifier 3 (inside the comparator block) store the offset voltage of amplifier 2.

IV. INCORPORATING ESTABLISHED ADC CIRCUIT TECHNIQUES

Here five established enabling ADC circuit techniques are briefly discussed, before describing this paper s contributions in more detail. The five techniques are bottom-plate sampling, distributed sampling, auto-zeroing, interpolation, and interleaving. Fig. 3 shows a subsection of the analog channel during sampling (designated as phase 1). By using distributed sampling, no sample-and-hold amplifier (SHA) is required, since the sampling function is performed by the first amplifier stage. This saves power and alleviates the input range restriction imposed by SHAs. However, the sampling instant for all parallel paths must be identically matched. This sampling instant is set by opening the shorting switch on amp 1, after which V_{IN} can no longer transfer net charge onto C_{IN}. Since the sampling switch is always at the virtual ground of the amplifier, it injects a constant charge onto C_{IN}, independent of the signal voltage. Often referred to as "bottom-plate" sampling, this technique avoids the distortion of signal-dependent charge injection. The opening of the T-gate connection of C_{IN} to V_{IN} at the end of phase 1 is delayed with respect to the sampling instant, and is indicated by "1d."

The offset difference between amp 1 and amp 2, resulting from statistical and process variations of their constituent tran-sistors, is sampled onto the input capacitors of amp 2 during the sampling phase. By thus "auto-zeroing" the offset of amp 1, the linearity errors in the ADC transfer function otherwise introduced by offsets between the parallel amp 1s are fully eliminated. Similarly, amp 2 s offset voltage is auto-zeroed by storing it on the input capacitors of amp 3. Amp 3 is not auto-zeroed, but the effect of its offset, referred to input, is reduced by the two previous gain stages.

After sampling, the C_{IN} s are connected to the coarse reference voltages, creating a difference voltage. This difference voltage is amplified by amplifiers 1 through 3 and applied to 17 comparators. Rather than generating all 17 voltages independently, for the 4-b MSBs plus over-range, interpolation by-2 between amp 1 and amp 2, and again by-2 between amp 2 and amp 3, reduces the number of input capacitors by 4x; see [7], [8]. As shown,

the interpolation between the outputs of two adjacent amplifiers is accomplished by connecting their outputs to two equal-valued capacitors forming the input of the next amplifier stage. Not only does interpolation reduce the front-end loading on the input signal V_{IN} and the reference voltages, but reduces power, area, and the dc nonlinearity errors as described in [5], [8].

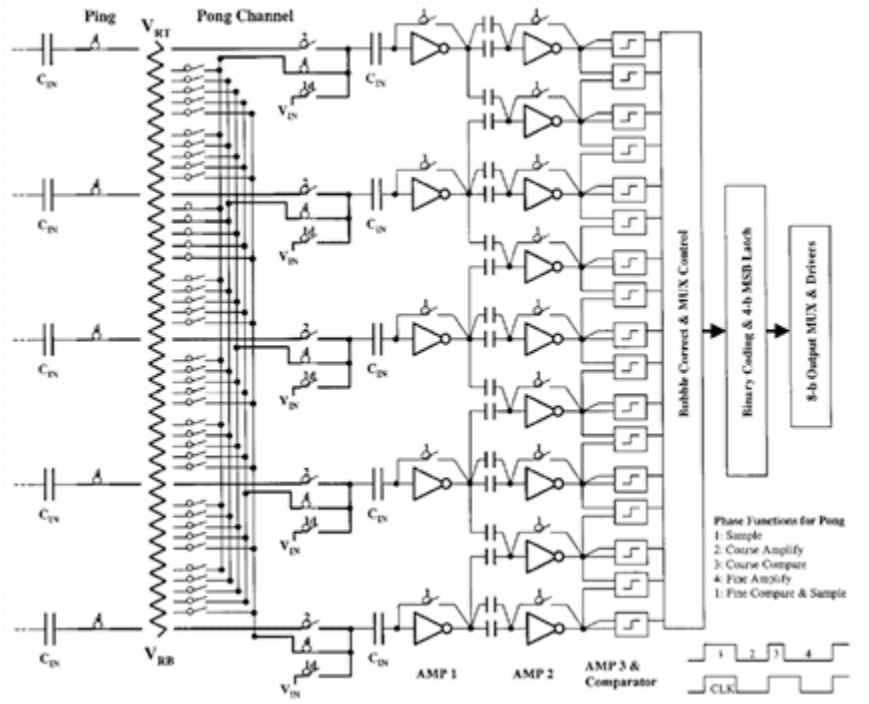

Fig. 4. Unified subranging ADC architecture, showing one complete analog channel (Pong, right), and part of the second interleaved channel (Ping, left). Both channels share the polysilicon reference resistor ladder with top node V_{RT} and bottom node V_{RB} . The switches connected to the C_{IN} s are T-gates,whose number indicates during which phase they are closed. The functions for each of Pong s phases are described bottom right).

Fig. 4 shows a detailed diagram of the fully unified ADC architecture. To achieve one conversion per clock cycle for the two-step algorithm, two channels are interleaved. Each works at one-half the conversion rate, and 180 out of phase. As shown, the two interleaved analog channels, Ping and Pong, are connected to a common reference ladder. The Ping channel is performing a coarse amplify using the coarse voltage taps on the reference ladder at the same time that the Pong channel is performing a fine amplify. Polysilicon resistor ladder terminals V_{RT} and V_{RB} define the conversion range. The switches leading to the input capacitor C_{IN} are T-gates, and their corresponding numbers show the phase during which they are closed. The Pong channel is shown in complete detail, including a functional description of each phase. During phase 1, V_{IN} is sampled by a distributed network formed by the five input capacitors, as previously described. In phase 2, the difference between each sampled voltage and the indicated major tap points on the reference ladder are amplified by amps 1, 2, and 3. During phase 3, this resulting difference is regenerated in 17 comparators to obtain the MSBs as demonstrated in Fig. 1. Because of the by-4 capacitive interpolation, the 17 digital outputs required just five front-end sampling capacitors. The coarse bits are latched at the end of phase 3. In phase 4, one of the 16 MUXs is switched onto the MUX bus, to generate the fine difference voltages, so that the four LSBs can be obtained by the comparators during the following phase 1.

To be continued in the July edition of the *National Edge*.

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