***LVDS based FPD-Link spans industries with Gigabits @ milliwatts!***


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# Technology Edge

## LVDS based FPD-Link spans industries with Gigabits @ milliwatts!

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LVDS is a high-speed low-power interface that is not only the defacto standard in Notebook displays today, but is also used in many datacom and telecom applications due to these very same benefits. It provides very high line transmission rates, requires little power, generates low noise levels, and is very robust. It is also able to reject common-mode noise that is twice the magnitude of the actual differential signal magnitude and is even hot-pluggable.

LVDS has evolved dramatically since its introduction by National as line drivers and receivers back in 1992. Since then it has evolved into FPD-Link (Flat Panel Display Link) targeted at Notebook displays and LDI (LVDS Display Interface) targeted at longer distance applications such as large embedded displays, All-in-1 PCs, and even Desktop Monitors. The semiconductor industry has also widely adopted the LVDS physical layer. This is evident by the wide array of suppliers which showcase LVDS products on their web sites. Line drivers and receivers are available from National Semiconductor, Texas Instruments, Pericom, Maxim, and Linear Technology to name a few. FPD-Link, invented by National back in 1993, is seconded sourced by Texas Instruments (Flat Link) and also Thine. This is not the end of the list of LVDS suppliers, there are many ASIC and FPGA vendors touting LVDS I/Os, multiple graphic chip manufactures have versions of their GUI controllers with the FPD-Link/LVDS transmitter integrated with the GUI. There is even one notable TMDS supplier that ships LVDS parts today (FPD Link Receivers integrated with timing controllers). This very wide base of support is driven from two angles, first is the inherent benefits of LVDS which are also know as the three Fs: fast, far, and friendly to use. The other is the wide market applicability of LVDS. LVDS has become the backbone interconnect of wireless infrastructure equipment, and the box hopping cable driver/receiver for datacom stackable hubs. It is also being deployed in imaging equipment, cameras, copiers and at the other end of the spectrum in automotive entertainment systems.

LVDS started back in the early 1990s at National, and was developed to provide an alternative to high power ECL line driving. By lowering the power level, several limiting attributes of ECL could be improved on. These included: the use of common power supply rails, compatibility with lower voltage power supply rails, higher levels of integration, and compatibility with low cost IC packaging. Once this was accomplished and validated, then integration started. National worked with several notebook manufacturers in Japan to define and implement what was to become FPD-Link. This chipset was a hit with the market and enabled XGA displays. National alone has shipped over fifty million chips to date not counting any of the other supplier s second source chips. It is estimated that over 95% of all notebooks shipped today with XGA resolution displays or higher utilize an LVDS interface.

Why was FPD-Link a hit? At that time SVGA displays where first being introduced. The pixel bandwidth demand of the panels was in the 720Mbps range. Prior to LVDS this bus was simply a wide CMOS single-ended bus; 18 bits wide plus three control signals and clock. This implementation was a challenge to notebook design. Power dissipation was high due to the three or five volt swing and also the transmission line load, noise margins were thin due to the single-ended transmission approach, and EMI was high due to: the swing, output current magnitude, output edge rate and transmission line. This typically required external filters of Rs and Cs to smooth the transition and therefore lower EMI. This approach consumed board space and drove up system cost. The old solution would have been to simply add more lines to increase throughput, but this would only aggravate the above issues. The problem was not this simple, as notebooks were on a miniaturization trend, the hinge area where the wires would pass through from mother board to display was also getting smaller, so adding more wires simply could not fit. FPD-Link came to the rescue, the chipset was composed of a transmitter that collected up the 18-bits of RGB information plus the three control signals and clock and converted that into 3 LVDS data pairs and clock. This provided multiple benefits from the start. First, the bus was squeezed from 22 lines to only 4 pairs. Instead of routing 22 lines through the hinge, only 8 wires were required now. This was an astounding 64% reduction in raw conductor count. Back on the motherboard, in most cases the external RC filters on the CMOS digital output bus could also be removed, lowering cost and freeing up printed circuit board space. Over on the

panel, the complementary function was deployed. The FPD-Link receiver deserializes the LVDS streams, and provides the pixel data and control signals to the TCON (Timing Controller) on the panel board. The block diagram of the FPD-Link device is shown in Figure 1.

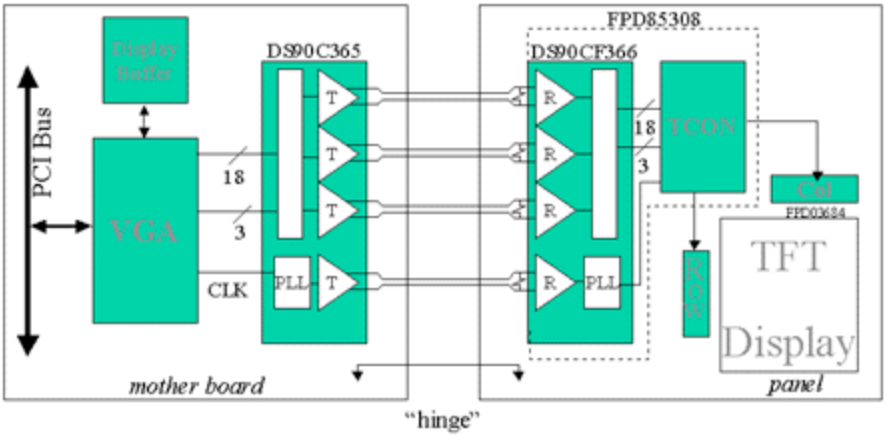


***Figure 1:*** *FPD-Link Block diagram*

Over the years FPD-Link has evolved 5 generations at National. These support lower voltages and higher resolution displays. Table 1 highlights the notable advancements that each generation brought to the industry:

| Year | National Chip | Application and Advancement |
|---|---|---|
| 1995 | DS90CF561/2 | 5V supply, supports SVGA at 40MHz or XGA with Dual pixel interface at 32.5MHz |
| 1996 | DS90CF563/4 | 5V supply, supports single pixel XGA at 65MHz |
| 1997 | DS90C383/4 | 3.3V supply, supports XGA at 65MHz, 8 bit resolution |
| 1998 | DS90C385/6 | 3.3V supply, supports high resolutions panels up to 85MHz |
| 2000 | DS90C387R | 3.3V supply, 12-bit DVO input, up to 85MHz |

***Table 1*** *FPD-Link Generations*

LVDS also evolved into LDI which stands for LVDS Display Interface. This was first jointly proposed to the VESA industry association jointly by National Semiconductor and also Texas Instruments in June 1998. National implemented the chipset, and it further enhances the capabilities of FPD-Link in line speed, throughput, and cable drive capability. Pixel clock rate support was raised from 65MHz to 112MHz doubling bandwidth. Next the chip was defined to be a dual pixel device. This meant it featured 8 serialized channels and supported 48 bits of pixel information. This doubling of channels also doubled the bandwidth. The faster clock rate support and also the dual pixel support provides over 5 Giga bit per second of throughput. This was enough to drive XGA, SXGA, UXGA, HDTV and even QXGA panels. The dual pixel approach was mocked by some at the time, however the idea has since been validated and is the best approach when cable distance and bit times are taken into account. The LDI chipset block diagram is shown in figure 2.

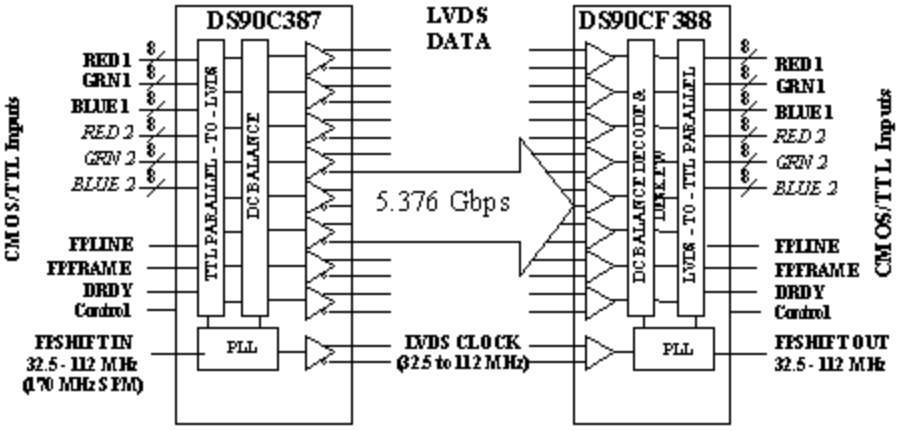


***Figure 2:*** *LDI Block Diagram*

Other enhancements to the chipset included a user selectable pre-emphasis feature, optional DC Balancing of the data payload, and a cable deskew feature. These three features allowed cable lengths to exceed 10 meters in length in most applications, and even 20 meters in some XGA applications.

Pre-emphasis adds additional output current during the transition time to counteract the filtering effects of the long cables (which act as a low pass filter). This provides a wide open eye pattern at the far end of the cable at the receiver inputs. Pre-emphasis is optimal to use, as it does not burn up any bandwidth on the bus. Every bit still carries one bit of pixel or control information.

DC Balancing is also an optional feature for long cable applications typically over 5 meters in length. This prevents the inter-symbol Interference (ISI) problem from closing down the eye pattern. Instead of sending long strings of ones or zeros that can fully charge the cable and then make if difficult for a transition to the opposite state to make it through the receiver s threshold. The transmitter basically monitors the data being sent and compares it to the prior frame of data that was just sent. It the line is charging to one direction too much it simply inverts the current data to discharge the line. Decode at the receiver is very simple, the receiver only needs to look at a flag bit which informs the receiver to invert the data back to its original state if set. This feature also helps to open the eye at the far end of long cables but comes with a penalty. The bit that is used to flag the receiver no longer caries pixel information. So for every 7 bits of data sent down a link, only 6 are carrying real information. Thus the link is 6/7 efficient or in percentage 86%. LDI (in non-DC Balanced mode) and FPD-Link sends 7 bits of information every 7 bits so they are perfect or 100% efficient. Other schemes are less efficient. Using an 8b/10b code (8 bits of information sent in every 10 bits) is only 80% efficient.

Twisted pair cables are commonly used on long cable applications due to their favorable cost, small size, and flexibility. They also tend to only have a single overall shield (unlike the shield per pair in twin-ax cables). But the twisted pair cables can have skew. Skew is defined as the difference in electrical length between the conductors of a cable. Pairs that run down the center of a cable tend to be shorter than ones that run down the outer rings of the cable. This can present a challenge for serialized data lines that are sent in parallel (8 plus clock in the case of LDI). Phase difference between the clock and data lines for FPD-Link was required to be in the 200 to 400ps range depending upon system details like clock rate. This was more than enough for the typical notebook with interconnects less than 12 inches in length. It has even been proven to be more than enough in other larger applications that used FPD-Link. Cables lengths of a few meters are commonly used. LDI wanted to further enhance this specification and extend the reach of FPD-Link. The LDI chipset when used in DC Balanced mode automatically provides the cable deskew function during the blanking interval. It is capable of deskewing up to +/- 1 LVDS bit time, and is very useful in deploying low cost twisted pair cables that are 5+ meters in length. These three enhancements extended the reach of FPD-Link.

The LDI chipset has also evolved 3 generations at National, supporting lower voltages and adding new features. Several other suppliers provide dual pixel LVDS based transmitters and receivers today also. Table 2 highlights

the notable advancements that each National LDI generation brought:

| Year | National Chip | Application and Advancement |
|---|---|---|
| 1998 | DS90C387/388 | 3V supply, over 5Gbps throughput, 112/224MHz |
| 2000 | DS90C387R | 3.3V supply, 12-bit DVO input, up to 85MHz |
| 2001-Q1 | DS90C38xx | 3.3V supply, supports UXGA at 162MHz, Dual Pixel |
| 2001-Q2 | DSxxxxxxx | Scaller functions |

***Table 2*** *LDI Generations*

**LVDS vs. TMDS**
There is confusion in the industry over the LVDS physical layer used by FPD-Link and LDI compared to the DVI Interface which uses the TMDS physical layer. The notable differences are discussed next.

**Output Driver Details**
LVDS is a push pull current-mode line driver. It steers a current down one side of the pair which returns on the other side of the pair. This is true odd-mode transmission, with equal and opposite current flow in the pair. This allows the driver to drive twisted pair, twin-ax, flex, or any closely-coupled trace without generating large amounts of EMI. This is due to several factors which include: the soft transitions of the LVDS driver, the low magnitude of current (3mA), the small voltage swing (300mV), the resulting small area of the ring attenna (created by the pair), and the tieing up and canceling effects of the fields due to the odd-mode transmission. The TMDS driver is also differential but steers current from one side to the other. DC wise current flows in only one side of the pair not both. This is the reason that the proximity of the power and ground lines to the signal pair is so important to control EMI. For this reason twin-axe cables tend to be recommended which use a shield per pair to contain the EMI and also provide a near by return path. The number of shields in a cable drives up cable cost at a much higher rate than the number of conductors in a cable.

**ANSI Open Standard**
LVDS as defined in the ANSI/TIA/EIA-644-A standard. This open standard is capable of rejecting up to +/-1V of common mode noise which can be coupled noise, or ground differences between the nodes of the bus. LVDS by its true differential nature provides a robust noise tolerant interface without restrictions of power supply voltages between the driver and receivers. It is common to have a driver powered from a 5V rail talking to a receiver powered from 3.3V with LVDS.

**LDI vs. DVI**
The two physical layers are used in their respective standards. DVI uses TMDS, and LDI uses LVDS. Once again there are notable differences between the two. These are discussed next.

**Pair Count and Shielding**
A 6-bit single pixel application using a LDI or FPD-Link interface requires 3 data pairs plus clock. The same application using DVI also requires 3 data pairs plus clock.

An 8-bit single pixel application using a LDI or FPD-Link interface requires 4 data pairs plus clock. The same application using DVI also requires 3 data pairs plus clock.

An 8-bit dual pixel application using a LDI interface requires 8 data pairs plus clock. The same application using DVI requires 6 data pairs plus clock (or 2 clocks if using 2 ICs).

DVI may require the same or 1 or 2 less pairs depending upon the application. But cable cost is not over pair count alone. Cable construction and the number of shields also come into the equation. Standard twisted pair cables with a single overall shield commonly used with LVDS tend to be lower cost that twin-ax cables, which require a shield per pair.

**MUX by 7 or by 10**

Sending less bits per clock period means larger data bits. Larger bits mean: more margin for data sampling, more tolerance to Process/voltage/temperature and supplier variations of the ICs, and lower frequency signals which translates to lower frequency noise and also lower power. At 160MHz, an LDI data bit is 892ps wide, where a DVI bit is only 625ps wide. Remember that this is the bit width and the bit can error by being early or late, so the ideal margin is only half the data bit at 446ps and 312ps respectively. Now from this transmitter pulse position variance, transmitter jitter, interconnect skew, and receiver strobe positions must be subtracted. These factors drive the case of "the more ps, the better". The two schemes are show in figure 3 below.

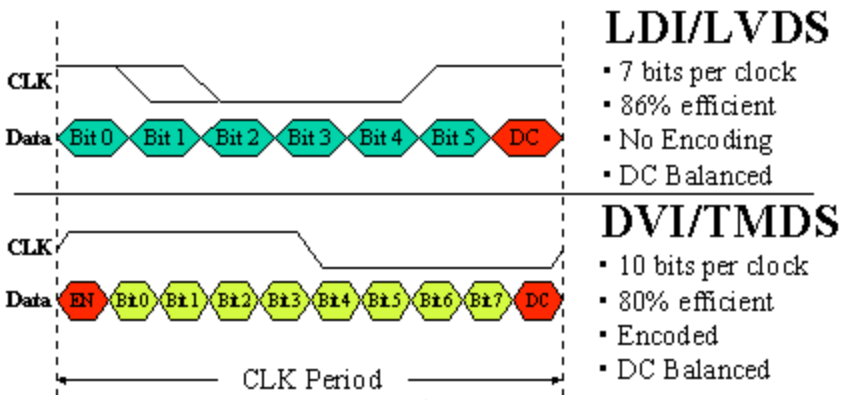


***Figure 3:*** *Data Bits per Clock Period DVI and LDI*

**Bandwidth of the Codes**

LDI when used in DC Balance mode is 86% efficient as discussed above. DVI is less efficient and is only 80% efficient. A dual pixel DVI application operating at 160MHz would be sending 1.92 Giga bits of wasted information that is not RGB pixel data. This is due to the encoding overhead alone.

**Minimize Transitions?**

LDI does not attempt to minimize transitions while sending active data. Since it operates at lower rates due to the divide by 7 this was not deemed necessary. During blanking, the LDI chipset sends the control bits (VSYNC, HSYNC, and DE) and also performs the deskew operation. What is unique about this is that the special characters (7 bits) it uses for these operations have only 2 transitions per frame. Blanking, if CRT compatible timing is used is about 25% of the total time. Thus LDI minimizes transitions 25% of the time for free. This minimizes power dissipation, keeps complexity low, and also keeps the repetition rates low. DVI on the other hand only minimizes transitions during active data. Some papers site 22% less transitions which is a good thing indeed and helps to reducing the higher frequency signaling that the 10 bit mux brings. The interesting thing is that during blanking, the special characters that DVI sends maximize transitions. So with CRT compatible timing, transitions are **maximized** with 8 per pair during blanking. This offsets the gains made during active data and increases power dissipation. Some case studies have shows that with typical data patterns, and taking into account blanking, that LDI has fewer transitions that DVI. The math of this is shown in table 3. The following example is based on an 8-bit single pixel application and compares LDI to DVI. Even with the one less data pair required, and the transition minimized code, the math proves that LDI has fewer transitions.

| **Active Data & Blanking** | **LDI** | **DVI** |
|---|---|---|
| Active Data 72.5 % | 3.5 transitions x 4 Pairs = 14 | 3.12 transitions x 3 Pairs = 9.36 |

| | | |
|---|---|---|
| Blanking 27.5 % | 2 transitions x 4 Pairs = 8 | 8 transitions x 3 Pairs = 24.0 |
| **Total 100 %** | **Total = 12.35 transitions avg.** | **Total = 13.39 transitions avg.** |

***Table 3*** *Transition Comparison*

Note: with 8 bits of data, avg. is 4 transitions, 4 22% reduction of transitions = 3.12
Example: 0.725(14) + 0.275(8) = 12.35

**Power Dissipation vs. Features**
LDI gains its low power dissipation attribute due to the lower switching rates of the data and also since it is less complex than its rival. The DC Balancing scheme and deskew feature provide the right amount of performance without burning excess current and adding complexity. This has also been one of the success points of FPD-link; it offered the right level of integration without consuming more than its share of power dissipation.

**The future of LVDS**
LVDS based FPD-Link is the defacto standard in notebooks, and higher levels of integration are continuing to further its market dominance. Integrated transmitters are available from several GUI chip suppliers for mainstream applications. Also, discrete receivers are less common today, as integration of the receiver with a timing controller eliminates the CMOS single-ended interface from FPD-Link receiver to the TCON. This helps to reduce EMI, footprint, cost and power dissipation of the TFT display module. Discrete transmitters and receivers are common on leading edge systems that push the performance above the available integrated parts in both process and features. LVDS has also created a new interface know as RSDS for Reduced Swing Differential Signaling. This interface, also invented by National brings all the benefits of LVDS performance to a chip-to-chip interconnect between the TCON and Column Drivers on the panel. Since it is more of a controlled environment and not connected via long cables, the swing was reduced even further to lower power and noise. This is the "RS" of RSDS. This exciting interface has enabled a new era of TFT flat panels that are thinner and more robust than their predecessors, and will continue to shape and drive TFT displays into the next generation of platforms and resolutions. LVDS and FPD-Link will continue to drive Notebook displays into the future. And joining the notebooks will be the Embedded displays leveraging the cost basis and performance of LVDS based Notebook displays. As for the desktop display standard, only the market and time will tell which competing standard will dominate. DVI holds the endorsement of a few key players, but in the end, market demand, ease of use, inter-operability, scalability, and economics are the driving factors which determine the winner. LVDS is delivering Gigabits at milliwatts for the datacom and telecom markets today along with notebook displays, and it stands ready for desktop displays as well.

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