DS92UT16

LVDS Product Selection: The benefits of LVDS in an ever-increasing portfolio of products

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The benefits of LVDS in an ever-increasing portfolio of products

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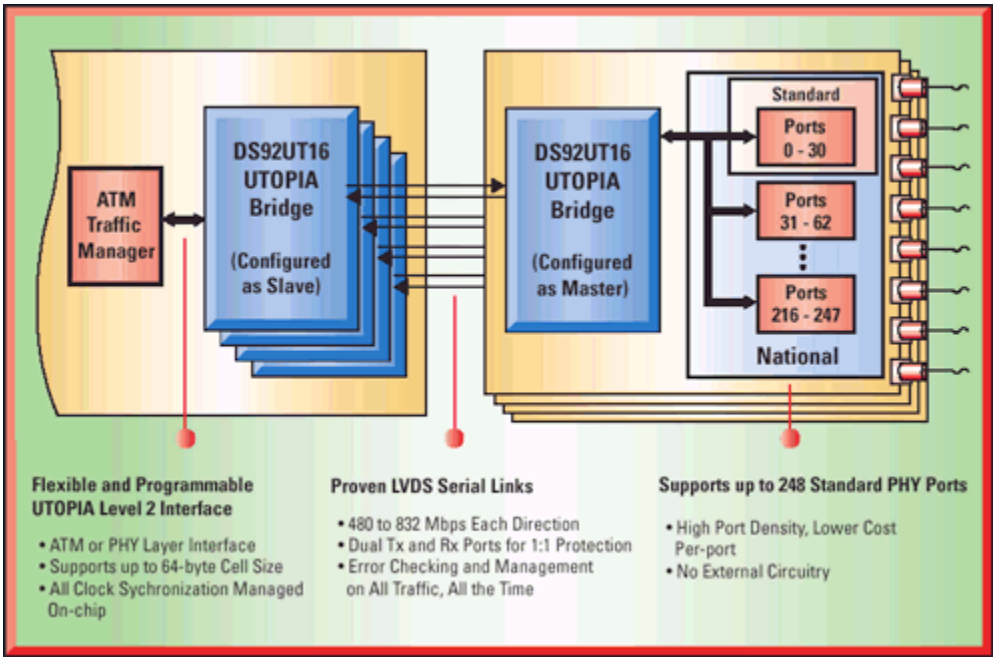
As technology becomes more integrated and the functionality of electronic systems becomes more complex, there is an increased need for a reliable way to transmit large amounts of data. Whether the data are going from chip-to-chip, board-to-board, or rack-to-rack, low-voltage differential signaling (LVDS) is a popular solution that can be used in many applications.

Meeting the LVDS standard

The LVDS (ANSI/TIA/EIA-644-A) standard was developed in 1995, and the fundamentals on which it was based give it many attractive qualities. LVDS typically uses a current-mode driver output from a 3.5-mA current source. This drives a differential line that is terminated by a 100-W resistor, generating about 350 mV across the receiver.

The ±350-mV voltage swing is typically centered on a 1.2-V offset voltage. Since LVDS uses a differential line, magnetic fields radiating from the media are canceled and little noise is produced. Also, using the current-mode driver lowers the risk of ringing or switching spikes. The differential method further enhances LVDS capabilities as the differential receiver rejects common-mode noise from external sources.



Bus LVDS technology enables multidrop configurations for distributing the UTOPIA bus to multiple bridge receivers with a 16-m cable length.

The excellent noise performance is not only desirable, but necessary to maintain and detect the low-voltage swing. This low-voltage swing, together with controlled edge rates, allow for high data rates ranging from 100 Mbits/s to over 1 Gbit/s.

The power consumed by the load is small because of the low-voltage swing and low-current source, 3.5 mA x 350 mV = 1.2 mW. Further advantages can be realized as higher data rates typically result in smaller bus sizes and, in turn, reduced cable and connector sizes.

LVDS is also a prevalent standard, as many semiconductor manufactures now supply a wide variety of drivers and receivers. Parts are available from National Semiconductor, Texas Instruments, STMicroelectronics, Maxim, Fairchild, and Pericom. Also, FPGA vendors such as Xilinx and Altera, and ASIC suppliers like LSI, are implementing LVDS I/O into their products. These manufacturers have designed chips useful in a wide variety of applications such as point-to-point data transmission, multidrop or multipoint bus architectures, serializing and deserializing, switching data, and distributing data.

Transmitting signals

Many simple drivers and receivers can assist in transmitting an LVDS signal from one point in a system to another. Several companies have wide portfolios of parts with single, dual, quad, octal, and even 16 input and/or output configurations that send LVDS signals at rates of over 600 Mbits/s.

It is also possible to transmit low-speed signals like TTL, CMOS, or LVPECL across an LVDS link, by performing simple level translations. In fact, many parts are designed to accept TTL/ CMOS or LVDS level signals directly on the input. Other drivers can accept LVPECL or LVDS inputs and act as translators.

Serializing/deserializing

Devices have been developed to serialize slower parallel buses in order to increase the amount of data that can be sent in a given period of time. This also results in a much smaller bus width, reducing cost in the system.

It may also be advantageous to serialize data primarily on the basis of reducing bus size. Large buses like the universal test and operation physical interface (UTOPIA) used in ATM switch fabric can be expensive to implement.

For example, the DS92UT16 LVDS bridge from National Semiconductor uses the high-speed capability of LVDS to serialize the UTOPIA bus into two differential pairs, one in each direction. This device allows the engineer to select either UTOPIA level 2 ATM layer (master) or PHY layer (slave). Bus LVDS technology enables multidrop configurations for distributing the UTOPIA bus to multiple bridge receivers with a 16-m cable length (see *figure*).

Backplane/multipoint architecture

Another popular implementation of LVDS, especially in telecommunications, is the backplane or multipoint architecture. These systems are designed so that several transceivers can be plugged into a single backplane. The system can be configured in one direction so that several slave cards receive information from one master card, or bidirectionally so that all the cards can communicate with one another. Typically, for these applications, parts are designed with a higher output current so they can drive a doubly terminated differential line.

In addition, National and TI have recently co-developed Multi-point LVDS (M-LVDS, TIA/EIA-899), which is a bidirectional standard that specifies a doubly terminated backplane with up to 32 nodes and data signaling rates up to 500 Mbits/s. The parts are expected this year.

Many times, such as in telecommunications, it is advantageous to route or switch signals to varying locations within a system. National, Maxim, TI, and Fairchild have developed cross-point switches to enable an engineer to multiplex, demultiplex, repeat, or split an LVDS signal.

When timing margins are tight, as with a high-speed system, it is generally necessary to have very uniform and precise clock signals throughout the circuit. Using LVDS clock repeaters will result in very little distortion and EMI that may disrupt important data signals on the board.

Another feature that is now being added to some LVDS products is in-system testing such as IEEE 1149.1 boundary-scan (JTAG) and At-speed built-in self-test (BIST). JTAG features ensure system integrity by checking for proper installation and uninterrupted board-level interconnects.

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