

Advanced Technology and New LDO Features for Highly Demanding Applications



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Technology Edge

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Most designers would agree that linear regulators are one of the most easy-to-use types of regulator available and, for that same reason, usually their most preferred type. But in today's highly demanding applications, it is increasingly difficult to get a high-performance design running by utilizing only linear solutions. This is when the questions arise: What resources can the designer use to his or her favor? What are the trade-offs and the actual limitations for choosing linear technology for DC-DC conversion over other topologies? Which LDOs have better efficiency than others for the same application? Does choosing one manufacturer's linear regulators over another make any difference?

The answers to these questions are not as simple as one might first think. There are several factors and specifications that make a major difference which are often overlooked that system designers need to consider. As power requirements increase, board sizes decrease, and minimum performance needs to be maintained, selecting the right LDO for the application can mean the difference between an effective or unworkable solution.

Heat, efficiency and packaging

All power that is pulled from the linear regulator's input that is not delivered to the output is simply dissipated as heat.

Dissipated power (P_d) is roughly estimated as:

$$P_d = (V_{IN} - V_{OUT}) * I_{OUT}$$

For a more accurate calculation, the term $V_{IN} * I_q$ needs to be added. Total dissipated power is then calculated as:

$$P_d = (V_{IN} - V_{OUT}) * I_{OUT} + V_{IN} * I_q$$

By using these above equations, downconverting 5V to 1.5V @ 350 mA makes a linear regulator dissipate at least:

$$(5 - 1.5) * 0.35 = 1.225W$$

of power as heat. Whether one considers this number high or low, the picture is not complete until it is determined to what extent those 1.225W will cause the IC temperature to rise as a function of the packaging, and (if surface mounted) the type and size of the PCB board used. While designers usually prefer the smallest standard package available, those typically provide the worst thermal performance as they have the highest thermal resistance values.

Small packages such as standard SOT-23 and SC-70 have q_{JA} values in the order of 200° to 400°C/W. Medium-sized SOT-223, TO-252 (DPAK) and other exposed-pad SMD packages (including PSOP and ETSSOP) have q_{JA} values in the 50° to 90°C/W. Usually only large packages (such as TO-220 and TO-263) have a favorable 40° to 60°C/W. The one exception to the package size rule is the leadless leadframe package (LLP®) because of its internal construction - the die is sitting directly top down on the metal that is exposed on the bottom of the package. (This is the only sub-miniature package that can offer thermal resistances as low as those found in their much larger counterparts.)

How much of an effect can these numbers have? With $P_d = 1.225W$, SOT-23 (2.85 mm x 3 mm) would theoretically have a temperature rise of at least 300°C; DPAK (6.6 mm x 9.7 mm) would rise around 80°C over ambient and only TO-263 (10.4 mm x 14.35 mm) or LLP (2.9 mm x 3.3 mm) would have a mere 50°C temperature increase. Wisely selecting the linear regulator IC package can determine whether or not the designer needs to migrate to a switching alternative.

I_q and CMOS LDOs

Quiescent current, or I_q (also called operating current or ground current), is an important factor for designers of low-power, minimal-current, battery-powered applications. But how often is it reviewed when discussing 1A, 2A, or 3A constant loads?

Hardly ever - a potentially costly mistake. Depending on the process technology used to build an LDO, I_q can dramatically increase with load current. Using bipolar LDOs as an example, I_q at 3A of load can be 200 mA or more. On the other hand, CMOS LDOs commonly have very low, load-independent I_q of 3 mA to 15 mA for full 3A loads or 100 μ A to 6 mA for 1A/2A loads. (See Figure 1 for a comparison of supply current vs load current in CMOS and bipolar manufacturing process technologies using standard 150 mA LDOs.)

So why is 200 mA vs 6 mA important for I_q when I_{OUT} is 3A anyway? As discussed earlier, total dissipated power determines whether or not an LDO is a viable solution, and while the first term in Pd is application driven (determined by V_{IN} and V_{OUT}), the second is totally I_q dependent and can turn into a discriminating factor. At 3.3 V_{IN} , for example, 200 mA of I_q means adding 660 mW of power to Pd or needing to migrate to a switcher solution. However, with 6 mA I_q , Pd will only increase around 20 mW (making almost no impact to the total dissipated power) and the designer can still effectively use linear regulators by wisely selecting the CMOS low- I_q alternative.

When shopping for I_q , it is always advised to review the inside pages of a datasheet for the values at full load. In our industry, it is easy to be misled with top-level I_q data from the datasheet specifications, which typically state values at minimal or no load.

Dropout and low V_{IN} LDOs

Is this low dropout regulator really low dropout? Think again. Datasheet specifications may claim 100 mV dropout (which might be true for any input voltage larger than the IC minimum V_{IN}), but if the application needs 1.2 V_{OUT} or lower (as many require these days) and the regulator needs at least 2.5V at the input to run (as with the typical 2.5V to 5.5V input range regulators), then the real dropout in the application is:

$$2.5V - 1.2V = 1.3V$$

Potentially, the application could run adequately, but the dissipated power (Pd) will carry all of the burden.

If a 1.5V rail or a 1.8V rail is available in the system, selecting an LDO with a lower minimum V_{IN} can severely increase efficiency, as well as reduce temperature rise and dissipated heat, even while the “published” dropout is the stated 100 mV. Using a 500 mA load for a 2.5V minimum V_{IN} LDO as an example:

$$Pd = (2.5 - 1.2) * 0.5 = 0.65W$$

However, for a 1.5V minimum V_{IN} LDO if used instead in the same application:

$$Pd = (1.5 - 1.2) * 0.5 = 0.15W$$

A 500 mW difference in Pd is definitely not small — would anybody deliberately give it away?

Conclusion

With today’s highly demanding applications, it is not as straightforward as it once was to design effective solutions using LDOs. However, by choosing regulators wisely, designers can still implement extremely cost-effective, low component-count, easy-to-design linear architectures by taking advantage of many usually overlooked parameters or by leveraging features not found in previous generations of LDOs. Some of these new key features include advanced thermally enhanced subminiature packaging, low I_q through the entire load current, ultra-low input voltages, and advanced CMOS LDO manufacturing process technology.

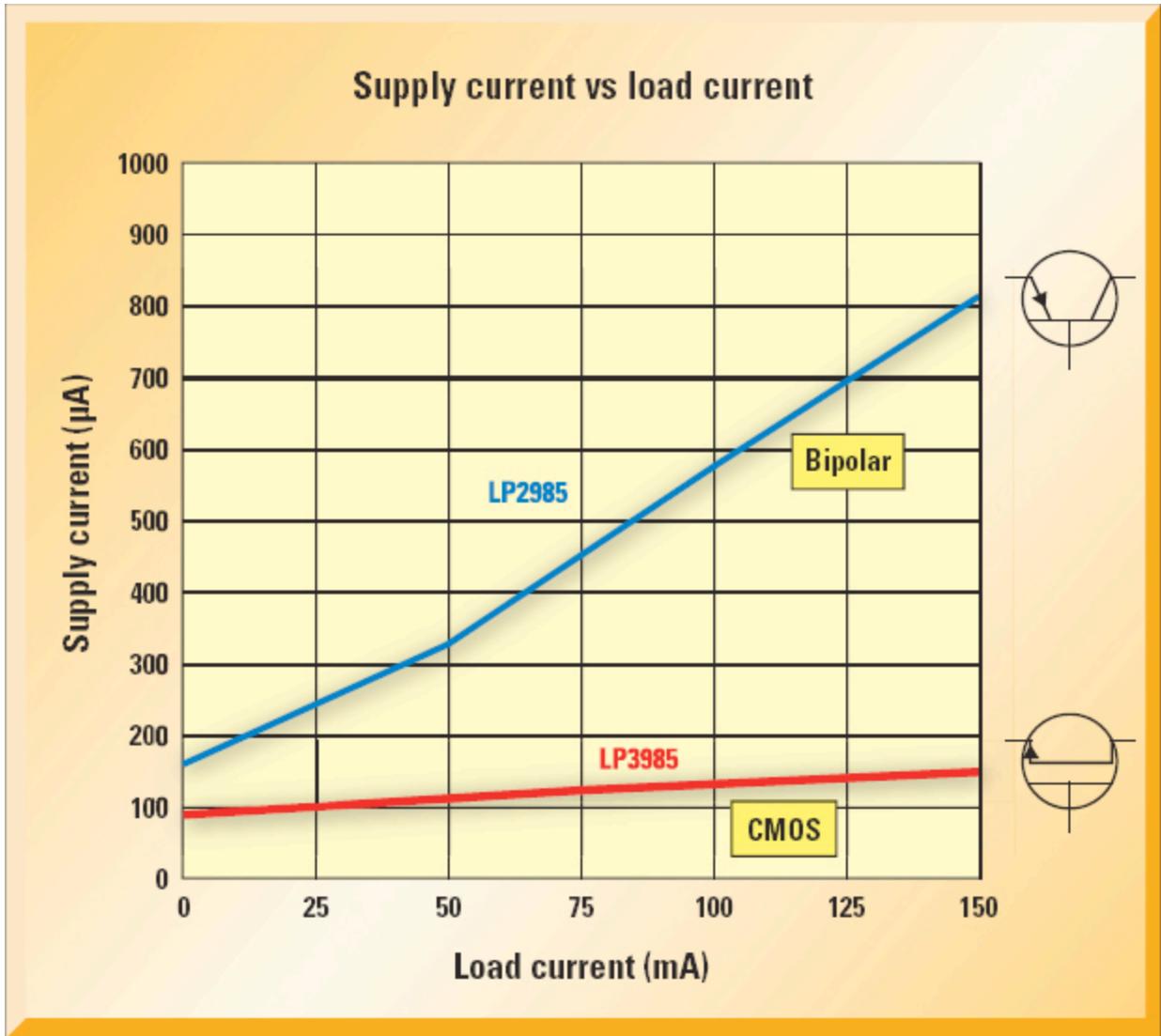


Figure 1. Supply current (I_q) comparison of CMOS/bipolar manufacturing process technologies for similar 150 mA LDOs over full load-current range

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