PowerWise Adaptive Voltage Scaling Minimizes Energy Consumption

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The world is unwiring itself at an astonishing rate. Wireless access points are on the rise world-wide. New modulation schemes are making it possible to do more with less bandwidth. Next generation wireless networks promising unprecedented data transfer rates are around the corner. With all this high speed infrastructure being laid, it is only natural to observe that we will use our wireless devices more and more. We will have higher expectations of our devices to be inconspicuously portable and have Olympic endurance. Manufacturers are quickly realizing that size and run time demands of their portable equipment can not be met by increasing energy density in batteries or even improving power management efficiency – the improvements in these technologies are saturating. To achieve the leap in wireless devices' functionality and run time, manufacturers are turning to high efficiency **energy** management of system functions. Decreasing the amount of energy it takes to complete a function means the battery has more energy left for other processes. This energy management philosophy is being developed for several common wireless functional blocks such as DSP and processor calculations, and the transmitter power amplifier. In particular, innovative ways of efficiently using the processor are becoming prevalent in wireless devices. National Semiconductor and ARM have teamed up to develop an energy management system that reduces the energy consumption of a processor to the minimum amount for a given clock frequency. This method, Adaptive Voltage Scaling (AVS), uses an open standard 2 wire, low power communication interface between the processor and the energy management unit (EMU) called PowerWise^{TM} Interface (PWI). The two combined provide for an intelligent and aware energy management system.

AVS in the general sense refers to a power supply rail that adjusts its voltage corresponding to the demands of its load. The load could be any compliant electronic device, although in the context of this paper, AVS refers to the method of adjusting supply voltage to any digital processor of a mobile phone. The enormous benefit of AVS is that for completing the same function, an AVS compliant processor will use 30% to 60% less energy than a fixed voltage processor. This is the kind of energy savings that will allow heavier use of our wireless devices while maintaining the operating time between charges.

The core concepts behind energy savings in AVS are:

1) The energy stored in every logic cell is proportional to Vdd^2. This comes from the fact that the energy stored in a capacitor is $1/2CV^2$.

2) The propagation delay through each logic cell is proportional to 1/Vdd.

3) If the clock frequency is reduced in a processor, the propagation delays can be longer, thus the supply voltage (Vdd) can be reduced and significant energy savings will be gained.

The way to reduce energy consumption in a processor, then, is to not only to reduce the clock frequency as low as possible, but, more importantly, to reduce the core supply voltage to the minimum amount for a given clock frequency. Figure 1 illustrates the energy savings gained with this method of frequency and voltage scaling.

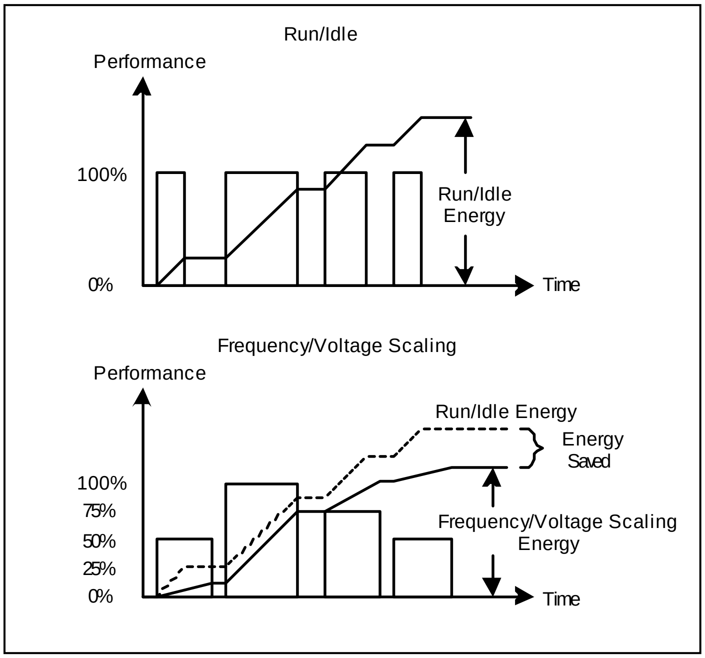

Figure 1. Traditionally, processing tasks are completed in a run/idle fashion. However, more energy savings are achieved by scaling frequency and voltage.

Getting Most of the Way There: Open Loop AVS

A simple approach to AVS is to generate a voltage vs. frequency table. These voltages are the minimum needed to maintain functionality over all parts and temperature. This is the approach used by most of the industry. While open loop AVS can yield a good amount of energy savings, it does not realize all the energy savings available. Every operating frequency/voltage pair in a processor must be characterized such that over parts and temperature the operating voltage is high enough to meet timing criteria. This characterized voltage must also include headroom for the power supply regulation error (typically 5 to 10%). Accounting for process, temperature, and power supply variation, the table based AVS is at best conservative, and requires tedious characterization at all the operating frequencies.

Realizing the Most Potential From Your Battery: Closed Loop AVS

Closed loop AVS brings a fresh approach to energy management. It takes the idea behind open loop AVS and realizes it in a completely different manner. The goal of the AVS system is to reduce the supply voltage to the minimum amount and still maintain critical path deadlines. Open loop AVS accomplishes this by regulating the supply voltage to a pre-characterized value that guarantees operation over process, temperature, and power supply variations. However, regulating to a pre-characterized voltage does not guarantee minimum energy consumption. This is guaranteed when the maximum propagation delay (and thus minimum voltage) is present for any given situation (frequency, process, temperature). Closed loop AVS in fact accomplishes this by regulating the propagation delay margin. In other words, no matter what lot the processor is from, nor the temperature or frequency it is operating at, the specified delay margin is maintained. Because of the voltage/propagation delay relationship, this condition necessarily requires that the supply voltage be at the acceptable minimum at all times.

The Mechanics of Closed Loop AVS

As shown in figure 2, the closed loop AVS system developed by National Semiconductor and ARM has two hardware components: the Intelligent Energy Manager^{TM} (IEM) and Adaptive Power Controller (APC), located in the processor, and the AVS compliant energy management unit (EMU). The ARM IEM determines the minimum performance (clock frequency) required by the processor for given tasks. The APC accepts a performance request from the IEM and determines the minimum voltage the processor can operate at for that performance level. It also commands the EMU to attain the lowest supply voltage for a given clock frequency. It is important to realize that the APC is synthesizable code operating in the processor, and it manages the IEM requests and voltage control without any intervention from the processor. All the software hooks for controlling performance are contained in the IEM. The APC controls the supply voltage transparent to the IEM, however it is coupled to the external EMU. The AVS EMU is equipped to interpret commands from the APC through a new open standard interface, PowerWise^{TM} Interface (PWI). PWI is a low power, 2 pin serial protocol specifically designed to meet the needs of next generation AVS portable systems.

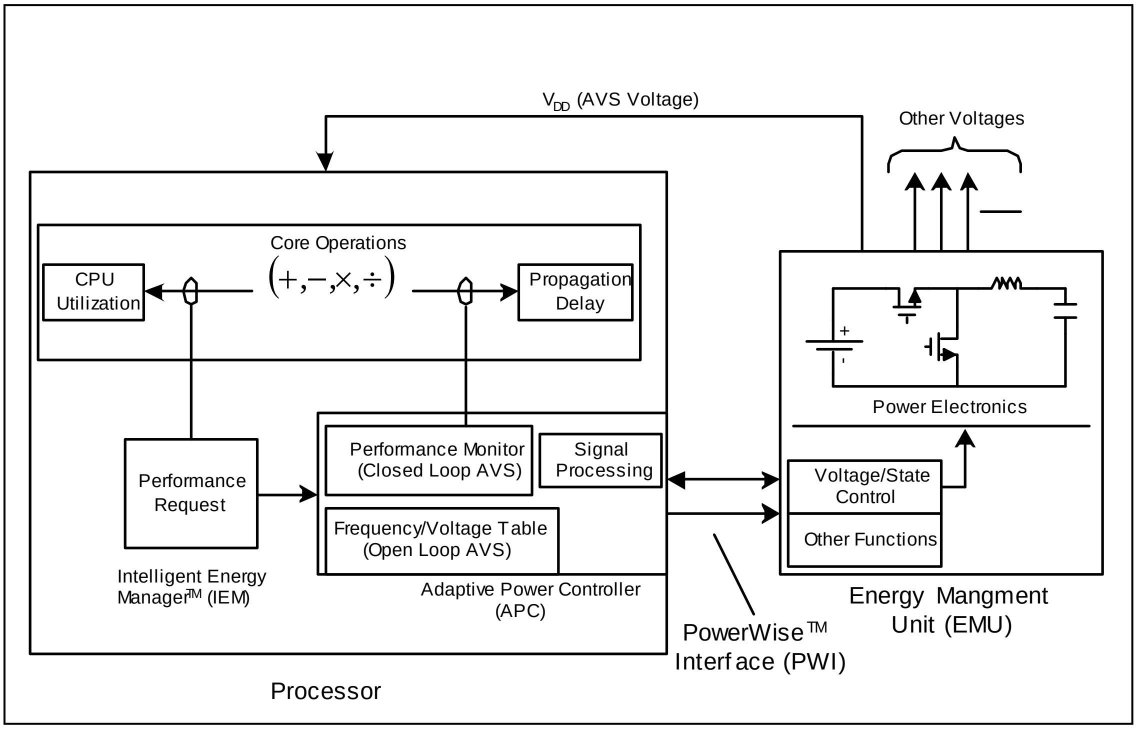

Figure 2. The closed loop AVS system consists of an Intelligent Energy Manager (IEM) and Adaptive Power Controller(APC) located in the processor, and an Energy Management Unit (EMU). The AVS loop regulates propagation delay margin to ensure the minimum supply voltage is achieved.

Closed loop AVS is distinguished from open loop, table based voltage scaling techniques in that it regulates the propagation delay margin in logic cells. In this system, the power supply voltage is a variable that increases or decreases, and the delay margin is a fixed parameter that is regulated over parts, temperature, and clock frequency. Many advantages arise from this methodology. Closed loop AVS relaxes the characterization process. There is no need for characterizing voltage/frequency tables because a delay margin is maintained by the AVS feedback loop. Another incentive is that less demand is placed on power supply regulation. The AVS loop adjusts the supply voltage as necessary, compensating for the +/- 5% tolerance typically allocated to power supply regulation. By and far the most beneficial advantage is that the minimum operating voltage is realized for all conditions, and can dynamically change as conditions change. For example, as temperature changes, the cell delays change, and the thus the voltage is adjusted to maintain the same delay margin – without using voltage/frequency tables. Figure 3 shows this temperature compensation. By using closed loop AVS, the designer can rest assured that the minimum voltage is being applied for any given clock frequency.

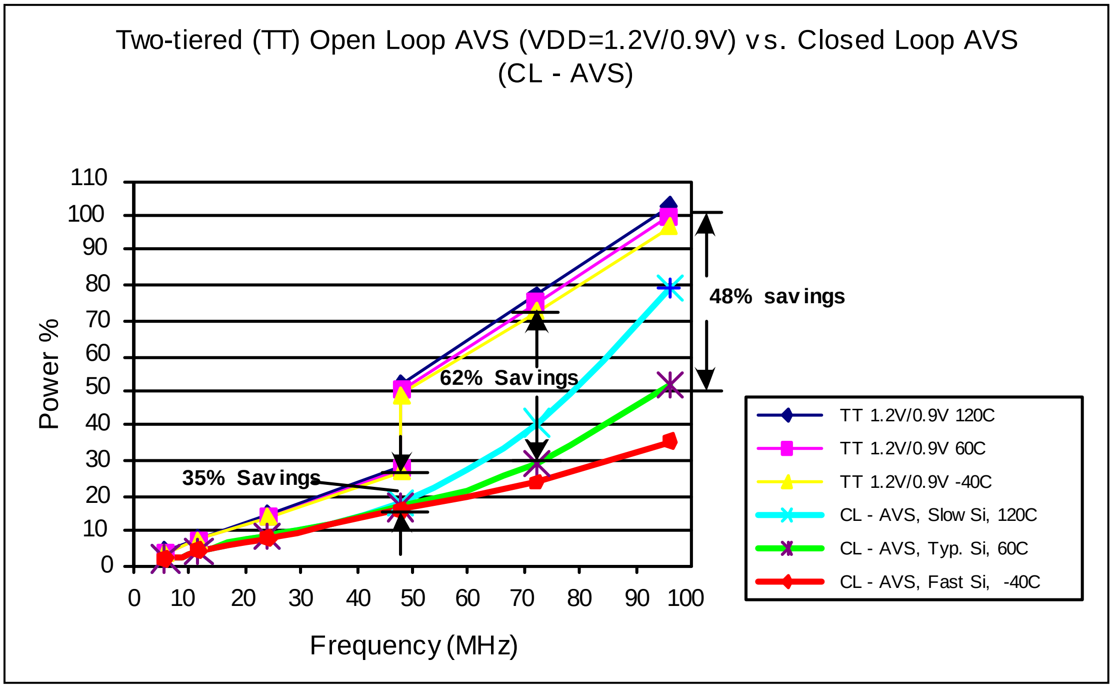

Figure 3. Closed loop AVS tracks temperature and process variations, and yields significant power savings over open loop AVS.

In Summary

The relentless pace at which portable devices are miniaturizing is matched by the rate at which new functions and applications are integrating into them. Batteries can not supply the energy needed to run these features, so the energy requirement itself must be lowered. Closed loop AVS minimizes the energy requirement in a processor by maintaining a minimum delay margin in the internal logic cells. This necessarily requires that the supply voltage be at the lowest value for valid operation. With these properties, systems employing closed loop AVS will require much less energy to run.

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