# Meeting the demand for more efficient and powerful onboard chargers

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## The electric vehicle (EV) market has been growing >40% a year since 2010, with original equipment manufacturers (OEMs) announcing more pure EV models up through the year 2023. The evolution toward more EVs rather than hybrids is a reaction to different countries' environmental policies, which mandate a transition from internal combustion engines (ICEs) to EVs.

In their Global EV Outlook 2017 Report, the Internal Energy Agency stated, "As of 2016,14 countries had established aggressive targets for the rapid deployment of EVs, with plans to phase out vehicles powered by ICEs. This list includes China, Germany, France, the United Kingdom, South Korea and eight states in the U.S. Several countries set a date for eliminating ICE vehicles entirely – see **Table 1**."

| *Country* | *Goal for transition to EVs* |
|---|---|
| *United Kingdom* | *Banning ICEs by 2040* |
| *France* | *End sales of ICEs by 2040* |
| *India* | *EVs only for sale by 2030* |
| *Norway* | *Only zero-emission vehicles by 2025* |

***Table 1.*** *Government plans to transition to EVs.*

Higher-capacity battery Higher-capacity battery packs, while reducing range anxiety, put exacting demands on the charging electronics – specifically the onboard charger. The onboard charger not only needs to accommodate higher power ratings to accommodate the higher power capacity, but it needs to have improved power density (volume and weight) and improved efficiency.

As more electric vehicles enter the market, the challenge for OEMs and Tier 1s will be to provide onboard charging solutions that can support multiple regions with different power-grid infrastructures. For example, EVs in China will need to support connections to a three-phase power line, while EVs in the U.S. will need to connect to a single-phase power line.

OEMs may want to supply variants with different power ratings from 3.3 kW to 22 kW.

Therefore, selecting an advanced topology to support high power with improved power density and efficiency within cost targets becomes more critical.

## Totem-pole PFC

Totem-pole PFC is an advanced power topology that is gaining attention, especially with the advent of wide-bandgap semiconductor devices such as gallium nitride (GaN) and silicon carbide (SiC). GaN and SiC's superior material properties compared to silicon devices enable high-power-switching power-conversion applications at higher temperatures, voltages and pulse-width modulation (PWM) frequencies.

## CCM totem-pole PFC

Because the reverse-recovery charge of a GaN/SiC field-effect transistor (FET) is much smaller and the internal capacitances are smaller compared to a silicon FET, the hard-switching operation of continuous conduction mode (CCM) totem-pole PFC is practical for commercial use. Totem-pole-based PFC has an efficiency advantage, as only two devices are in the path of the current at a time (relative to the traditional bridge-based PFC and recent bridgeless PFC topologies). By limiting the switching frequency to around 100 kHz, it's possible to achieve 98-99% efficiency or higher with a GaN- or SiC-based design because the converter is hard switched.

## C2000™ real-time MCUs for CCM totem-pole PFC

C2000 real-time MCUs are controllers designed specifically for power electronics applications. The TMS320F28004x can control a totem-pole PFC with CCM and with GaN/SiC FETs. The F28004x has inherent device features and software libraries that make development of a totem-pole PFC smaller, cheaper and simpler for faster time to market.

## The features on the F28004x include:

- An optimized central processing unit (DSP) core enabling fast execution of a control loop greater than 100 kHz. The on-chip trigonometric math unit (TMU) accelerates trigonometric operations, increasing control-loop execution speeds when running a software phase-locked loop (PLL) – a requirement in a totem-pole PFC application.
- A control law accelerator (CLA) for offloading current, and voltage control-loop interrupt service routines (ISRs) from the CPU to increase performance and bandwidth. A higher loop bandwidth means better tracking of the input current and thus lower total harmonic distortion, as well as a faster DC bus response and a smaller DC bus capacitor.
- Advanced pulse-width modulators (PWMs) for handling adaptive dead time for zero-voltage switching (ZVS) and phase-shedding techniques, improving efficiency under heavy and light loads.
- An integrated comparator subsystem (CMPSS) that integrates protection for overcurrent and overvoltage without any external circuitry, thus making the board smaller and lower in cost. The flexible X-Bar architecture combines trips from multiple sources such as the CMPSS and general-purpose inputs/outputs (GPIOs) that signal gate-driver faults quickly and easily without external logic or circuitry.

## Speeding up totem-pole control-loop execution

Solving low power factors at low loads often requires special techniques for controlling the input grid voltage for a totem-pole PFC onboard charger. Implementing these techniques (one example being a digital PLL-based vector cancellation) requires a software PLL to control the voltage from the grid. A software PLL can extract and manipulate grid angles but requires many sine and cosine operations that burden control-loop performance. Here, the F280049 TMU can help improve performance.

The TMU is an enhanced instruction set of the C28x digital signal processor (DSP) core that helps efficiently execute trigonometric and arithmetic operations commonly used in control system applications. The TMU accelerates several specific trigonometric math operations that would otherwise be quite cycle-intensive. These operations include sine, cosine, arctangent, divide and square root, as shown in **Table 2**.

| Operation | C equivalent operation |
|---|---|
| Multiply by 2*pi | a = b *2pi |
| Divide by 2*pi | a = b / 2pi |
| Divide | a = b / c |
| Square Root | a = sqrt(b) |
| Sin Per Unit | a = sin(b*2pi) |
| Cos Per Unit | a = cos(b*2pi) |
| Arc Tangent Per Uit | a = atan(b)/2pi |
| Arc Tangent 2 and Quadrant Operation | Operation to assist in calculating ATANPU2 |

***Table 2.*** *TMU supported instructions summary.*

For totem-pole PFC topologies that need to implement a software PLL, the TMU can greatly increase the execution of control code and enable control loops at >100 kHz. This translates into increased efficiency when driving SiC and GaN metal-oxide semiconductor field-effect transistors (MOSFETs).

| Software PLL run without TMU | Software PLL run with TMU |
|---|---|
| 175 cycles | 115 cycles (35% savings) |

***Table 3.*** *Software PLL cycle improvements with TMU.*

## Using the CLA on C2000 MCUs to alleviate the CPU burden

Another way to improve overall real-time control performance for a CCM totem-pole PFC design is through the control law accelerator (CLA). The CLA is a co-processor available on C2000 MCUs. It is an independent floating-point processor that has direct access to control peripherals like the analog-to-digital converter (ADC) and PWM modules. This access enables the CLA to execute real-time control algorithms in parallel with the C28x CPU, effectively doubling system bandwidth and reducing sample-to-output latency.

The CLA enables the offloading of control ISR functions from the main C28x CPU core. For the F28004x device family, you can offload both the control ISR (100 kHz) for the current loop and voltage loop and the instrumentation ISR (10 kHz) to the CLA. On the F28004x, for example, the C28x CPU usage could be greater than 40% for a 100 kHz loop (not including advanced options such as phase shedding and adaptive dead time) and greater than 10% for the 10 kHz loop that runs the voltage loop and instrumentation functions. Thus, the total CPU use could be greater than 50%. The CLA option reduces the CPU burden to 0% when offloading both ISRs to the CLA.

## Advanced PWMs for improved efficiency

In order to increase efficiency in a CCM totem-pole PFC design, the latest generation of C2000 PWM modules can implement advanced techniques such as adaptive dead time and phase shedding. In CCM, the dead-time control for synchronous rectification is critical in terms of short-circuit protection and efficiency. An optimal dead time eliminates the risk of shoot-through and prevents excessive conduction losses from body-diode conduction of the synchronous FET. The goal of optimal dead time is not to turn on the active FET and synchronous FET simultaneously, which requires fine actuation of the PWMs found on the F28004x device, where shadowed action qualifiers and shadowed dead-band can turn on the FETs at the precise time.

In addition to adaptive dead-time control, phase shedding can be an effective technique to improve efficiency in interleaved applications by optimizing for conduction and switching losses. Again, shadowed action qualifiers can provide precise PWM actuation by enabling and disabling phases anywhere within a given AC cycle.

## CRM totem-pole PFC

Designers need to overcome many challenges when implementing a high-frequency totem-pole PFC in order to achieve increased efficiency with higher power density. The first challenge is achieving zero voltage switching (ZVS) across line, load, and the full AC cycle. Although a CCM PFC design can achieve very high efficiency with sufficient total harmonic distortion (THD) numbers, because CCM PFC uses a hard-switching technique (with hard turn-on and turn-off switching), it's not possible to maintain such high efficiency with GaN and SiC at PWM frequencies higher than 500 kHz. Only soft-switching techniques via ZVS or zero current switching (ZCS) can avoid switching losses at these high switching frequencies.

For a traditional totem-pole PFC, it is fairly straightforward to achieve ZVS when the input voltage is less than half the output voltage. When the input voltage is above half the output voltage threshold, however, it may not be possible to achieve ZVS because the diodes do not allow any negative inductor current that would facilitate zero voltage across the FET.

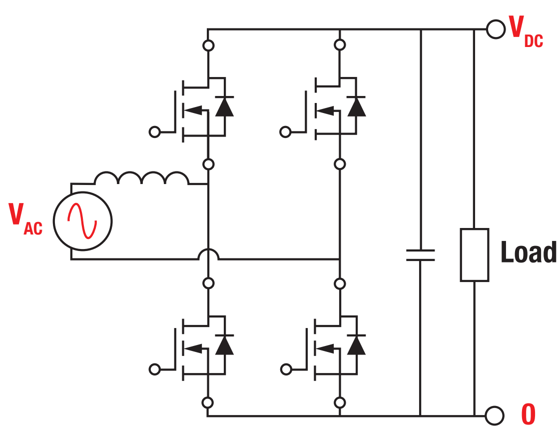


***Figure 1.*** *Totem-pole PFC.*

ZVS is possible if you replace the diodes with low-frequency FETs and operate in critical conduction mode (CRM). This makes CRM totem-pole PFC very suitable for high-frequency applications. Totem-pole CRM PFC uses the resonance between the inductor and FET capacitance to achieve ZVS. With ZVS soft-switching techniques, it is possible to push the switching frequency of CRM totem-pole PFC from the 100 kHz range to the megahertz range, thereby achieving both high efficiency and high power density.

## C2000 real-time MCUs for CRM totem-pole PFC

In addition to the features mentioned in the context of CCM totem-pole PFC, features on the TMS320F28004x will also work in a CRM totem-pole PFC design. A CRM totem-pole PFC uses these features to achieve ZVS across line, load and the full AC cycle:

- The voltage across the MOSFET indicates the presence or absence of hard switching in CRM PFC. This voltage is indirectly measured with tightly coupled features of the C2000 MCU such as the F28004x CMPSS and type-4 PWMs, with the PWM turn-on time instantaneously adjusted to achieve desired ZVS operation.
- Variable PWM switching frequencies require PWMs with global one-shot reload functionality to update all PWMs in a single cycle.

## Analog integration

The CMPSS on the F28004x is a subsystem that contains two windowed comparators and two internal digital-to-analog converters (DACs). The CMPSS can be useful for implementing a CRM totem-pole PFC because when the GaN or SiC FET is operating in hard-switching mode, a simple resistor-capacitor circuit can generate a test signal indicating hard-switching operation. The on-chip CMPSS can easily take advantage of this test signal with its built-in "blanking" feature and send a signal to the CPU indicating hard-switching operation. The CPU can then adjust the turn-on instant of the active PWM to implement a ZVS extension scheme and maintain ZVS operation under all conditions.

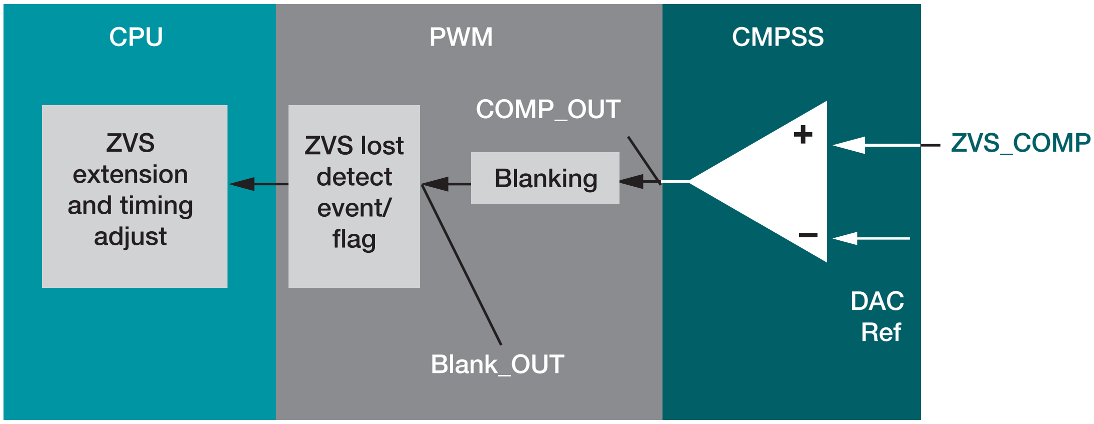


*__Figure 2.__ The CPU can adjust the turn-on instant of the active PWM to implement a ZVS extension.*

The absence of the test signal indicates operation with soft switching, and in the case of soft switching, the CPU decreases the switch off time to avoid operating the converter in discontinuous conduction mode (DCM), which may lead to unnecessary body-diode losses.

## PWM waveform generation for variable frequency

Interleaved totem-pole CRM PFC requires a variable frequency, where the PWM switching frequency of operation frequently changes during runtime. For reliable operation, the changing frequencies must not produce any glitches or irregular PWM behavior. Guaranteeing correct PWM waveform generation for all PWM outputs of an interleaved CRM PFC with changing frequencies under all operating conditions is a big challenge for the controller. Incorrect PWM waveform generation can lead to converter failure or significant system or component damage. **Figure 3** shows how a missed PWM period update can cause a converter failure.

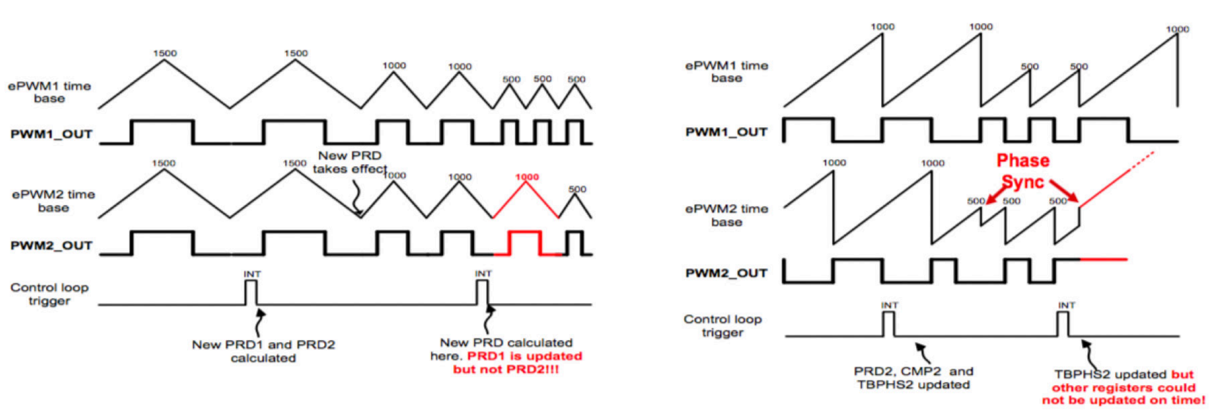


*__Figure 3.__ Challenges for variable-frequency PWM waveform generation.*

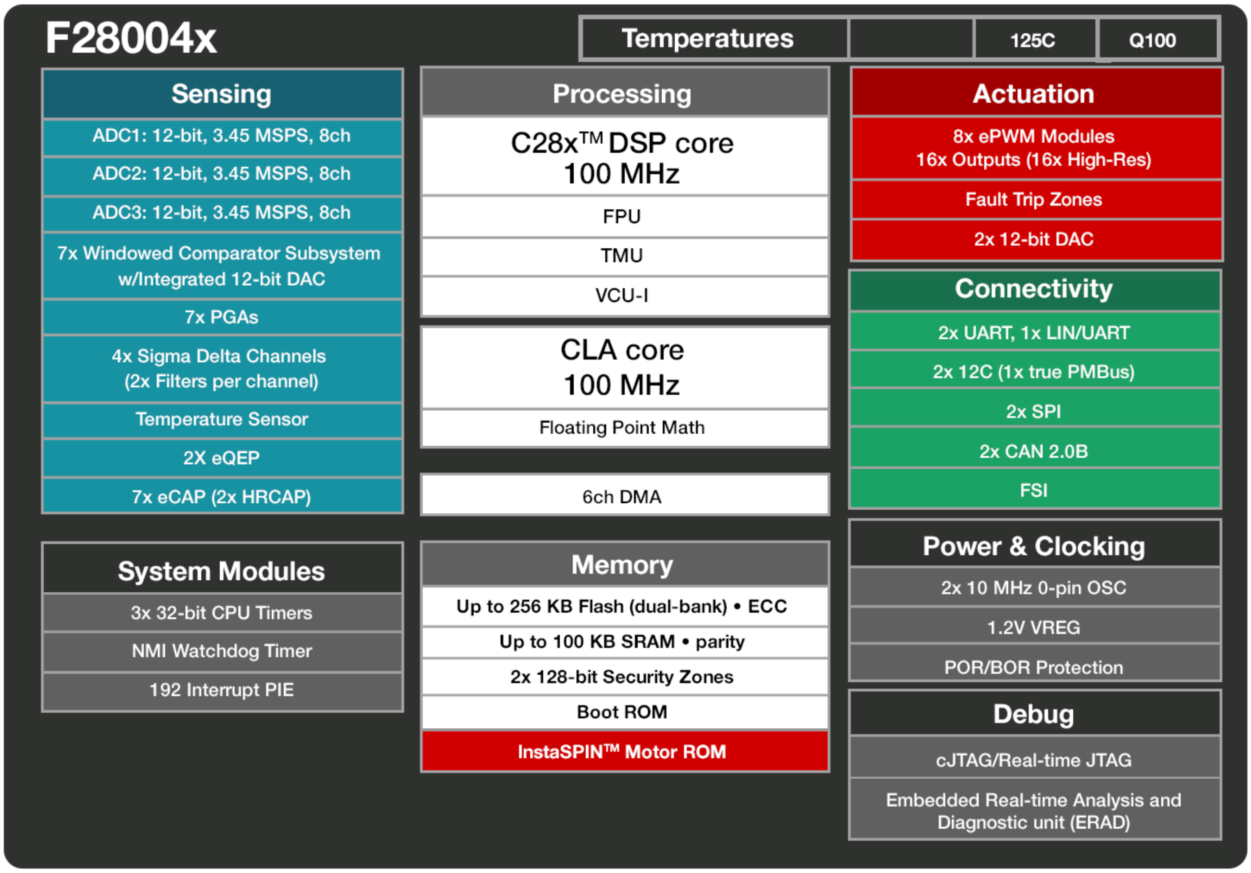


***Figure 4.*** *The new C2000 F28004x series.*

The C2000 implementation of a global one-shot reload is a key mechanism to ensure correct PWM waveform generation for all PWM outputs. Global one-shot reload ensures that all period, duty, phase and deadband updates take effect within the switching cycle where the new frequency is needed. This provides a clean transition from one frequency to the other for all phases. In contrast, using a general-purpose timer without a one-shot and global reload function limits the maximum switching frequency, because it requires more cycles in order to avoid incorrect PWM generation. The number of cycles becomes increasingly difficult with the addition of more phases.

## The C2000 TMS320F280049 MCU

The F28004x is a new series in the C2000 MCU family (**Figure 4**) designed specifically for power-control applications.

The F28004x includes:

- 100 MHz performance, with a 100 MHz parallel improved CLA option.
- TMU, floating-point unit and Viterbi complex-unit performance accelerators.
- As many as seven CMPSSs.
- Three high-performance ADCs with a post-processing block, programmable gain amplifiers and a flexible comparator subsystem.
- Flexible timers: fourth-generation enhanced pulse-width modulator (ePWM) modules with 150 ps resolution, complex waveform generation and synchronization capability.
- 256 KB and 128 KB flash memory options.
- 100 KB of full-speed random access memory (RAM).

## C2000 MCU-based totem-pole PFC reference designs

For more information on implementing a totem-pole PFC with SiC and GaN FETs for an onboard charger module based on C2000 real-time MCUs, see 98.5% Efficiency, 6.6-kW Totem-Pole PFC Reference Design for HEV/EV Onboard Charger and Highly Efficient, 1.6kW High Density GaN Based CRM Totem-Pole PFC Converter Reference Design.

## Conclusion

As more power electronic companies develop higher-power modules for onboard chargers, they will consider topologies such as totem-pole PFC, which can efficiently control GaN and SiC MOSFETs that require much higher PWM switching frequencies (>500 kHz). The C2000 F28004x real-time MCU series builds on a rich portfolio of optimal solutions that help designers solve challenges related to the designs highlighted in this white paper and other advanced power topologies.