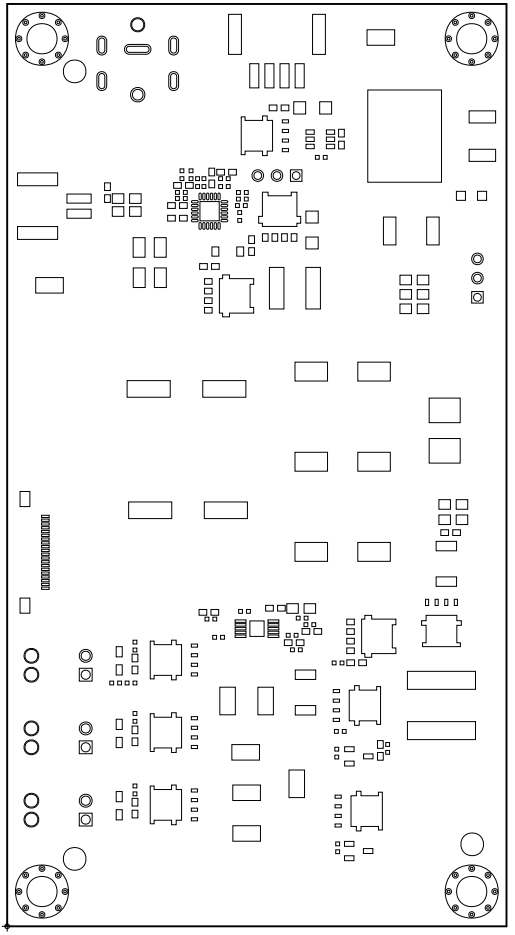
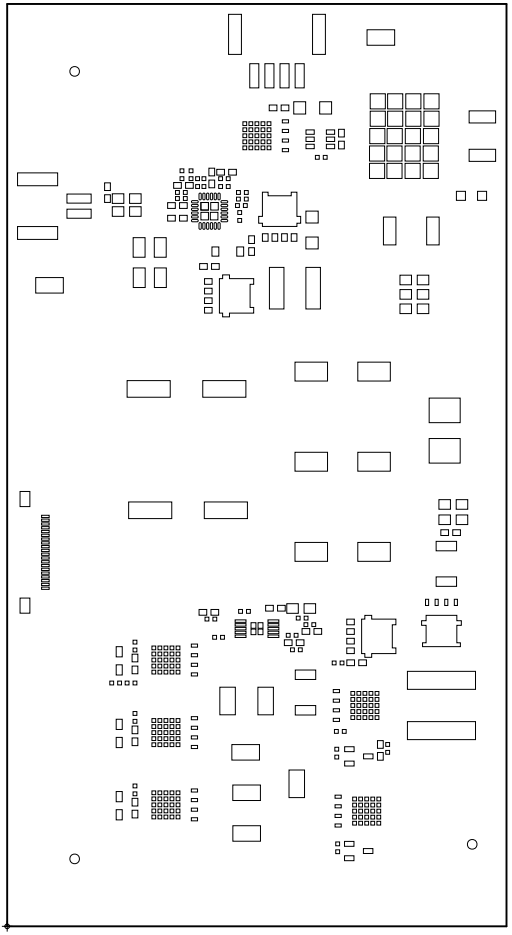
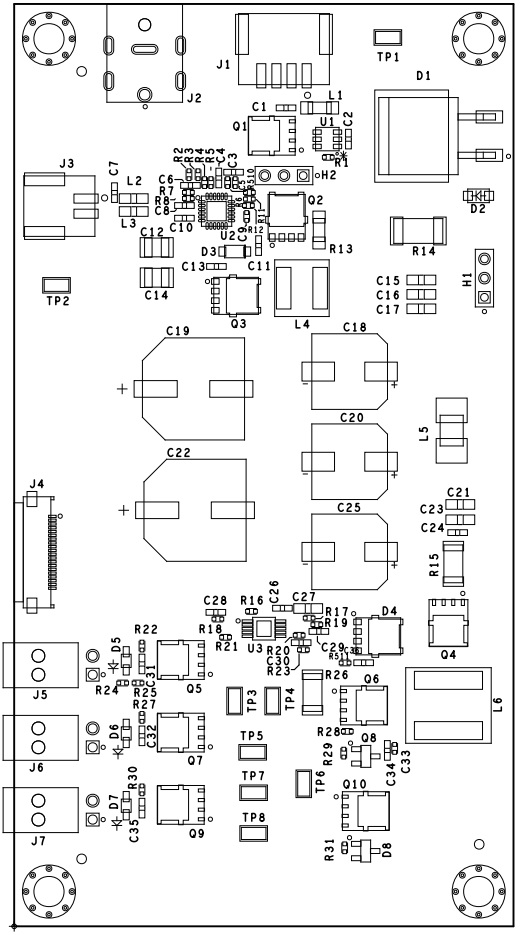


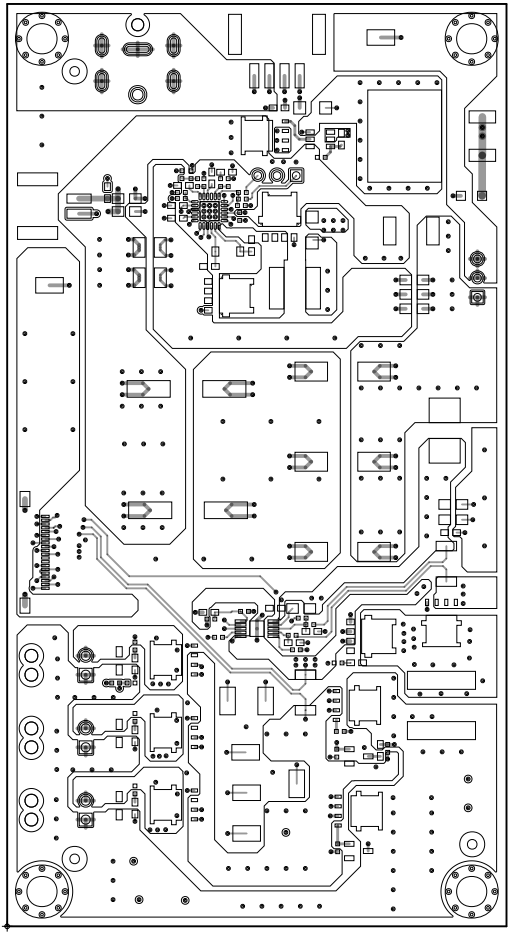
BOARD NAME: DLP5530Q1EVM	DESCRIPTION: SOLDERMASK - TOP SIDE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A



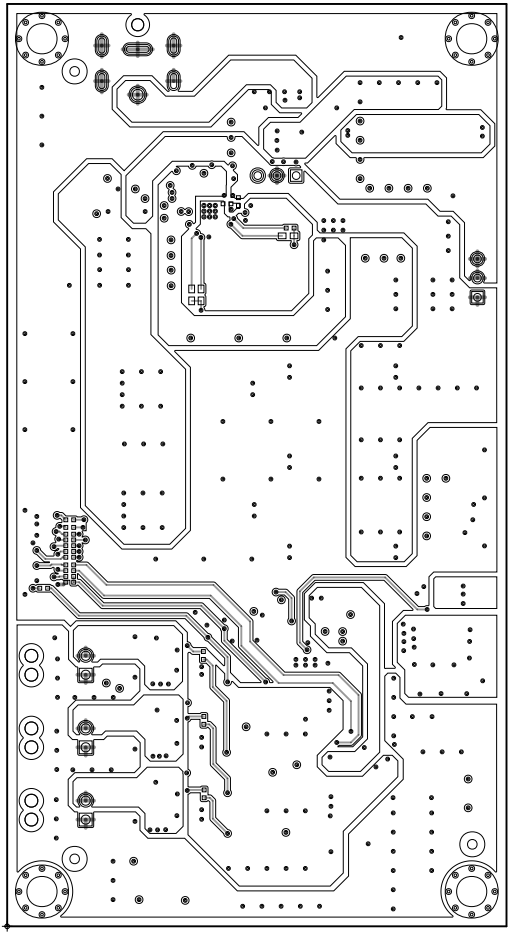
BOARD NAME: DLP5530Q1EVM	DESCRIPTION: SOLDERPASTE - TOP SIDE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A



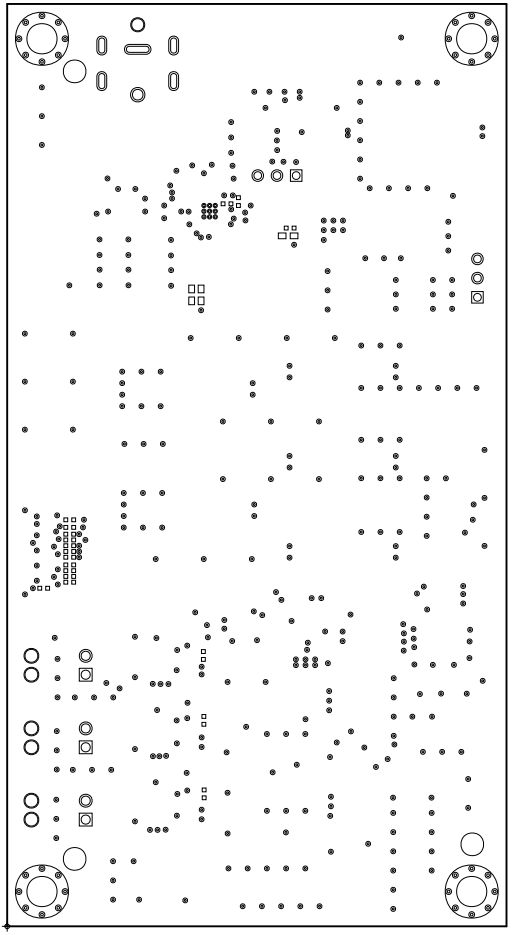
BOARD NAME: DLP5530Q1EVM		DESCRIPTION: ASSEMBLY - TOP SIDE	
PROJECT #: DLP029		DATE: 04-AUG-2019	REVISION: A



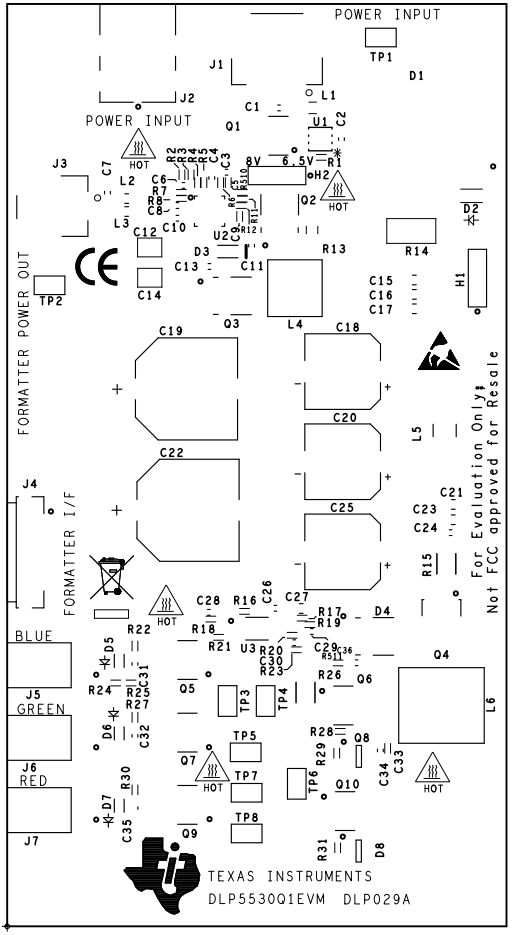
BOARD NAME: DLP5530Q1EVM	DESCRIPTION: LAYER 01 - TOP SIDE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A



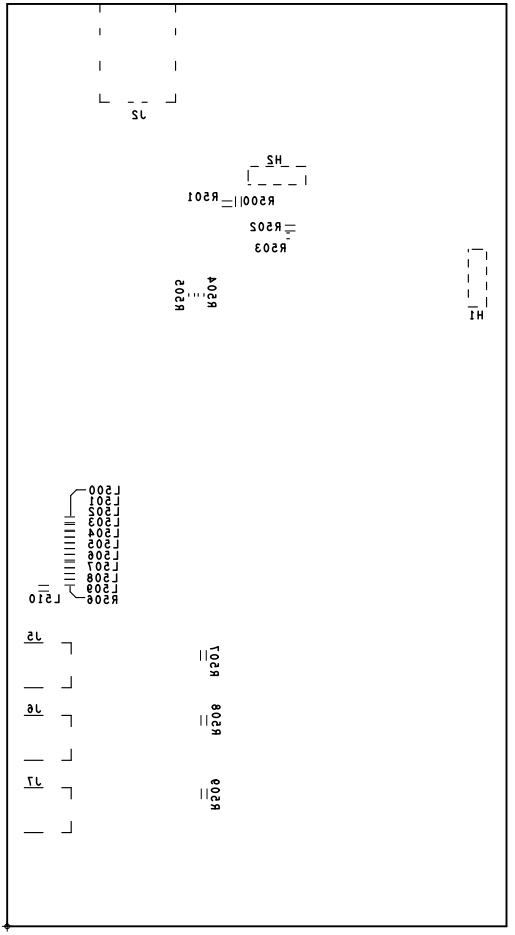
BOARD NAME: DLP5530Q1EVM	DESCRIPTION: LAYER 04 - BOTTOM SIDE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A



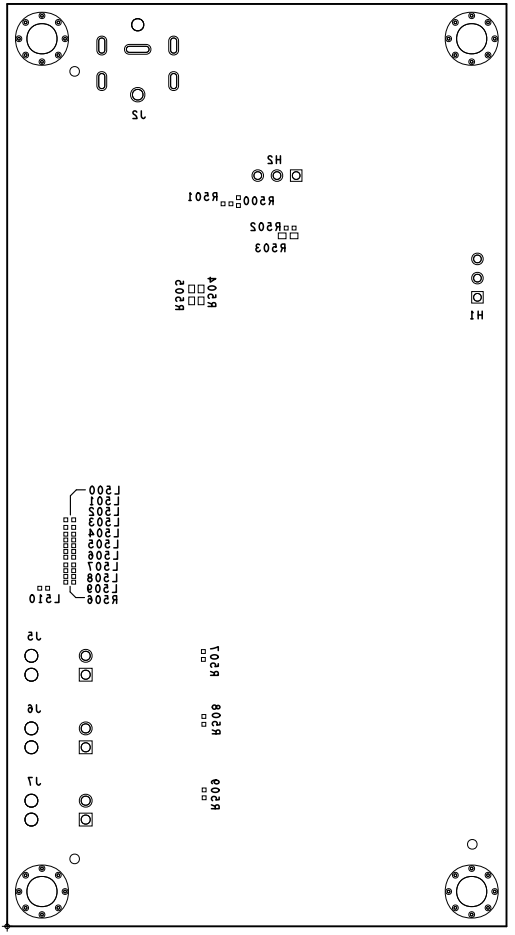
BOARD NAME: DLP5530Q1EVM	DESCRIPTION: SOLDERMASK - BOTTOM SIDE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A



BOARD NAME: DLP5530Q1EVM	DESCRIPTION: SILKSCREEN - TOP SIDE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A

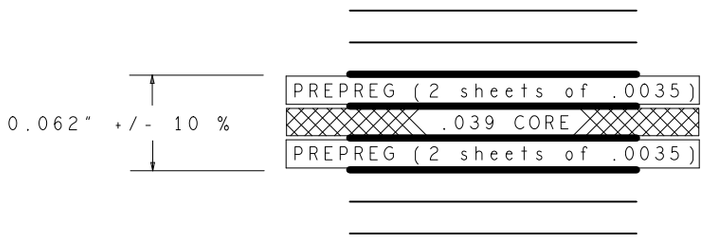


BOARD NAME: DLP5530Q1EVM		DESCRIPTION: SILKSCREEN - BOTTOM SIDE	
PROJECT #: DLP029		DATE: 04-AUG-2019	REVISION: A



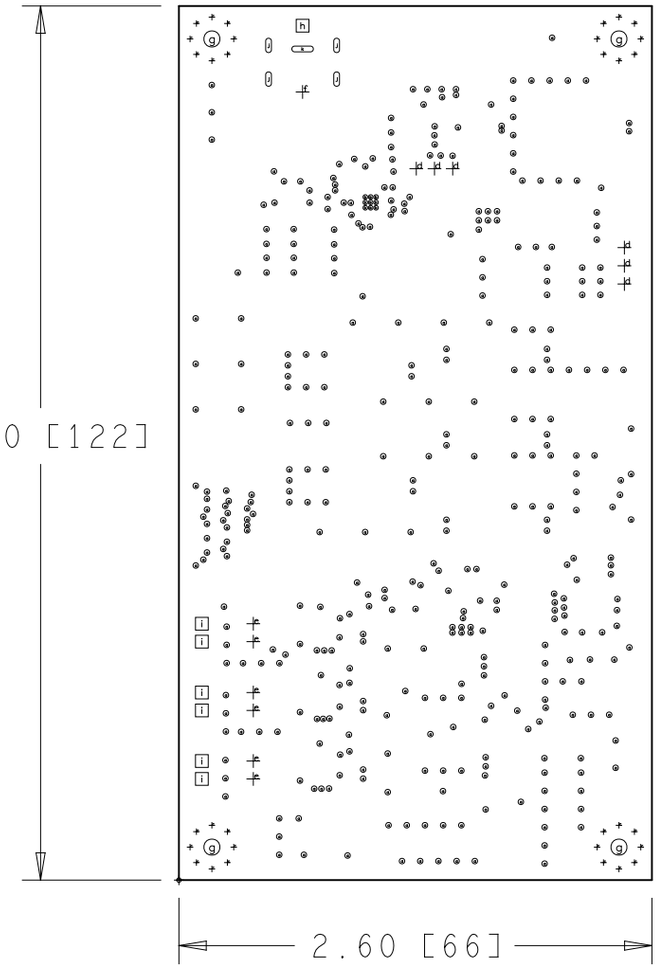
BOARD NAME: DLP5530Q1EVM	DESCRIPTION: ASSEMBLY - BOTTOM SIDE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A

LAYER STACKUP



LAYER DEFINITION	FINISH Cu WT.
SILKSCREEN PRIMARY SIDE	
SOLDERMASK PRIMARY SIDE	
LAYER 1 PRIMARY SIDE	2 oz
LAYER 2 (GND PLANE)	2 oz
LAYER 3 (PWR SPLIT PLANE)	2 oz
LAYER 4 SECONDARY SIDE	2 oz
SOLDERMASK SECONDARY SIDE	
SILKSCREEN SECONDARY SIDE	

THIS IN A NON-IMPEDANCE CONTROLLED BOARD



COMPONENT SIDE SHOWN
ALL DIMENSIONS ARE IN INCHES[mm]

BOARD NAME: DLP5530Q1EVM	DESCRIPTION: FAB LAYER	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A

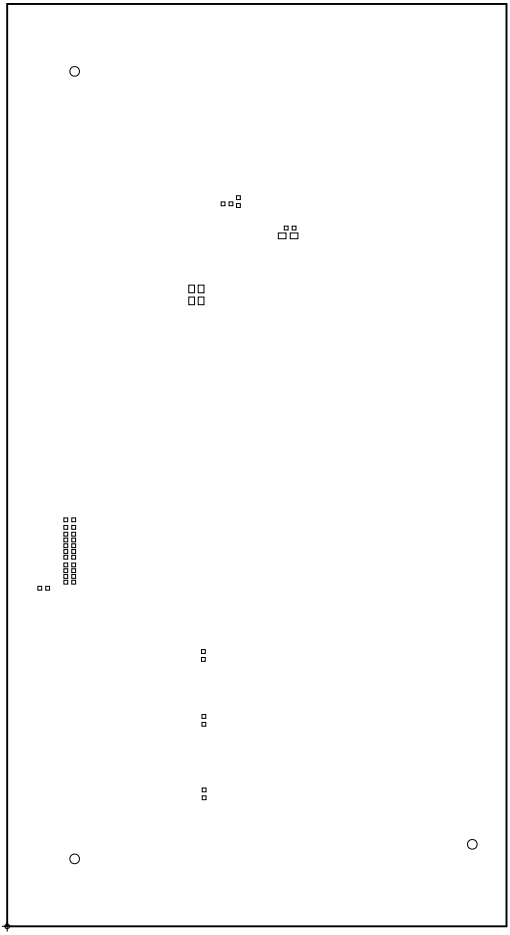
FAB NOTES:

1. ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED. ALL BOARD OUTLINE DIMENSION TOLERANCES ARE +/- .010".
2. THE PWB SHALL BE FABRICATED TO IPC-6012, CLASS 2 AND WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2. CURRENT REVISIONS.
3. BOARD MATERIAL SHALL BE 180 Tg/340 Td ISOLA FR-370HR OR EQUIVALENT, RoHS COMPLIANT AND LEAD FREE ASSEMBLY CAPABLE. BOARD MATERIAL SHALL MEET OR EXCEED IPC-4101B. RoHS CERTIFICATE OF CONFORMANCE SHALL BE DELIVERED WITH EACH LOT.
4. THE BOARD NEEDS TO BE CONSTRUCTED AND MARKED WITH UL94V-0 FLAME-RETARDANT MATERIAL AND eFILE NUMBER.
5. MINIMUM COPPER WALL THICKNESS OF PLATED-THRU HOLES TO BE .001 INCH, WITH A MINIMUM ANNULAR RING OF .001 INCH.
6. OVERALL BOARD THICKNESS TO BE .062 +/- 10% AND APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES, MEASURED FROM COPPER TO COPPER.
7. MAX. WARP & TWIST TO BE .0075 INCHES PER INCH.
8. BOARD MUST BE ELECTRICALLY TESTED USING SUPPLIED IPC-D-356 NETLIST.

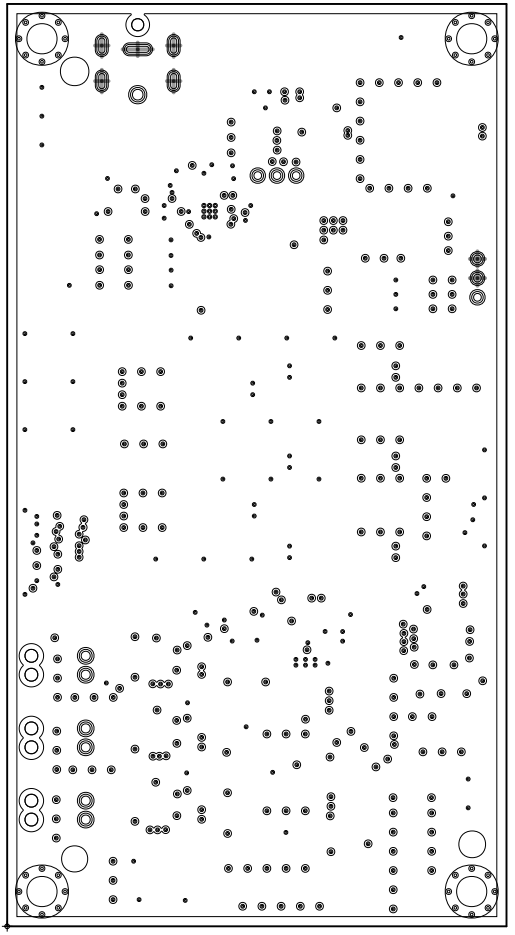
PROCESS NOTES:

1. PLATE ALL EXPOSED AREAS WITH ELECTROLESS IMMERSION GOLD, NICKEL 100 MIN MICROINCHES THK GOLD 2-6 MICROINCHES THK.
2. APPLY LPI SOLDERMASK OVER BARE COPPER (SMOBC), COLOR: GREEN. SOLDERMASK SHALL CONFORM TO IPC-SM-840, CLASS H. CURRENT REV. VIAS ARE TENTED OVER ON TOP SIDE ONLY (DESIGN INTENT) REMAINING FOLLOW AS PER ARTWORK.
3. FABRICATION VENDOR IS ALLOWED TO INCREASE SOLDERMASK COMPONENT PADS BY A MAXIMUM 1 MIL ON EACH SIDE OVER THE COPPER PAD IN ORDER TO MEET TOOLING REQUIREMENTS WHILE MAINTAINING WEBBING BETWEEN ADJACENT PADS.
4. APPLY LPI SILKSCREEN OR EQUIVALENT PER THE ARTWORK. COLOR: WHITE.

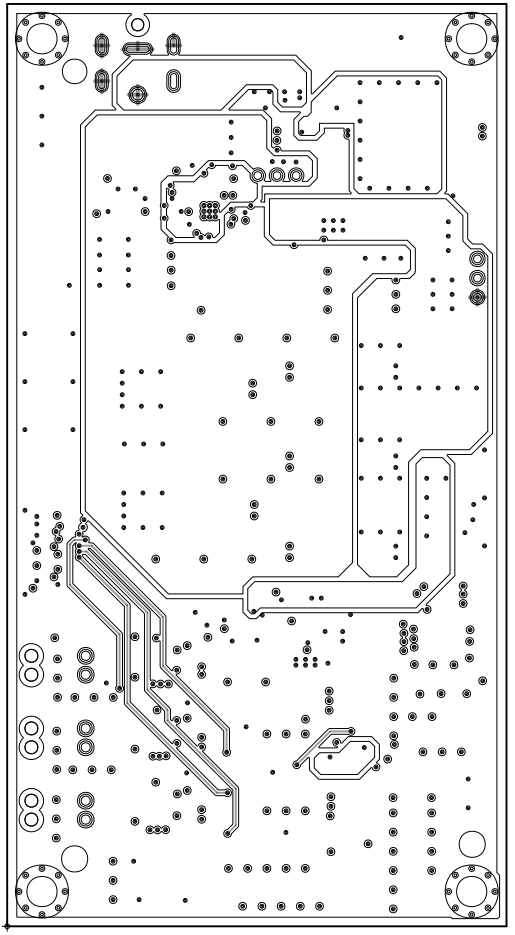
DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
◎	10.0	+0.0/-10.0	PLATED	394
◉	12.0	+0.0/-12.0	PLATED	9
+	14.0	+3.0/-3.0	PLATED	32
⧺	40.0	+2.99/-2.99	PLATED	6
⧺	47.24	+1.97/-1.97	PLATED	6
⧺	55.12	+3.94/-0.0	PLATED	1
ⓖ	157.0	+3.0/-3.0	PLATED	4
h	62.99	+3.94/-0.0	NON-PLATED	1
i	66.93	+2.0/-2.0	NON-PLATED	6
▯	78.74x31.5	+2.01/-2.01	PLATED	4
⬭	118.11x31.5	+2.01/-2.01	PLATED	1



BOARD NAME: DLP5530Q1EVM	DESCRIPTION: SOLDERPASTE - BOTTOM SIDE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A



BOARD NAME: DLP5530Q1EVM	DESCRIPTION: LAYER 02 - GND PLANE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A



BOARD NAME: DLP5530Q1EVM	DESCRIPTION: LAYER 03 - PWR SPLIT PLANE	
PROJECT #: DLP029	DATE: 04-AUG-2019	REVISION: A