

# TPSM82866AA0SRDJR PSpice Transient Model Features and Limitations

- \* Model Usage Notes:
- \* A. The following features have been modeled
  - \* a. 100% duty cycle operation
  - \* b. RON and variation with VIN
  - \* c. Current Limit and HICCUP
  - \* d. Output discharge functionality
  - \* e. Selectable Fixed and Adjustable output voltage configuration.
  - \* f. Power Save Mode or Forced PWM Mode.
  - \* g. Power Good and UVLO
- \* B. Features have not been modeled
  - \* 1. Operating Quiescent Current
  - \* 2. Shutdown Current
  - \* 3. Temperature dependent characteristics.
  - \* 4. Ground pins have been tied to 0V internally. Therefore, this model cannot be used for inverting topologies.
- \* C. Application Notes
  - \* 1. The parameter STEADY\_STATE and VOUT has been used to reach the steady state faster.
    - \* Keep STEADY\_STATE = 0 and VOUT = output voltage value, to observe startup behaviour
    - \* Keep STEADY\_STATE = 1 and VOUT = output voltage value, for faster Steady state.
  - \* 2. After enabling the device (EN>1V), there is an enable delay (tDelay)= 700us before the device starts switching.
    - \* After tDelay output voltage ramps up the value set by external resistor R4 (at VSET/MODE pin) in 1ms.
  - \* 3. For R4=10K or LOW and R4=249K or HIGH, Device works in Adjustable Output Voltage Configuration.
  - \* 4. Once the device reaches steady state, VSET/MODE pin can be used to run the device in FPWM/PFM mode.
    - \* Keep VSET/MODE = LOW, device runs in PFM
    - \* Keep VSET/MODE = HIGH, device runs in FPWM
    - \* Connect VSET/MODE to 5.5V DC (not to VIN) to model the device in FPWM mode with an adjustable output voltage.
    - \* In the actual application, connect VSET/MODE to VIN.
  - \* 5. The PG pin becomes high under the condition-  $0.91 \times VOUT\_NOM = VVOS = 1.11 \times VOUT\_NOM$