

TPS546x25 PSpice Transient Model

Features, Application Notes, and Limitations

Simulator	Cadence PSpice 17.4 or later	Model scope	Single-phase transient operation
Default testbench	VIN = 12 V, VOUT = 1.2 V, IOOUT = 50 A	Validated range	VIN = 4 V to 18 V; IOOUT = 100 mA to 50 A

A. Features Modeled

1. TPS546E25, TPS546C25, and TPS546B25 device variants are supported.
2. Output voltage can be configured using the external feedback network or the **VSEL_FB** programming resistance.
3. Switching frequency, ramp, and control-loop gain are configured using the **MSEL2** programming resistance.
4. FCCM/DCS operating-mode behavior is configured using the **PMB_ADDR** programming resistance.
5. Overcurrent protection, soft start, and applicable fault-latch behavior are configured using the **MSEL1** programming resistance.
6. Open-drain power-good output behavior is modeled.
7. Output overvoltage and undervoltage protection behavior is modeled.
8. Enable and enable-delay behavior is modeled.

B. Features Not Modeled

1. Operating quiescent current.
2. Shutdown current.
3. Thermal shutdown and other temperature-dependent characteristics.
4. Voltage, current, and temperature telemetry and input-power monitoring.
5. Multiphase operation and current sharing between multiple devices.
6. Inverting topologies. The model is intended for the grounded, non-inverting buck configuration shown in the supplied testbench.

C. Application Notes

1. The model is encrypted and requires Cadence PSpice version 17.4 or later.
2. The reference design is based on the TPS546E25 EVM schematic and uses similar input-voltage, output-voltage, and load conditions.
3. The supplied testbench is configured for **VIN = 12 V**, **VOUT = 1.2 V**, and **IOUT = 50 A** for each simulated output.
4. The model has been corner tested over **VIN = 4 V to 18 V** and **IOUT = 100 mA to 50 A**. Operation outside these ranges has not been validated.
5. Select exactly one device variant by setting its parameter to 1 and the other two variant parameters to 0:
TPS546E25: TPS546E25=1, TPS546C25=0, TPS546B25=0
TPS546C25: TPS546E25=0, TPS546C25=1, TPS546B25=0
TPS546B25: TPS546E25=0, TPS546C25=0, TPS546B25=1
6. Set **FAST_SS=0** to observe the complete startup sequence. Set **FAST_SS=1** to shorten the startup interval and reach steady state more quickly. FAST_SS=1 should not be used when evaluating startup timing or startup waveforms.
7. Select **R_MSEL1**, **R_MSEL2**, **R_PMB_ADDR**, and **R_VSEL_FB** according to the device datasheet and the intended operating configuration.
8. When a modeled PVIN overvoltage, VOUT undervoltage, or VOUT overvoltage fault is configured as latching, the device remains disabled until the simulation is restarted after the fault condition has been removed.
9. The model supports single-phase operation only.
10. The supplied transient simulation runs for **600 us** and requires approximately **25 minutes** on a four-core, 2.8 GHz computer. Actual runtime depends on the computer, PSpice version, simulation settings, and saved waveform count.

Model-use guidance

This behavioral model is intended for transient evaluation of startup, steady-state switching behavior, configuration settings, and the supported protection functions. It is not intended for thermal, efficiency, quiescent-current, or telemetry analysis.