LM5117 PSPICE Model Validation Report

Date: 15SEP2014

Revision: 1.0

Author: Seema S

Simulator Names and Versions:

- PSPICE 16.2.0.p001

Description of Model: LM5117, Wide Input Range Synchronous Buck Controller with Analog Current Monitor

Document Revision History:

REVISION NO.	DESCRIPTION	REVISION DATE	REMARKS
1.0	Initial Release	10JUL2012	-
1.1	Implemented CM, Hiccup current limit and VCC DIS feature	15SEP2014	-

Contents

1. Model Modifications

Implemented the CM feature, Hiccup current limit and VCCDIS functionality.

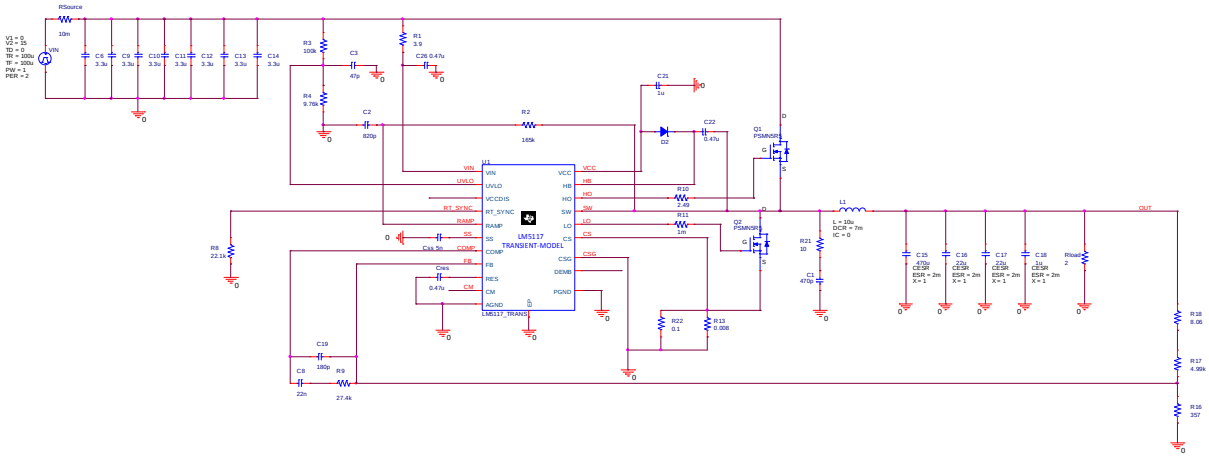
2. Analysis Parameters

2.1 PSPICE

Transient
.OPTIONS STEPGMIN
.OPTIONS SKIPBP
.OPTIONS RELTOL = 0.002
.OPTIONS VNTOL = 1u
.OPTIONS ABSTOL = 10n
.OPTIONS CHGTOL=10f
.OPTIONS GMIN = 1E-9
.OPTIONS ITL1 = 1000
.OPTIONS ITL2 = 1000
.OPTIONS ITL4 = 1000
Maximum step size = 10n

3. PSPICE Published schematic

PSPICE Schematic:



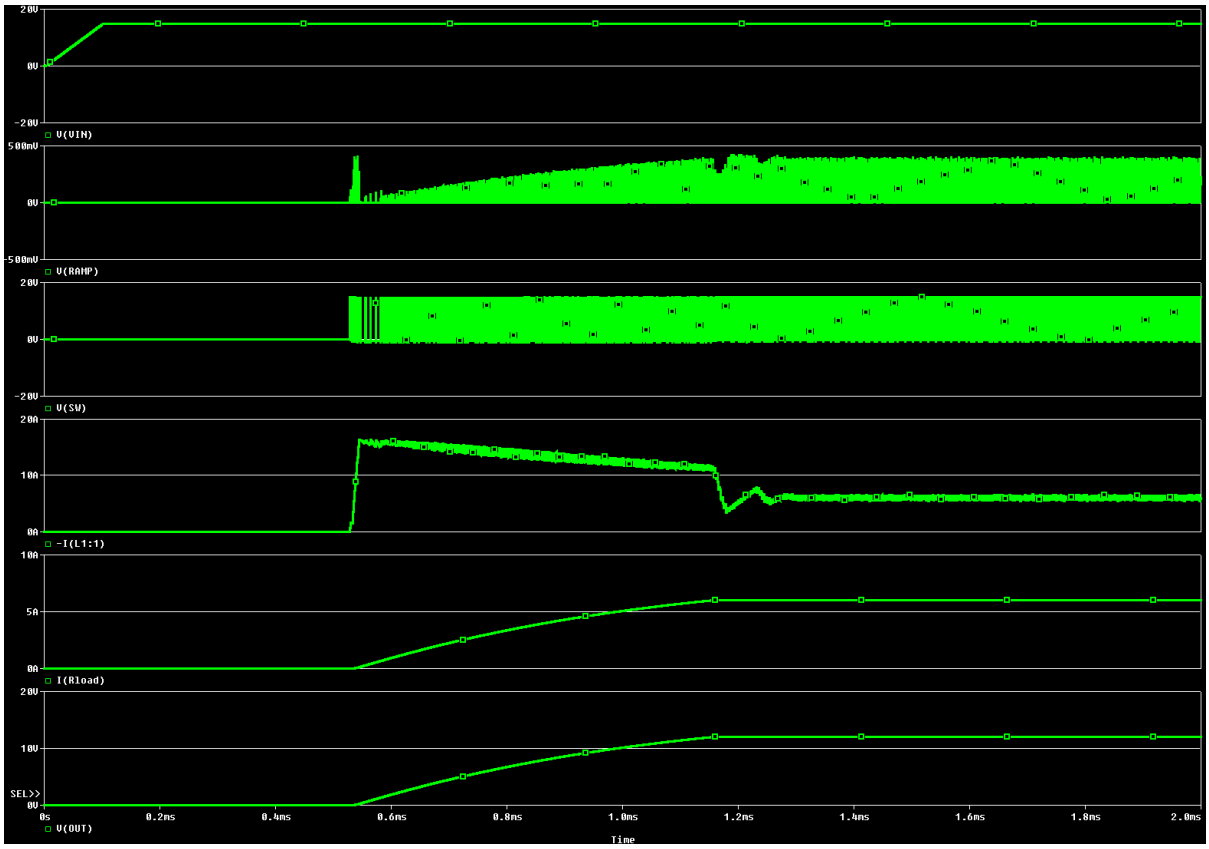
Description:

1. This model has been tested for an input voltage range of 15V to 55V and a load current range of 1mA to 9A.
2. The test bench has been configured for VIN = 15V and VOUT = 12V.
3. Operating Frequency is set to 230 kHz by setting RT=22.1kΩ.
4. Thermal shutdown for this part has not been modelled.

Test Conditions and Additional Analysis Options (if any):

1. VIN = 15V
2. Rload=1.333Ω , IRload = 6A
3. Frequency =230 kHz; RT=22.1kΩ

Simulated Results:-



Tabulation of Results:

PARAMETER	PSPICE	EVM	UNIT
Average Vout	12.003	12	V
Average RLoad	6.007	6	A
Vout Ripple	-	-	mV
Switching Frequency	227.45	230	kHz

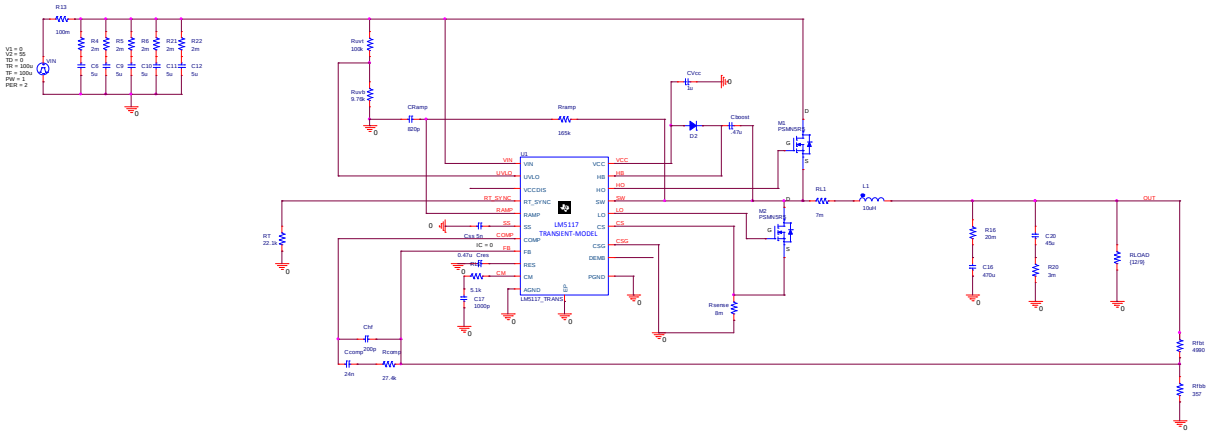
Conclusion: The simulation results are matching to acceptable level.

4. Validation across EVM corners

4.1 Simulation of Transient test-bench

4.1.1 Condition 1 (VIN_{MAX}= 55V & $IRload_{MAX}$ = 9A)

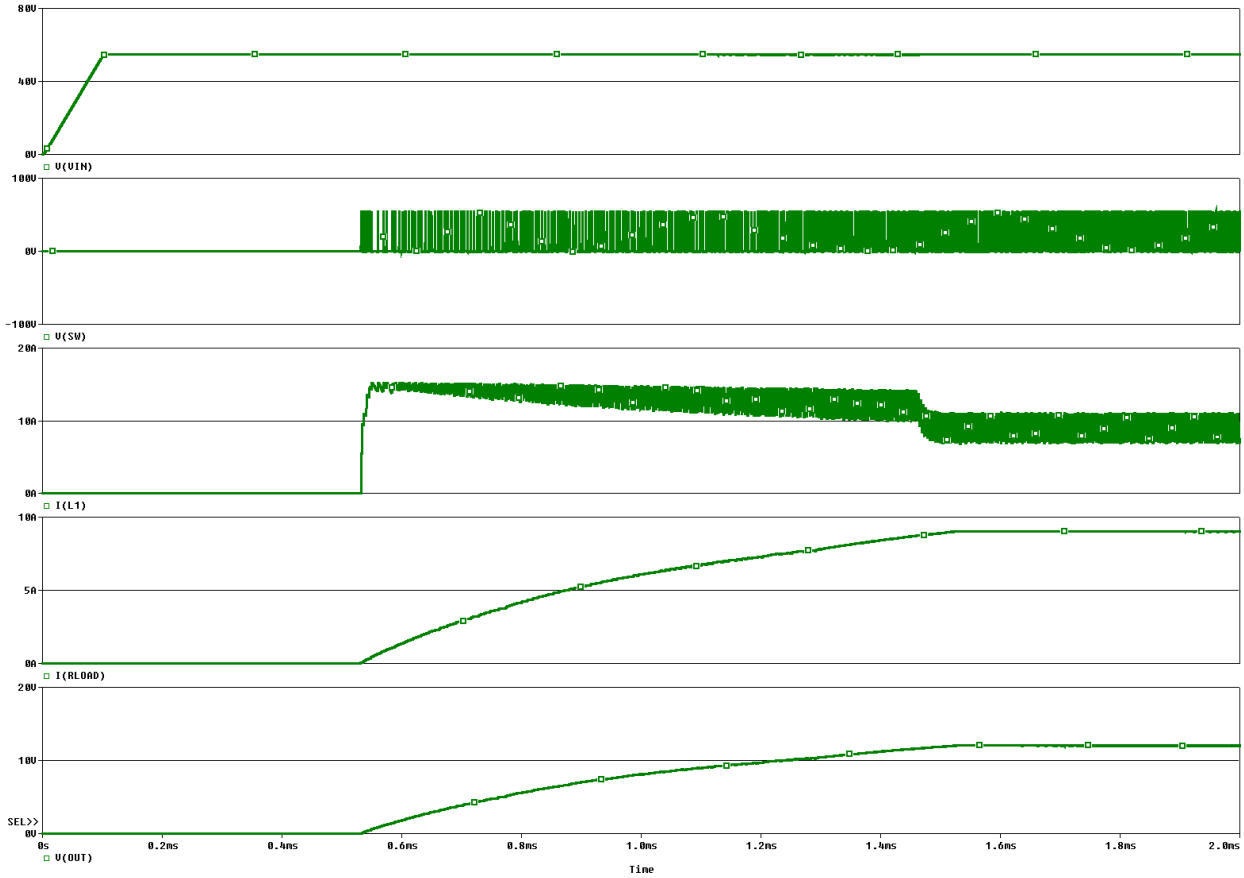
PSPICE Schematic:



Test Conditions:

1. VIN = 55V,
2. Rload=1.33Ω , IRload =9A
3. Frequency =230 kHz RT=22.1kΩ

Simulated Results:-



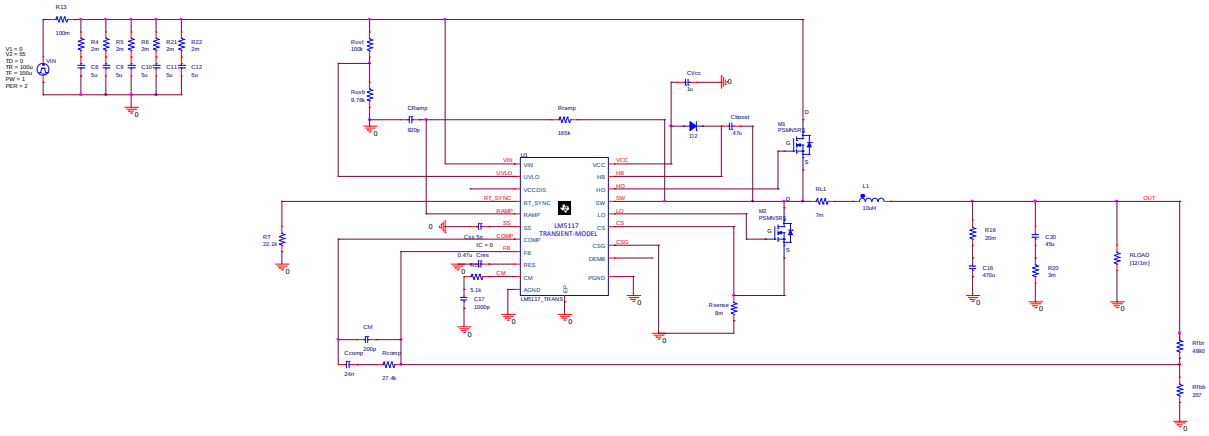
Tabulation of Results:

PARAMETER	PSPICE	EVM	UNIT
Average Vout	12.020	12	V
Average RLoad	9.0147	9	A
Vout Ripple	37.175	-	mV
Switching Frequency	222.57	230	kHz

Conclusion: The simulation results are matching to acceptable level.

4.1.2 Condition 2 (VIN_{MAX}= 55V & $IRload_{MIN}$ = 1mA)

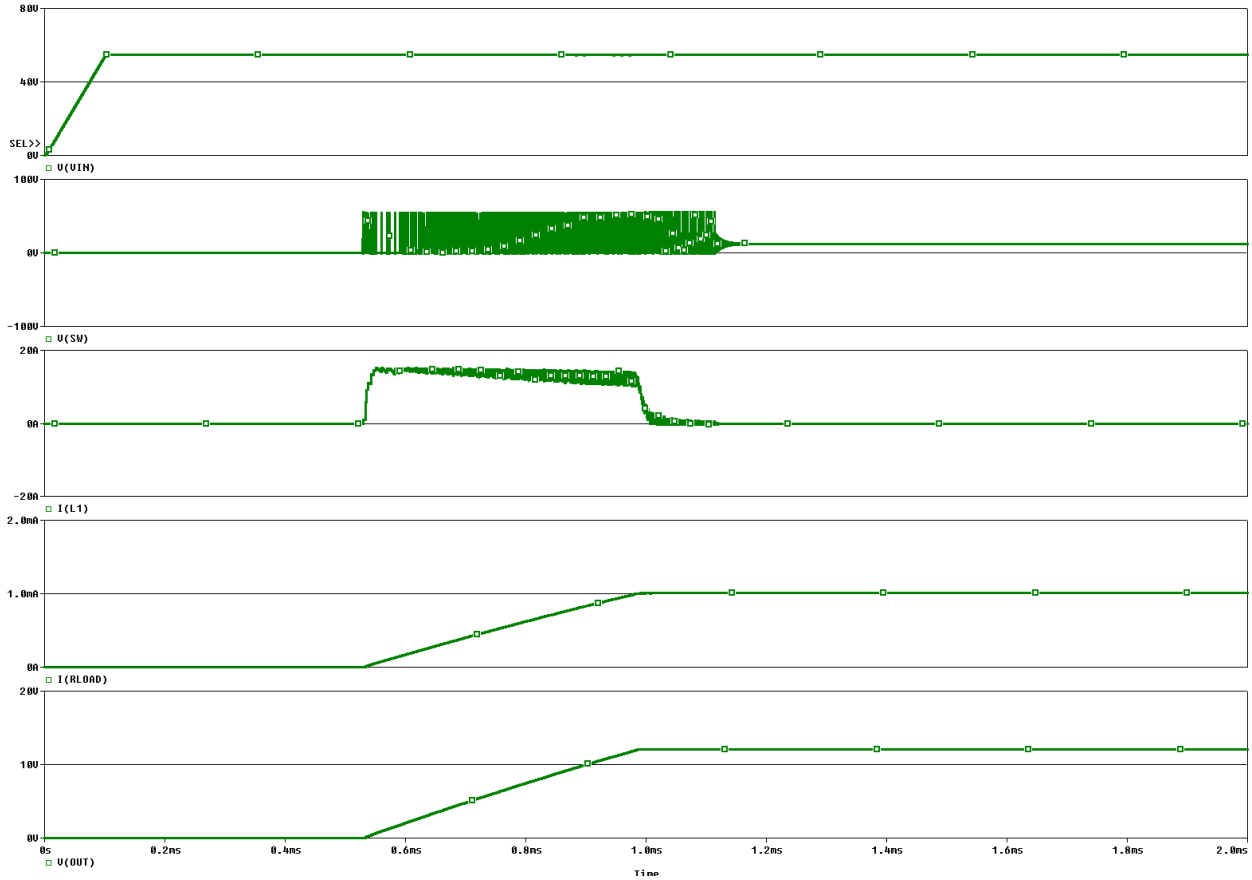
PSPICE Schematic:



Test Conditions:

1. VIN = 55V,
2. Rload=12kΩ , IRload = 1mA
3. Frequency =230 kHz , RT=22.1kΩ

Simulated Results:-



Tabulation of Results:

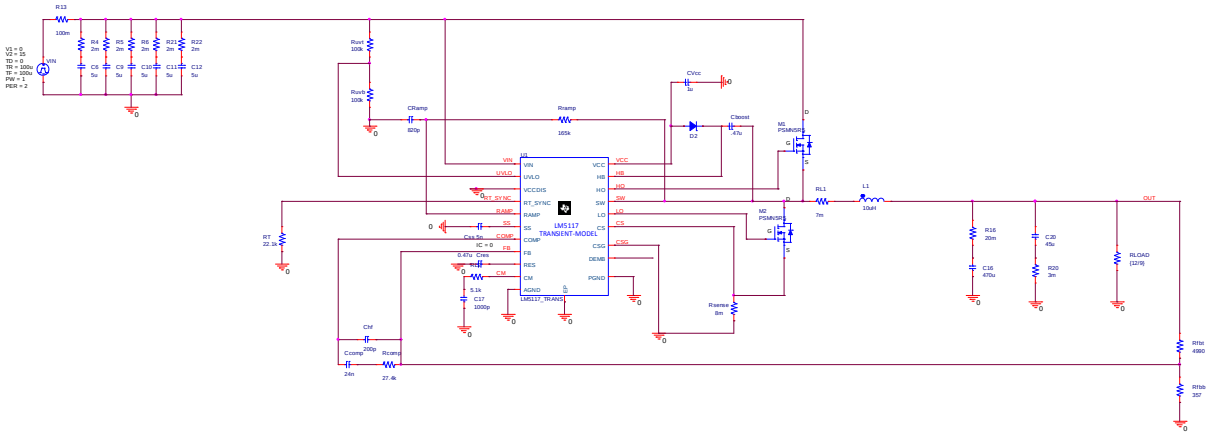
PARAMETER	PSPICE	EVM	UNIT
Average Vout	12.110	12	V
Average RLoad	1	1	mA
Vout Ripple	*	-	mV
Switching Frequency	*	230	kHz

Note:- * Device is in Discontinues mode.

Conclusion: The simulation results are matching to acceptable level.

4.1.3 Condition 3 (VIN_{MIN}= 15V & $IRload_{MAX}$ = 9A)

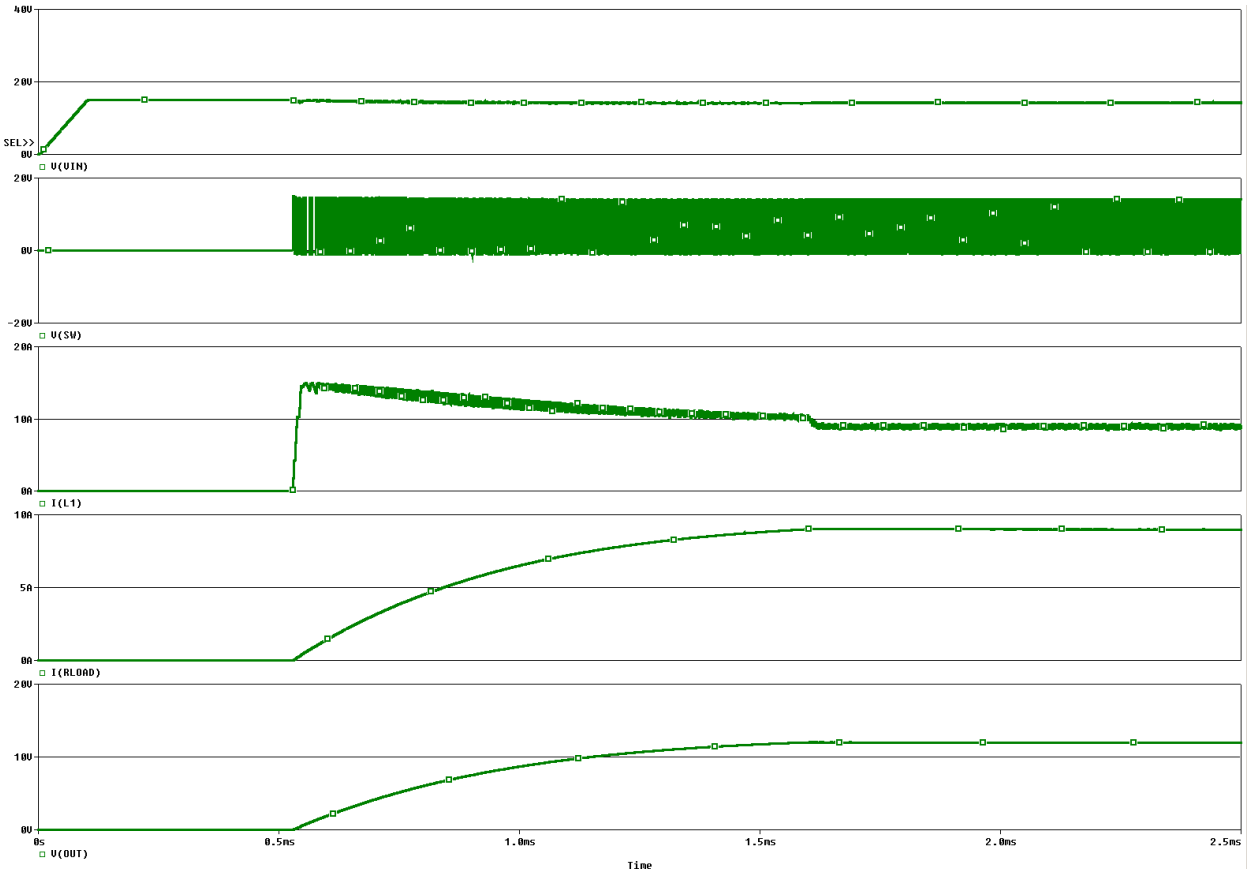
PSPICE Schematic:



Test Conditions:

1. VIN = 15V,
2. Rload=1.333Ω, IRload = 9A
3. Frequency =230 kHz, RT=22.1kΩ

Simulated Results:-



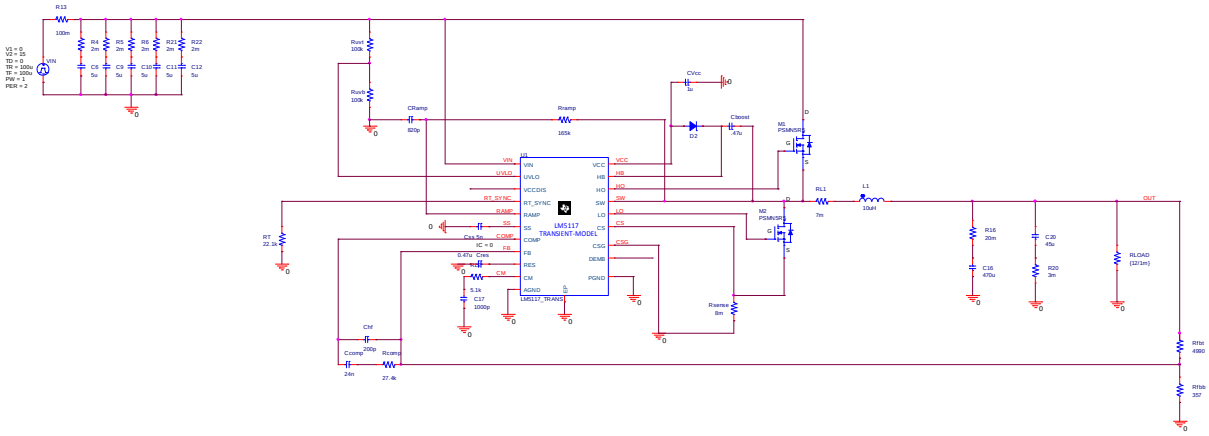
Tabulation of Results:

PARAMETER	PSPICE	EVM	UNIT
Average Vout	11.989	12	V
Average RLoad	8.9914	9	A
Vout Ripple	9.995	-	mV
Switching Frequency	226.57	230	kHz

Conclusion: The simulation results are matching to acceptable level.

4.1.4 Condition 4 (VIN_{MIN}= 15V & $Irload_{MIN}$ = 1mA)

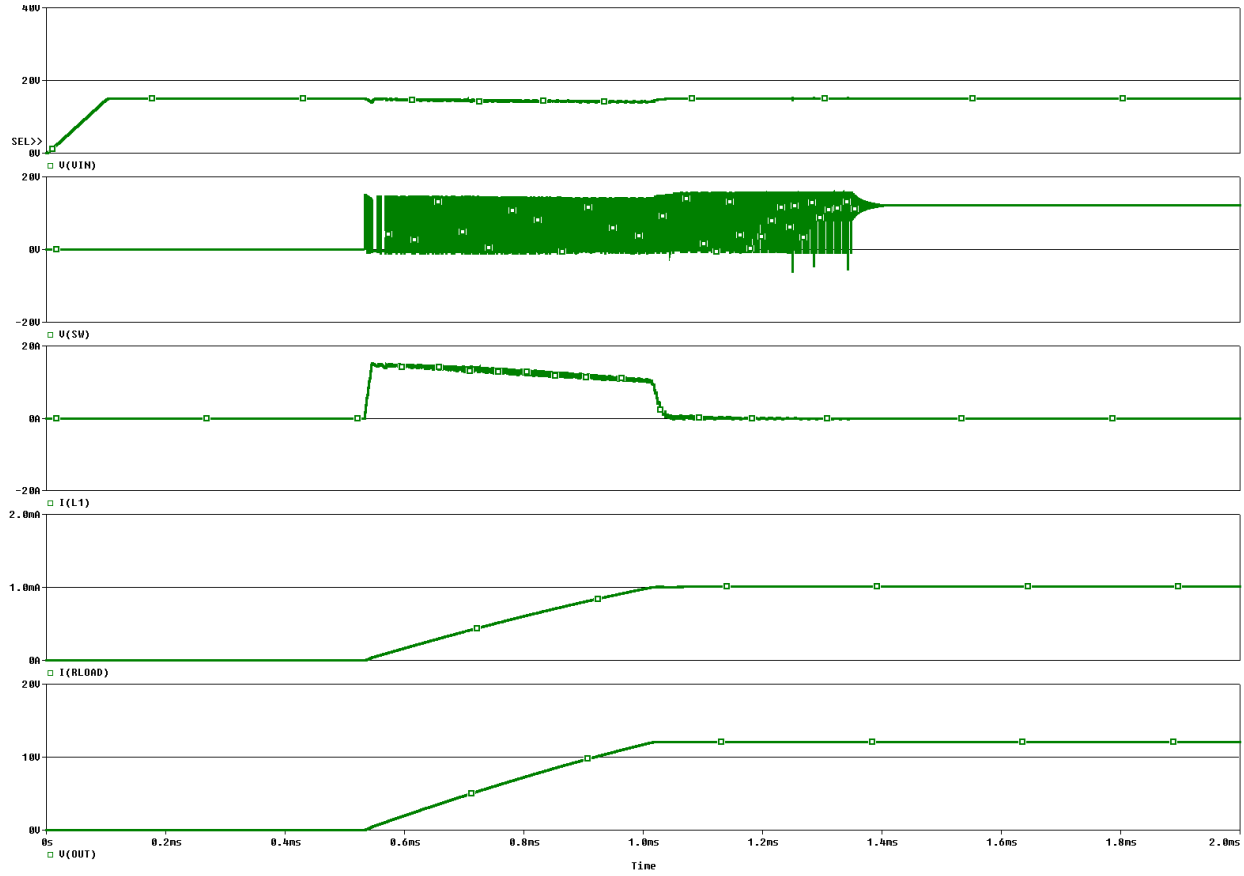
PSPICE Schematic:



Test Conditions:

1. VIN = 15V,
2. RLoad=12kΩ , IRload = 1mA
3. Frequency =230 kHz RT=22.1kΩ

Simulated Results:-



Tabulation of Results:

PARAMETER	PSPICE	EVM	UNIT
Average Vout	12.066	12	V
Average RLoad	1	1	mA
Vout Ripple	*	-	mV
Switching Frequency	*	230	kHz

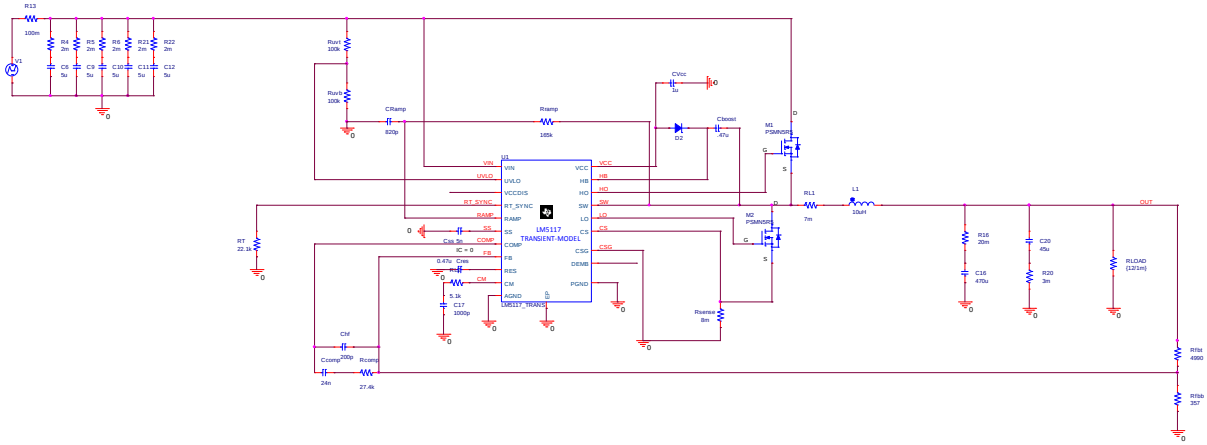
Note: - * Device is in Discontinues mode.

Conclusion: The simulation results are matching to acceptable level.

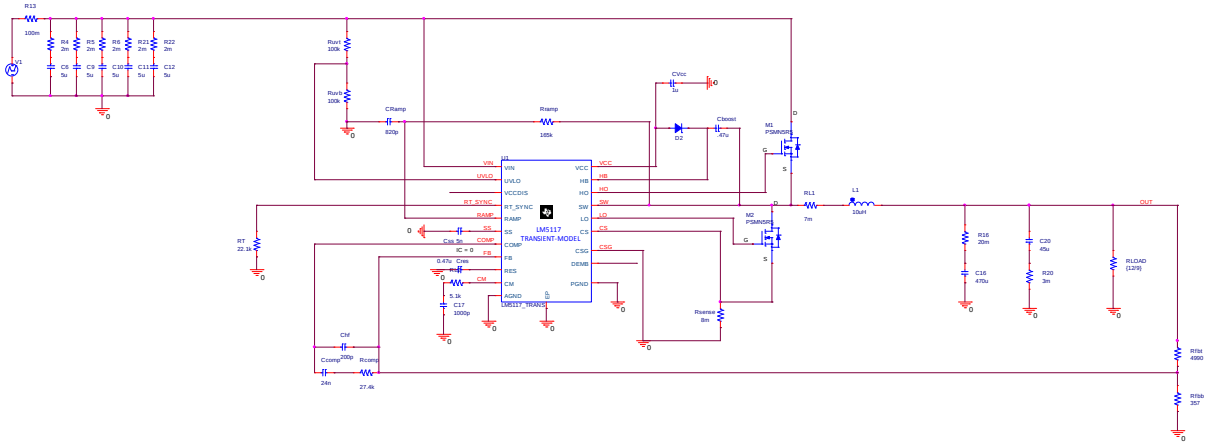
5. Additional test-benches

5.1 Line Transient

PSPICE Schematic for Condition1 (IRLOAD = 1mA, VIN =15V – 55V – 15V):



PSPICE Schematic for Condition2 (IRload = 9A, VIN =15V – 55V – 15V):



Description:

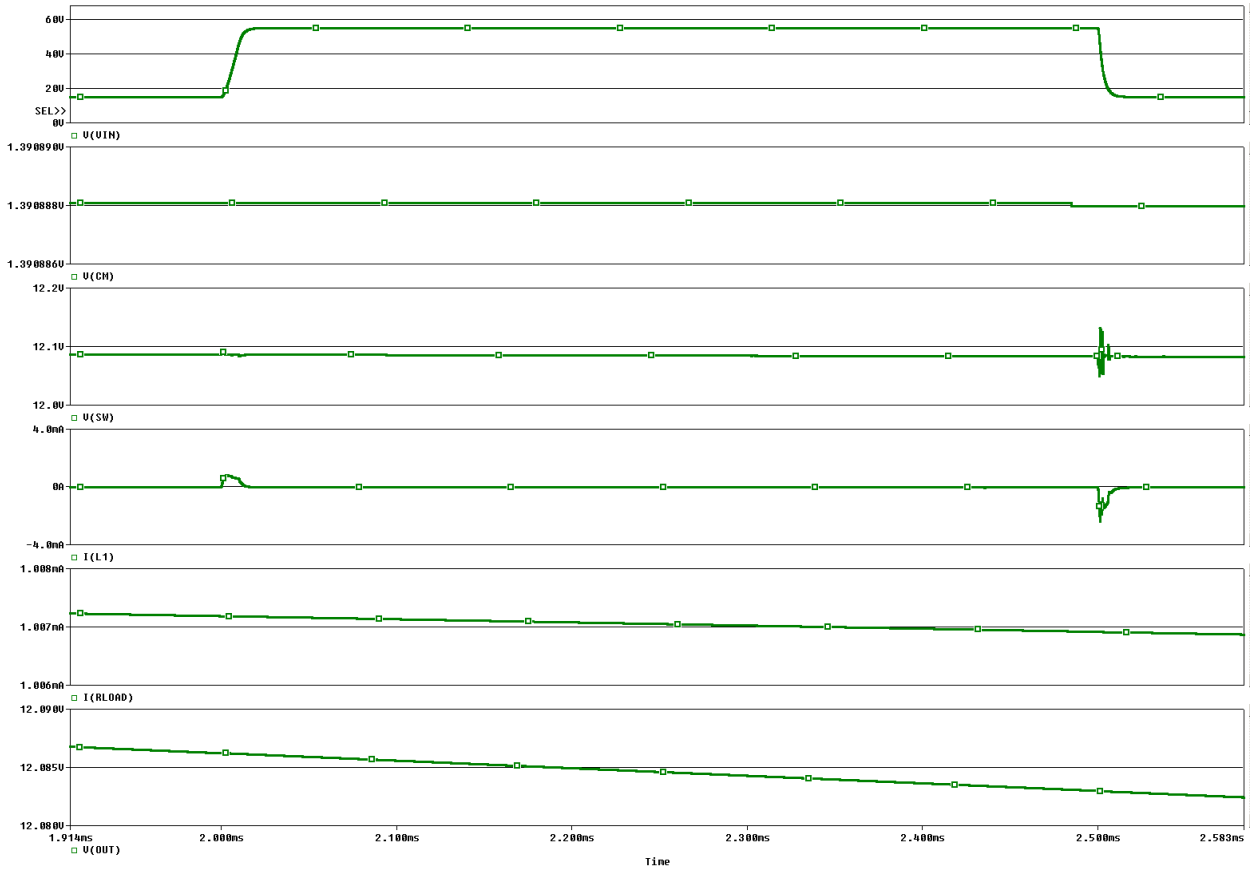
1. The test bench has been configured to test the line transient response of the model for following two conditions.

    a. Condition1: VIN = 15V – 55V – 15V, IRLOAD = 1mA
    b. Condition2: VIN = 15V – 55V – 15V, IRLOAD = 9A

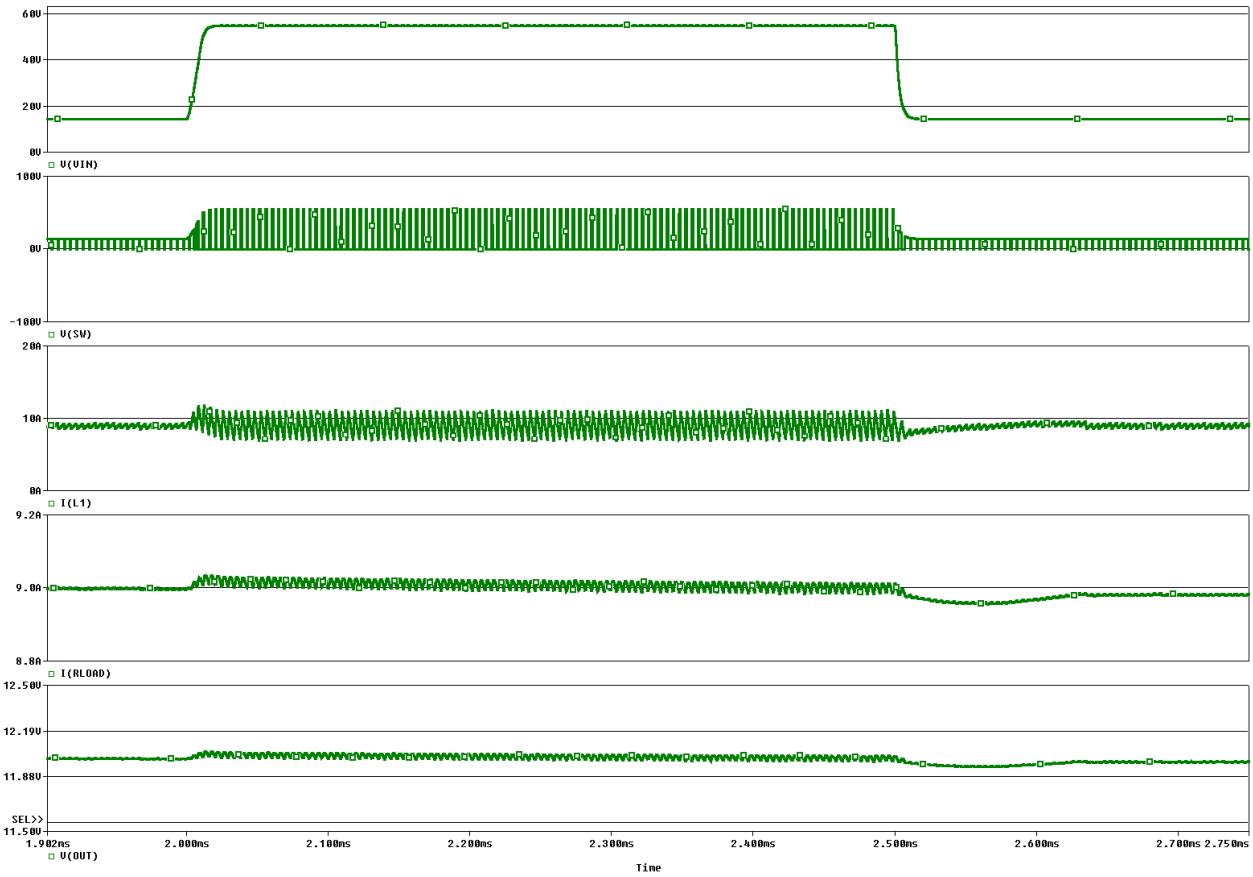
Test Conditions:

1. Condition1: VIN = 15V – 55V – 15V, IRLOAD = 1mA
2. Condition2: VIN = 15V – 55V – 15V, IRLOAD = 9A
3. VIN is varied with rise and fall time of 10us.

Simulated Results for Condition1: VIN = 15V – 55V – 15V, IRLOAD = 1mA



Overlaid Results for Condition2: VIN = 15V – 55V – 15V, IRload = 9A



Tabulation of Results:

Condition1 (VIN = 15V-55V-15V, IRLOAD = 1mA):

PARAMETERS	PSPICE	DATASHEET	UNITS
OVERSHOOT	**-**	**-**	mV
TSETTLE (OVER)	#	**-**	us
UNDERSHOOT	**-**	**-**	mV
TSETTLE (UNDER)	#	**-**	us

 # Overshoot and undershoot values are less than 1% of steady state value.

Condition2 (VIN = 15V-55V-15V, IRLOAD = 9A):

PARAMETERS	PSPICE	DATASHEET	UNITS
OVERSHOOT	*****	**-**	mV
TSETTLE (OVER)	#	**-**	us
UNDERSHOOT	48	**-**	mV
TSETTLE (UNDER)	#	**-**	us

Note:- * No overshoot observed. Only a DC shift 42mV is observed

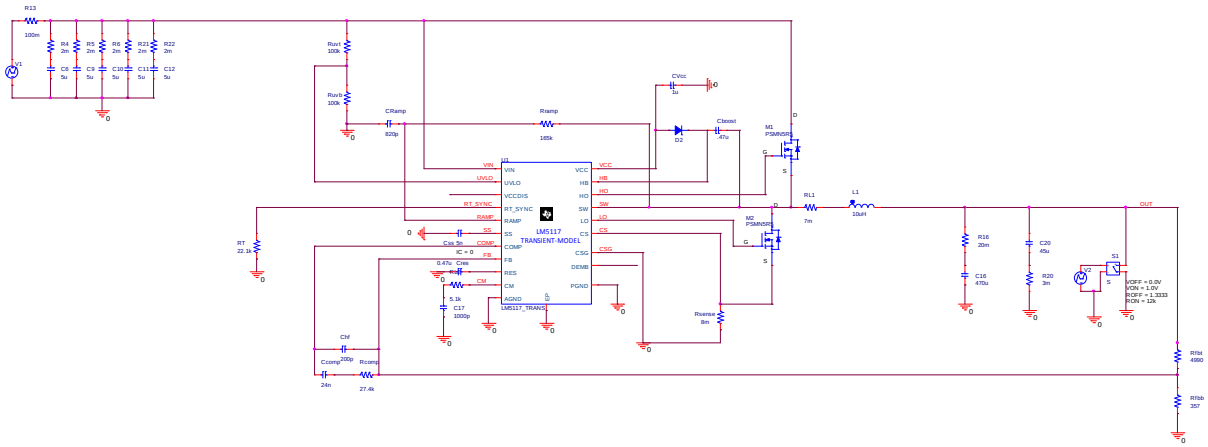
Overshoot and undershoot values are less than 1% of steady state value.

Conclusion:

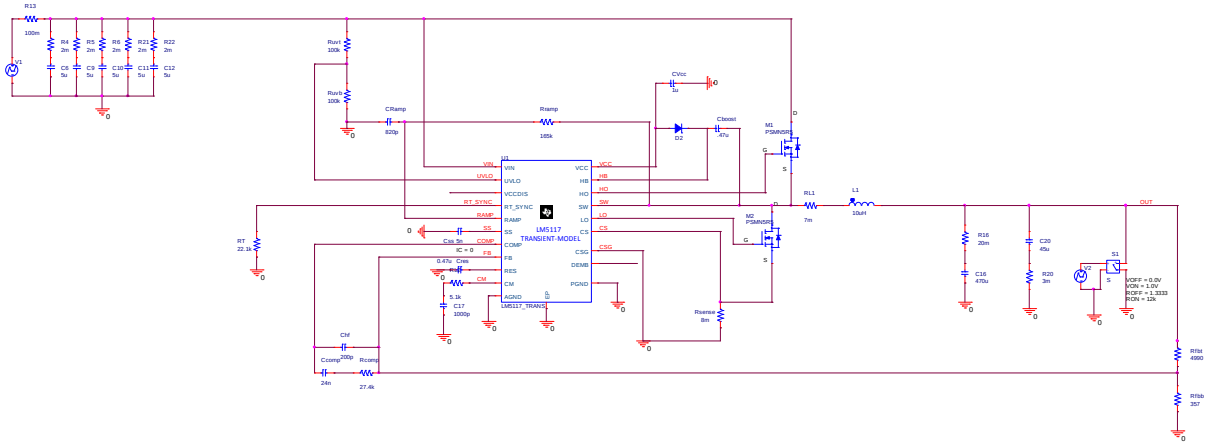
The simulation results of IsSpice and PSPICE are matching to acceptable level.

5.2 Load Transient

PSPICE Schematic for Condition1 (IRload = 9A – 1mA – 9A, VIN = 55V):



PSPICE Schematic for Condition2 (IRload= 9A – 1mA – 9A, VIN = 15V):



Description:

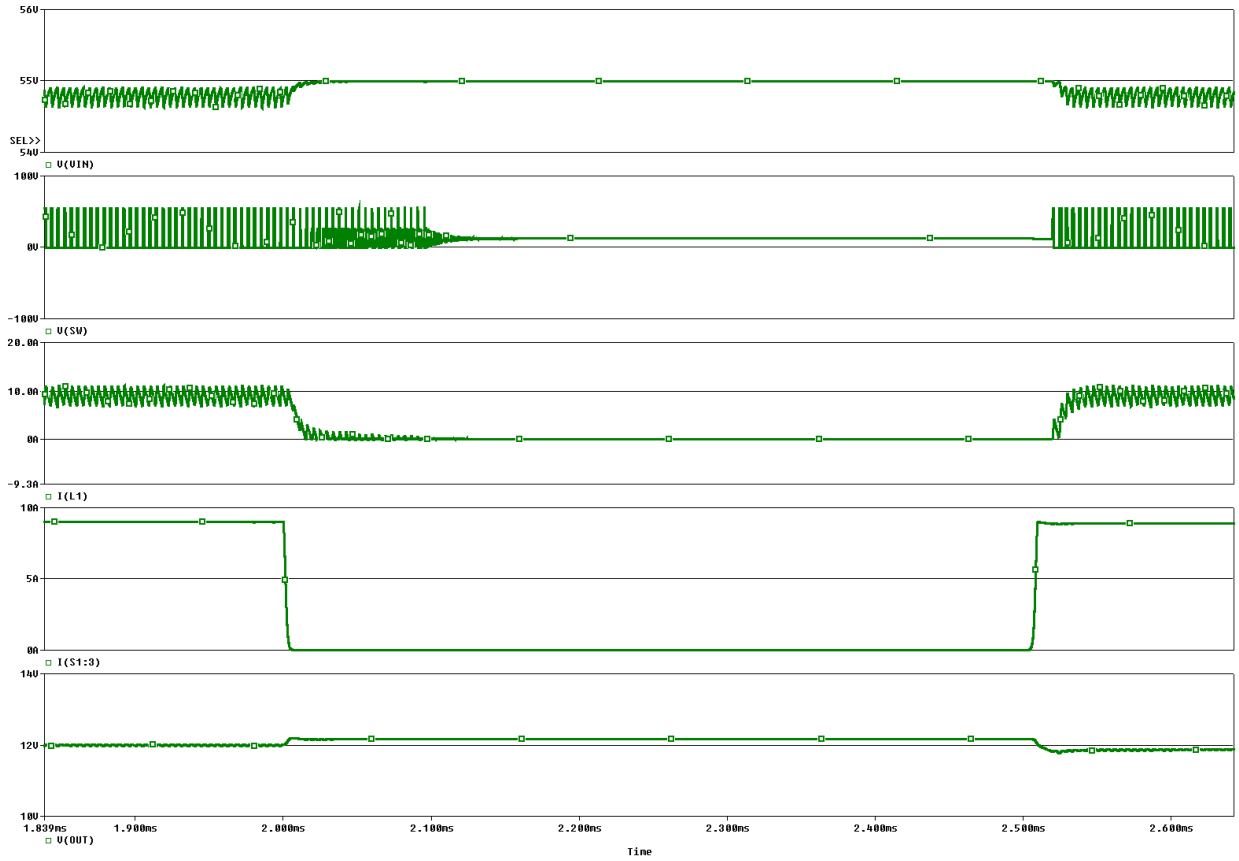
1. The test bench has been configured to test the load transient response of the model for following two conditions.

    a) Condition1: VIN = 55V, IRload = 9A-1mA-9A
    b) Condition2: VIN = 15V, IRload = 9A-1mA-9A

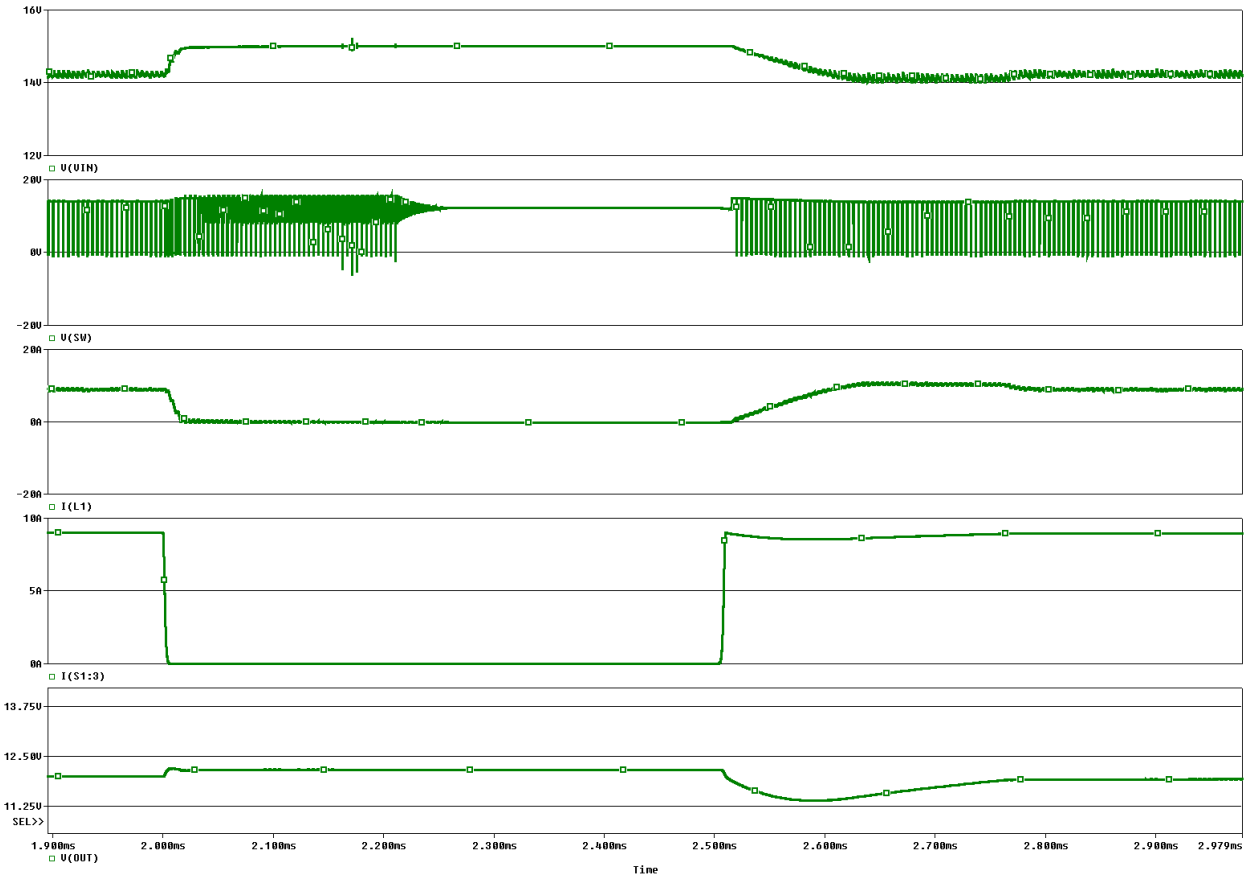
Test Conditions:

1. Condition1: VIN = 55V, IRLOAD =9A-1mA-9A
2. Condition2: VIN = 15V, IRLOAD = 9A-1mA-9A
3. IRLOAD is varied with rise and fall time of 10us.

Simulation Results for Condition1: VIN = 55V, IRLOAD = 9A-1mA-9A



Simulation Results for Condition2: VIN = 15V, IRLOAD = 9A-1mA-9A



Tabulation of Results:

Condition1 (VIN = 55V, IRLOAD = (9A-1mA-9A):

PARAMETERS	PSPICE	DATASHEET	UNITS
OVERSHOOT	*	-	mV
$T_{SETTLE\ (OVER)}$	-	-	us
UNDERSHOOT	37	-	mV
$T_{SETTLE\ (UNDER)}$	#	-	us

Note: - * DC shift of 197mV is observed at the output.
Undershoot observed is less than 1% of VOUT

Condition2 (VIN = 15V, = 9A-1mA-9A):

PARAMETERS	PSPICE	DATASHEET	UNITS
OVERSHOOT	*	-	mV
$T_{SETTLE\ (OVER)}$	-	-	us
UNDERSHOOT	605.43	-	mV
$T_{SETTLE\ (UNDER)}$	237.44	-	us

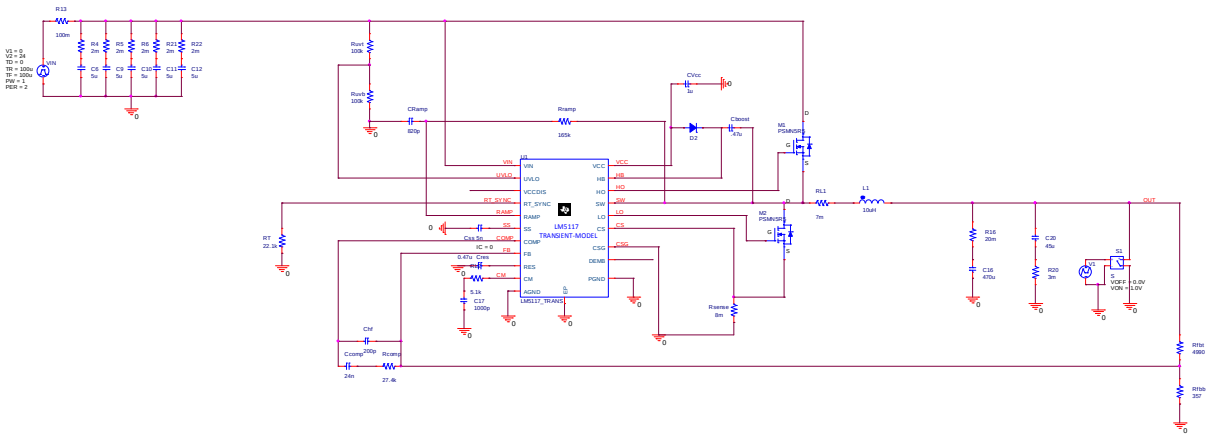
Note: - * DC shift of 148mV is observed at the output.

Conclusion:

The simulation results of PSPICE are matching to acceptable level.

5.3 Current Limit

PSPICE Schematic:



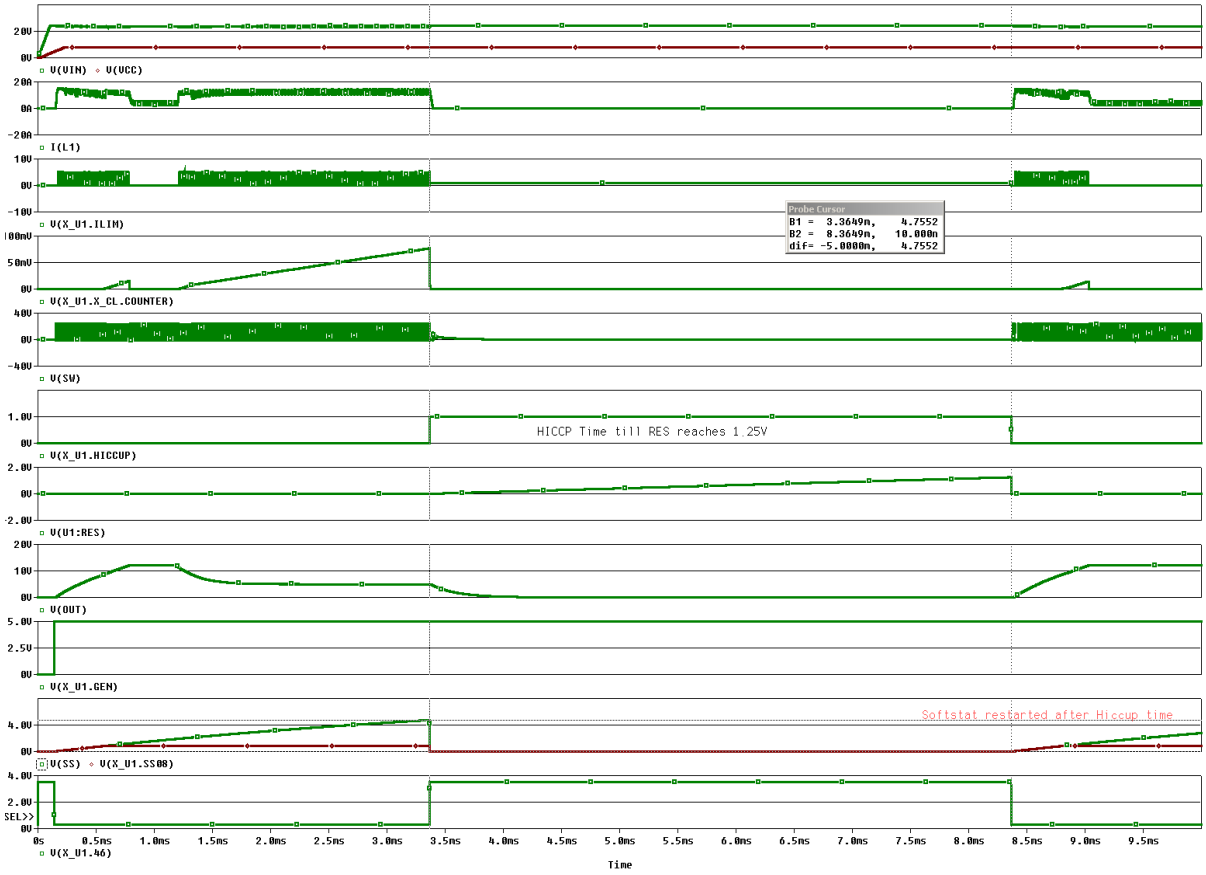
Description:

1. The test bench has been configured for 15V input and VOUT=12V
2. After output reaches steady state RLOAD is varied from 1.33Ω to 500mΩ.

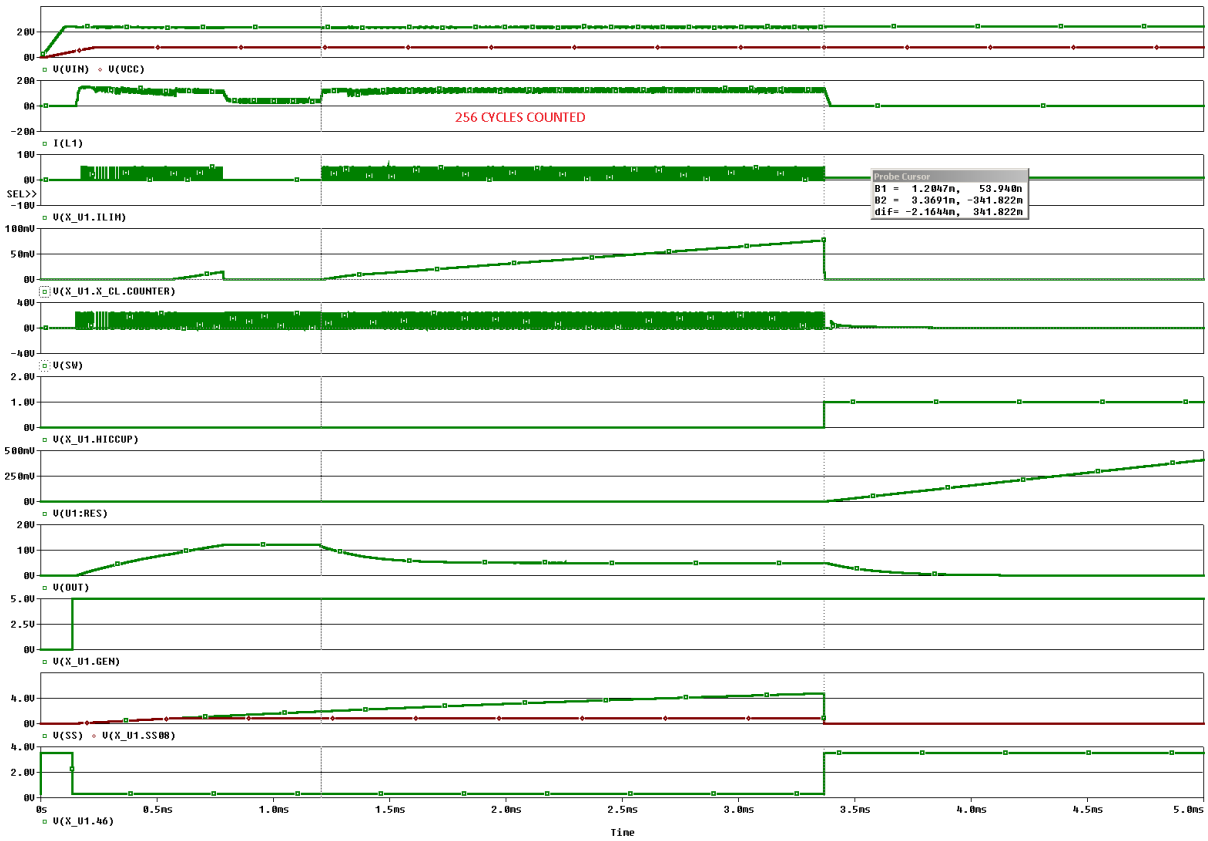
Test Conditions:

1. VIN = 24V
2. RLOAD is varied from 1.33Ω to 0.5Ω in 10us at 1.2ms.

Simulated Results:



Counter :-



Tabulation of Results:

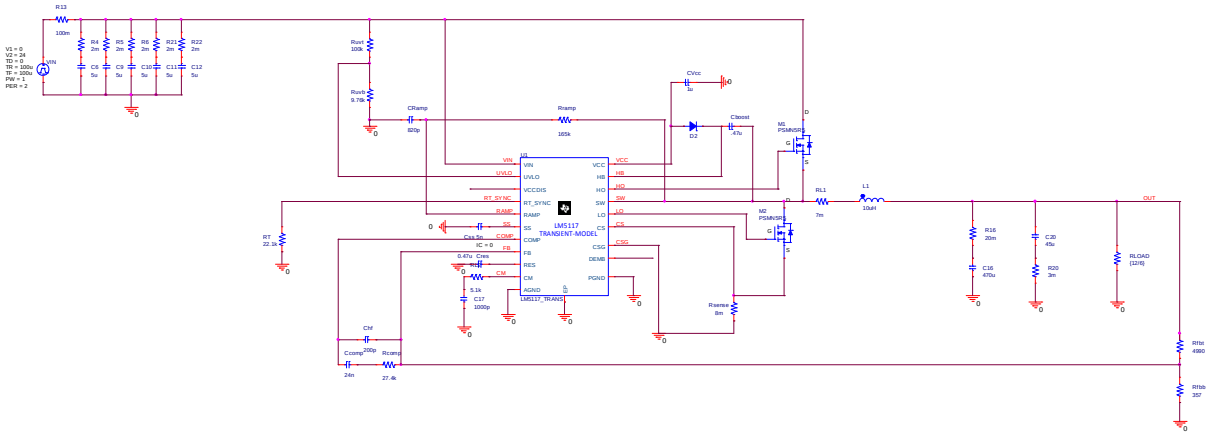
PARAMETERS	PSPICE	DATASHEET	UNITS
Peak Inductor Current	14.22	20	A

Conclusion:

When the current limit is hit for consecutive 256 cycles, the Internal SS pin is discharged and the Capacitor connected across the RES is charged with 10uA of current. When the voltage across the RES pin crosses the 1.25V the internal SS s started again.

5.4 Current Monitor Functionality

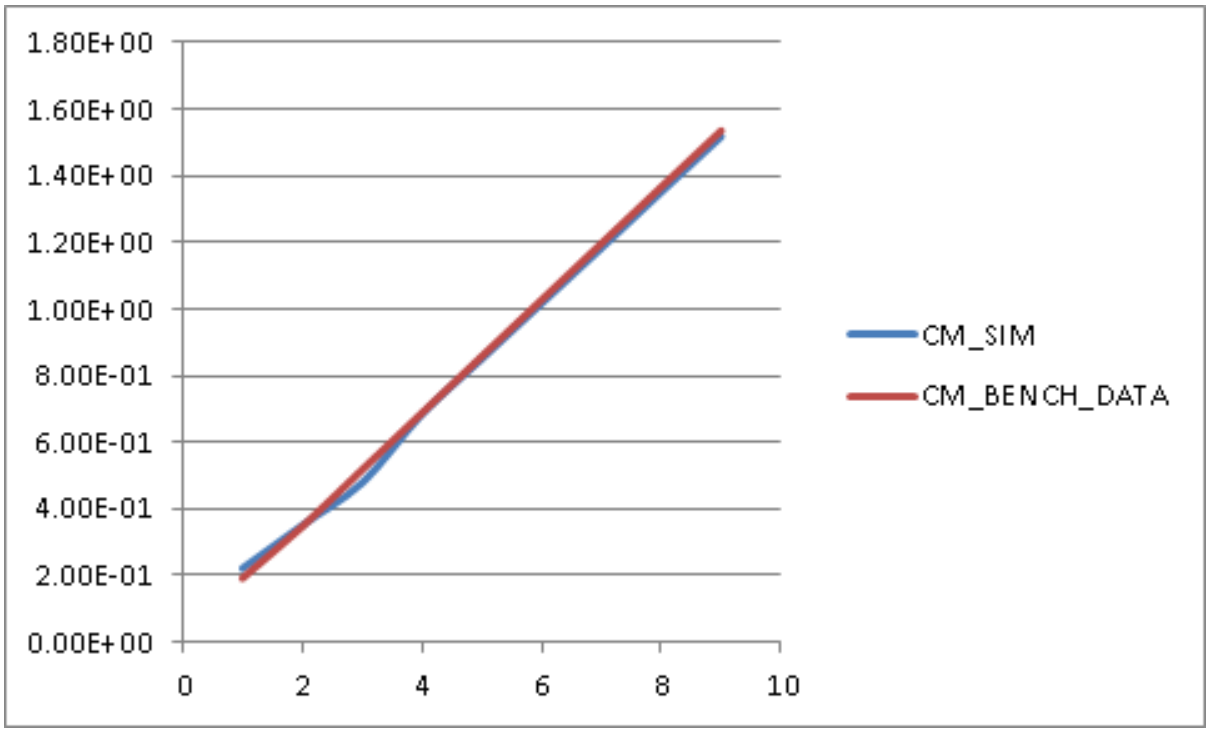
PSPICE Schematic:



Description:

1. The test bench has been configured for 24V input and VOUT=12V to measure the volatage across the CM pin for different loads from 1A-9A in step of 1A.

Overlaid Graph of the CM voltage vs the load current (Overlaid with the bench results)

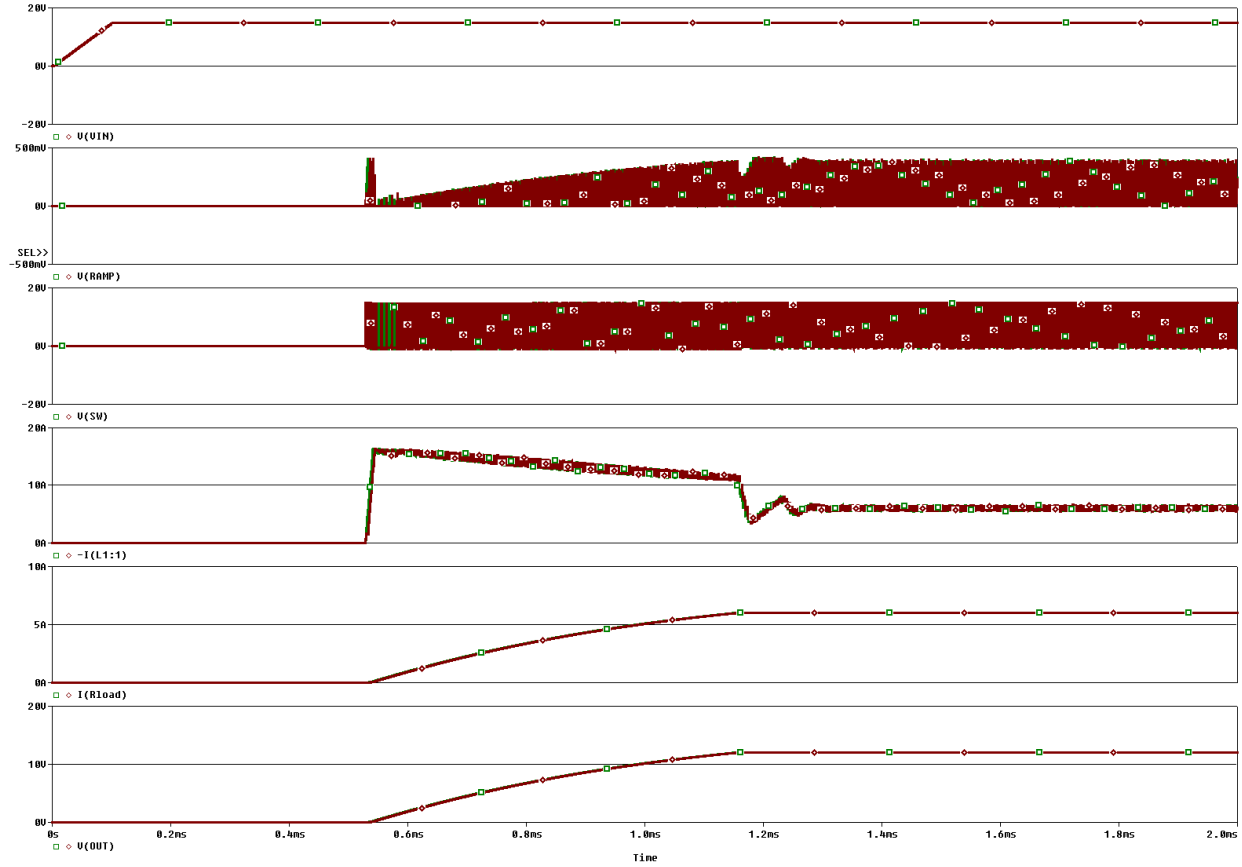


Conclusion:-

The simulated results are matching well with the Bench data for different Load current conditions.

6. Validation of Encrypted Model

Overlaid Results:



Conclusion:

- To validate the encrypted model, the START-UP testbench has been simulated using transient encrypted model.
- The results of simulation are overlaid on the simulation results of the unencrypted model.
- The overlaid results match within acceptable limits.