

TMDSCSK8127

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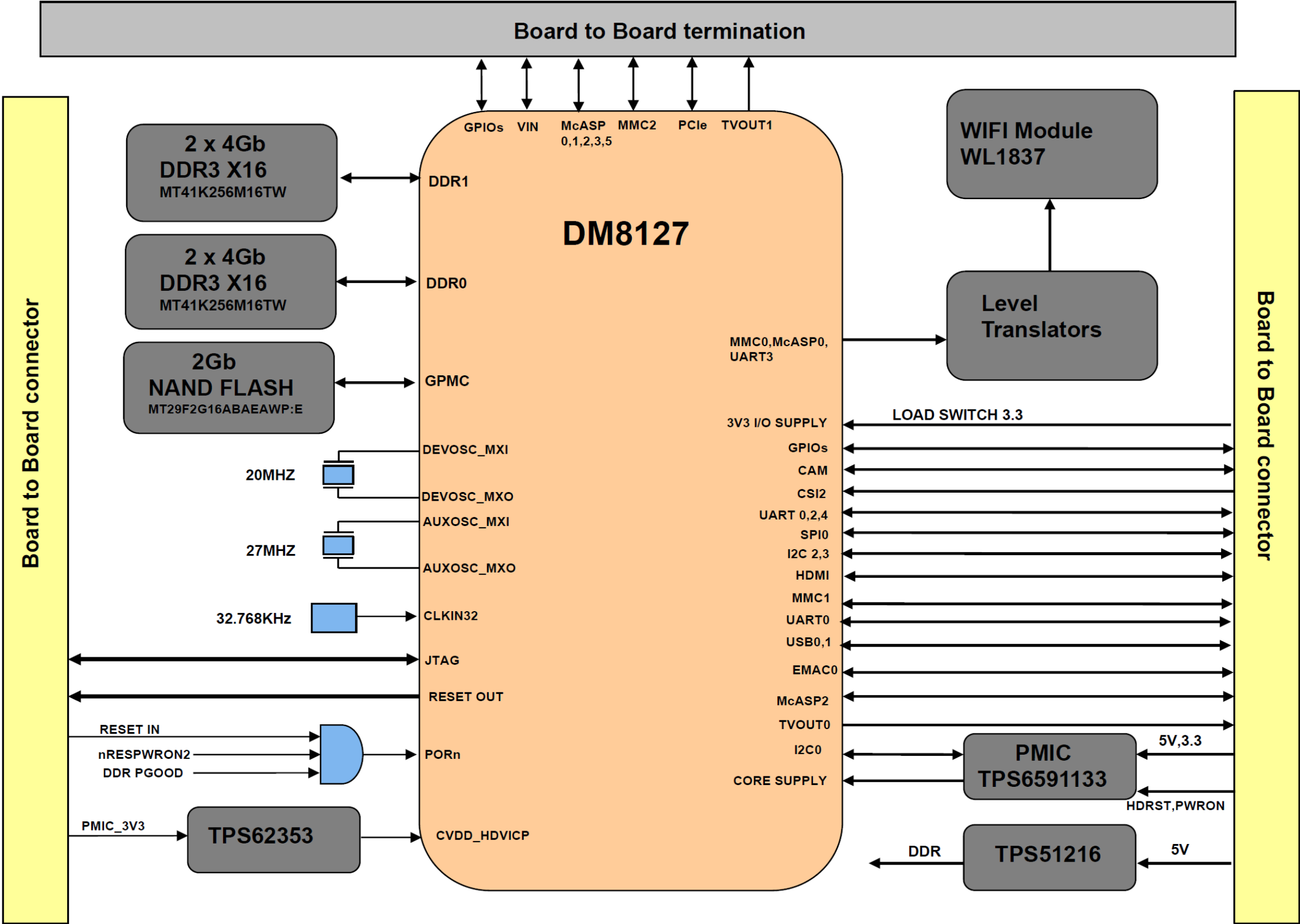
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REV	PRDN_A
VER	2.0

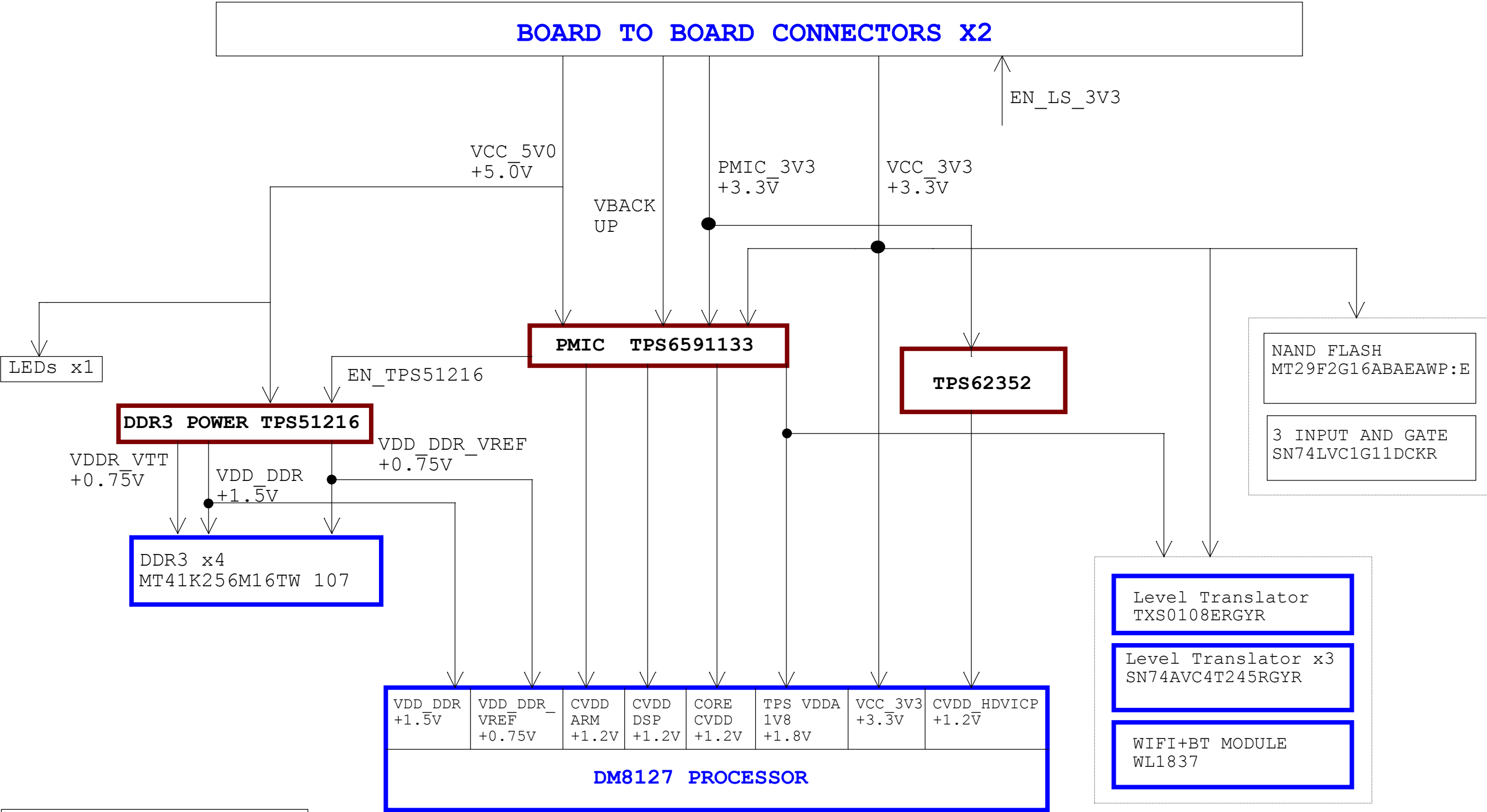
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	22nd SEP 2016	REVA to REVB change list implemented	Mistral Design Team	AJIT M B	AJIT M B
0.2	4th NOV 2016	I2C0 SDA and I2C0 SCL lines to PMIC updated	Mistral Design Team	AJIT M B	AJIT M B
0.3	17th NOV 2016	R36 Changed from 10K to 1K Reviewed & Baselined	Mistral Design Team	AJIT M B	AJIT M B
1.0	17th NOV 2016	Baselined	Mistral Design Team	AJIT M B	AJIT M B
1.1	6th JAN 2017	SD card Part# added to hardware schematics page	Mistral Design Team	AJIT M B	AJIT M B
2.0	6th JAN 2017	Baselined	Mistral Design Team	AJIT M B	AJIT M B

TMDSCSK8127 BLOCK DIAGRAM



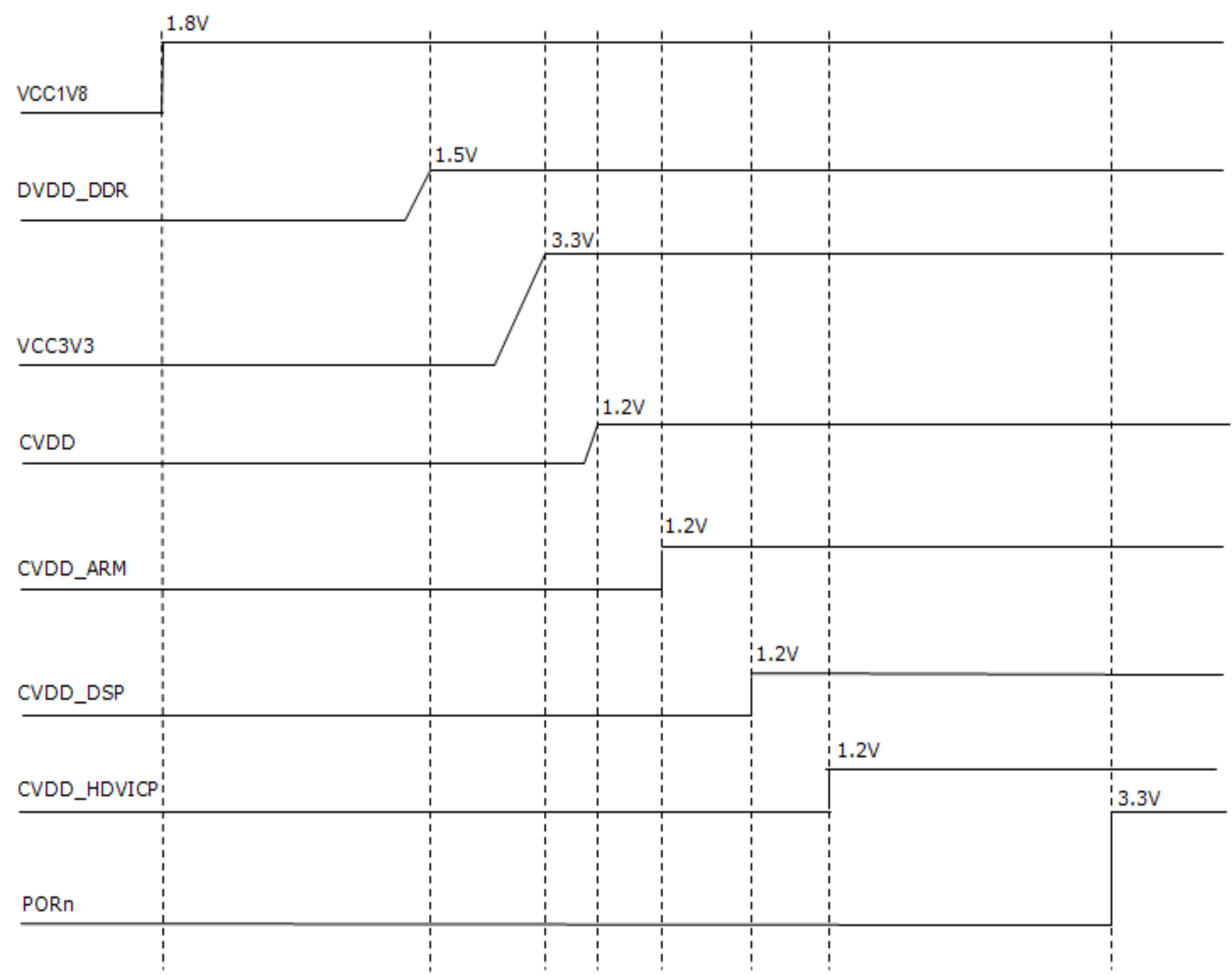
POWER FLOW DIAGRAM



NOTE:

- REGULATORS
- DEVICES
- Multiple powered device

POWER UP SEQUENCE



POWER CALCULATION

DM8127_SOM											
Part Number	QTY	CVDD (DC DC CTRL)	CVDD_ARM (PMIC VDD1)	CVDD_DSP (PMIC VDD2)	VDD_1V8 (PMIC VIO)	VDDA_1V8	TPS62353YZGT (CVDD_HDVIC P)	TPS51116 (VCC_1V5)	DDR_VTT 0.75	VCC_3V3 (Carrier Card)	PMIC_3V3
TMS320DM8127	1	1125.00	365.00	409.00	53.00	53.00	0.00	402.00		139.00	
DDR3	4							1040	544		
MT29F4G16ABAEAWP	1									30	
TXS0108EPWR	1				0.036					0.108	
WL1837MOD	1									909.0909091	
SN74AVC4T245RGYR	3				300					300	
SN74LVC1G11DCKR	1									100	
SN74CBTLV3257RGYR	1									128	
Total (mA)		1125.00	365.00	409.00	353.04	53.00	0.00	1762.00	544.00	1606.20	610.67
Input voltage		5	3.3	3.3	3.3		3.3	5	1.5	5	5
Efficiency		0.85	0.85	0.85	0.85		0.85	0.85	0.85	0.85	0.85
Quiescent current (mA)											
Output Voltage		1.2	1.2	1.2	1.8		1.2	1.5	0.75	3.3	3.3
Current Drawn from Input		317.6470588	156.1497326	174.973262	226.5471658	53.00	0	621.8823529	320	1247.166212	474.167419
Current Drawn from 5V(mA)	2660.863042										

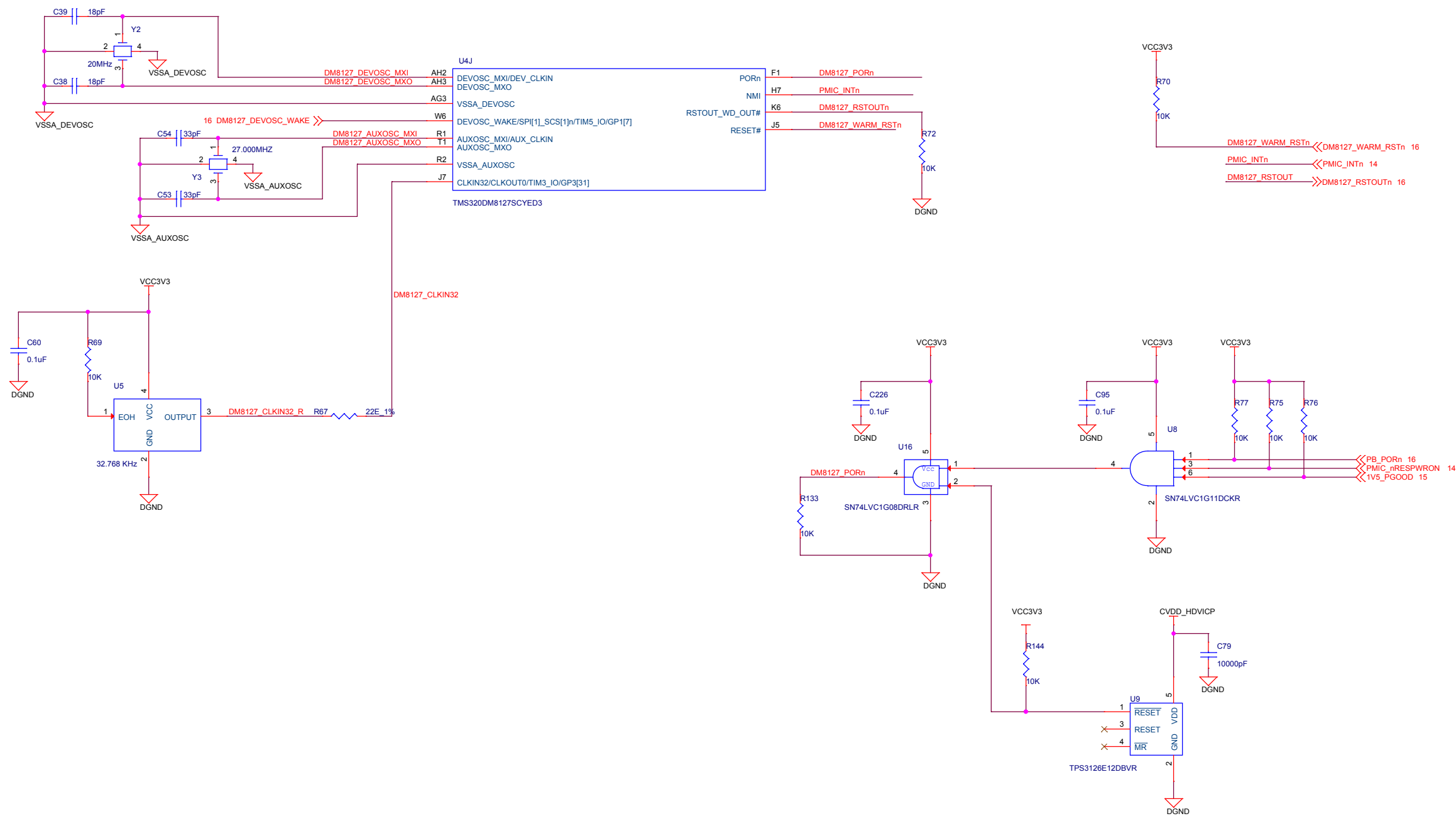
GPIO TABLE

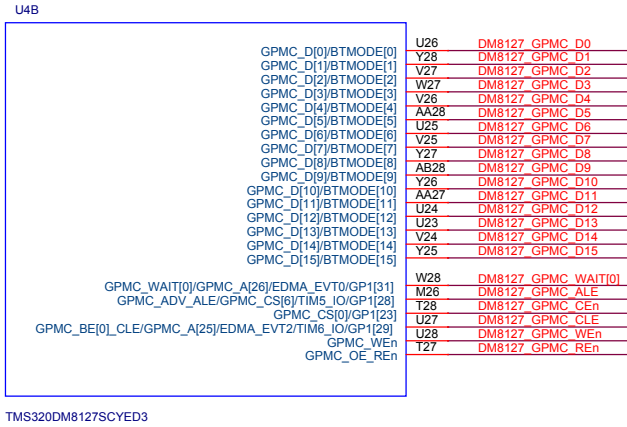
GPIO NAME	PROCESSOR PIN	PURPOSE	Internal/ External PU/PD states
DM8127_GPMC_WPn	AG7 (GP2[22])	WRITE PROTECT TO NAND FLASH	IPD
DM8127_WLAN_IRQ	AG28 (GP3[21])	INTERRUPT FROM WL1837 MOD	IPU
DM8127_WLAN_EN	L7 (GP0[27])	WLAN ENABLE SIGNAL TO WIFI MODULE (WL1837)	IPD
DM8127_BT_EN	T2 (GP0[30])	BLUETOOTH ENABLE SIGNAL TO WIFI MODULE (WL1837)	IPD
DM8127_PMIC_SLEEP	AG27 (GP3[14])	PMIC SLEEP INPUT	IPD
BB_ENET_RSTn	AF27 (GP3[20])	ETHERNET PHY RESET	IPU
BB_GPIO2_6	V23 (GP2[6])	SWITCH 1	IPD
BB_GPIO1_13	AE28 (GP1[13])	SWITCH 2	IPD
BB_GPIO1_1	AG6 (GP1[1])	SWITCH3	IPU
BB_GPIO1_15	AD28 (GP1[15])	SWITCH4	IPU
BB_GPIO1_30	V28 (GP1[30])	LED1	IPD
BB_GPIO1_16	AC28 (GP1[16])	LED2	IPD
BB_GPIO0_8	R5 (GP0[8])	LED3	IPD
BB_GPIO3_30	AF28 (GP3[30])	LED4	IPU
BB_GPIO1_0	AH6 (GP1[0])	LED5	IPU

I2C TABLE

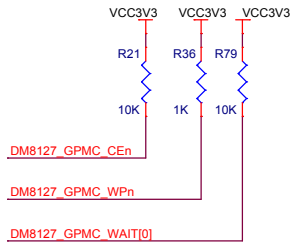
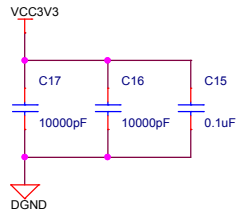
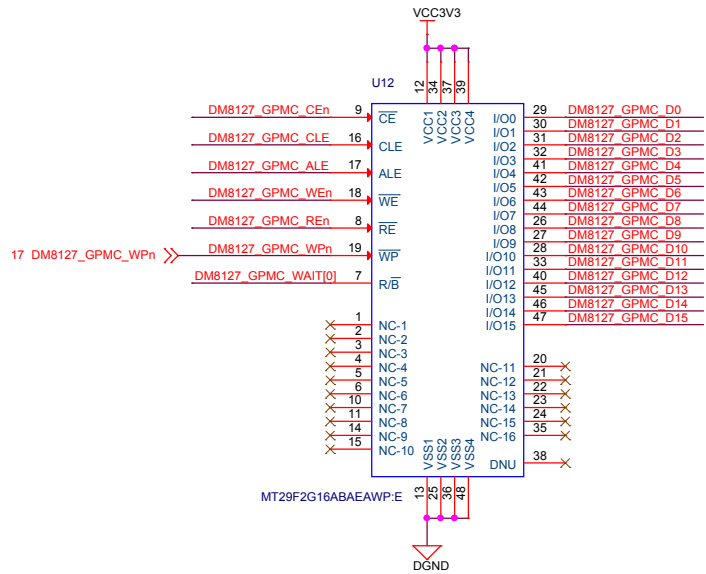
MASTER	I2C USED	SLAVE DEVICE	ADDRESS
DM8127 PROCESSOR	I2C0	PMIC	0x2D (General Purpose)
	I2C1/ HDMI	Audio Codec (TLV320AIC3104)	0x18
		Display Device	Depends on connected HDMI monitor
	I2C2	Camera Module	0x10 (Camera Sensor)
			0x2D (LVDS module)

DM8127 CLOCKS AND RESET





NAND FLASH



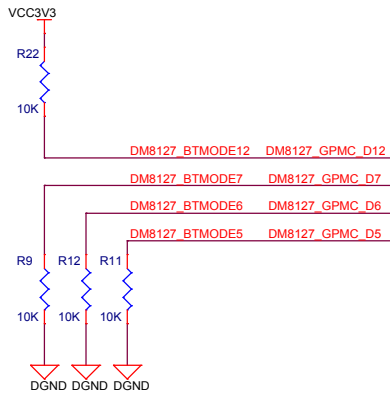
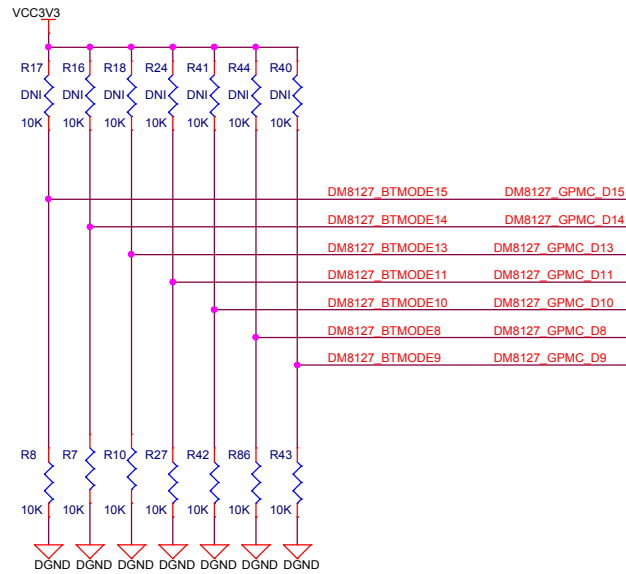
BOOTMODE SELECTION

BOOTMODE PIN	DEFAULT SETTING	DESCRIPTION
BTMODE15	0	GPMC CS0 Wait disabled
BTMODE14	0	GPMC CS0 Address/Data not muxed
BTMODE13	0	
BTMODE12	1	GPMC CS0 16bit Data bus
BTMODE11	0	RSTOUT is asserted when a Watchdog Timer reset, POR, RESET, or Emulation/ Software-Global Cold/Warm reset occurs
BTMODE10	0	GPMC Option A
BTMODE9	0	MII (GMII) Ethernet PHY Mode
BTMODE8	0	
BTMODE7	0	RSV
BTMODE6	0	RSV
BTMODE5	0	RSV
BTMODE[4:0]	10011	NAND BOOT
	10111	MMC BOOT

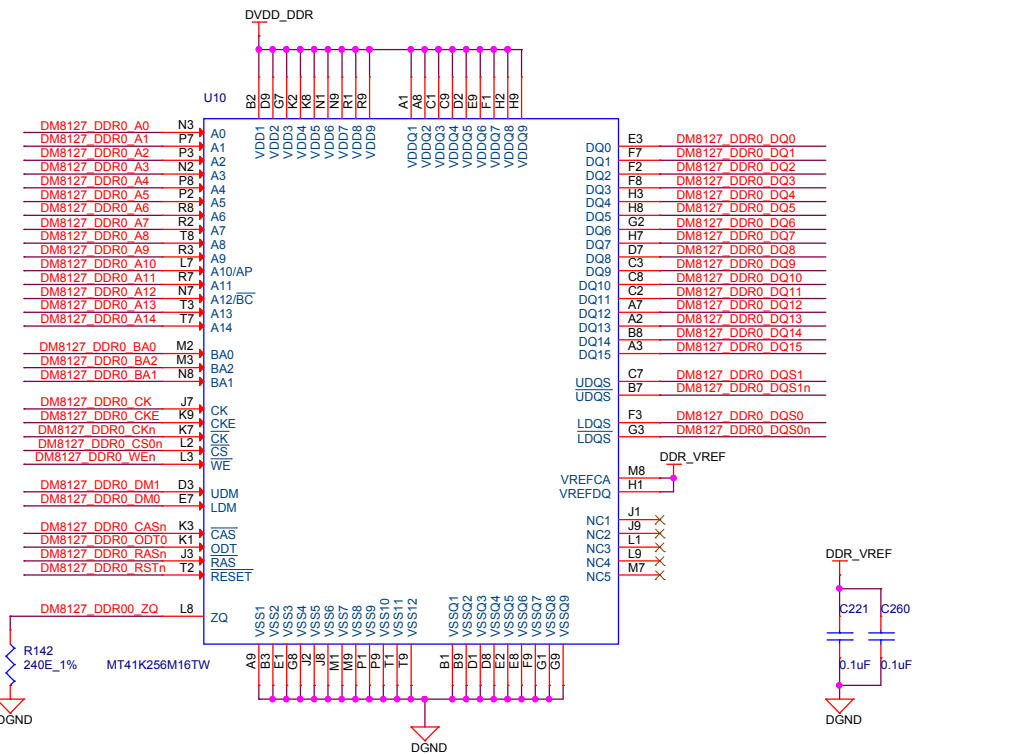
BOOTMODE SELECTION

SW1	SELECTION
ON	MMC BOOT
OFF	NAND

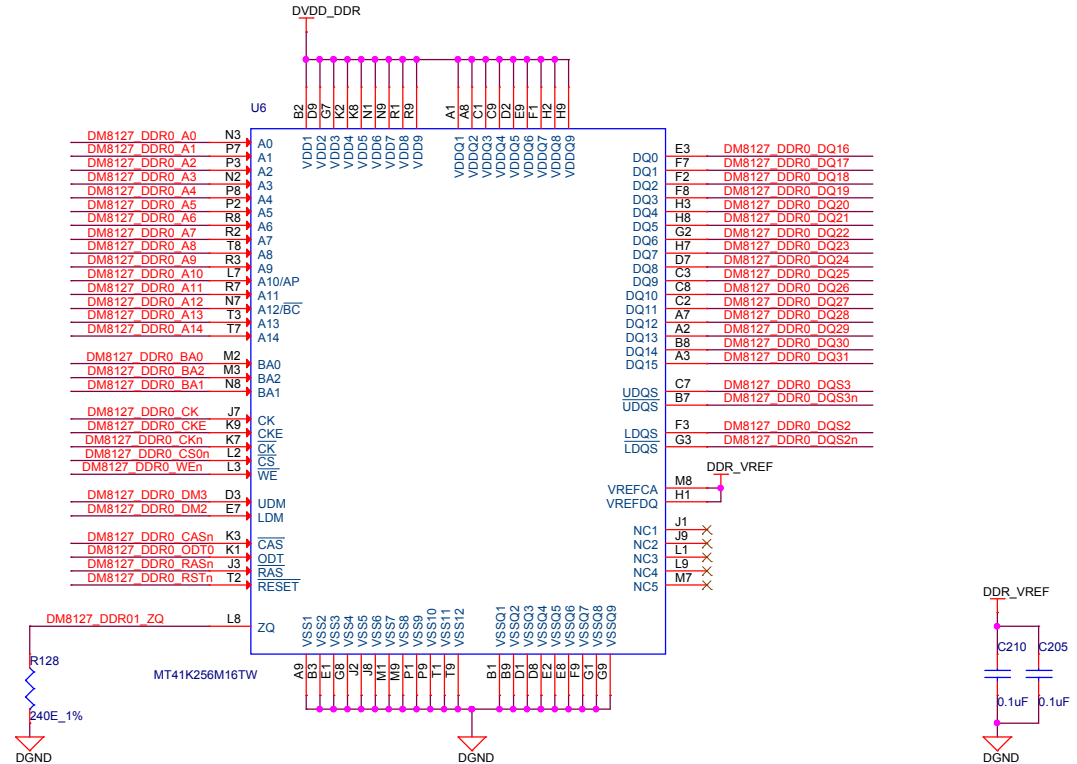
BOOTMODES



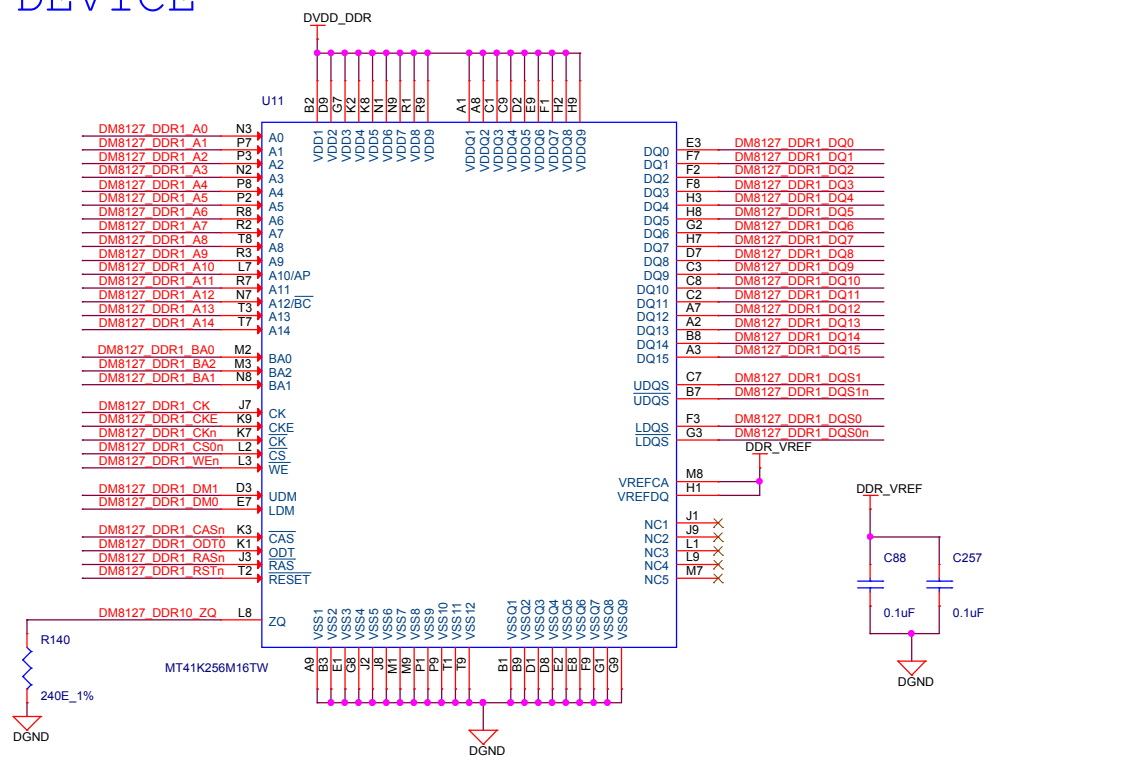
DDR3 DEVICE



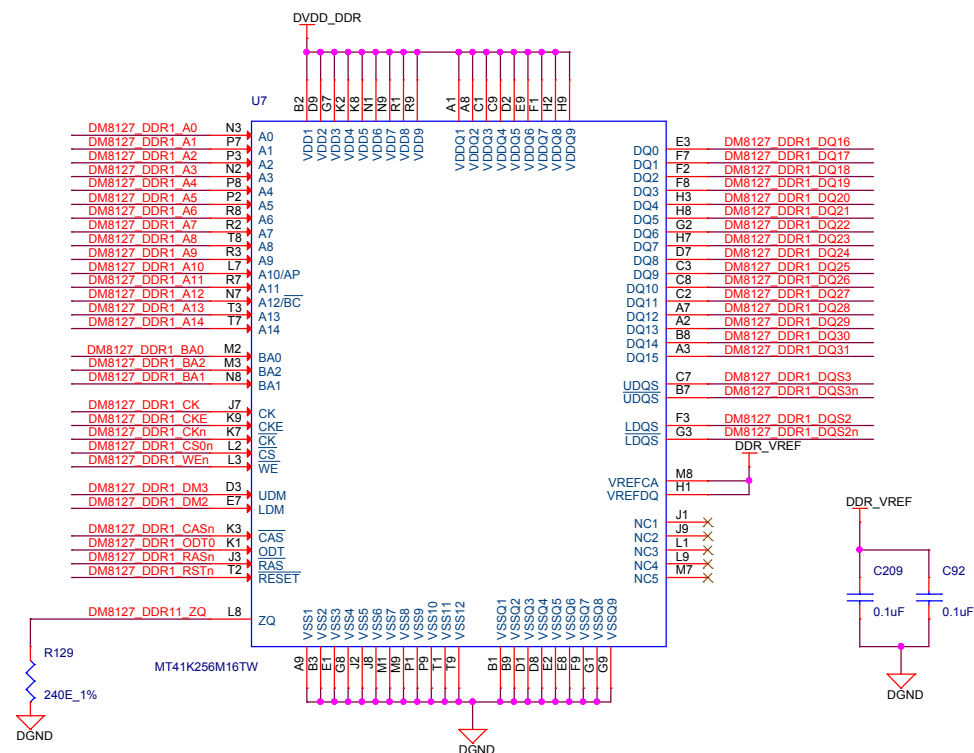
DDR3 DEVICE



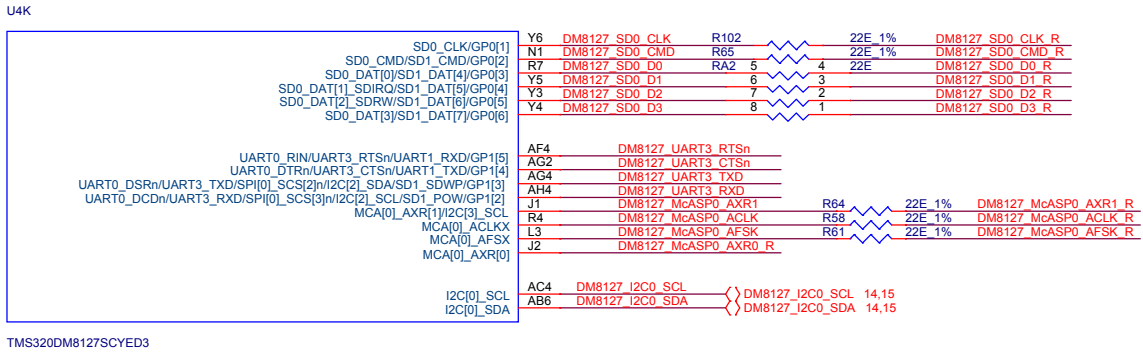
DDR3 DEVICE



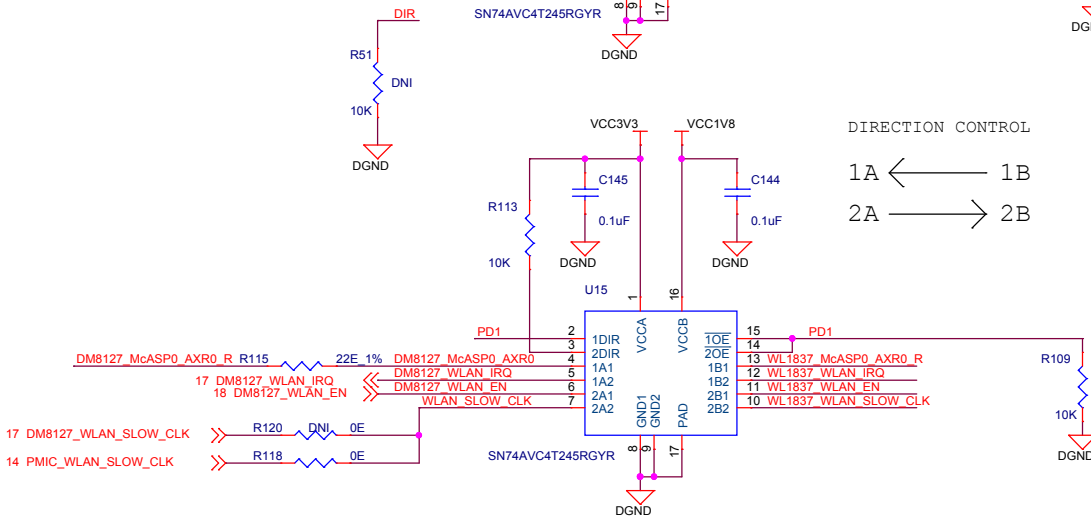
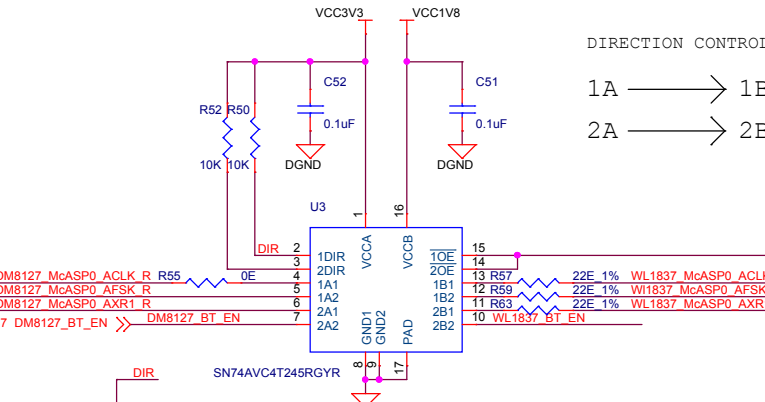
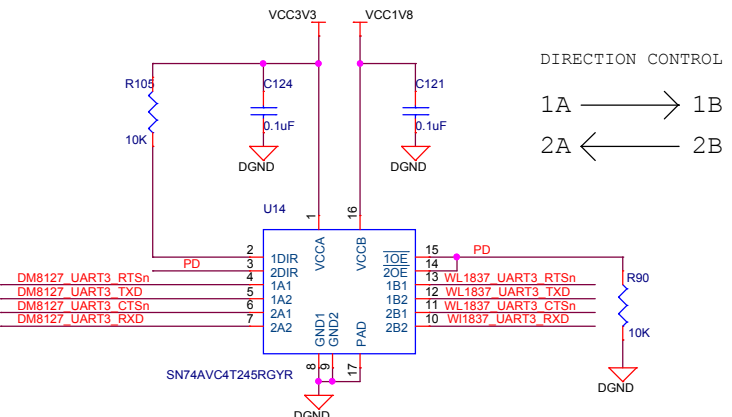
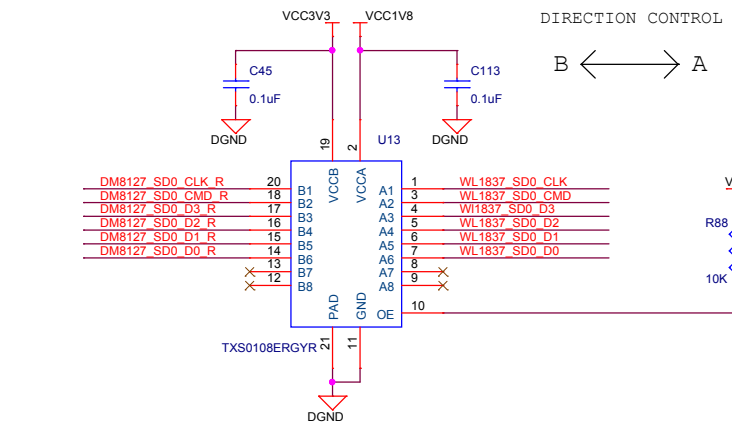
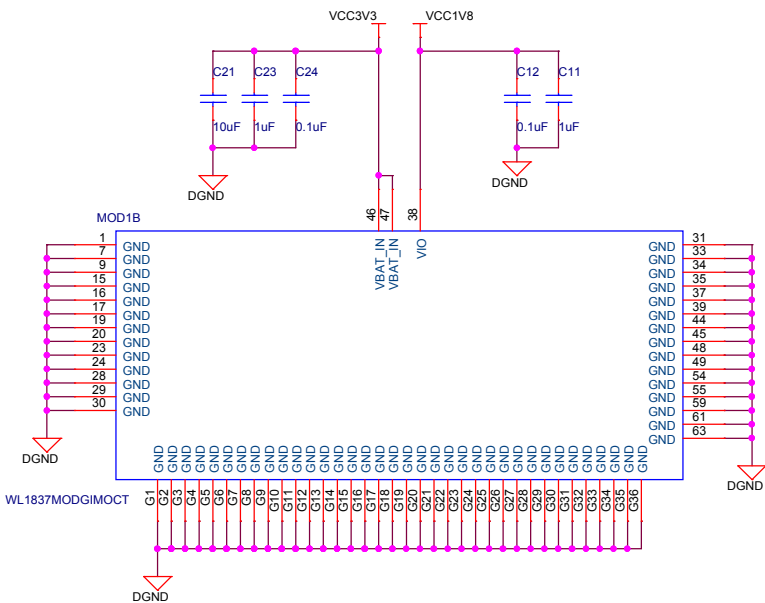
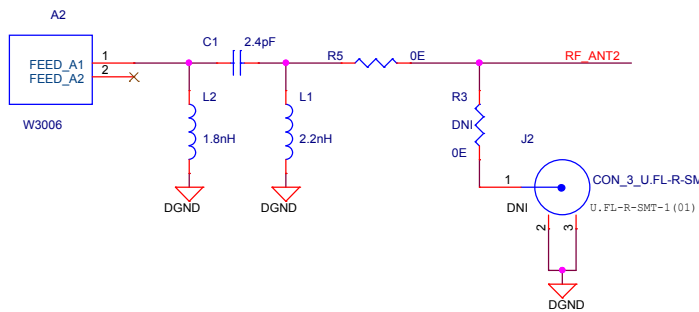
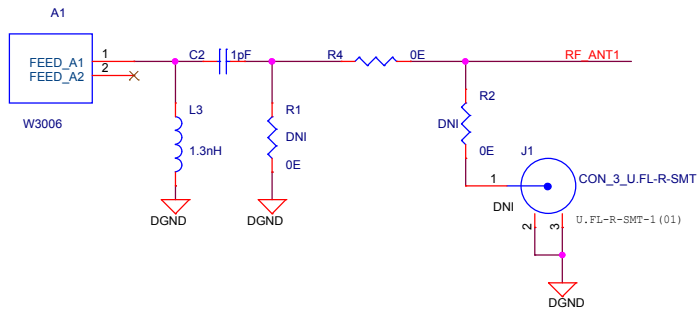
DDR3 DEVICE

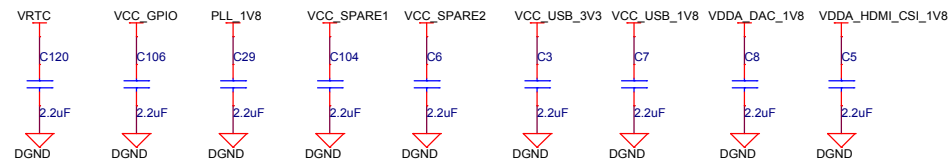


WLAN, BT LEVEL TRANSLATORS

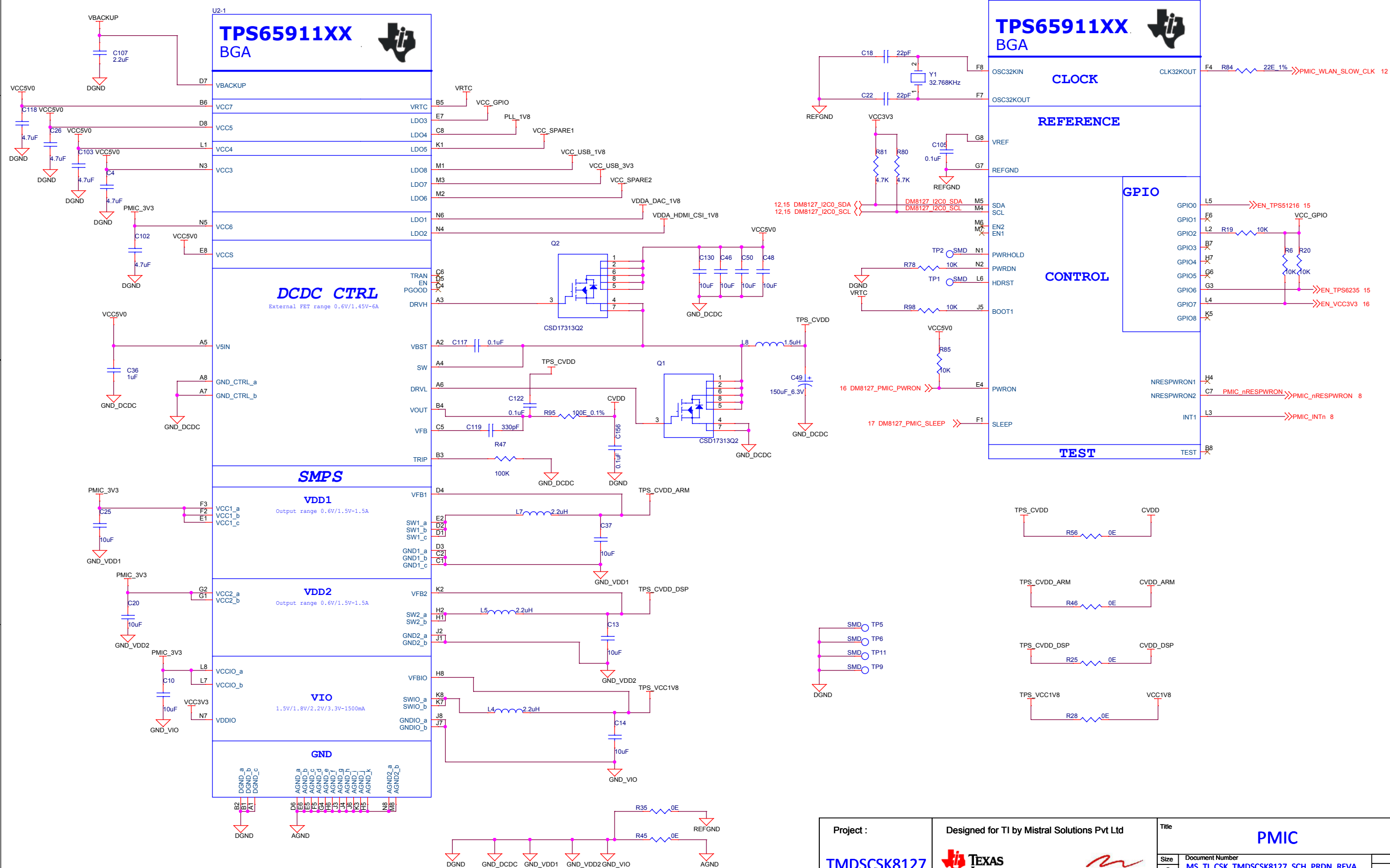


WL1837 MODULE

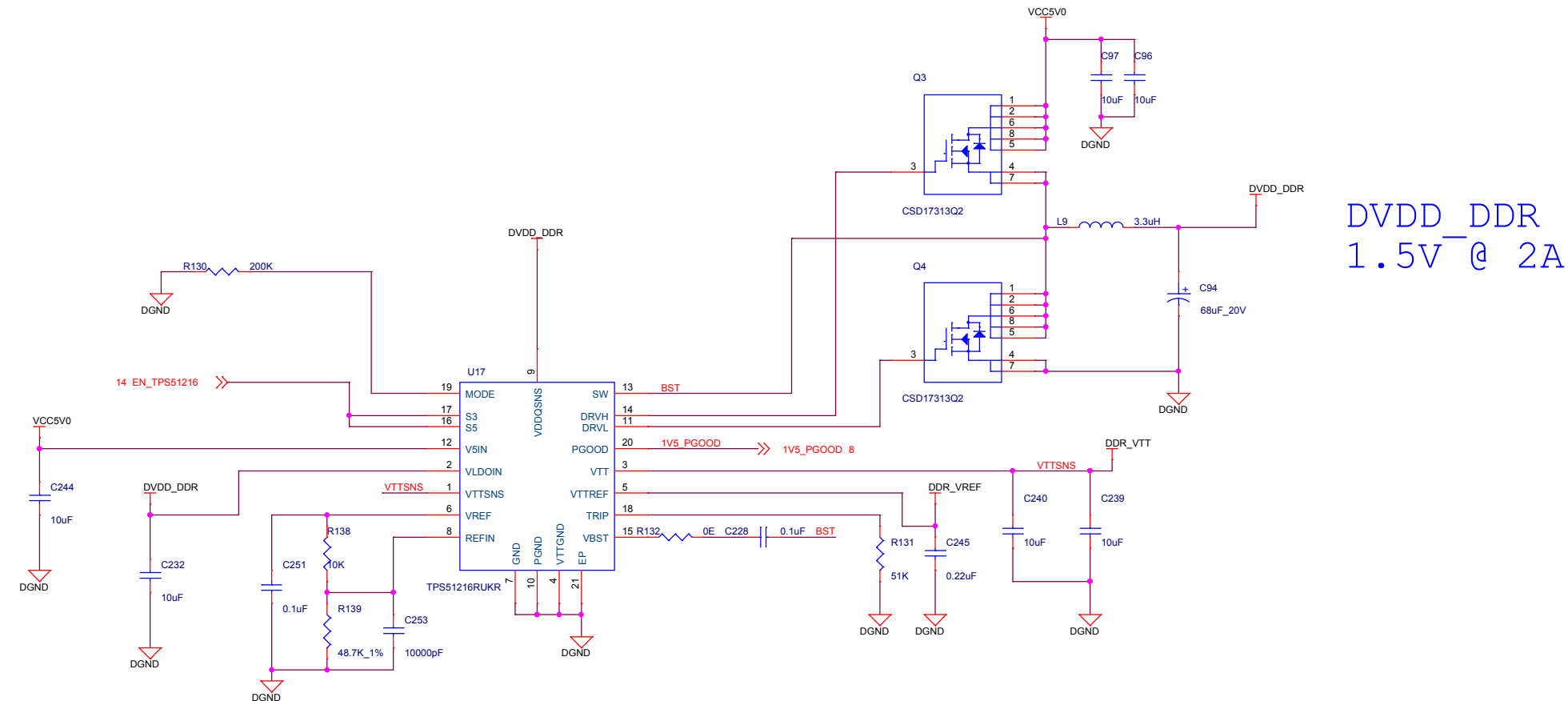




PMIC

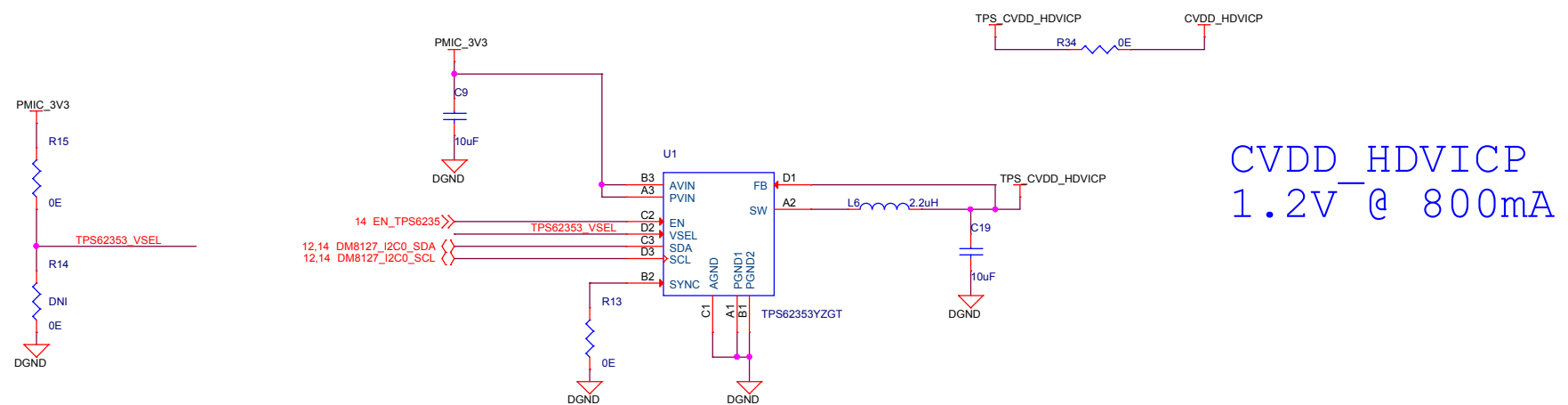


DDR3 POWER



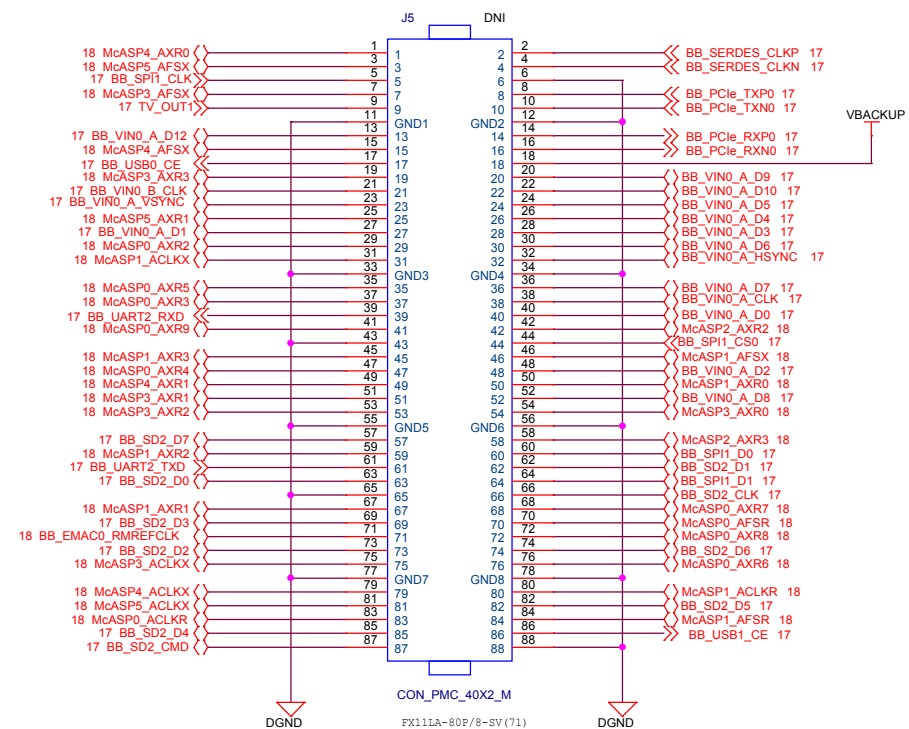
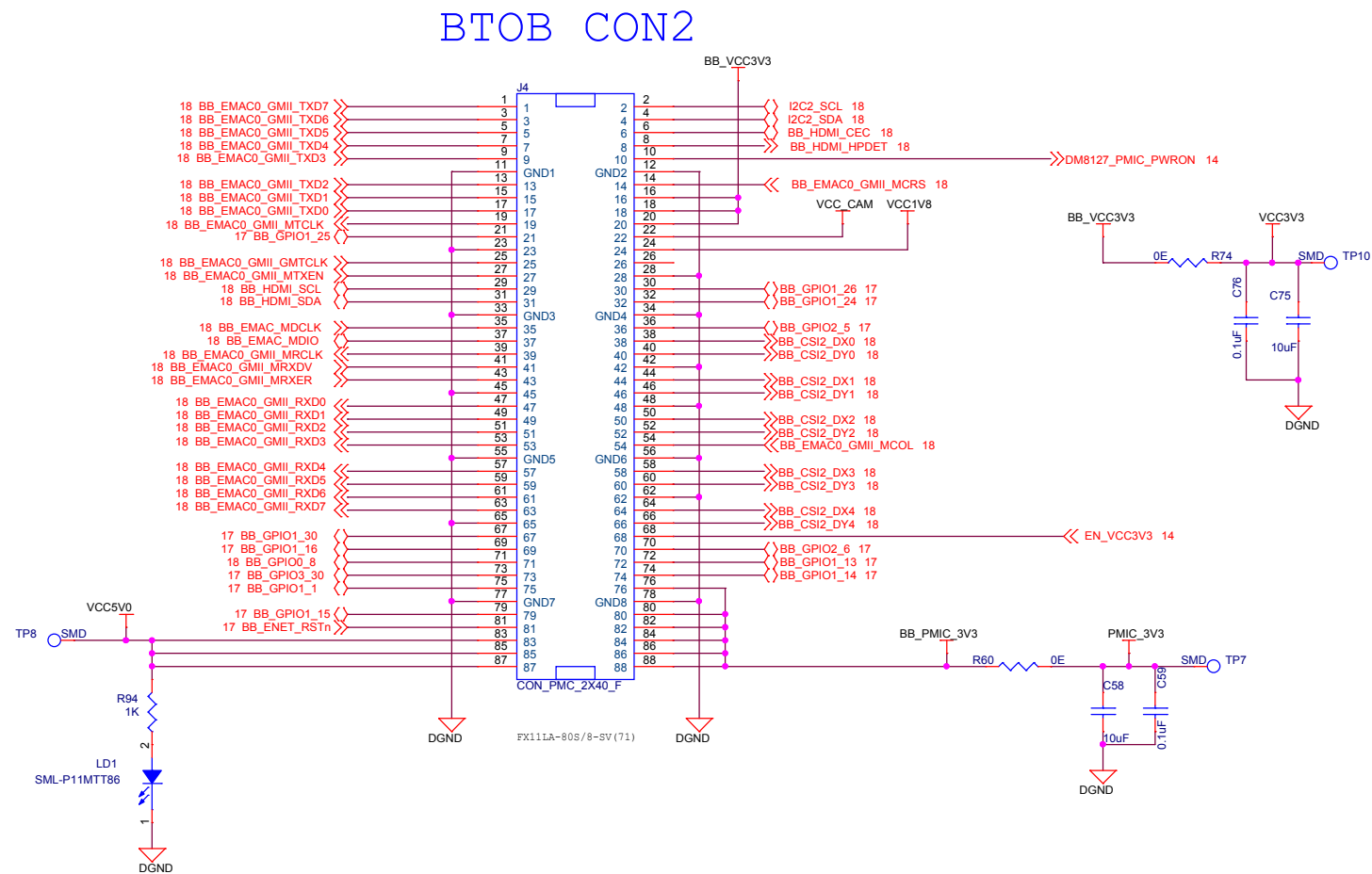
DVDD_DDR
1.5V @ 2A

CVDD HDVICP

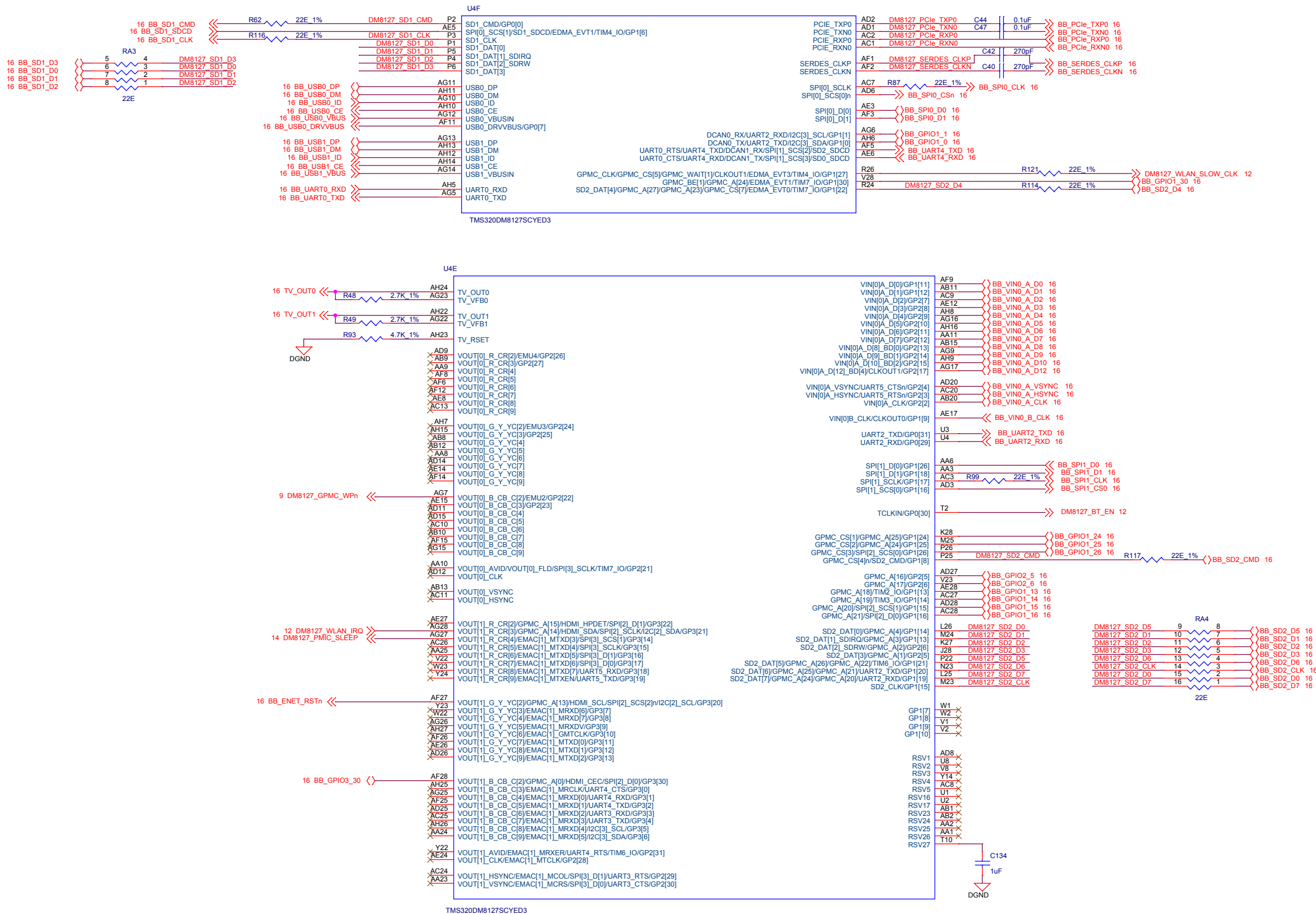


CVDD HDVICP
1.2V @ 800mA

BOARD TO BOARD TERMINATION



BOARD TO BOARD SIGNALS

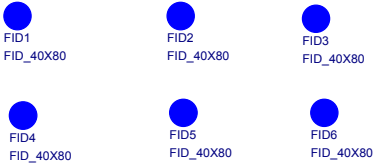


BOARD TO BOARD SIGNALS



HARDWARE SCHEMATICS

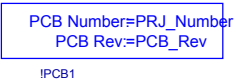
FIDUCIALS



MicroSD CARD



LOGOs & LABELs



Serial No:



ASSY REV



[Label Assembly Note](#)

ZZ1

The boards and components must be baked before assembly

[Label Assembly Note](#)

ZZ2

Provide serial numbers to the assembled boards for identification

[Label Assembly Note](#)

ZZ3

Please carry out the cold points check verification and provide the report for each assembled board

[Label Assembly Note](#)

ZZ4

The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

[Label Assembly Note](#)

ZZ5

All MSL components should be baked as per JEDEC standard

[Label Assembly Note](#)

ZZ6

PCB should be baked at 120 degree for 8 hours

[Label Assembly Note](#)

ZZ7

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

[Label Assembly Note](#)

ZZ8

These assemblies are ESD sensitive, ESD precautions shall be observed.

[Label Assembly Note](#)

ZZ9

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Project :

TMDSCSK8127

Designed for TI by Mistral Solutions Pvt Ltd



Title
HARDWARE SCHEMATICS

Size	Document Number	Rev
C	MS_TI_CSK_TMDSCSK8127_SCH_PRDN_REVA	PRDN_A
Date:	Friday, January 06, 2017	Sheet 19 of 19