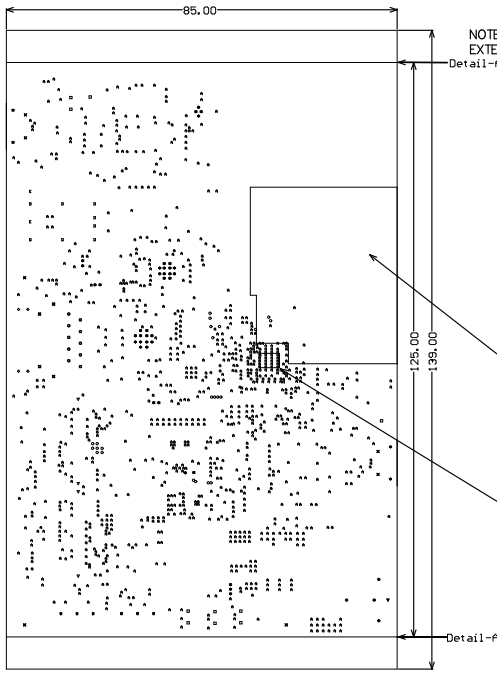
Symbol	Count	Hole Size	Plated	Hole Type	Hole Tolerance (+)	Hole Tolerance (-)	Drill Layer Pair	Routed Path Length
✖	3	160.00mil (4.064mm)	PTH	Round			Top Layer - Bottom Layer	-
⧈	2	127.95mil (3.250mm)	NPTH	Round			Top Layer - Bottom Layer	-
E	2	88.58mil (2.250mm)	NPTH	Round			Top Layer - Bottom Layer	-
⊠	2	66.93mil (1.700mm)	PTH	Round			Top Layer - Bottom Layer	-
▽	1	62.99mil (1.600mm)	NPTH	Round	3.94mil (0.100mm)	0.00mil (0.000mm)	Top Layer - Bottom Layer	-
B	6	51.18mil (1.300mm)	PTH	Round			Top Layer - Bottom Layer	-
▽	4	40.16mil (1.020mm)	NPTH	Round			Top Layer - Bottom Layer	-
◇	4	40.16mil (1.020mm)	PTH	Round			Top Layer - Bottom Layer	-
□	10	40.00mil (1.016mm)	PTH	Round			Top Layer - Bottom Layer	-
D	8	39.37mil (1.000mm)	PTH	Round	1.97mil (0.050mm)	1.97mil (0.050mm)	Top Layer - Bottom Layer	-
⌬	10	35.43mil (0.900mm)	PTH	Round			Top Layer - Bottom Layer	-
⌑	4	33.47mil (0.850mm)	PTH	Round			Top Layer - Bottom Layer	-
○	23	10.00mil (0.254mm)	PTH	Round	3.00mil (0.076mm)	3.00mil (0.076mm)	Top Layer - Bottom Layer	-
A	1055	8.00mil (0.203mm)	PTH	Round	3.00mil (0.076mm)	3.00mil (0.076mm)	Top Layer - Bottom Layer	-
✱	39	7.87mil (0.200mm)	PTH	Round			Top Layer - Bottom Layer	-
✲	4	23.62mil (0.600mm)	PTH	Slot			Top Layer - Bottom Layer	27.56mil (0.700mm)
◎	4	39.37mil (1.000mm)	PTH	Rectangle			Top Layer - Bottom Layer	(Mixed)
	1181 Total							

Slot definitions : **Routed Path Length** = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

2 IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	MICROSTRIP	L1	10.6	---	50	L02
02	EDGE COUPLED MICROSTRIP	L1	6	4	90	L02
03	EDGE COUPLED MICROSTRIP	L1	5	5	100	L02
04	UNCOATED COPLANAR	L1	8.4	3.94	50	L02
05	EDGE COUPLED STRIPLINE	L3	4.7	7.3	100	L02/L04
06	STRIPLINE	L3, L6	5.5	---	50	L02/L04,L05,L07
07	MICROSTRIP	L8	8.3	---	50	L07
08	EDGE COUPLED MICROSTRIP	L8	5	5.5	90	L07
09	EDGE COUPLED MICROSTRIP	L8	4	6	100	L07
10	EDGE COUPLED MICROSTRIP	L8	4	14	120	L07

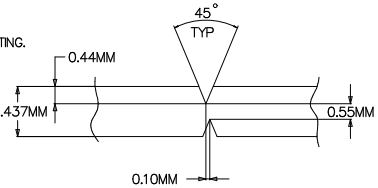


THIS IS AN IMPEDANCE CONTROLLED BOARD.

NOTE :
EXTERNAL LAYER CU THICKNESSES ARE FINISHED THICKNESS AFTER PLATING.

2 LAYER STACKUP

Layer	Name	Material	Thickness	Constant		Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.80mil	3.5		
3	Top Layer	Copper	1.40mil			
4	Dielectric 1	8ID3009	5.00mil	9		
5	GND1	Copper	1.40mil			
6	Dielectric 2	FR-4 High Tg	5.00mil	4.04		
7	SIG1	Copper	0.70mil			
8	Dielectric 3	FR-4 High Tg	10.00mil	4.04		
9	PWR1	Copper	1.40mil			
10	Dielectric 4	FR-4 High Tg	5.00mil	4.04		
11	PWR2	Copper	1.40mil			
12	Dielectric 5	FR-4 High Tg	10.00mil	4.04		
13	SIG2	Copper	0.70mil			
14	Dielectric 6	FR-4 High Tg	5.00mil	4.04		
15	GND2	Copper	1.40mil			
16	Dielectric 7	FR-4 High Tg	5.00mil	4.04		
17	Bottom Layer	Copper	1.40mil			
18	Bottom Solder	Solder Resist	0.80mil	3.5		
19	Bottom Overlay					



DETAIL-A(V. SCORE DETAILS)
SCALE:NTS

NOTES : UNLESS OTHERWISE SPECIFIED.

1. FABRICATE PER IPC-6012A CLASS 2.
2. FOR IMPEDANCE DETAILS REFER STACKUP & IMPEDANCE TABLE.
3. PRINTED WIRING BOARD SHALL COMPLY WITH REQUIREMENTS OF ANSI/J-STD-003.
4. SURFACE FINISH: IMMERSION SILVER
5. SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR RED.
6. SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.
7. THIS PRINTED WIRING BOARD IS DESIGNED WITH A MINIMUM CONDUCTOR WIDTH AND SPACING OF 4 MIL & 3.7 MILS.
8. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
9. ALL VIAS SHOULD BE FILLED WITH NON CONDUCTIVE EPOXY AND SURFACE SHOULD BE FLAT
10. VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
11. MANUFACTURER'S IDENTIFICATION, DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
12. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL
13. BOARD DIMENSIONS ARE IN MM.
14. BOW AND TWIST SHALL NOT EXCEED 0.7% OF LONGEST SIDE
15. TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
16. PCB Material must meet or exceed UL94V-0 requirements.
    PCB must bear the UL94V-0 registered material ID number.
17. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL
18. ON BOTTOM LAYER SOLDER MASK SHOULD BE OPENED IN THE INDICATED AREA.
19. 5.9MIL VIA ONLY ON PAD SHOULD BE FILLED WITH CONDUCTIVE COPPER AND SURFACE SHOULD BE FLAT. FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON TOP SIDE.

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 3.7 MIL
MIN. VIA PAD SIZE: 13.77MIL
MINIMUM ANNULAR RING 0.1mm (3.9MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 2 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER REFER STACKUP
THICKNESS: [ ] 64 MIL (1.63mm) +/-10% [X] OTHER 56.57MIL +/-10%
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [X] OTHER REFER NOTE 4

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[X] 8 & 10 MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[X] BOARD IMPEDANCE SHALL BE FOLLOWED AS PER THE IMPEDANCE SPECIFICATION TABLE.
[ ]

TEXAS INSTRUMENTS

PROJECT TITLE: xWR2944EVM
DESIGNED FOR: Public Release
FILE NAME: PROC113D_BRD.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC113	REV: D	SVN REV: Not In VersionControl
LAYER NAME = M1 Board Outline / M2 Board Dimensions / M3 Drill Drawing / M10 Fab Notes / M11 Title Sheet / M12 Stackup	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 1/19/2023 11:58:07 AM	TEXAS INSTRUMENTS	

ENGINEER:	LAYOUT BY:
Adrian Ozer	Mistral
SCALE: 0.66	ALTIUM DESIGNER VERSION: 18.1.9.240