





A

A

- Z21 
- Z22 
- Z23 
- Z24 

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4 High Tg	20.00mil	4.2	
5	GND	Copper	1.40mil		
6	Dielectric2	FR-4 High Tg	17.00mil	4.8	
7	PWR	Copper	1.40mil		
8	Dielectric 3	FR-4 High Tg	20.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

ALL VIAS ARE TENTED EXCEPT THERMAL VIAS  
THIS IS NOT AN IMPEDENCE CONTROLLED BOARD

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.076mm (3MIL) EXTERNAL  
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

☐ FR-408

☒ FR-4 High Tg

☐ OTHER

THICKNESS: ☒ 63 MIL (1.6mm) +/-10% ☐ OTHER

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC\_DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER

☒ MATTE

☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG

☐ IMM. TIN/SILVER OR EQUIV

☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE

☐ N.C. ROUTE

☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

☒ ANSI IPC-A-600F CLASS ->

☐ 1

☒ 2

☐ 3

☒ RoHS

☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE

TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:  
TIDA-00420\_ADC\_BIM

DESIGNED FOR:  
PUBLIC RELEASE

FILE NAME:  
TIDA-00420\_ADC\_BIM-E2.PcbDoc

ENGINEER:  
SREENIVASA KALLIKUPPA

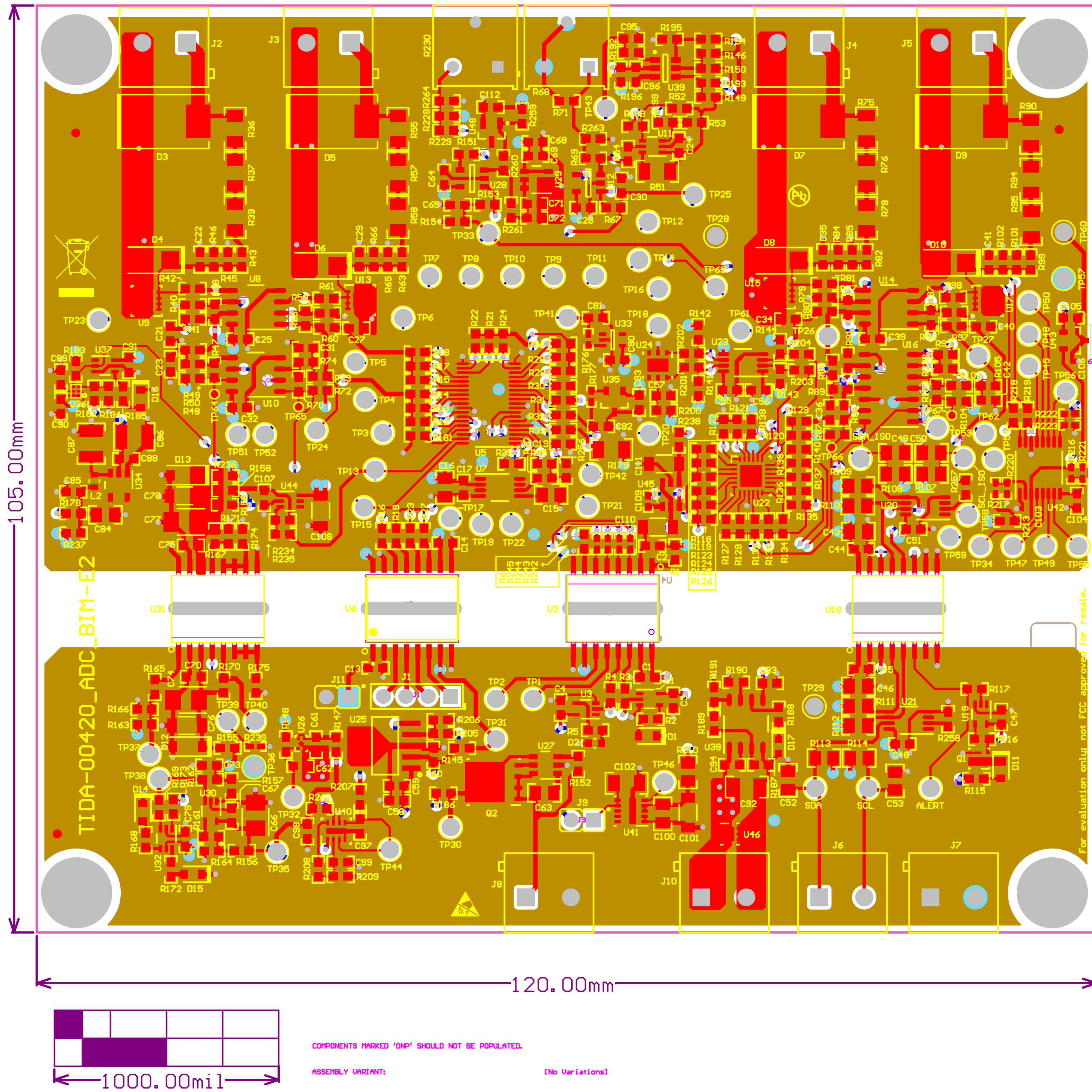
LAYOUT BY:  
Avinash N

SCALE: 1.00

ALTUM DESIGNER VERSION:  
18.1.9.240

B

B



ALL ARTWORK VIEWED FROM TOP SIDE	3	BOARD #:	TIDA-00420_ADC_BIM	REV:	E2	SUN REV:	Not In Version Control
LAYER NAME =	8	DESIGNED FOR:	Public Release	TID #:	00420		
PLOT NAME =	Multi-layer Composite Print	GENERATED:	3/5/2021 1:56:18 PM			TEXAS INSTRUMENTS	

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