ADS9308V8I 24-Bit, 16-Channel, Simultaneous-Sampling, Precision ADC for Voltage and Current Sensing

1 Features

- 16-channel, 24-bit simultaneous sampling ADC
  - 8 current sense and 8 voltage sense inputs
  - Data rate up to 125kSPS on each channel
- Programmable zero-drift current sense amplifier
  - Differential input impedance (Z_{IN}): 0.5MΩ
  - Input offset drift: 0.1µV/°C
  - Gain drift: 5ppm/°C
  - Input range: ±25mV, ±50mV, ±100mV, ±150mV, ±200mV
  - Common mode range: ±18V
- Programmable voltage sense amplifier
  - Input impedance: 1MΩ
  - Input offset drift: 1ppm/°C
  - Gain drift: 0.8ppm/°C
  - Input range: ±50V, ±25V, ±12.5V, ±10V, ±6.25V, ±5V, ±2.5V
  - Supports single-ended and differential inputs
  - Common mode range: ±12.5V
- Power Supply
  - Analog supplies: 5V and 1.8V
  - Digital I/O supply: 1.8V to 3.3V
- Temperature range: –40°C to +125°C

2 Applications

- Battery cell formation and test equipment
- Multichannel current and voltage sensing
- Power telemetry
- Test and measurement

3 Description

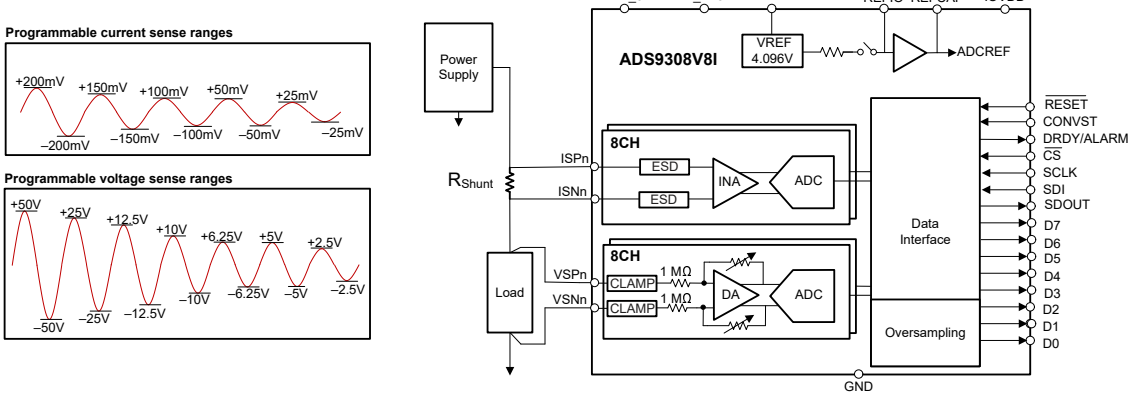
The ADS9308V8I is a 16-channel, 24-bit successive approximation (SAR) analog-to-digital converter (ADC) with integrated analog front end for simultaneous current and voltage sensing. The device integrates eight zero-drift programmable gain amplifiers for current sensing, and eight low-drift programmable gain difference amplifiers for voltage sensing. The ADC inputs can be directly connected to the power supply to measure voltage and current simultaneously. The device delivers a maximum throughput of 125kSPS on each channel. The device also features a low-drift, precision reference with a buffer to drive the ADC.

The ADS9308V8I includes a flexible digital interface, allowing the device to be used with a variety of host controllers. Users can configure the serial interface to read the ADC output on 1-lane, 2-lane, 4-lane, and 8-lane. The device also has flexibility to operate the ADC as 2-CH, 4-CH, 8-CH and 16-CH simultaneous sampling ADC.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS9308V8I	RSK (VQFN, 64)	8.00mm × 8.00mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Device Block Diagram

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4 Pin Configuration and Functions

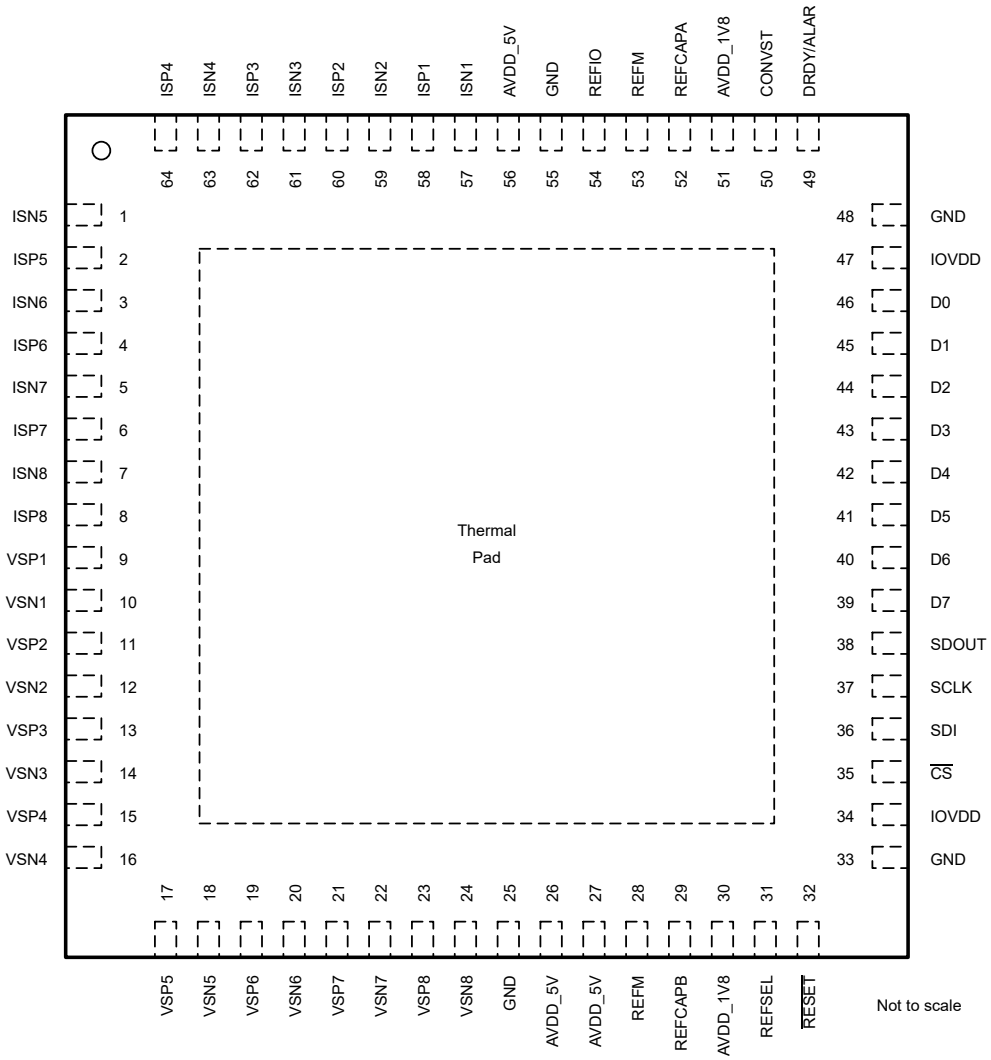

Figure 4-1. RSK Package, 64-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
ISN1	57	AI	Current sense channel 1, negative input.
ISP1	58	AI	Current sense channel 1, positive input.
ISN2	59	AI	Current sense channel 2, negative input.
ISP2	60	AI	Current sense channel 2, positive input.
ISN3	61	AI	Current sense channel 3, negative input.
ISP3	62	AI	Current sense channel 3, positive input.
ISN4	63	AI	Current sense channel 4, negative input.

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Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
ISP4	64	AI	Current sense channel 4, positive input.
ISN5	1	AI	Current sense channel 5, negative input.
ISP5	2	AI	Current sense channel 5, positive input.
ISN6	3	AI	Current sense channel 6, negative input.
ISP6	4	AI	Current sense channel 6, positive input.
ISN7	5	AI	Current sense channel 7, negative input.
ISP7	6	AI	Current sense channel 7, positive input.
ISN8	7	AI	Current sense channel 8, negative input.
ISP8	8	AI	Current sense channel 8, positive input.
VSP1	9	AI	Voltage sense channel 1, positive input.
VSN1	10	AI	Voltage sense channel 1, negative input.
VSP2	11	AI	Voltage sense channel 2, positive input.
VSN2	12	AI	Voltage sense channel 2, negative input.
VSP3	13	AI	Voltage sense channel 3, positive input.
VSN3	14	AI	Voltage sense channel 3, negative input.
VSP4	15	AI	Voltage sense channel 4, positive input.
VSN4	16	AI	Voltage sense channel 4, negative input.
VSP5	17	AI	Voltage sense channel 5, positive input.
VSN5	18	AI	Voltage sense channel 5, negative input.
VSP6	19	AI	Voltage sense channel 6, positive input.
VSN6	20	AI	Voltage sense channel 6, negative input.
VSP7	21	AI	Voltage sense channel 7, positive input.
VSN7	22	AI	Voltage sense channel 7, negative input.
VSP8	23	AI	Voltage sense channel 8, positive input.
VSN8	24	AI	Voltage senses channel 8, negative input.
AVDD_1V8	30, 51	P	1.8V power-supply. Connect 1µF and 0.1µF decoupling capacitors to GND.
AVDD_5V	26, 27, 56	P	5V analog supply. Connect 1µF and 0.1µF decoupling capacitors to GND.
DRDY/ALARM	49	DIO	Data ready or alarm; active high.
CONVST	50	DI	Logic input to control start of conversion.
$\overline{CS}$	35	DI	Chip-select input for the SPI configuration; active low.
D0	46	DO	Serial output data lane 0.
D1	45	DO	Serial output data lane 1.
D2	44	DO	Serial output data lane 2.
D3	43	DO	Serial output data lane 3.
D4	42	DO	Serial output data lane 4.
D5	41	DO	Serial output data lane 5.
D6	40	DO	Serial output data lane 6.
D7	39	DO	Serial output data lane 7.
GND	25, 33, 48, 55	P	Ground.
IOVDD	34, 47	P	Digital I/O supply for the data interface. Connect 1µF and 0.1µF decoupling capacitors to GND.
REFCAPA	52	AO	Reference amplifier output pin. Connect a low ESR 1µF, X7R decoupling capacitor between pin 52 and 53.
REFIO	54	AIO	This pin acts as an internal reference output when REFSEL is high; this pin functions as input pin for the external reference when REFSEL is low; decouple with REFM on pin 53 using a 4.7µF capacitor.
REFCAPB	29	AO	Reference amplifier output pin. Connect a low ESR 1µF, X7R decoupling capacitor between pin 29 and 28.
REFM	28, 53	P	Reference GND pins. Short these pins to GND plane external to the device on the PCB.
REFSEL	31	DI	Logic input to select reference voltage source for the ADC. Connect REFSEL to GND for the external reference. Connect REFSEL to IOVDD for the internal reference.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{\text{RESET}}$	32	DI	Reset input for the device; active low.
SCLK	37	DI	Serial clock input for the data interface.
SDI	36	DI	Serial data input for the data interface.
SDOUT	38	DO	Serial data output for the user registers or single lane data output.
Thermal Pad	-	P	Exposed thermal pad. Connect to GND.

(1) AI = analog input; AO = analog output; AIO = analog input/output; DI = digital input; DO = digital output; DIO = digital input/output; P = power supply; and NC = no connect.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD_5V to GND	–0.3	6	V
AVDD_1V8 to GND	–0.3	2.1	V
IOVDD to GND	–0.3	3.6	V
VSPn and VSNn to GND	–50	50	V
VSPn – VSNm, between any adjacent voltage sense pin	–50	50	V
ISPx and ISNx to GND	–20	20	V
REFIO to GND	GND – 0.3	VREF (4.096) + 0.3	V
REFM to GND	GND – 0.3	GND + 0.3	V
Digital inputs to GND	GND – 0.3	3.6	V
Input current to any pin except supply pins(2)	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pin current must be limited to 10mA or less.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	Voltage sense input pins (VSPn and VSNn)	±8000	V
			Current sense input pins (ISPn and ISNn)	±8000	V
			All other pins	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD_5V	Analog power supply	AVDD_5V to GND	4.75	5	5.25	V
AVDD_1V8	Power supply	AVDD_1V8 to GND	1.71	1.8	1.89	V
IOVDD	Digital interface power supply	IOVDD to GND	1.71		3.6	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	External reference	4.092	4.096	4.100	V
ANALOG INPUTS						
ISPn	Current sense positive input		–18		18	V
ISNn	Current sense negative input		–18		18	V
VSPn	Voltage sense positive input		–50		50	V
VSNn	Voltage sense negative input	Differential input, CM_RANGE_AINn = 0	–50		50	V
VSNn	Voltage sense negative input	Single-ended input, CM_RANGE_AINn = 5,6	–0.5		0.5	V
VSPn – VSNm	Voltage between adjacent pins		–50		50	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		ADS93x8V8I RSK (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

at AVDD = 4.75V to 5.25V, AVDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal VREF = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE						
	Resolution, no missing codes		24			Bits
	Output data rate				125	kSPS
	Input bias current	ISPn–ISNn = 0mV, V_{CM} = –18V to 18V		1		nA
Z_{IN}	Differential input impedance	All gains		0.5		MΩ
IS_{FSR}	Full-scale current sense input range (ISPn – ISNn)		–25		25	mV
			–50		50	mV
			–100		100	mV
			–150		150	mV
			–200		200	mV
IS_{CM}	Current sense common mode input range		–18		18	V
	Current sense analog input LPF bandwidth (–3dB)	All input ranges		400		kHz
	Offset drift(2)	All gains		±0.1		µV/°C
	Gain drift(2) (3)	All gains		±5		ppm/°C
	INL	All gains		±15		ppm
	SNR, ODR = 62.5kSPS, OSR =16	Range = ±200mV		90.4		dB
		Range = ±150mV		88.9		dB
		Range = ±100mV		87.1		dB
		Range = ±50mV		83		dB
		Range = ±25mV		77.4		dB
THD	Total harmonic distortion	All ranges		–104		dB
	CMRR	At DC		140		dB
VOLTAGE SENSE						
	Resolution, no missing codes		24			Bits
	Output data rate				125	kSPS
R_{IN}	Input impedance	All input ranges		1		MΩ
	Input impedance thermal drift	All input ranges		10		ppm/°C
VS_{FSR}	Full-scale voltage sense input range (VSPn - VSNn)	INPUT_RANGE_VSn[2:0] = 010b	–2.5		2.5	V
		INPUT_RANGE_VSn[2:0] = 000b	–5		5	V
		INPUT_RANGE_VSn[2:0] = 011b	–6.25		6.25	V
		INPUT_RANGE_VSn[2:0] = 100b	–10		10	V
		INPUT_RANGE_VSn[2:0] = 101b	–12.5		12.5	V
		INPUT_RANGE_VSn[2:0] = 001b	–25		25	V
		INPUT_RANGE_VSn[2:0] = 110b, single-ended	–50		50	V
VS_{CM}	Voltage sense common mode input range	Differential input (CM_RANGE_AINn = 0)	–12.5		12.5	V

at AVDD = 4.75V to 5.25V, AVDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal VREF = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BW_{(-3dB)}$	Analog input LPF -3dB bandwidth	Low-bandwidth filter, all input ranges		25.5		kHz
		Wide-bandwidth filter, V_{FSR} = ±2.5V		280		kHz
		Wide-bandwidth filter, V_{FSR} = ±5V		325		kHz
		Wide-bandwidth filter, V_{FSR} = ±6.25V		300		kHz
		Wide-bandwidth filter, V_{FSR} = ±10V, ±12.5V		350		kHz
		Wide-bandwidth filter, V_{FSR} = ±25V, ±50V		400		kHz
INL	Integral nonlinearity	All ranges		±15		ppm
	Offset error	All ranges		±60		ppm
	Offset error thermal drift	All ranges		1.2		ppm/°C
	Gain error(2) (3)	All ranges		±0.012		%
	Gain error thermal drift(2) (3)	All ranges		1		ppm/°C
SNR_{LOW_BW}	Signal-to-noise ratio in low-bandwidth mode (–0.1dBFS input at 1kHz, ODR = 62.5kSPS, OSR =16)	Range = ±2.5V		92		dBFS
		Range = ±5V, ±6.25V		95.5		dBFS
		Range = ±10V, ±12.5V		97.5		dBFS
		Range = ±25V		99		dBFS
		Range = ±50V		100		dBFS
SNR_{HI_BW}	Signal-to-noise ratio in high-bandwidth mode (–0.1dBFS input at 1kHz, ODR = 62.5kSPS, OSR =16)	Range = ±2.5V		89.6		dBFS
		Range = ±5V		92.6		dBFS
		Range = ±6.25V		94.2		dBFS
		Range = ±10V		95.3		dBFS
		Range = ±12.5V		96.5		dBFS
		Range = ±25V		98		dBFS
		Range = ±50V		99		dBFS
THD	Total harmonic distortion	All ranges		–103		dB
	CMRR	At dc, CM error correction enabled, measured with ΔV_{CM} = 25V		100		dB
INTERNAL REFERENCE						
VREF(1)	Voltage on REFIO pin (configured as output)	1µF capacitor on REFIO pin, T_A = 25°C		4.096		V
	Reference temperature drift	1µF capacitor on REFIO pin, T_A = 25°C		15		ppm/°C
	Reference buffer output impedance			1		kΩ
	Reference turn-on time	1µF capacitor on REFCAP pin			30	ms
EXTERNAL REFERENCE INPUT						
REF_{LKG}	Reference input leakage current				±10	nA
DIGITAL INPUTS						
V_{IL}	Input low logic level threshold				0.3 IOVDD	V
V_{IH}	Input high logic level threshold		0.7 IOVDD			V
DIGITAL OUTPUTS						
V_{OL}	Output low logic level	I_{OL} = 200µA sink	0		0.4	V
V_{OH}	Output high logic level	I_{OH} = 200µA source	IOVDD–0.4		IOVDD	V
POWER SUPPLY						
	Total power dissipation	Maximum throughput		230		mW
I_{AVDD_5V}	Supply current from AVDD_5V	Maximum throughput, internal reference		30		mA
I_{AVDD_1V8}	Supply current from AVDD_1V8	Maximum throughput, internal reference		32		mA

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at AVDD = 4.75V to 5.25V, AVDD_1V8 = 1.75V to 1.85V, IOVDD = 1.75V to 3.3V, internal VREF = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IOVDD}	Supply current from IOVDD	Maximum throughput		6		mA

(1) Does not include the variation in voltage resulting from solder shift effects.
(2) The specifications include full operating temperature range after offset error calibration at T_A = 25°C.
(3) These specifications include full temperature range variation but not the error contribution from internal reference.

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5.6 Timing Requirements

at AVDD_5V = 4.75V to 5.25V, AVDD_1V8 = 1.7V to 1.9V, IOVDD = 1.7V to 3.6V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

		MIN	MAX	UNIT
CONVST				
f_{CONVST}	ADC sampling frequency, free running continuous clock	100	1000	kHz
t_{CONVST}	Sampling time interval	1 / f_{CONVST}		µs
t_{PH_CV}	CONVST pulse high time	50		ns
t_{PL_CV}	CONVST pulse low time	50		ns
SERIAL INTERFACE				
f_{SCLK}	Maximum SCLK frequency		80	MHz
t_{SCLK}	Minimum SCLK time period	20		ns
t_{PH_SCLK}	SCLK high time	0.45	0.55	t_{SCLK}
t_{PL_SCLK}	SCLK low time	0.45	0.55	t_{SCLK}
t_{hi_CS}	Pulse duration: $\overline{CS}$ high	5		ns
t_{su_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK capture edge	12		ns
t_{ht_CSCK}	Hold time: last SCLK falling edge to $\overline{CS}$ rising time	10		ns
t_{su_CKDI}	Setup time: SDI data valid to the corresponding SCLK rising edge	3		ns
t_{ht_CKDI}	Hold time: SCLK rising edge to corresponding data valid on SDI	1		ns
t_{su_DRDYCS}	Setup time: DRDY rising edge to CS falling edge	0		ns
t_{ht_DRDYCS}	Hold time: DRDY rising edge to CS rising edge	0		ns

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5.7 Switching Characteristics

at AVDD_5V = 4.75V to 5.25V, AVDD_1V8 = 1.7V to 1.9V, IOVDD = 1.7V to 3.6V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
RESET					
t_{PU}	Power-up time for device			100	ms
SERIAL INTERFACE					
t_{d_CSDO}	Delay time: CS falling edge to data valid on SDOUT and D[7:0]			16	ns
t_{dz_CSDO}	Delay time: CS rising edge to SDOUT and D[7:0] going Hi-Z			7.5	ns
t_{vt_CKDO}	Valid time: SCLK launch edge to previous data valid on SDOUT and D[7:0]		7.6		ns
t_{d_CKDO}	Delay time: SCLK launch edge to corresponding data valid on SDOUT and D[7:0]			17	ns
DRDY AND ALARM					
t_{CYC}	ADC cycle time period	At maximum f_{CONVST}	10		µs
t_{CONV}	Conversion time	OSR = 8, and at maximum f_{CONVST}	8	8.25	µs
		OSR >= 8	(N-1) × t_{CONVST} + 1	(N-1) × t_{CONVST} + 1.25	µs
$t_{d\_CVDRDY\_hi}$	Time delay between CONVST falling edge to DRDY rising edge			t_{CONV}	ns
$t_{d\_CVDRDY\_lo}$	Time delay between CONVST falling edge to DRDY falling edge			10	ns
t_{d_ALARM}	Time delay between CONVST to new ALARM valid			t_{CONV}	µs

5.8 Timing Diagrams

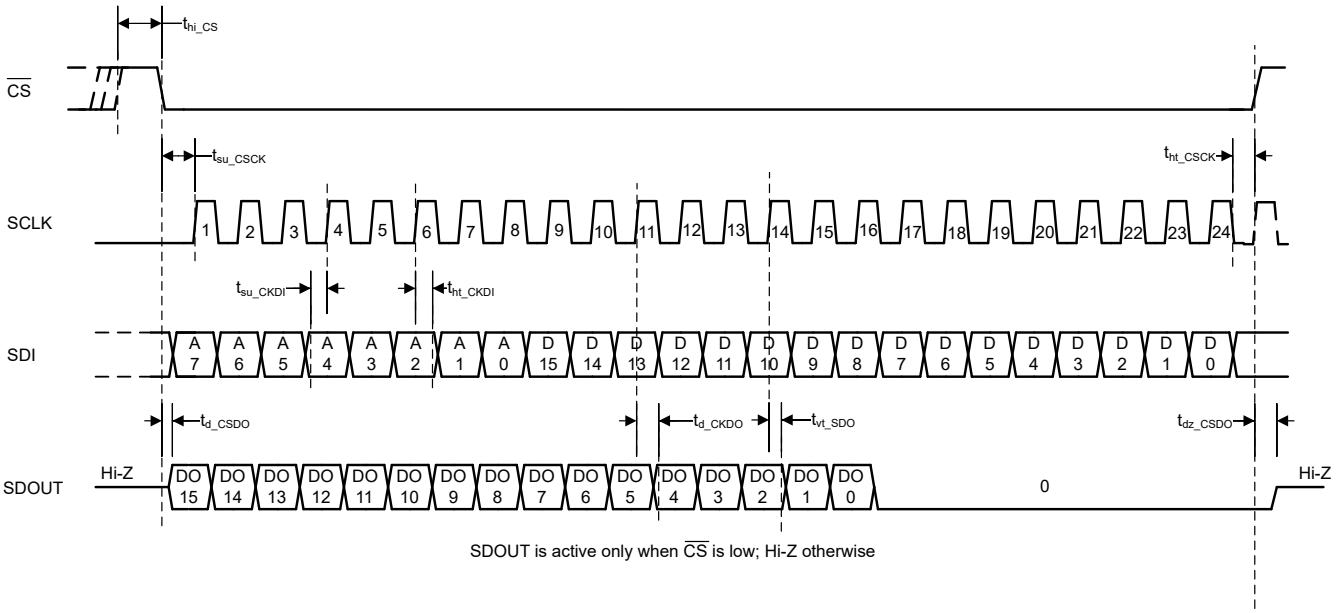

Figure 5-1. Timing for Register Read and Write Operations

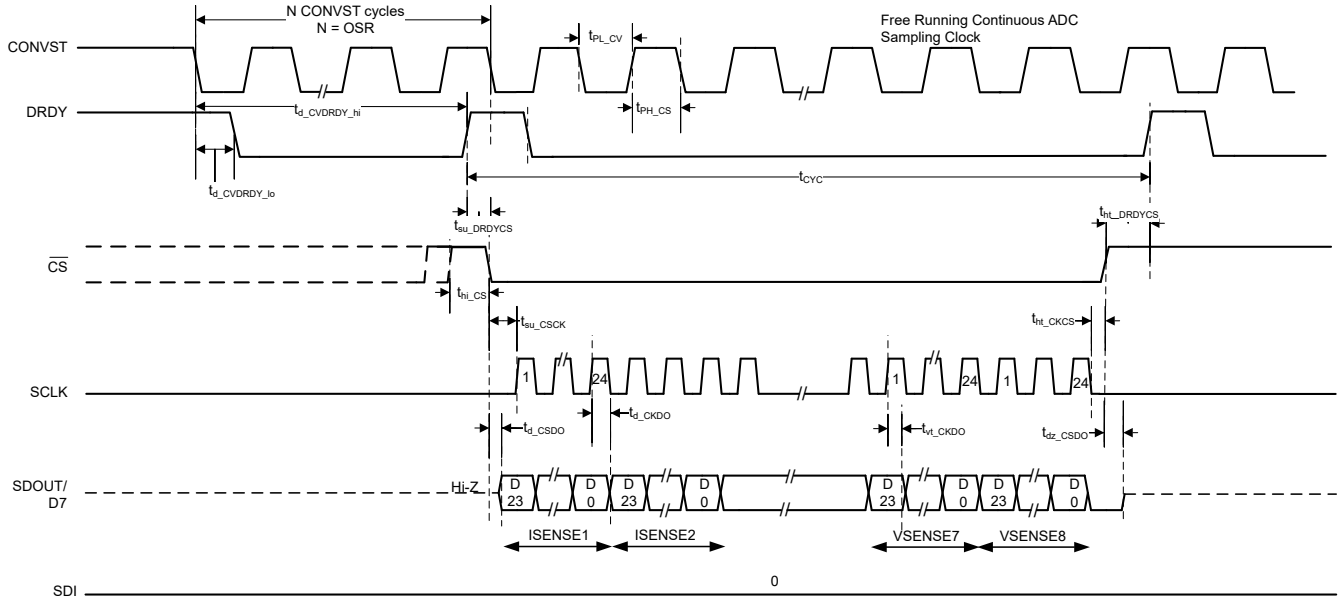

Figure 5-2. ADC Conversion Data Read Timing: 1-Data Lane

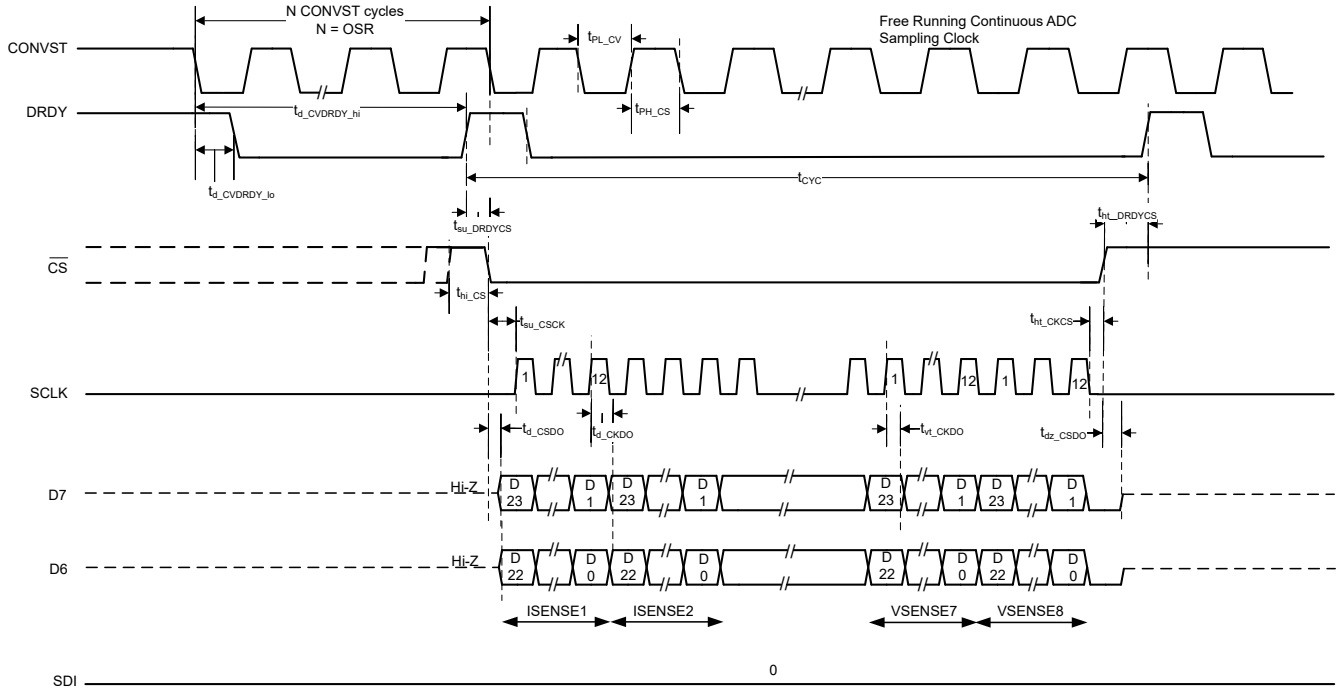

Figure 5-3. ADC Conversion Data Read Timing: 2-Data Lane

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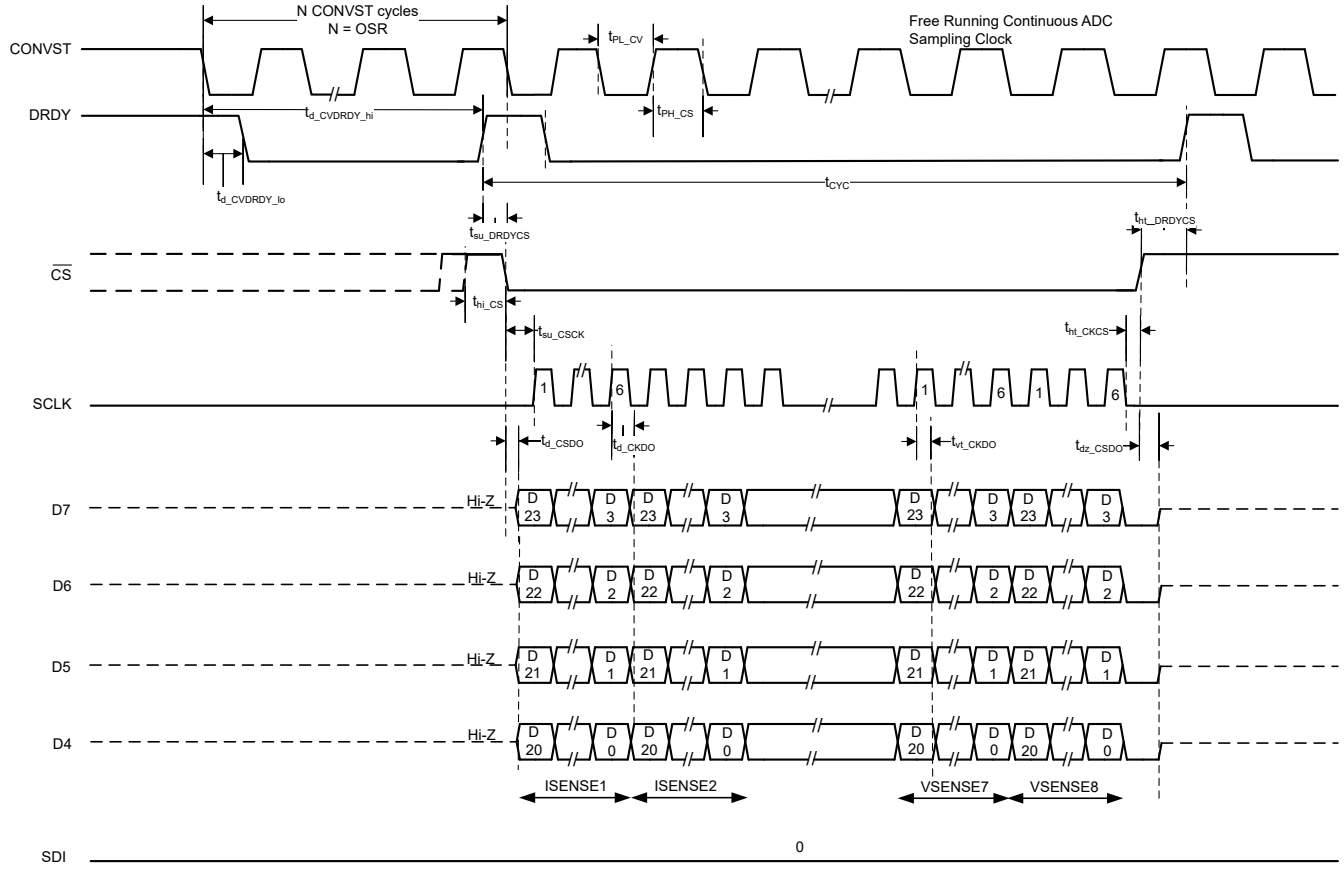

Figure 5-4. ADC Conversion Data Read Timing: 4-Data Lane

ADVANCE INFORMATION

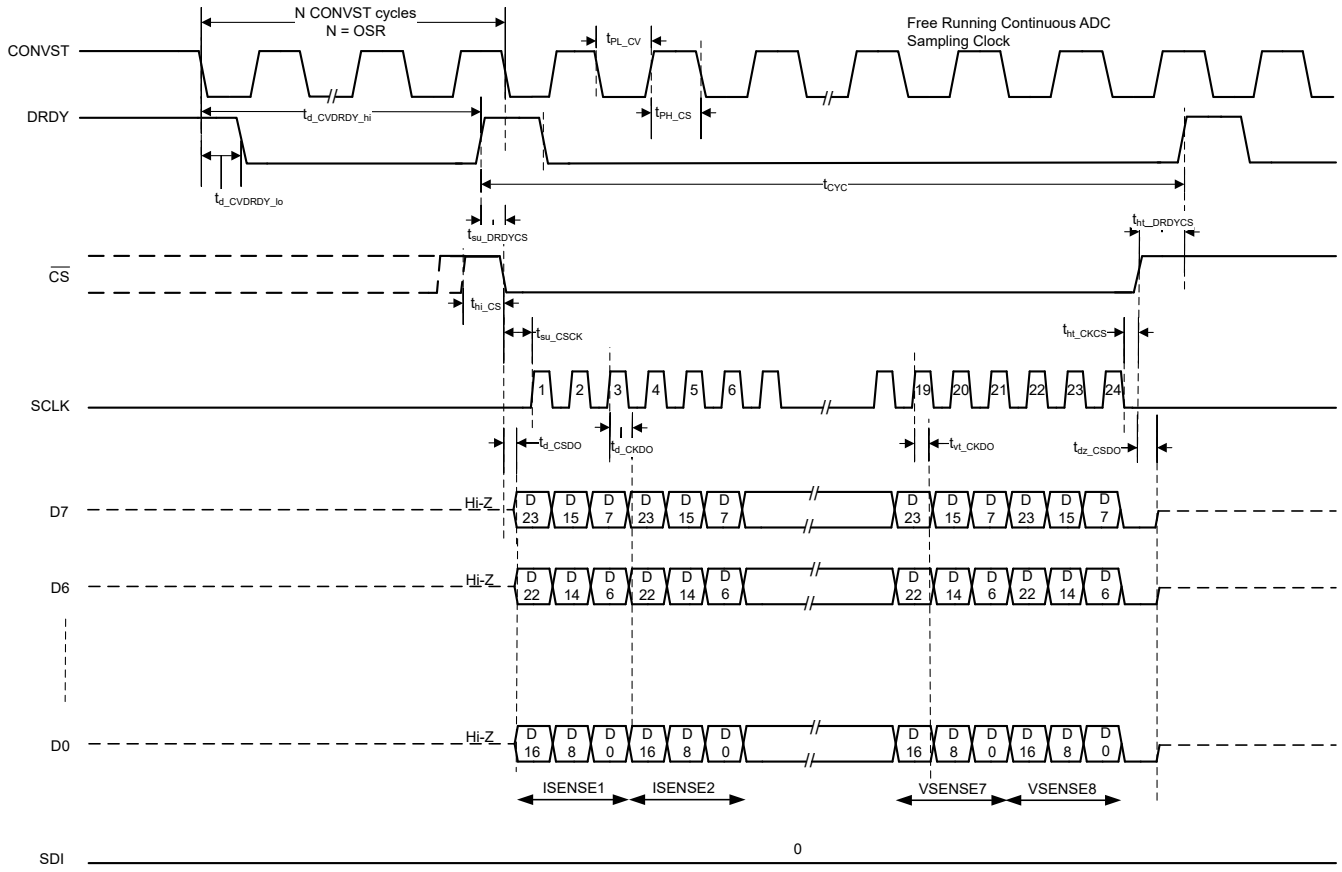

Figure 5-5. ADC Conversion Data Read Timing: 8-Data Lane

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6 Detailed Description

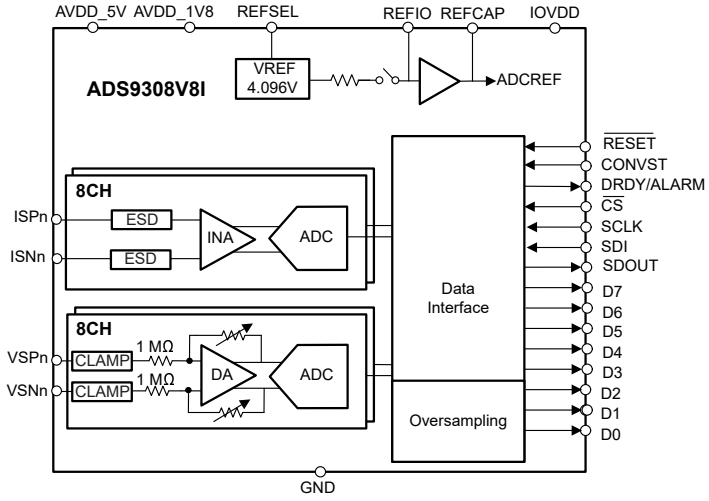
6.1 Overview

The ADS9308V8I is a 16-channel, 24-bit successive approximation (SAR) analog-to-digital converter (ADC) with integrated analog front end for simultaneous current and voltage sensing. The device is designed for high-accuracy current and voltage monitoring applications, enabling direct connection to power supply rails without the need for external signal conditioning components. The current sense path integrates eight zero-drift programmable gain instrumentation amplifiers (INA) with ESD protection, optimized for shunt-based current sensing. These amplifiers provide high common-mode rejection and zero-drift performance, enabling accurate low-side or high-side current measurement. The voltage sense path integrates eight programmable difference amplifiers with ESD protection, capable of sensing voltages up to ±50V.

The ADC analog inputs can be directly connected to the power supply to measure voltage and current simultaneously. The input channels are designed to sustain the maximum rated voltage even in the absence of AVDD and IOVDD supplies, eliminating the need for power sequencing when monitoring multiple power rails. The device includes an integrated 4.096V precision voltage reference (VREF), selectable through the REFSEL pin. The reference is internally buffered and routed through the REFIO and REFCAP pins to generate a stable reference voltage for the ADCs.

The ADS9308V8I supports a maximum throughput of 125kSPS on each channel and includes a programmable digital filter that can be used to reduce input signal noise, improve overall noise performance, and lower the total conversion throughput. A flexible digital interface allows the device to be used with a variety of host controllers, configured through SPI communication. Conversion results are output through SCLK, SDOUT, and CS signals, as well as a parallel data bus (D0–D7), with support for 1-lane, 2-lane, 4-lane, and 8-lane serial interface configurations. In applications where fewer channels are required, the device can be configured to operate as a 2-channel, 4-channel, and 8-channel simultaneous sampling mode.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Current Sense Programmable Gain Amplifier

The ADS9308V8I features eight programmable gain instrumentation amplifiers. Table 6-1 lists the supported input ranges. The analog input range can be configured independently for each channel with the INPUT_RANGE_ISn[2:0] register fields in PGA_CONFIG_ISn registers.

Table 6-1. Current Sense PGA Input Ranges

RANGE	INPUT_RANGE_ISn
±25mV	0
±50mV	1
±100mV	2
±150mV	3
±200mV	4

6.3.2 Voltage Sense Programmable Gain Amplifier (VPGA)

The ADS9308V8I features voltage sense programmable amplifiers. The PGA supports both single-ended and differential inputs with a bipolar signal swing. In differential-input mode, the voltage sense PGA can take maximum common mode voltage of ±12.5V. In signal-ended mode, the maximum common mode voltage supported is ±(RANGE / 2). Table 6-2 lists the supported analog input ranges. Configure the analog input range independently for each channel with the INPUT_RANGE_VSn[2:0] register fields in PGA_CONFIG_AINx registers.

Table 6-2. Analog Input Ranges

INPUT TYPE	RANGE	INPUT_RANGE_VSn	CM_RANGE_VSn
Single-ended	±50V	6	5
Single-ended	±25V	1	5
Single-ended	±12.5V	5	5
Single-ended	±10V	4	5
Single-ended	±6.25V	3	5
Single-ended	±5V	0	5
Single-ended	±2.5V	2	5
Differential	±25V	1	0
Differential	±12.5V	5	0
Differential	±10V	4	0
Differential	±6.25V	3	0
Differential	±5V	0	0
Differential	±2.5V	2	0
Single-ended open wire safe	±12.5V	5	6
Single-ended open wire safe	±10V	4	6
Single-ended open wire safe	±6.25V	3	6
Single-ended open wire safe	±5V	0	6
Single-ended open wire safe	±2.5V	2	6

Each voltage sense channel features an anti-aliasing, low-pass filter (LPF) at the output of the PGA. Table 6-3 lists the various programmable LPF options available in the ADS9308V8I, corresponding to the analog input range. The following illustrates the frequency responses for low-bandwidth and wide-bandwidth LPF configurations. Select the analog input bandwidth for the each analog input channels with the PGA_SEL bit field in the PGA_BW_SEL_AINn registers. By default, the all PGA are in low-bandwidth mode.

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Table 6-3. Voltage Sense, Low-Pass Filter Corner Frequency

LPF	PGA_BW_SEL_AINn	ANALOG INPUT RANGE	CORNER FREQUENCY (–3dB)
Low-bandwidth	0	All input ranges	25.5kHz
Wide-bandwidth	1	±2.5V	280kHz
		±5V	325kHz
		±6.25V	300kHz
		±10V, ±12.5V	350kHz
		±25V, ±50V	400kHz

6.3.3 ADC Transfer Function

The ADS9308V8I outputs 24 bits of conversion data in either straight-binary or binary two's complement formats. By default, ADC output is in binary two's complement format. Set EN_OFS_BINARY to 1'b for straight-binary format. The format for the output codes is the same across all analog channels. Figure 6-1 shows the transfer characteristics for the ADS9308V8I.

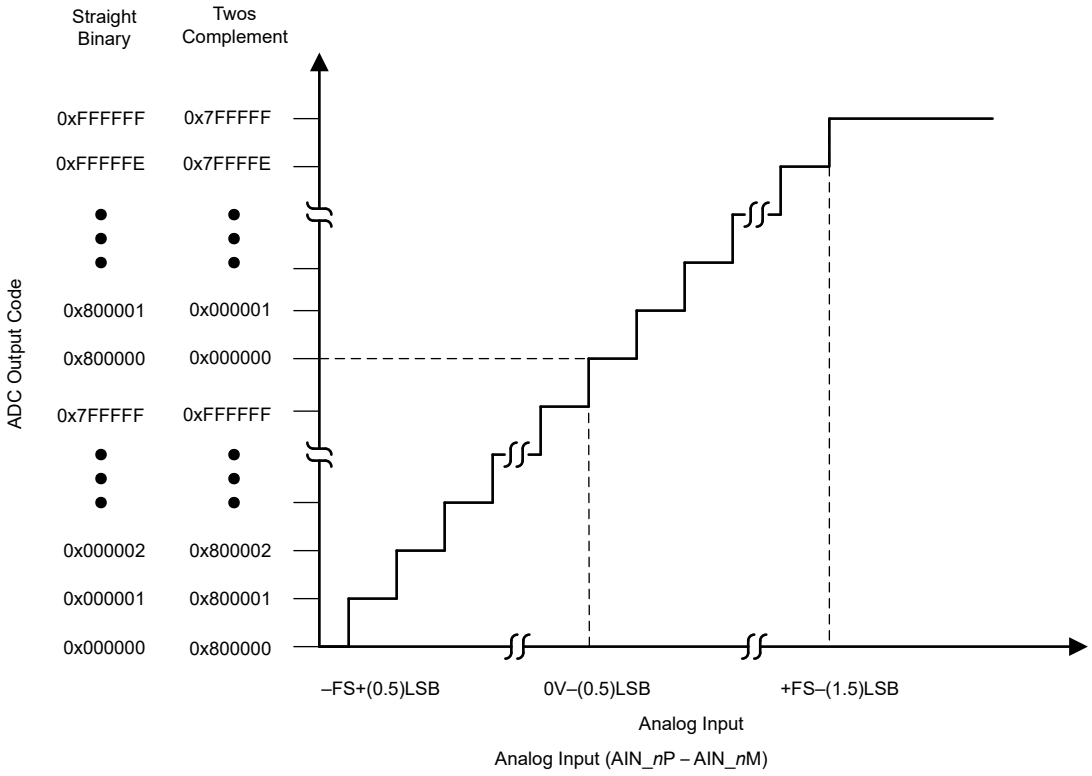

Figure 6-1. ADC Transfer Characteristics

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6.3.4 Reference

The ADS93x8V8I has a precision, low-drift voltage reference internal to the device. For best performance, filter the internal reference noise by connecting a 4.7µF ceramic bypass capacitor to the REFIO pin, and connect 1µF ceramic capacitors directly between REFCAPA and REFM pins, and between the REFCAPB and REFM pins, shows in the Figure 6-2 and Figure 6-3. On power up, as described in Table 6-4, the reference source is selected by the REFSEL pin or by the values in the REFSEL_CTRL and EXT_REF_EN fields in address 0x10 in the ADS93x8V8I Common register bank.

Table 6-4. ADC Voltage Reference Source Selection

REFSEL INPUT	REFSEL_CTRL_DIS	EXT_REF_EN	ADC REFERENCE SOURCE
Low	0b	X	ADC reference is selected using REFSEL pin. External reference on REFIO pin.
High	0b	X	ADC reference is selected using REFSEL pin. Internal reference is active.
X	1b	0b	ADC reference is selected using EXT_REF_EN bit field in 0x10 register. Internal reference is active.
X	1b	1b	ADC reference is selected using EXT_REF_EN bit field in 0x10 register. External reference is selected. Force external reference on REFIO pin.

Note

1. If the external reference is not applied in the external reference operation, the device goes into power-down mode.

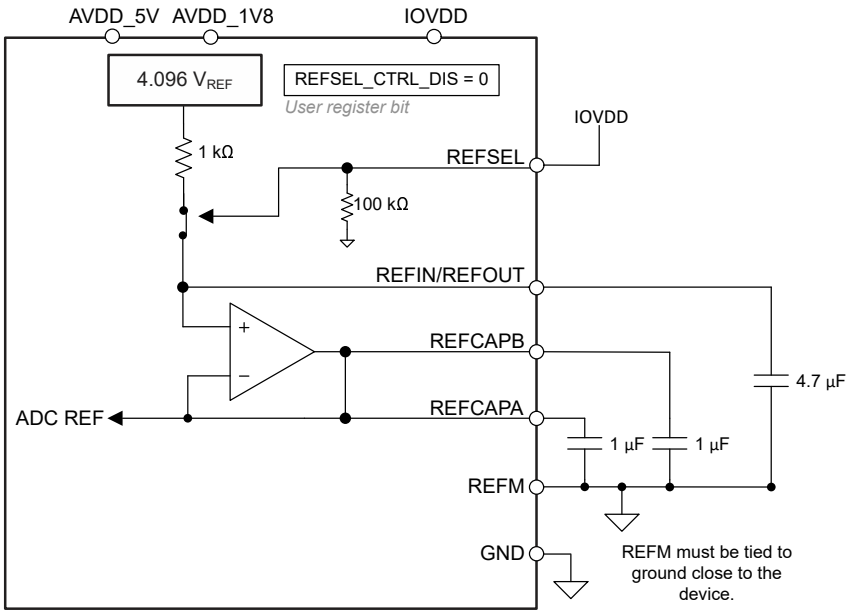

Figure 6-2. Internal Reference Voltage

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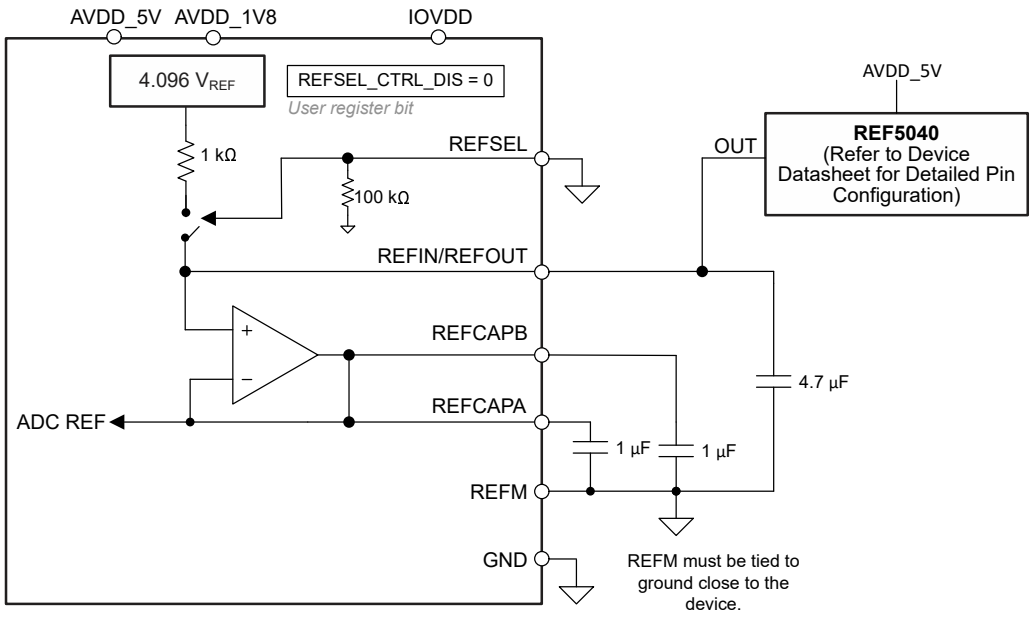

Figure 6-3. External Reference Voltage

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6.3.5 Digital Averaging Filter

The ADS9308V8I features a block averaging digital filter that can be used in slower throughput applications requiring lower noise and higher dynamic range. The overall throughput of the ADC decreases proportionally with increase in the oversampling ratio of the block average filter. Initialize the GEN_CFG5 register field before using the on-chip digital filters of the ADS9308V8I. Write 0b to 1b on the DIGITAL_FILT_SYSREF bit field in the DIGITAL_FILTER register. Verify at least one t_{CONVST} delay time, and then write DIGITAL_FILT_SYSREF bit to 0b, shown in Figure 6-4.

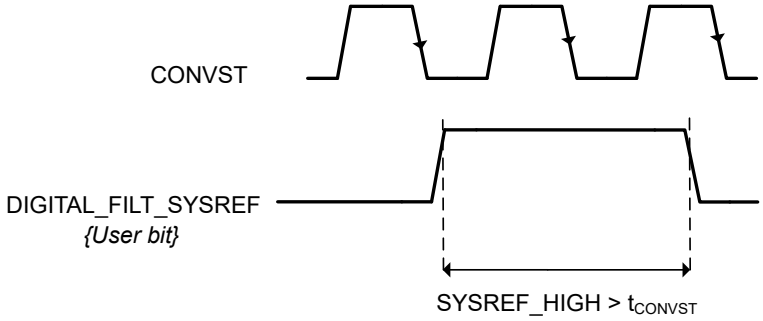

Figure 6-4. Digital Filter SYSREF and CONVST

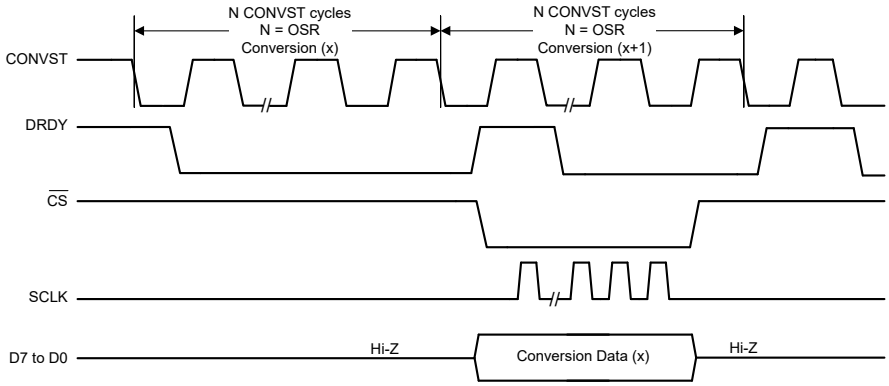

Figure 6-5. ADC Output During Oversampling

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6.3.6 Data Interface

The ADS9308V8I supports 1-lane, 2-lane, 4-lane, and 8-lane mode data read serial interface. Select the data interface as described in Table 6-5. The ADC supports 16-bit and 24-bit ADC data length. The ADC data length is configured using DOUT_LENGTH[1:0] field in the GEN_CFG3 register (0x0A). The 24-bit ADC conversion result is output MSB first in a 24-bit data packet and the last eight bits are zeroes when oversampling is disabled.

Use the registers in Table 6-5 to configure the data interface.

Table 6-5. Register Configurations For Data Interface Modes

INTERFACE MODE	FIGURE	DOUT_LANE_SEL[1:0] (ADDRESS = 0x0A)	ADC_DATA_SDOUT_EN (ADDRESS = 0x0A)
8-lane, D[7:0]	Figure 5-5	0	0
4-lane, D[7:4]	Figure 5-4	1	0
2-lane, D[7:6]	Figure 5-3	2	0
1-lane, D7	Figure 5-2	3	0
1-lane, SDOUT	Figure 5-2	3	1

6.3.6.1 ADC Channel Modes

ADS93x8V8I contains a digital feature to select the number of ADC channels on the data interface. Table 6-6 shows the possible combinations supported in the device. In all modes, the lowest channel number gets transmitted first. Figure 6-7 shows an 8-channel ADC data read mode when ADC_CH_SEL = 0xxb.

Table 6-6. ADC Channel Modes

ADC_NUM_SEL	ADC_CH_SEL	ADC CHANNELS REPORTED	ADC OUTPUT
00b (Default)	xxxb	16 (Default)	IS1, IS2, IS3, IS4, IS5, IS6, IS7, IS8, VS1, VS2, VS3, VS4, VS5 VS6, VS7, VS8
01b	0xxb	8	IS1, IS2, IS3, IS4, VS5, VS6, VS7, VS8
01b	1xxb	8	IS5, IS6, IS7, IS8, VS1, VS2, VS3, VS4
10b	00xb	4	IS1, IS2, VS7, VS8
10b	01xb	4	IS3, IS4, VS5, VS6
10b	10xb	4	IS5, IS6, VS3, VS4
10b	11xb	4	IS7, IS8, VS1, VS2
11b	000b	2	IS1, VS8
11b	001b	2	IS2, VS7
11b	010b	2	IS3, VS6
11b	011b	2	IS4, VS5
11b	100b	2	IS5, VS4
11b	101b	2	IS6, VS3
11b	110b	2	IS7, VS2
11b	111b	2	IS8, VS1

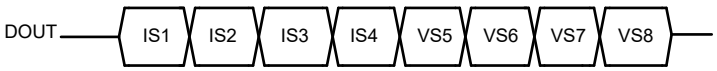

Figure 6-6. 8 Channel ADC Data Read, ADC_NUM_SEL =01b, ADC_CH_SEL = 0xxb

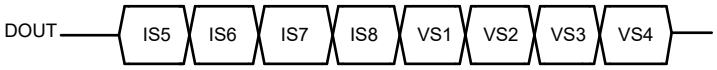

Figure 6-7. 8 Channel ADC Data Read, ADC_NUM_SEL =01b, ADC_CH_SEL = 1xxb

6.4 Device Functional Modes

6.4.1 Reset

Reset the ADS9308V8I with a logic 0 on the $\overline{\text{RESET}}$ pin or write 1b to the SW_RST bit field of address 0x01 in the ADS93x8V8I Common register bank. The device registers are initialized to the default values after reset and the device is initialized with a sequence of register write operations.

The $\overline{\text{RESET}}$ pin is an active-low digital input. A dedicated reset pin allows the device to be reset at any time in an asynchronous manner. All digital circuitry in the device is reset when the $\overline{\text{RESET}}$ pin is set to logic low and this condition remains active until the pin returns high.

6.4.2 Normal Operation

After the ADS9308V8I is powered-up, the ADS9308V8I converts analog input voltages to digital output voltages at the falling edge of CONVST signal. A minimum delay time, t_{PU}, is needed after device reset (see the Section 5.7).

6.4.3 Standby Mode

The device supports a low-power standby mode in which only part of the circuit is powered down. The analog front-end, signal-conditioning circuit for each channel and the internal reference is powered down in this mode. To put the device in the low-power standby mode, set the DEVICE_PDN bit field of the PDN_CTL register to 1b.

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6.5 Programming

6.5.1 Register Write Operation

The ADS9308V8I 16-bit registers are grouped in 3 register banks, ADS93x8V8I Common, IS1 - IS8 Channel, and VS1 - VS8 Channel, and are addressable with an 8-bit register address. The ADS93x8V8I Common register bank is selected for read or write operation by writing 0x0001 to BANK_SEL register, address 0x02. The PAGE_SEL register, address 0x2, is unique among all register banks, and always accessible irrespective of PAGE_SEL bits. A 24-bit serial communication frame is required to write data to configuration registers. The 24-bit register read frame consists of an 8-bit register address and new 16-bit register value. The data on SDI is latched on the rising edge of SCLK. The write command is decoded on the $\overline{CS}$ rising edge and the specified register is updated with the 16-bit data specified in the register write operation. The 24-bit SPI frame for a register write is shown in Figure 6-8, and the steps required to write a register are described in Table 6-7.

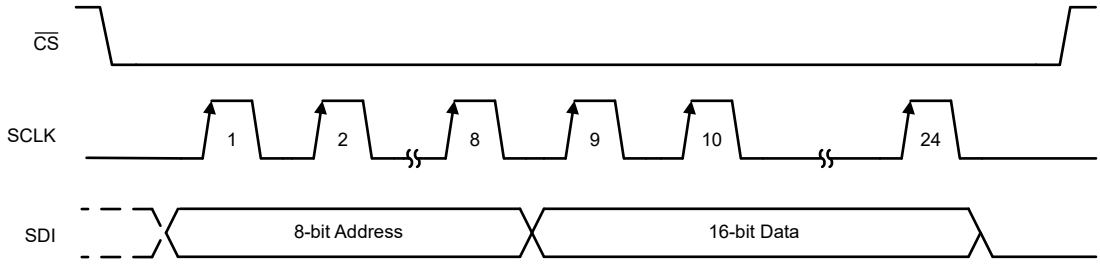

Figure 6-8. Register Write Frame

Table 6-7. Register Write Sequence

FRAME NUMBER	SDI[23:0]		DESCRIPTION
	SDI[23:16] = REG_ADDR	SDI[15:0] = REG_ADDR DATA	
1	0x02	0x0001	Selects register bank 0. For register bank 1 and 2, write 0x02 and 0x04 respectively.
2	REG_ADDR	REG_ADDR DATA	Writes user data to the desired address. Repeat this step for the required number of register writes.

6.5.2 Register Read Operation

The register banks for register read operation is selected using BANK_SEL register, address 0x02. To read registers in ADS93x8V8I Common register bank, write 0x0001, to the BANK_SEL register. Similarly, write 0x0002 and 0x0004 to BANK_SEL register, to read registers in IS1 - IS8 Channel and VS1 - VS8 Channel banks respectively. As illustrated in Figure 6-9, 24-bit SPI frames are required to read registers. Figure 6-9 describes the sequence required to read N number of registers in a register bank, and the steps required are described in Table 6-8.

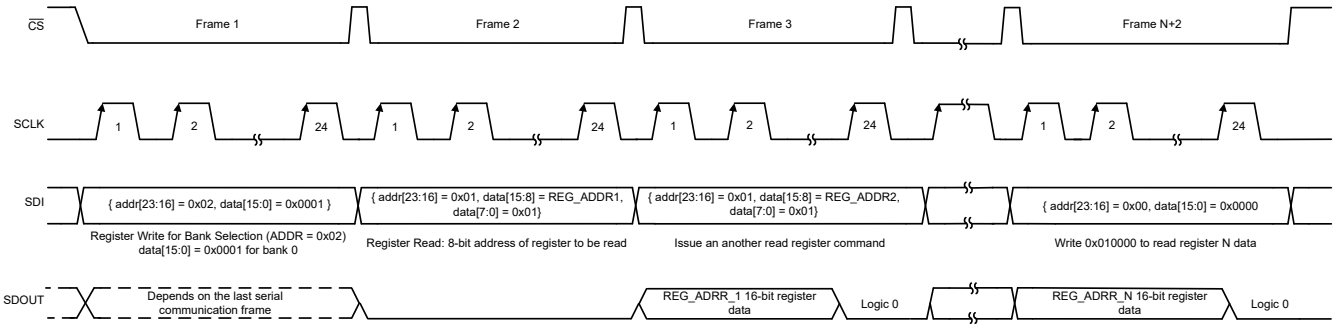

Figure 6-9. Register Read

Table 6-8. Register Read Sequence

FRAME NUMBER	24-bit SDI frame		SDOUT[23:0]	DESCRIPTION
	SDI[23:16]	SDI [15:0]		
1	0x02	0x0001 for register bank 0, 0x0002 for register bank 1, 0x0004 for register bank 2	X	Selects the register bank.
2	0x01	SDIN[15:8] = REG_ADDR1, SDIN[7:0] = 0x01	0x000000	Register read operation for register address REG_ADDR1. The register data, REG_ADDR1, is received in the next serial communication frame.
3	0x01	SDIN[15:8] = REG_ADDR1, SDIN[7:0] = 0x01	SDOUT[23:8] = REG_ADDR1 DATA, SDOUT[7:0]= 0x00	Register read operation for register address REG_ADDR2. The register data, REG_ADDR1, is received in this frame. The register data, REG_ADDR2, is received in the next serial communication frame.
N+2	0x00	0x0000	SDOUT[23:8]= REG_ADDRN DATA, SDOUT[7:0]= 0x00	Write 0x000000 to the SDIN to read register value, address REG_ADDR, selected in the previous serial communication frame.

6.5.3 Initialization Sequence

As shown in Section 6.5.3, initialize the ADS93x8V8I with a sequence of register writes after device power up or reset. Step 2 to Step 9 initializations are required for pre-production sample units.

Table 6-9. ADS93x8V8I Initialization Example

STEP NUMBER	REGISTER		DESCRIPTION
	SDIN[23:16] = REG_ADDR	SDIN[15:0] = REG_ADDR DATA	
1	0x01	0x0002	Software reset
	Wait 1ms		
2	0x02	0x0001	Selects ADS9308V8I common register bank
3	0x14	0x0040	Minimum OSR supported is 8. User can program OSR multiple of 8, i.e. 16, 32, 64 and 128.
4	0x14	0x0041	Set SYSREF to 1b
	Wait 10µs		
5	0x14	0x0040	Set SYSREF to 0b
6	0x02	0x0002	Selects ADS9308V8I INA register bank
7	0x3A	0x0400	Configures the INA
8	0x02	0x0001	Selects ADS9308V8I common register bank
9	0x11	0x1000	Configures the INA. Set this to 0x1000 for maximum ODR of 125kSPS. For ODR less than equal to 62.5kSPS, program this field to 0x4000.

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Table 6-9. ADS93x8V8I Initialization Example (continued)

STEP NUMBER	REGISTER		DESCRIPTION
	SDIN[23:16] = REG_ADDR	SDIN[15:0] = REG_ADDR DATA	
10 [user dependent]	0x0A	0x003A	User programs this register based on system requirements. 0x003A selects ADC conversion data size of 24b, and 1-lane mode data output on SDOUT pin.

6.6 Register Maps

6.6.1 ADS93x8V8I Common Registers

Table 6-10 lists the memory-mapped registers for the ADS93x8V8I Common registers. All register offset addresses not listed in Table 6-10 should be considered as reserved locations and the register contents should not be modified.

Table 6-10. ADS93x8V8I_Common

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	GEN_CFG1	REG_RD_ADD[7:0]							
		RESERVED						SW_RST	REG_RD_EN
0x02	BANK_SEL	RESERVED							
		RESERVED					BANK_SEL[2:0]		
0x07	DIAG_CTRL	RESERVED							RESET_DETECT_FLAG
		RESERVED							
0x08	PDN_CTL	RESERVED							
		RESERVED							DEVICE_PDN
0x09	GEN_CFG2	RESERVED				DAISY_CHN_LOC[3:0]			
		DAISY_CHN_NUM[3:0]				RESERVED			DAISY_CHN_EN
0x0A	GEN_CFG3	RESERVED			EN_OFS_BINARY	RESERVED		EN_XOR_PATT	EN_DIAG_FLAG
		RESERVED		DOUT_LANE_SEL[1:0]		DOUT_LENGTH[1:0]		ADC_DATA_SDOUT_EN	RESERVED
0x0B	XOR_BITS_CTL	RESERVED							
		XOR_MODE[1:0]		NUM_XOR_BITS[1:0]		RESERVED			XOR_BIT_SEL
0x0C	DRDY_ALARM_SEL	ALRM_MASK[7:0]							
		RESERVED		ALRM_TYPE	ALRM_POL	DRDY_ALRM_SEL[3:0]			
0x0D	GEN_CFG4	RESERVED							
		RESERVED		ALRM_DIS	RESERVED	DIG_DELAY_EN	RESERVED	DRIVE_STRENGTH[1:0]	
0x0E	DIG_DELAY_CFG1	RESERVED	DIG_DELAY_SDOUT[2:0]			DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
		DIG_DELAY_D2[2:0]		DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]		
0x0F	DIG_DELAY_CFG2	RESERVED				DIG_DELAY_D7[2:0]			DIG_DELAY_D6[2:0]
		DIG_DELAY_D6[2:0]		DIG_DELAY_D5[2:0]			DIG_DELAY_D4[2:0]		
0x10	ANA_CFG1	RESERVED							
		RESERVED						REFSEL_CTRL_DIS	EXT_REF_EN
0x11	ANA_CFG2	RESERVED							
		RESERVED	ADC_CH_SEL[2:0]			ADC_NUM_SEL[1:0]		RESERVED	
0x14	DIG_FILTER	RESERVED							
		BLK_AVG_OSR[3:0]				RESERVED			DIG_FILT_SYSREF
0x15	GEN_CFG5	RESERVED							
		RESERVED				T_MODE_OVR_EN	T_MODE	RESERVED	
0x21	DEVICE_ID	RESERVED							
		DEVICE_ID[7:0]							

Complex bit access types are encoded to fit into small table cells. Table 6-11 shows the codes that are used for access types in this section.

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Table 6-11. ADS93x8V8I Common Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.1.1 GEN_CFG1 Register (Address = 0x01) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-10. GEN_CFG1 Register

15	14	13	12	11	10	9	8
REG_RD_ADD[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED						SW_RST	REG_RD_EN
R/W-000000b						R/W-0b	R/W-0b

Table 6-12. GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	REG_RD_ADD[7:0]	R/W	00000000b	Register read address
7:2	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
1	SW_RST	R/W	0b	Writing 1b to this bit resets the device.
0	REG_RD_EN	R/W	0b	Register read enable

6.6.1.2 BANK_SEL Register (Address = 0x02) [Reset = 0x0001]

Return to the Summary Table.

Figure 6-11. BANK_SEL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000000b							
7	6	5	4	3	2	1	0
RESERVED						BANK_SEL[2:0]	
R/W-0000000000000b						R/W-001b	

Table 6-13. BANK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R/W	0000000000000b	Reserved. Do not change from the default reset value.
2:0	BANK_SEL[2:0]	R/W	001b	Register bank selection. 001b = Common Registers 010b = IS1 - IS8 Channel Registers 100b = VS1 - VS8 Channel Registers

6.6.1.3 DIAG_CTRL Register (Address = 0x07) [Reset = 0x0100]

Return to the Summary Table.

Figure 6-12. DIAG_CTRL Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED						RESET_DETECT_FLAG
R/W-0b	R/W-000000b						R/W-1b
7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 6-14. DIAG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
14:9	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
8	RESET_DETECT_FLAG	R/W	1b	Indicates reset of the device, User writes this bit to 0b. If the ADC undergoes reset, the bit is set to 1b. This bit can be read on the SDOUT status bits.
7:6	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
5	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
4	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
1	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
0	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.

6.6.1.4 PDN_CTL Register (Address = 0x08) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-13. PDN_CTL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
RESERVED							DEVICE_PDN
R/W-0000000000000000b							R/W-0b

Table 6-15. PDN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED	R/W	0000000000000 00b	Reserved. Do not change from the default reset value.
0	DEVICE_PDN	R/W	0b	Device power down control. 0b = Normal operation 1b = Device is in power down

6.6.1.5 GEN_CFG2 Register (Address = 0x09) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-14. GEN_CFG2 Register

15	14	13	12	11	10	9	8
RESERVED				DAISY_CHN_LOC[3:0]			
R/W-0000b				R/W-0000b			
7	6	5	4	3	2	1	0
DAISY_CHN_NUM[3:0]				RESERVED			DAISY_CHN_EN
R/W-0000b				R/W-000b			R/W-0b

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Table 6-16. GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.
11:8	DAISY_CHN_LOC[3:0]	R/W	0000b	Location of the device in the daisy chain configuration.
7:4	DAISY_CHN_NUM[3:0]	R/W	0000b	Total number of devices in the daisy chain configuration.
3:1	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
0	DAISY_CHN_EN	R/W	0b	Daisy chain configuration enable. 0b = Daisy chain configuration disabled 1b = Daisy chain configuration enabled

6.6.1.6 GEN_CFG3 Register (Address = 0x0A) [Reset = 0x0108]

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Figure 6-15. GEN_CFG3 Register

15	14	13	12	11	10	9	8
RESERVED			EN_OFS_BINARY	RESERVED		EN_XOR_PATT	EN_DIAG_FLAG
R/W-000b			R/W-0b	R/W-00b		R/W-0b	R/W-1b
7	6	5	4	3	2	1	0
RESERVED		DOUT_LANE_SEL[1:0]		DOUT_LENGTH[1:0]		ADC_DATA_SDOUT_EN	RESERVED
R/W-00b		R/W-00b		R/W-10b		R/W-0b	R/W-0b

Table 6-17. GEN_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
12	EN_OFS_BINARY	R/W	0b	ADC conversion data output format selection. 0b = Two's complement 1b = Offset binary
11:10	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
9	EN_XOR_PATT	R/W	0b	Enables XOR operation on the ADC conversion result. 0b = XOR operation is disabled 1b = Bit-wise XOR operation on ADC conversion result is enabled
8	EN_DIAG_FLAG	R/W	1b	Enables status bits after the ADC conversion data output.
7:6	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
5:4	DOUT_LANE_SEL[1:0]	R/W	00b	Data lane selection. 00b = 8 lanes 01b = 4 lanes 10b = 2 lanes 11b = 1 lane
3:2	DOUT_LENGTH[1:0]	R/W	10b	ADC data size selection. 00b = 16-bit 01b = Reserved 10b = 24-bit
1	ADC_DATA_SDOUT_EN	R/W	0b	ADC data output on SDOUT pin enable in single lane mode. 0b = ADC data output on D7 1b = ADC data output on SDOUT pin
0	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.

6.6.1.7 XOR_BITS_CTL Register (Address = 0x0B) [Reset = 0x0000]

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Figure 6-16. XOR_BITS_CTL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000b							
7	6	5	4	3	2	1	0
XOR_MODE[1:0]		NUM_XOR_BITS[1:0]		RESERVED			XOR_BIT_SEL
R/W-00b		R/W-00b		R/W-000b			R/W-0b

Table 6-18. XOR_BITS_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R/W	00000000b	Reserved. Do not change from the default reset value.
7:6	XOR_MODE[1:0]	R/W	00b	Set the XOR_MODE to 3.
5:4	NUM_XOR_BITS[1:0]	R/W	00b	Select the number of XOR bits for ADC output randomizer. Set this bit field to 3.
3:1	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
0	XOR_BIT_SEL	R/W	0b	Set this bit to 1b for PRBS bits. 0b = PRBS

6.6.1.8 DRDY_ALARM_SEL Register (Address = 0x0C) [Reset = 0x0000]

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Figure 6-17. DRDY_ALARM_SEL Register

15	14	13	12	11	10	9	8
ALRM_MASK[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED		ALRM_TYPE	ALRM_POL	DRDY_ALRM_SEL[3:0]			
R/W-00b		R/W-0b	R/W-0b	R/W-0000b			

Table 6-19. DRDY_ALARM_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALRM_MASK[7:0]	R/W	00000000b	Alarm mask selection. Each bit controls the mask for every alarm mode when OR'ed output of each alarm is selected on ALARM pin.
7:6	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
5	ALRM_TYPE	R/W	0b	Alarm type selection. Applicable only for DWC. 0b = Level based 1b = Pulse based
4	ALRM_POL	R/W	0b	DRDY/ALARM polarity selection. 0b = Active high 1b = Active low
3:0	DRDY_ALRM_SEL[3:0]	R/W	0000b	DRDY/ALARM selection. 0000b = ADC data ready flag (DRDY) 0001b = DWC output 0010b = Reserved 0011b = Reserved 0100b = Reserved 0101b = Reserved 0110b = Reserved 0111b = Reserved 1000b = OR'ed of all above flags with individual mask before ORing

6.6.1.9 GEN_CFG4 Register (Address = 0x0D) [Reset = 0x0000]

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Figure 6-18. GEN_CFG4 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000b							
7	6	5	4	3	2	1	0
RESERVED		ALRM_DIS	RESERVED	DIG_DELAY_EN	RESERVED	DRIVE_STRENGTH[1:0]	
R/W-0000000000b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b	

Table 6-20. GEN_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R/W	0000000000b	Reserved. Do not change from the default reset value.
5	ALRM_DIS	R/W	0b	Alarm function disable. 0b = Enabled 1b = Disabled
4	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.

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Table 6-20. GEN_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIG_DELAY_EN	R/W	0b	Control for digital delay on the output buffer path. 0b = Normal device operation. 1b = Digital delay on the output buffer path is enabled. The magnitude is controlled by DIG_DELAY_CFG1 and DIG_DELAY_CFG2.
2	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
1:0	DRIVE_STRENGTH[1:0]	R/W	00b	Control to configure the drive strength of the digital output buffer.. 00b = Normal device operation 01b = 0.5 x drive strength 10b = 2 x drive strength 11b = 1.5 x drive strength

6.6.1.10 DIG_DELAY_CFG1 Register (Address = 0x0E) [Reset = 0x0000]

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Figure 6-19. DIG_DELAY_CFG1 Register

15	14	13	12	11	10	9	8
RESERVED	DIG_DELAY_SDOUT[2:0]			DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
R/W-0b	R/W-000b			R/W-000b			R/W-000b
7	6	5	4	3	2	1	0
DIG_DELAY_D2[2:0]			DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]	
R/W-000b			R/W-000b			R/W-000b	

Table 6-21. DIG_DELAY_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
14:12	DIG_DELAY_SDOUT[2:0]	R/W	000b	Programmable digital delay on SDOUT. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
11:9	DIG_DELAY_D3[2:0]	R/W	000b	Programmable digital delay on D3. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
8:6	DIG_DELAY_D2[2:0]	R/W	000b	Programmable digital delay on D2. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
5:3	DIG_DELAY_D1[2:0]	R/W	000b	Programmable digital delay on D1. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
2:0	DIG_DELAY_D0[2:0]	R/W	000b	Programmable digital delay on D0. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay

6.6.1.11 DIG_DELAY_CFG2 Register (Address = 0x0F) [Reset = 0x0000]

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Figure 6-20. DIG_DELAY_CFG2 Register

15	14	13	12	11	10	9	8

Figure 6-20. DIG_DELAY_CFG2 Register (continued)

RESERVED					DIG_DELAY_D7[2:0]		DIG_DELAY_D6[2:0]
R/W-0000b					R/W-000b		R/W-000b
7	6	5	4	3	2	1	0
DIG_DELAY_D6[2:0]			DIG_DELAY_D5[2:0]			DIG_DELAY_D4[2:0]	
R/W-000b			R/W-000b			R/W-000b	

Table 6-22. DIG_DELAY_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.
11:9	DIG_DELAY_D7[2:0]	R/W	000b	Programmable digital delay on D7. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
8:6	DIG_DELAY_D6[2:0]	R/W	000b	Programmable digital delay on D6. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
5:3	DIG_DELAY_D5[2:0]	R/W	000b	Programmable digital delay on D5. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
2:0	DIG_DELAY_D4[2:0]	R/W	000b	Programmable digital delay on D4. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay

6.6.1.12 ANA_CFG1 Register (Address = 0x10) [Reset = 0x0000]

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Figure 6-21. ANA_CFG1 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
RESERVED						REFSEL_CTRL_DIS	EXT_REF_EN
R/W-0000000000000000b						R/W-0b	R/W-0b

Table 6-23. ANA_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	R/W	00000000000000b	Reserved. Do not change from the default reset value.
1	REFSEL_CTRL_DIS	R/W	0b	REFSEL pin control disable. 0b = Enabled 1b = Disabled
0	EXT_REF_EN	R/W	0b	ADC reference select. 0b = Internal reference 1b = External reference

6.6.1.13 ANA_CFG2 Register (Address = 0x11) [Reset = 0x0000]

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Figure 6-22. ANA_CFG2 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED						
R/W-0b	R/W-00000000b						
7	6	5	4	3	2	1	0
RESERVED	ADC_CH_SEL[2:0]			ADC_NUM_SEL[1:0]		RESERVED	
R/W-00000000b	R/W-000b			R/W-00b		R/W-00b	

Table 6-24. ANA_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
14:7	RESERVED	R/W	00000000b	Reserved. Do not change from the default reset value.
6:4	ADC_CH_SEL[2:0]	R/W	000b	Select the ADC channels corresponding to ADC_NUM_SEL. These configurations work when ADC_NUM_SEL is not 00'b.
3:2	ADC_NUM_SEL[1:0]	R/W	00b	Select the number of ADCs that are undergoing conversion. When ADC_NUM_SEL is 00'b, ADC_CH_SEL is don't care. 00b = 16 Channels (Default) 01b = 8 Channels 10b = 4 Channels 11b = 2 Channels
1:0	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.

6.6.1.14 DIG_FILTER Register (Address = 0x14) [Reset = 0x0000]

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Figure 6-23. DIG_FILTER Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000b							
7	6	5	4	3	2	1	0
BLK_AVG_OSR[3:0]				RESERVED			DIG_FILT_SYSREF
R/W-0000b				R/W-000b			R/W-0b

Table 6-25. DIG_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R/W	00000000b	Reserved. Do not change from the default reset value.
7:4	BLK_AVG_OSR[3:0]	R/W	0000b	Oversampling ratio (OSR) configuration for block average filter. Minimum supported OSR is 8. 0000b = Reserved 0001b = Reserved 0010b = Reserved 0011b = Reserved 0100b = 8 samples averaged 0101b = Reserved 0110b = 12 samples averaged 0111b = 16 samples averaged 1000b = Reserved 1001b = 32 samples averaged 1010b = 64 samples averaged 1011b = 128 samples averaged
3:1	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
0	DIG_FILT_SYSREF	R/W	0b	Writing 1b to this bit resets the average filter at the falling edge of CONVST.

6.6.1.15 GEN_CFG5 Register (Address = 0x15) [Reset = 0x0000]

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Figure 6-24. GEN_CFG5 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							

Figure 6-24. GEN_CFG5 Register (continued)

7	6	5	4	3	2	1	0
RESERVED				T_MODE_OVR_EN	T_MODE	RESERVED	RESERVED
R/W-000000000000b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 6-26. GEN_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3	T_MODE_OVR_EN	R/W	0b	This bit enables T_MODE (truncate mode feature). Set this bit to 1b before configuring the T_MODE field.
2	T_MODE	R/W	0b	This bit allows the user to truncate the ADC output to 16b when using test pattern of this device.
1	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
0	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.

6.6.1.16 DEVICE_ID Register (Address = 0x21) [Reset = 0x0085]

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Figure 6-25. DEVICE_ID Register

15	14	13	12	11	10	9	8
RESERVED							
R-00000000b							
7	6	5	4	3	2	1	0
DEVICE_ID[7:0]							
R-10000101b							

Table 6-27. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	00000000b	Reserved. Do not change from the default reset value.
7:0	DEVICE_ID[7:0]	R	10000101b	Device ID.

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6.6.2 IS1 - IS8 Channel Registers

Table 6-28 lists the memory-mapped registers for the IS1 - IS8 Channel registers. All register offset addresses not listed in Table 6-28 should be considered as reserved locations and the register contents should not be modified.

Table 6-28. IS1 - IS8 Channel

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	PGA_CONFIG_IS1_2	RESERVED					INPUT_RANGE_IS2[2:0]		
		RESERVED					INPUT_RANGE_IS1[2:0]		
0x09	PGA_CONFIG_IS3_4	RESERVED					INPUT_RANGE_IS4[2:0]		
		RESERVED					INPUT_RANGE_IS3[2:0]		
0x0A	PGA_CONFIG_IS5_6	RESERVED					INPUT_RANGE_IS6[2:0]		
		RESERVED					INPUT_RANGE_IS5[2:0]		
0x0B	PGA_CONFIG_IS7_8	RESERVED					INPUT_RANGE_IS8[2:0]		
		RESERVED					INPUT_RANGE_IS7[2:0]		
0x11	OFS_IS1	RESERVED						OFS_IS1[9:0]	
		OFS_IS1[9:0]							
0x12	OFS_IS2	RESERVED						OFS_IS2[9:0]	
		OFS_IS2[9:0]							
0x13	OFS_IS3	RESERVED						OFS_IS3[9:0]	
		OFS_IS3[9:0]							
0x14	OFS_IS4	RESERVED						OFS_IS4[9:0]	
		OFS_IS4[9:0]							
0x15	OFS_IS5	RESERVED						OFS_IS5[9:0]	
		OFS_IS5[9:0]							
0x16	OFS_IS6	RESERVED						OFS_IS6[9:0]	
		OFS_IS6[9:0]							
0x17	OFS_IS7	RESERVED						OFS_IS7[9:0]	
		OFS_IS7[9:0]							
0x18	OFS_IS8	RESERVED						OFS_IS8[9:0]	
		OFS_IS8[9:0]							
0x19	GAN_IS1	RESERVED		GAN_IS1[13:0]					
		GAN_IS1[13:0]							
0x1A	GAN_IS2	RESERVED		GAN_IS2[13:0]					
		GAN_IS2[13:0]							
0x1B	GAN_IS3	RESERVED		GAN_IS3[13:0]					
		GAN_IS3[13:0]							
0x1C	GAN_IS4	RESERVED		GAN_IS4[13:0]					
		GAN_IS4[13:0]							
0x1D	GAN_IS5	RESERVED		GAN_IS5[13:0]					
		GAN_IS5[13:0]							
0x1E	GAN_IS6	RESERVED		GAN_IS6[13:0]					
		GAN_IS6[13:0]							
0x1F	GAN_IS7	RESERVED		GAN_IS7[13:0]					
		GAN_IS7[13:0]							
0x20	GAN_IS8	RESERVED		GAN_IS8[13:0]					
		GAN_IS8[13:0]							
0x21	DWC_CFG	DWC_STAT_RST	RESERVED			DWC_GLITCH_FILT[3:0]			
		DWC_EN_IS8	DWC_EN_IS7	DWC_EN_IS6	DWC_EN_IS5	DWC_EN_IS4	DWC_EN_IS3	DWC_EN_IS2	DWC_EN_IS1
0x22	DWC_TH_IS1	HIGH_TH_IS1[7:0]							
		LOW_TH_IS1[7:0]							
0x23	DWC_TH_IS2	HIGH_TH_IS2[7:0]							
		LOW_TH_IS2[7:0]							

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Table 6-28. IS1 - IS8 Channel (continued)

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x24	DWC_TH_IS3	HIGH_TH_IS3[7:0]							
		LOW_TH_IS3[7:0]							
0x25	DWC_TH_IS4	HIGH_TH_IS4[7:0]							
		LOW_TH_IS4[7:0]							
0x26	DWC_TH_IS5	HIGH_TH_IS5[7:0]							
		LOW_TH_IS5[7:0]							
0x27	DWC_TH_IS6	HIGH_TH_IS6[7:0]							
		LOW_TH_IS6[7:0]							
0x28	DWC_TH_IS7	HIGH_TH_IS7[7:0]							
		LOW_TH_IS7[7:0]							
0x29	DWC_TH_IS8	HIGH_TH_IS8[7:0]							
		LOW_TH_IS8[7:0]							
0x2A	DWC_HYS_IS1_2	HYS_IS2[7:0]							
		HYS_IS1[7:0]							
0x2B	DWC_HYS_IS3_4	HYS_IS4[7:0]							
		HYS_IS3[7:0]							
0x2C	DWC_HYS_IS5_6	HYS_IS6[7:0]							
		HYS_IS5[7:0]							
0x2D	DWC_HYS_IS7_8	HYS_IS8[7:0]							
		HYS_IS7[7:0]							
0x2E	TP_CFG	RESERVED							
		RESERVED	TP_MODE[2:0]			RESERVED	TP_DIS_IDX	TP_UP_DN_EN	TP_EN
0x2F	TP_IS1	TP_IS1[15:0]							
		TP_IS1[15:0]							
0x30	TP_IS2	TP_IS2[15:0]							
		TP_IS2[15:0]							
0x31	TP_IS3	TP_IS3[15:0]							
		TP_IS3[15:0]							
0x32	TP_IS4	TP_IS4[15:0]							
		TP_IS4[15:0]							
0x33	TP_IS5	TP_IS5[15:0]							
		TP_IS5[15:0]							
0x34	TP_IS6	TP_IS6[15:0]							
		TP_IS6[15:0]							
0x35	TP_IS7	TP_IS7[15:0]							
		TP_IS7[15:0]							
0x36	TP_IS8	TP_IS8[15:0]							
		TP_IS8[15:0]							
0x37	GEN_CFG1	RESERVED							
		RESERVED						OFS_CORR_EN	GAN_CORR_EN
0x3E	DWC_FLAG_IS1_8	HIGH_FLAG_IS8	HIGH_FLAG_IS7	HIGH_FLAG_IS6	HIGH_FLAG_IS5	HIGH_FLAG_IS4	HIGH_FLAG_IS3	HIGH_FLAG_IS2	HIGH_FLAG_IS1
		LOW_FLAG_IS8	LOW_FLAG_IS7	LOW_FLAG_IS6	LOW_FLAG_IS5	LOW_FLAG_IS4	LOW_FLAG_IS3	LOW_FLAG_IS2	LOW_FLAG_IS1

Complex bit access types are encoded to fit into small table cells. Table 6-29 shows the codes that are used for access types in this section.

Table 6-29. IS1 - IS8 Channel Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		

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Table 6-29. IS1 - IS8 Channel Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.2.1 PGA_CONFIG_IS1_2 Register (Address = 0x08) [Reset = 0x0000]

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Figure 6-26. PGA_CONFIG_IS1_2 Register

15	14	13	12	11	10	9	8
RESERVED						INPUT_RANGE_IS2[2:0]	
R/W-00000b						R/W-000b	
7	6	5	4	3	2	1	0
RESERVED						INPUT_RANGE_IS1[2:0]	
R/W-00000b						R/W-000b	

Table 6-30. PGA_CONFIG_IS1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_IS2[2:0]	R/W	000b	IS2 analog input range selection. 000b = ±25mV 001b = ±50mV 010b = ±100mV 011b = ±150mV 100b = ±200mV
7:3	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_IS1[2:0]	R/W	000b	IS1 analog input range selection. 000b = ±25mV 001b = ±50mV 010b = ±100mV 011b = ±150mV 100b = ±200mV

6.6.2.2 PGA_CONFIG_IS3_4 Register (Address = 0x09) [Reset = 0x0000]

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Figure 6-27. PGA_CONFIG_IS3_4 Register

15	14	13	12	11	10	9	8
RESERVED						INPUT_RANGE_IS4[2:0]	
R/W-00000b						R/W-000b	
7	6	5	4	3	2	1	0
RESERVED						INPUT_RANGE_IS3[2:0]	
R/W-00000b						R/W-000b	

Table 6-31. PGA_CONFIG_IS3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_IS4[2:0]	R/W	000b	IS4 analog input range selection. 000b = ±25mV 001b = ±50mV 010b = ±100mV 011b = ±150mV 100b = ±200mV
7:3	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.

Table 6-31. PGA_CONFIG_IS3_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	INPUT_RANGE_IS3[2:0]	R/W	000b	IS3 analog input range selection. 000b = ±25mV 001b = ±50mV 010b = ±100mV 011b = ±150mV 100b = ±200mV

6.6.2.3 PGA_CONFIG_IS5_6 Register (Address = 0x0A) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-28. PGA_CONFIG_IS5_6 Register

15	14	13	12	11	10	9	8
RESERVED						INPUT_RANGE_IS6[2:0]	
R/W-00000b						R/W-000b	
7	6	5	4	3	2	1	0
RESERVED						INPUT_RANGE_IS5[2:0]	
R/W-00000b						R/W-000b	

Table 6-32. PGA_CONFIG_IS5_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_IS6[2:0]	R/W	000b	IS6 analog input range selection. 000b = ±25mV 001b = ±50mV 010b = ±100mV 011b = ±150mV 100b = ±200mV
7:3	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_IS5[2:0]	R/W	000b	IS5 analog input range selection. 000b = ±25mV 001b = ±50mV 010b = ±100mV 011b = ±150mV 100b = ±200mV

6.6.2.4 PGA_CONFIG_IS7_8 Register (Address = 0x0B) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-29. PGA_CONFIG_IS7_8 Register

15	14	13	12	11	10	9	8
RESERVED						INPUT_RANGE_IS8[2:0]	
R/W-00000b						R/W-000b	
7	6	5	4	3	2	1	0
RESERVED						INPUT_RANGE_IS7[2:0]	
R/W-00000b						R/W-000b	

Table 6-33. PGA_CONFIG_IS7_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_IS8[2:0]	R/W	000b	IS8 analog input range selection. 000b = ±25mV 001b = ±50mV 010b = ±100mV 011b = ±150mV 100b = ±200mV
7:3	RESERVED	R/W	00000b	Reserved. Do not change from the default reset value.

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Table 6-33. PGA_CONFIG_IS7_8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	INPUT_RANGE_IS7[2:0]	R/W	000b	IS7 analog input range selection. 000b = ±25mV 001b = ±50mV 010b = ±100mV 011b = ±150mV 100b = ±200mV

6.6.2.5 OFS_IS1 Register (Address = 0x11) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-30. OFS_IS1 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_IS1[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_IS1[9:0]							
R/W-0000000000b							

Table 6-34. OFS_IS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_IS1[9:0]	R/W	0000000000b	Offset correction register for IS1. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.2.6 OFS_IS2 Register (Address = 0x12) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-31. OFS_IS2 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_IS2[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_IS2[9:0]							
R/W-0000000000b							

Table 6-35. OFS_IS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_IS2[9:0]	R/W	0000000000b	Offset correction register for IS2. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.2.7 OFS_IS3 Register (Address = 0x13) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-32. OFS_IS3 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_IS3[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_IS3[9:0]							
R/W-0000000000b							

Figure 6-32. OFS_IS3 Register (continued)

Table 6-36. OFS_IS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_IS3[9:0]	R/W	0000000000b	Offset correction register for IS3. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.2.8 OFS_IS4 Register (Address = 0x14) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-33. OFS_IS4 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_IS4[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_IS4[9:0]							
R/W-0000000000b							

Table 6-37. OFS_IS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_IS4[9:0]	R/W	0000000000b	Offset correction register for IS4. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.2.9 OFS_IS5 Register (Address = 0x15) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-34. OFS_IS5 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_IS5[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_IS5[9:0]							
R/W-0000000000b							

Table 6-38. OFS_IS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_IS5[9:0]	R/W	0000000000b	Offset correction register for IS5. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.2.10 OFS_IS6 Register (Address = 0x16) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-35. OFS_IS6 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_IS6[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_IS6[9:0]							

Figure 6-35. OFS_IS6 Register (continued)

R/W-0000000000b

Table 6-39. OFS_IS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_IS6[9:0]	R/W	0000000000b	Offset correction register for IS6. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.2.11 OFS_IS7 Register (Address = 0x17) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-36. OFS_IS7 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_IS7[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_IS7[9:0]							
R/W-0000000000b							

Table 6-40. OFS_IS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_IS7[9:0]	R/W	0000000000b	Offset correction register for IS7. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.2.12 OFS_IS8 Register (Address = 0x18) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-37. OFS_IS8 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_IS8[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_IS8[9:0]							
R/W-0000000000b							

Table 6-41. OFS_IS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_IS8[9:0]	R/W	0000000000b	Offset correction register for IS8. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.2.13 GAN_IS1 Register (Address = 0x19) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-38. GAN_IS1 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_IS1[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0

Figure 6-38. GAN_IS1 Register (continued)

GAN_IS1[13:0]
R/W-00000000000000b

Table 6-42. GAN_IS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_IS1[13:0]	R/W	00000000000000b	Gain correction register for IS1. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_ISn[13:0] / 10000h).

6.6.2.14 GAN_IS2 Register (Address = 0x1A) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-39. GAN_IS2 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_IS2[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_IS2[13:0]							
R/W-00000000000000b							

Table 6-43. GAN_IS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_IS2[13:0]	R/W	00000000000000b	Gain correction register for IS2. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_ISn[13:0] / 10000h).

6.6.2.15 GAN_IS3 Register (Address = 0x1B) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-40. GAN_IS3 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_IS3[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_IS3[13:0]							
R/W-00000000000000b							

Table 6-44. GAN_IS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_IS3[13:0]	R/W	00000000000000b	Gain correction register for IS3. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_ISn[13:0] / 10000h).

6.6.2.16 GAN_IS4 Register (Address = 0x1C) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-41. GAN_IS4 Register

15	14	13	12	11	10	9	8

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Figure 6-41. GAN_IS4 Register (continued)

15	14	13	12	11	10	9	8
RESERVED				GAN_IS4[13:0]			
R/W-00b				R/W-00000000000000b			
7	6	5	4	3	2	1	0
GAN_IS4[13:0]							
R/W-00000000000000b							

Table 6-45. GAN_IS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_IS4[13:0]	R/W	00000000000000b	Gain correction register for IS4. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_ISn[13:0] / 10000h).

6.6.2.17 GAN_IS5 Register (Address = 0x1D) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-42. GAN_IS5 Register

15	14	13	12	11	10	9	8
RESERVED				GAN_IS5[13:0]			
R/W-00b				R/W-00000000000000b			
7	6	5	4	3	2	1	0
GAN_IS5[13:0]							
R/W-00000000000000b							

Table 6-46. GAN_IS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_IS5[13:0]	R/W	00000000000000b	Gain correction register for IS5. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_ISn[13:0] / 10000h).

6.6.2.18 GAN_IS6 Register (Address = 0x1E) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-43. GAN_IS6 Register

15	14	13	12	11	10	9	8
RESERVED				GAN_IS6[13:0]			
R/W-00b				R/W-00000000000000b			
7	6	5	4	3	2	1	0
GAN_IS6[13:0]							
R/W-00000000000000b							

Table 6-47. GAN_IS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_IS6[13:0]	R/W	00000000000000b	Gain correction register for IS6. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_ISn[13:0] / 10000h).

6.6.2.19 GAN_IS7 Register (Address = 0x1F) [Reset = 0x0000]

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Figure 6-44. GAN_IS7 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_IS7[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_IS7[13:0]							
R/W-00000000000000b							

Table 6-48. GAN_IS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_IS7[13:0]	R/W	00000000000000b	Gain correction register for IS7. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_ISn[13:0] / 10000h).

6.6.2.20 GAN_IS8 Register (Address = 0x20) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-45. GAN_IS8 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_IS8[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_IS8[13:0]							
R/W-00000000000000b							

Table 6-49. GAN_IS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_IS8[13:0]	R/W	00000000000000b	Gain correction register for IS8. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_ISn[13:0] / 10000h).

6.6.2.21 DWC_CFG Register (Address = 0x21) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-46. DWC_CFG Register

15	14	13	12	11	10	9	8
DWC_STAT_RST	RESERVED			DWC_GLITCH_FILT[3:0]			
R/W-0b	R/W-000b			R/W-0000b			
7	6	5	4	3	2	1	0
DWC_EN_IS8	DWC_EN_IS7	DWC_EN_IS6	DWC_EN_IS5	DWC_EN_IS4	DWC_EN_IS3	DWC_EN_IS2	DWC_EN_IS1
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 6-50. DWC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DWC_STAT_RST	R/W	0b	Digital window comparator reset control. Write 1'b to reset.
14:12	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
11:8	DWC_GLITCH_FILT[3:0]	R/W	0000b	Digital window comparator glitch rejection filter control. Comparator flag is set only when ADC data exceeds the threshold for consecutive number of DWC_GLITCH_FILT[3:0] cycles.

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Table 6-50. DWC_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	DWC_EN_IS8	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
6	DWC_EN_IS7	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
5	DWC_EN_IS6	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
4	DWC_EN_IS5	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
3	DWC_EN_IS4	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
2	DWC_EN_IS3	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
1	DWC_EN_IS2	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
0	DWC_EN_IS1	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled

6.6.2.22 DWC_TH_IS1 Register (Address = 0x22) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-47. DWC_TH_IS1 Register

15	14	13	12	11	10	9	8
HIGH_TH_IS1[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_IS1[7:0]							
R/W-00000000b							

Table 6-51. DWC_TH_IS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_IS1[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_IS1[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.2.23 DWC_TH_IS2 Register (Address = 0x23) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-48. DWC_TH_IS2 Register

15	14	13	12	11	10	9	8
HIGH_TH_IS2[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_IS2[7:0]							
R/W-00000000b							

Table 6-52. DWC_TH_IS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_IS2[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

Table 6-52. DWC_TH_IS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	LOW_TH_IS2[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.2.24 DWC_TH_IS3 Register (Address = 0x24) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-49. DWC_TH_IS3 Register

15	14	13	12	11	10	9	8
HIGH_TH_IS3[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_IS3[7:0]							
R/W-00000000b							

Table 6-53. DWC_TH_IS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_IS3[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_IS3[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.2.25 DWC_TH_IS4 Register (Address = 0x25) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-50. DWC_TH_IS4 Register

15	14	13	12	11	10	9	8
HIGH_TH_IS4[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_IS4[7:0]							
R/W-00000000b							

Table 6-54. DWC_TH_IS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_IS4[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_IS4[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.2.26 DWC_TH_IS5 Register (Address = 0x26) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-51. DWC_TH_IS5 Register

15	14	13	12	11	10	9	8
HIGH_TH_IS5[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_IS5[7:0]							
R/W-00000000b							

Table 6-55. DWC_TH_IS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_IS5[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_IS5[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.2.27 DWC_TH_IS6 Register (Address = 0x27) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-52. DWC_TH_IS6 Register

15	14	13	12	11	10	9	8
HIGH_TH_IS6[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_IS6[7:0]							
R/W-00000000b							

Table 6-56. DWC_TH_IS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_IS6[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_IS6[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.2.28 DWC_TH_IS7 Register (Address = 0x28) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-53. DWC_TH_IS7 Register

15	14	13	12	11	10	9	8
HIGH_TH_IS7[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_IS7[7:0]							
R/W-00000000b							

Table 6-57. DWC_TH_IS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_IS7[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_IS7[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.2.29 DWC_TH_IS8 Register (Address = 0x29) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-54. DWC_TH_IS8 Register

15	14	13	12	11	10	9	8
HIGH_TH_IS8[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_IS8[7:0]							
R/W-00000000b							

Table 6-58. DWC_TH_IS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_IS8[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_IS8[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.2.30 DWC_HYS_IS1_2 Register (Address = 0x2A) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-55. DWC_HYS_IS1_2 Register

15	14	13	12	11	10	9	8
HYS_IS2[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
HYS_IS1[7:0]							
R/W-00000000b							

Table 6-59. DWC_HYS_IS1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_IS2[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.
7:0	HYS_IS1[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

6.6.2.31 DWC_HYS_IS3_4 Register (Address = 0x2B) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-56. DWC_HYS_IS3_4 Register

15	14	13	12	11	10	9	8
HYS_IS4[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_IS3[7:0]							
R/W-00000000b							

Table 6-60. DWC_HYS_IS3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_IS4[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds.
7:0	HYS_IS3[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

6.6.2.32 DWC_HYS_IS5_6 Register (Address = 0x2C) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-57. DWC_HYS_IS5_6 Register

15	14	13	12	11	10	9	8
HYS_IS6[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_IS5[7:0]							
R/W-00000000b							

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Table 6-61. DWC_HYS_IS5_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_IS6[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds.
7:0	HYS_IS5[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

6.6.2.33 DWC_HYS_IS7_8 Register (Address = 0x2D) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-58. DWC_HYS_IS7_8 Register

15	14	13	12	11	10	9	8
HYS_IS8[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_IS7[7:0]							
R/W-00000000b							

Table 6-62. DWC_HYS_IS7_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_IS8[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds.
7:0	HYS_IS7[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

6.6.2.34 TP_CFG Register (Address = 0x2E) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-59. TP_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000b							
7	6	5	4	3	2	1	0
RESERVED	TP_MODE[2:0]			RESERVED	TP_DIS_IDX	TP_UP_DN_EN	TP_EN
R/W-000000000b	R/W-000b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 6-63. TP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED	R/W	000000000b	Reserved. Do not change from the default reset value.
6:4	TP_MODE[2:0]	R/W	000b	Test pattern mode selection. 000b = Constant pattern 001b = Reserved 010b = Ramp pattern 011b = Reserved 100b = Reserved 101b = Reserved
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2	TP_DIS_IDX	R/W	0b	When set to 1b, channel index insertion in test pattern is disabled.
1	TP_UP_DN_EN	R/W	0b	Test pattern increment mode. 0b = Increment happens at channel frame boundary. 1b = Increment happens at every CONVST.
0	TP_EN	R/W	0b	Test pattern enable for IS1 to IS8. 0b = ADC conversion result is launched on the data interface 1b = Digital test pattern is launched on the data interface

6.6.2.35 TP_IS1 Register (Address = 0x2F) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-60. TP_IS1 Register

15	14	13	12	11	10	9	8

Figure 6-60. TP_IS1 Register (continued)

TP_IS1[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_IS1[15:0]							
R/W-0000000000000000b							

Table 6-64. TP_IS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_IS1[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for IS1.

6.6.2.36 TP_IS2 Register (Address = 0x30) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-61. TP_IS2 Register

15	14	13	12	11	10	9	8
TP_IS2[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_IS2[15:0]							
R/W-0000000000000000b							

Table 6-65. TP_IS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_IS2[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for IS2.

6.6.2.37 TP_IS3 Register (Address = 0x31) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-62. TP_IS3 Register

15	14	13	12	11	10	9	8
TP_IS3[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_IS3[15:0]							
R/W-0000000000000000b							

Table 6-66. TP_IS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_IS3[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for IS3.

6.6.2.38 TP_IS4 Register (Address = 0x32) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-63. TP_IS4 Register

15	14	13	12	11	10	9	8
TP_IS4[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0

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Figure 6-63. TP_IS4 Register (continued)

TP_IS4[15:0]
R/W-0000000000000000b

Table 6-67. TP_IS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_IS4[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for IS4.

6.6.2.39 TP_IS5 Register (Address = 0x33) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-64. TP_IS5 Register

15	14	13	12	11	10	9	8
TP_IS5[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_IS5[15:0]							
R/W-0000000000000000b							

Table 6-68. TP_IS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_IS5[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for IS5.

6.6.2.40 TP_IS6 Register (Address = 0x34) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-65. TP_IS6 Register

15	14	13	12	11	10	9	8
TP_IS6[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_IS6[15:0]							
R/W-0000000000000000b							

Table 6-69. TP_IS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_IS6[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for IS6.

6.6.2.41 TP_IS7 Register (Address = 0x35) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-66. TP_IS7 Register

15	14	13	12	11	10	9	8
TP_IS7[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_IS7[15:0]							
R/W-0000000000000000b							

Table 6-70. TP_IS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_IS7[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for IS7.

6.6.2.42 TP_IS8 Register (Address = 0x36) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-67. TP_IS8 Register

15	14	13	12	11	10	9	8
TP_IS8[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_IS8[15:0]							
R/W-0000000000000000b							

Table 6-71. TP_IS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_IS8[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for IS8.

6.6.2.43 GEN_CFG1 Register (Address = 0x37) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-68. GEN_CFG1 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				RESERVED		OFS_CORR_EN	GAN_CORR_EN
R/W-000000000000b				R/W-00b		R/W-0b	R/W-0b

Table 6-72. GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3:2	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
1	OFS_CORR_EN	R/W	0b	Offset correction enable for IS 1 to IS8. 0b = Disabled 1b = Enabled
0	GAN_CORR_EN	R/W	0b	Gain correction enable for IS 1 to IS8. 0b = Disabled 1b = Enabled

6.6.2.44 DWC_FLAG_IS1_8 Register (Address = 0x3E) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-69. DWC_FLAG_IS1_8 Register

15	14	13	12	11	10	9	8
HIGH_FLAG_IS8	HIGH_FLAG_IS7	HIGH_FLAG_IS6	HIGH_FLAG_IS5	HIGH_FLAG_IS4	HIGH_FLAG_IS3	HIGH_FLAG_IS2	HIGH_FLAG_IS1
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b
7	6	5	4	3	2	1	0
LOW_FLAG_IS8	LOW_FLAG_IS7	LOW_FLAG_IS6	LOW_FLAG_IS5	LOW_FLAG_IS4	LOW_FLAG_IS3	LOW_FLAG_IS2	LOW_FLAG_IS1
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

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Table 6-73. DWC_FLAG_IS1_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	HIGH_FLAG_IS8	R	0b	Digital window comparator high flag for IS8.
14	HIGH_FLAG_IS7	R	0b	Digital window comparator high flag for IS7.
13	HIGH_FLAG_IS6	R	0b	Digital window comparator high flag for IS6.
12	HIGH_FLAG_IS5	R	0b	Digital window comparator high flag for IS5.
11	HIGH_FLAG_IS4	R	0b	Digital window comparator high flag for IS4.
10	HIGH_FLAG_IS3	R	0b	Digital window comparator high flag for IS3.
9	HIGH_FLAG_IS2	R	0b	Digital window comparator high flag for IS2.
8	HIGH_FLAG_IS1	R	0b	Digital window comparator high flag for IS1.
7	LOW_FLAG_IS8	R	0b	Digital window comparator low flag for IS8.
6	LOW_FLAG_IS7	R	0b	Digital window comparator low flag for IS7.
5	LOW_FLAG_IS6	R	0b	Digital window comparator low flag for IS6.
4	LOW_FLAG_IS5	R	0b	Digital window comparator low flag for IS5.
3	LOW_FLAG_IS4	R	0b	Digital window comparator low flag for IS4.
2	LOW_FLAG_IS3	R	0b	Digital window comparator low flag for IS3.
1	LOW_FLAG_IS2	R	0b	Digital window comparator low flag for IS2.
0	LOW_FLAG_IS1	R	0b	Digital window comparator low flag for IS1.

6.6.3 VS1 - VS8 Channel Registers

Table 6-74 lists the memory-mapped registers for the VS1 - VS8 Channel registers. All register offset addresses not listed in Table 6-74 should be considered as reserved locations and the register contents should not be modified.

Table 6-74. VS1 - VS8 Channel

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	PGA_CONFIG_VS7_8	CME_CORR_EN_VS7	CM_RANGE_VS7[2:0]			RESERVED	INPUT_RANGE_VS7[2:0]		
		CME_CORR_EN_VS8	CM_RANGE_VS8[2:0]			RESERVED	INPUT_RANGE_VS8[2:0]		
0x09	PGA_CONFIG_VS5_6	CME_CORR_EN_VS5	CM_RANGE_VS5[2:0]			RESERVED	INPUT_RANGE_VS5[2:0]		
		CME_CORR_EN_VS6	CM_RANGE_VS6[2:0]			RESERVED	INPUT_RANGE_VS6[2:0]		
0x0A	PGA_CONFIG_VS3_4	CME_CORR_EN_VS3	CM_RANGE_VS3[2:0]			RESERVED	INPUT_RANGE_VS3[2:0]		
		CME_CORR_EN_VS4	CM_RANGE_VS4[2:0]			RESERVED	INPUT_RANGE_VS4[2:0]		
0x0B	PGA_CONFIG_VS1_2	CME_CORR_EN_VS1	CM_RANGE_VS1[2:0]			RESERVED	INPUT_RANGE_VS1[2:0]		
		CME_CORR_EN_VS2	CM_RANGE_VS2[2:0]			RESERVED	INPUT_RANGE_VS2[2:0]		
0x0C	PGA_BW_SEL_VS1_8	PGA_BW_SEL_VS1[1:0]		PGA_BW_SEL_VS2[1:0]		PGA_BW_SEL_VS3[1:0]		PGA_BW_SEL_VS4[1:0]	
		PGA_BW_SEL_VS5[1:0]		PGA_BW_SEL_VS6[1:0]		PGA_BW_SEL_VS7[1:0]		PGA_BW_SEL_VS8[1:0]	
0x11	OFS_VS8	RESERVED						OFS_VS8[9:0]	
		OFS_VS8[9:0]							
0x12	OFS_VS7	RESERVED						OFS_VS7[9:0]	
		OFS_VS7[9:0]							
0x13	OFS_VS6	RESERVED						OFS_VS6[9:0]	
		OFS_VS6[9:0]							
0x14	OFS_VS5	RESERVED						OFS_VS5[9:0]	
		OFS_VS5[9:0]							
0x15	OFS_VS4	RESERVED						OFS_VS4[9:0]	
		OFS_VS4[9:0]							
0x16	OFS_VS3	RESERVED						OFS_VS3[9:0]	
		OFS_VS3[9:0]							
0x17	OFS_VS2	RESERVED						OFS_VS2[9:0]	
		OFS_VS2[9:0]							
0x18	OFS_VS1	RESERVED						OFS_VS1[9:0]	
		OFS_VS1[9:0]							
0x19	GAN_VS8	RESERVED		GAN_VS8[13:0]					
		GAN_VS8[13:0]							
0x1A	GAN_VS7	RESERVED		GAN_VS7[13:0]					
		GAN_VS7[13:0]							
0x1B	GAN_VS6	RESERVED		GAN_VS6[13:0]					
		GAN_VS6[13:0]							
0x1C	GAN_VS5	RESERVED		GAN_VS5[13:0]					
		GAN_VS5[13:0]							
0x1D	GAN_VS4	RESERVED		GAN_VS4[13:0]					
		GAN_VS4[13:0]							
0x1E	GAN_VS3	RESERVED		GAN_VS3[13:0]					
		GAN_VS3[13:0]							
0x1F	GAN_VS2	RESERVED		GAN_VS2[13:0]					
		GAN_VS2[13:0]							
0x20	GAN_VS1	RESERVED		GAN_VS1[13:0]					
		GAN_VS1[13:0]							

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Table 6-74. VS1 - VS8 Channel (continued)

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x21	DWC_CFG	DWC_RST	RESERVED			DWC_GLITCH_FILT[3:0]			
		DWC_EN_VS1	DWC_EN_VS2	DWC_EN_VS3	DWC_EN_VS4	DWC_EN_VS5	DWC_EN_VS6	DWC_EN_VS7	DWC_EN_VS8
0x22	DWC_TH_VS8	HIGH_TH_VS8[7:0]							
		LOW_TH_VS8[7:0]							
0x23	DWC_TH_VS7	HIGH_TH_VS7[7:0]							
		LOW_TH_VS7[7:0]							
0x24	DWC_TH_VS6	HIGH_TH_VS6[7:0]							
		LOW_TH_VS6[7:0]							
0x25	DWC_TH_VS5	HIGH_TH_VS5[7:0]							
		LOW_TH_VS5[7:0]							
0x26	DWC_TH_VS4	HIGH_TH_VS4[7:0]							
		LOW_TH_VS4[7:0]							
0x27	DWC_TH_VS3	HIGH_TH_VS3[7:0]							
		LOW_TH_VS3[7:0]							
0x28	DWC_TH_VS2	HIGH_TH_VS2[7:0]							
		LOW_TH_VS2[7:0]							
0x29	DWC_TH_VS1	HIGH_TH_VS1[7:0]							
		LOW_TH_VS1[7:0]							
0x2A	DWC_HYS_VS7_8	HYS_VS8[7:0]							
		HYS_VS7[7:0]							
0x2B	DWC_HYS_VS5_6	HYS_VS6[7:0]							
		HYS_VS5[7:0]							
0x2C	DWC_HYS_VS3_4	HYS_VS4[7:0]							
		HYS_VS3[7:0]							
0x2D	DWC_HYS_VS1_2	HYS_VS2[7:0]							
		HYS_VS1[7:0]							
0x2E	TP_CFG	RESERVED							
		RESERVED	TP_MODE[2:0]			RESERVED	TP_DIS_IDX	TP_UP_DN_EN	TP_EN
0x2F	TP_VS8	TP_VS8[15:0]							
		TP_VS8[15:0]							
0x30	TP_VS7	TP_VS7[15:0]							
		TP_VS7[15:0]							
0x31	TP_VS6	TP_VS6[15:0]							
		TP_VS6[15:0]							
0x32	TP_VS5	TP_VS5[15:0]							
		TP_VS5[15:0]							
0x33	TP_VS4	TP_VS4[15:0]							
		TP_VS4[15:0]							
0x34	TP_VS3	TP_VS3[15:0]							
		TP_VS3[15:0]							
0x35	TP_VS2	TP_VS2[15:0]							
		TP_VS2[15:0]							
0x36	TP_VS1	TP_VS1[15:0]							
		TP_VS1[15:0]							
0x37	GEN_CFG1	RESERVED							
		RESERVED						OFS_CORR_EN	GAN_CORR_EN
0x3E	DWC_FLAG_VS1_8	HIGH_FLAG_VS1	HIGH_FLAG_VS2	HIGH_FLAG_VS3	HIGH_FLAG_VS4	HIGH_FLAG_VS5	HIGH_FLAG_VS6	HIGH_FLAG_VS7	HIGH_FLAG_VS8
		LOW_FLAG_VS1	LOW_FLAG_VS2	LOW_FLAG_VS3	LOW_FLAG_VS4	LOW_FLAG_VS5	LOW_FLAG_VS6	LOW_FLAG_VS7	LOW_FLAG_VS8

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Complex bit access types are encoded to fit into small table cells. Table 6-75 shows the codes that are used for access types in this section.

Table 6-75. VS1 - VS8 Channel Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.3.1 PGA_CONFIG_VS7_8 Register (Address = 0x08) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-70. PGA_CONFIG_VS7_8 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_VS7	CM_RANGE_VS7[2:0]			RESERVED	INPUT_RANGE_VS7[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_VS8	CM_RANGE_VS8[2:0]			RESERVED	INPUT_RANGE_VS8[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 6-76. PGA_CONFIG_VS7_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_VS7	R/W	0b	Common mode error correction enable.
14:12	CM_RANGE_VS7[2:0]	R/W	000b	Select input signal type. 000b = Differential (±12.5V CM Range) 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_VS7[2:0]	R/W	000b	VS7 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_VS8	R/W	0b	Common mode error correction enable.
6:4	CM_RANGE_VS8[2:0]	R/W	000b	Select input signal type. 000b = Differential (±12.5V CM Range) 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_VS8[2:0]	R/W	000b	VS8 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

6.6.3.2 PGA_CONFIG_VS5_6 Register (Address = 0x09) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-71. PGA_CONFIG_VS5_6 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_VS5	CM_RANGE_VS5[2:0]			RESERVED	INPUT_RANGE_VS5[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_VS6	CM_RANGE_VS6[2:0]			RESERVED	INPUT_RANGE_VS6[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 6-77. PGA_CONFIG_VS5_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_VS5	R/W	0b	Common mode error correction enable.
14:12	CM_RANGE_VS5[2:0]	R/W	000b	Select input signal type. 000b = Differential (±12.5V CM Range) 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_VS5[2:0]	R/W	000b	VS5 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_VS6	R/W	0b	Common mode error correction enable.
6:4	CM_RANGE_VS6[2:0]	R/W	000b	Select input signal type. 000b = Differential (±12.5V CM Range) 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_VS6[2:0]	R/W	000b	VS6 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

6.6.3.3 PGA_CONFIG_VS3_4 Register (Address = 0x0A) [Reset = 0x0000]

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Figure 6-72. PGA_CONFIG_VS3_4 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_VS3	CM_RANGE_VS3[2:0]			RESERVED	INPUT_RANGE_VS3[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_VS4	CM_RANGE_VS4[2:0]			RESERVED	INPUT_RANGE_VS4[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 6-78. PGA_CONFIG_VS3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_VS3	R/W	0b	Common mode error correction enable.
14:12	CM_RANGE_VS3[2:0]	R/W	000b	Select input signal type. 000b = Differential (±12.5V CM Range) 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.

Table 6-78. PGA_CONFIG_VS3_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	INPUT_RANGE_VS3[2:0]	R/W	000b	VS3 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_VS4	R/W	0b	Common mode error correction enable.
6:4	CM_RANGE_VS4[2:0]	R/W	000b	Select input signal type. 000b = Differential (±12.5V CM Range) 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_VS4[2:0]	R/W	000b	VS4 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

6.6.3.4 PGA_CONFIG_VS1_2 Register (Address = 0x0B) [Reset = 0x0000]

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Figure 6-73. PGA_CONFIG_VS1_2 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_VS1	CM_RANGE_VS1[2:0]			RESERVED	INPUT_RANGE_VS1[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_VS2	CM_RANGE_VS2[2:0]			RESERVED	INPUT_RANGE_VS2[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 6-79. PGA_CONFIG_VS1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_VS1	R/W	0b	Common mode error correction enable.
14:12	CM_RANGE_VS1[2:0]	R/W	000b	Select input signal type. 000b = Differential (±12.5V CM Range) 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_VS1[2:0]	R/W	000b	VS1 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_VS2	R/W	0b	Common mode error correction enable.
6:4	CM_RANGE_VS2[2:0]	R/W	000b	Select input signal type. 000b = Differential (±12.5V CM Range) 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.

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Table 6-79. PGA_CONFIG_VS1_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	INPUT_RANGE_VS2[2:0]	R/W	000b	VS2 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

6.6.3.5 PGA_BW_SEL_VS1_8 Register (Address = 0x0C) [Reset = 0x0000]

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Figure 6-74. PGA_BW_SEL_VS1_8 Register

15	14	13	12	11	10	9	8
PGA_BW_SEL_VS1[1:0]		PGA_BW_SEL_VS2[1:0]		PGA_BW_SEL_VS3[1:0]		PGA_BW_SEL_VS4[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	
7	6	5	4	3	2	1	0
PGA_BW_SEL_VS5[1:0]		PGA_BW_SEL_VS6[1:0]		PGA_BW_SEL_VS7[1:0]		PGA_BW_SEL_VS8[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 6-80. PGA_BW_SEL_VS1_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PGA_BW_SEL_VS1[1:0]	R/W	00b	VS1 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
13:12	PGA_BW_SEL_VS2[1:0]	R/W	00b	VS2 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
11:10	PGA_BW_SEL_VS3[1:0]	R/W	00b	VS3 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
9:8	PGA_BW_SEL_VS4[1:0]	R/W	00b	VS4 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
7:6	PGA_BW_SEL_VS5[1:0]	R/W	00b	VS5 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
5:4	PGA_BW_SEL_VS6[1:0]	R/W	00b	VS6 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
3:2	PGA_BW_SEL_VS7[1:0]	R/W	00b	VS7 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
1:0	PGA_BW_SEL_VS8[1:0]	R/W	00b	VS8 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved

6.6.3.6 OFS_VS8 Register (Address = 0x11) [Reset = 0x0000]

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Figure 6-75. OFS_VS8 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_VS8[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_VS8[9:0]							
R/W-0000000000b							

Table 6-81. OFS_VS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_VS8[9:0]	R/W	0000000000b	Offset correction register for VS8. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.3.7 OFS_VS7 Register (Address = 0x12) [Reset = 0x0000]

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Figure 6-76. OFS_VS7 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_VS7[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_VS7[9:0]							
R/W-0000000000b							

Table 6-82. OFS_VS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_VS7[9:0]	R/W	0000000000b	Offset correction register for VS7. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.3.8 OFS_VS6 Register (Address = 0x13) [Reset = 0x0000]

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Figure 6-77. OFS_VS6 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_VS6[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_VS6[9:0]							
R/W-0000000000b							

Table 6-83. OFS_VS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_VS6[9:0]	R/W	0000000000b	Offset correction register for VS6. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.3.9 OFS_VS5 Register (Address = 0x14) [Reset = 0x0000]

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Figure 6-78. OFS_VS5 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_VS5[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_VS5[9:0]							
R/W-0000000000b							

Table 6-84. OFS_VS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_VS5[9:0]	R/W	0000000000b	Offset correction register for VS5. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.3.10 OFS_VS4 Register (Address = 0x15) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-79. OFS_VS4 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_VS4[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_VS4[9:0]							
R/W-0000000000b							

Table 6-85. OFS_VS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_VS4[9:0]	R/W	0000000000b	Offset correction register for VS4. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.3.11 OFS_VS3 Register (Address = 0x16) [Reset = 0x0000]

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Figure 6-80. OFS_VS3 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_VS3[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_VS3[9:0]							
R/W-0000000000b							

Table 6-86. OFS_VS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_VS3[9:0]	R/W	0000000000b	Offset correction register for VS3. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.3.12 OFS_VS2 Register (Address = 0x17) [Reset = 0x0000]

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Figure 6-81. OFS_VS2 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_VS2[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_VS2[9:0]							
R/W-0000000000b							

Table 6-87. OFS_VS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_VS2[9:0]	R/W	0000000000b	Offset correction register for VS2. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.3.13 OFS_VS1 Register (Address = 0x18) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-82. OFS_VS1 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_VS1[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_VS1[9:0]							
R/W-0000000000b							

Table 6-88. OFS_VS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_VS1[9:0]	R/W	0000000000b	Offset correction register for VS1. The offset value is in two's complement representation and is added to the conversion result. The offset operation precedes the gain operation.

6.6.3.14 GAN_VS8 Register (Address = 0x19) [Reset = 0x0000]

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Figure 6-83. GAN_VS8 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_VS8[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_VS8[13:0]							
R/W-00000000000000b							

Table 6-89. GAN_VS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_VS8[13:0]	R/W	00000000000000b	Gain correction register for VS8. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_VSn[13:0] / 10000h).

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6.6.3.15 GAN_VS7 Register (Address = 0x1A) [Reset = 0x0000]

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Figure 6-84. GAN_VS7 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_VS7[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_VS7[13:0]							
R/W-00000000000000b							

Table 6-90. GAN_VS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_VS7[13:0]	R/W	00000000000000b	Gain correction register for VS7. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_VSn[13:0] / 10000h).

6.6.3.16 GAN_VS6 Register (Address = 0x1B) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-85. GAN_VS6 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_VS6[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_VS6[13:0]							
R/W-00000000000000b							

Table 6-91. GAN_VS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_VS6[13:0]	R/W	00000000000000b	Gain correction register for VS6. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_VSn[13:0] / 10000h).

6.6.3.17 GAN_VS5 Register (Address = 0x1C) [Reset = 0x0000]

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Figure 6-86. GAN_VS5 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_VS5[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_VS5[13:0]							
R/W-00000000000000b							

Table 6-92. GAN_VS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.

Table 6-92. GAN_VS5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:0	GAN_VS5[13:0]	R/W	0000000000000b	Gain correction register for VS5. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_VSn[13:0] / 10000h).

6.6.3.18 GAN_VS4 Register (Address = 0x1D) [Reset = 0x0000]

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Figure 6-87. GAN_VS4 Register

15	14	13	12	11	10	9	8
RESERVED			GAN_VS4[13:0]				
R/W-00b			R/W-00000000000000b				
7	6	5	4	3	2	1	0
GAN_VS4[13:0]							
R/W-00000000000000b							

Table 6-93. GAN_VS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_VS4[13:0]	R/W	0000000000000b	Gain correction register for VS4. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_VSn[13:0] / 10000h).

6.6.3.19 GAN_VS3 Register (Address = 0x1E) [Reset = 0x0000]

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Figure 6-88. GAN_VS3 Register

15	14	13	12	11	10	9	8
RESERVED			GAN_VS3[13:0]				
R/W-00b			R/W-00000000000000b				
7	6	5	4	3	2	1	0
GAN_VS3[13:0]							
R/W-00000000000000b							

Table 6-94. GAN_VS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_VS3[13:0]	R/W	0000000000000b	Gain correction register for VS3. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_VSn[13:0] / 10000h).

6.6.3.20 GAN_VS2 Register (Address = 0x1F) [Reset = 0x0000]

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Figure 6-89. GAN_VS2 Register

15	14	13	12	11	10	9	8
RESERVED			GAN_VS2[13:0]				
R/W-00b			R/W-00000000000000b				
7	6	5	4	3	2	1	0
GAN_VS2[13:0]							
R/W-00000000000000b							

Figure 6-89. GAN_VS2 Register (continued)

Table 6-95. GAN_VS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_VS2[13:0]	R/W	00000000000000b	Gain correction register for VS2. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_VSn[13:0] / 10000h).

6.6.3.21 GAN_VS1 Register (Address = 0x20) [Reset = 0x0000]

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Figure 6-90. GAN_VS1 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_VS1[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_VS1[13:0]							
R/W-00000000000000b							

Table 6-96. GAN_VS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_VS1[13:0]	R/W	00000000000000b	Gain correction register for VS1. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_VSn[13:0] / 10000h).

6.6.3.22 DWC_CFG Register (Address = 0x21) [Reset = 0x0000]

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Figure 6-91. DWC_CFG Register

15	14	13	12	11	10	9	8
DWC_RST	RESERVED			DWC_GLITCH_FILT[3:0]			
R/W-0b	R/W-000b			R/W-0000b			
7	6	5	4	3	2	1	0
DWC_EN_VS1	DWC_EN_VS2	DWC_EN_VS3	DWC_EN_VS4	DWC_EN_VS5	DWC_EN_VS6	DWC_EN_VS7	DWC_EN_VS8
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 6-97. DWC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DWC_RST	R/W	0b	Digital window comparator reset control. Write 1'b to reset.
14:12	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
11:8	DWC_GLITCH_FILT[3:0]	R/W	0000b	Digital window comparator glitch rejection filter control. Comparator flag is set only when ADC data exceeds the threshold for consecutive number of DWC_GLITCH_FILT[3:0] cycles.
7	DWC_EN_VS1	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
6	DWC_EN_VS2	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
5	DWC_EN_VS3	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
4	DWC_EN_VS4	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled

Table 6-97. DWC_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DWC_EN_VS5	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
2	DWC_EN_VS6	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
1	DWC_EN_VS7	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
0	DWC_EN_VS8	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled

6.6.3.23 DWC_TH_VS8 Register (Address = 0x22) [Reset = 0xFF00]

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Figure 6-92. DWC_TH_VS8 Register

15	14	13	12	11	10	9	8
HIGH_TH_VS8[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_VS8[7:0]							
R/W-00000000b							

Table 6-98. DWC_TH_VS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_VS8[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_VS8[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.3.24 DWC_TH_VS7 Register (Address = 0x23) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-93. DWC_TH_VS7 Register

15	14	13	12	11	10	9	8
HIGH_TH_VS7[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_VS7[7:0]							
R/W-00000000b							

Table 6-99. DWC_TH_VS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_VS7[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_VS7[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.3.25 DWC_TH_VS6 Register (Address = 0x24) [Reset = 0xFF00]

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Figure 6-94. DWC_TH_VS6 Register

15	14	13	12	11	10	9	8
HIGH_TH_VS6[7:0]							

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Figure 6-94. DWC_TH_VS6 Register (continued)

R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_VS6[7:0]							
R/W-00000000b							

Table 6-100. DWC_TH_VS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_VS6[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_VS6[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.3.26 DWC_TH_VS5 Register (Address = 0x25) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-95. DWC_TH_VS5 Register

15	14	13	12	11	10	9	8
HIGH_TH_VS5[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_VS5[7:0]							
R/W-00000000b							

Table 6-101. DWC_TH_VS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_VS5[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_VS5[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.3.27 DWC_TH_VS4 Register (Address = 0x26) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-96. DWC_TH_VS4 Register

15	14	13	12	11	10	9	8
HIGH_TH_VS4[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_VS4[7:0]							
R/W-00000000b							

Table 6-102. DWC_TH_VS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_VS4[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_VS4[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.3.28 DWC_TH_VS3 Register (Address = 0x27) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-97. DWC_TH_VS3 Register

15	14	13	12	11	10	9	8

Figure 6-97. DWC_TH_VS3 Register (continued)

HIGH_TH_VS3[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_VS3[7:0]							
R/W-00000000b							

Table 6-103. DWC_TH_VS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_VS3[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_VS3[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.3.29 DWC_TH_VS2 Register (Address = 0x28) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-98. DWC_TH_VS2 Register

15	14	13	12	11	10	9	8
HIGH_TH_VS2[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_VS2[7:0]							
R/W-00000000b							

Table 6-104. DWC_TH_VS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_VS2[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_VS2[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.3.30 DWC_TH_VS1 Register (Address = 0x29) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-99. DWC_TH_VS1 Register

15	14	13	12	11	10	9	8
HIGH_TH_VS1[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_VS1[7:0]							
R/W-00000000b							

Table 6-105. DWC_TH_VS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_VS1[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_VS1[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

6.6.3.31 DWC_HYS_VS7_8 Register (Address = 0x2A) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-100. DWC_HYS_VS7_8 Register

15	14	13	12	11	10	9	8
HYS_VS8[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
HYS_VS7[7:0]							
R/W-00000000b							

Table 6-106. DWC_HYS_VS7_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_VS8[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.
7:0	HYS_VS7[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

6.6.3.32 DWC_HYS_VS5_6 Register (Address = 0x2B) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-101. DWC_HYS_VS5_6 Register

15	14	13	12	11	10	9	8
HYS_VS6[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_VS5[7:0]							
R/W-00000000b							

Table 6-107. DWC_HYS_VS5_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_VS6[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds.
7:0	HYS_VS5[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

6.6.3.33 DWC_HYS_VS3_4 Register (Address = 0x2C) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-102. DWC_HYS_VS3_4 Register

15	14	13	12	11	10	9	8
HYS_VS4[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_VS3[7:0]							
R/W-00000000b							

Table 6-108. DWC_HYS_VS3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_VS4[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds.
7:0	HYS_VS3[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

6.6.3.34 DWC_HYS_VS1_2 Register (Address = 0x2D) [Reset = 0xFF00]

Return to the Summary Table.

Figure 6-103. DWC_HYS_VS1_2 Register

15	14	13	12	11	10	9	8
HYS_VS2[7:0]							
R/W-11111111b							

Figure 6-103. DWC_HYS_VS1_2 Register (continued)

7	6	5	4	3	2	1	0
HYS_VS1[7:0]							
R/W-00000000b							

Table 6-109. DWC_HYS_VS1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_VS2[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds.
7:0	HYS_VS1[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

6.6.3.35 TP_CFG Register (Address = 0x2E) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-104. TP_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000b							
7	6	5	4	3	2	1	0
RESERVED	TP_MODE[2:0]			RESERVED	TP_DIS_IDX	TP_UP_DN_EN	TP_EN
R/W-000000000b	R/W-000b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 6-110. TP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED	R/W	000000000b	Reserved. Do not change from the default reset value.
6:4	TP_MODE[2:0]	R/W	000b	Test pattern mode selection. 000b = Constant pattern 001b = Reserved 010b = Ramp pattern 011b = Reserved 100b = Reserved 101b = Reserved
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2	TP_DIS_IDX	R/W	0b	When set to 1b, channel index insertion in test pattern is disabled.
1	TP_UP_DN_EN	R/W	0b	Test pattern increment mode. 0b = Increment happens at channel frame boundary. 1b = Increment happens at every CONVST.
0	TP_EN	R/W	0b	Test pattern enable for VS1 to VS8. 0b = ADC conversion result is launched on the data interface 1b = Digital test pattern is launched on the data interface

6.6.3.36 TP_VS8 Register (Address = 0x2F) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-105. TP_VS8 Register

15	14	13	12	11	10	9	8
TP_VS8[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_VS8[15:0]							
R/W-0000000000000000b							

Table 6-111. TP_VS8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_VS8[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for VS8.

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6.6.3.37 TP_VS7 Register (Address = 0x30) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-106. TP_VS7 Register

15	14	13	12	11	10	9	8
TP_VS7[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_VS7[15:0]							
R/W-0000000000000000b							

Table 6-112. TP_VS7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_VS7[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for VS7.

6.6.3.38 TP_VS6 Register (Address = 0x31) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-107. TP_VS6 Register

15	14	13	12	11	10	9	8
TP_VS6[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_VS6[15:0]							
R/W-0000000000000000b							

Table 6-113. TP_VS6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_VS6[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for VS6.

6.6.3.39 TP_VS5 Register (Address = 0x32) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-108. TP_VS5 Register

15	14	13	12	11	10	9	8
TP_VS5[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_VS5[15:0]							
R/W-0000000000000000b							

Table 6-114. TP_VS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_VS5[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for VS5.

6.6.3.40 TP_VS4 Register (Address = 0x33) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-109. TP_VS4 Register

15	14	13	12	11	10	9	8

Figure 6-109. TP_VS4 Register (continued)

TP_VS4[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_VS4[15:0]							
R/W-0000000000000000b							

Table 6-115. TP_VS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_VS4[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for VS4.

6.6.3.41 TP_VS3 Register (Address = 0x34) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-110. TP_VS3 Register

15	14	13	12	11	10	9	8
TP_VS3[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_VS3[15:0]							
R/W-0000000000000000b							

Table 6-116. TP_VS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_VS3[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for VS3.

6.6.3.42 TP_VS2 Register (Address = 0x35) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-111. TP_VS2 Register

15	14	13	12	11	10	9	8
TP_VS2[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_VS2[15:0]							
R/W-0000000000000000b							

Table 6-117. TP_VS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_VS2[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for VS2.

6.6.3.43 TP_VS1 Register (Address = 0x36) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-112. TP_VS1 Register

15	14	13	12	11	10	9	8
TP_VS1[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0

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Figure 6-112. TP_VS1 Register (continued)

TP_VS1[15:0]
R/W-0000000000000000b

Table 6-118. TP_VS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_VS1[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for VS1.

6.6.3.44 GEN_CFG1 Register (Address = 0x37) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-113. GEN_CFG1 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000000000b							
7	6	5	4	3	2	1	0
RESERVED						OFS_CORR_EN	GAN_CORR_EN
R/W-00000000000000b						R/W-0b	R/W-0b

Table 6-119. GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	R/W	00000000000000b	Reserved. Do not change from the default reset value.
1	OFS_CORR_EN	R/W	0b	Offset correction enable for VS 1 to VS8. 0b = Disabled 1b = Enabled
0	GAN_CORR_EN	R/W	0b	Gain correction enable for VS 1 to VS8. 0b = Disabled 1b = Enabled

6.6.3.45 DWC_FLAG_VS1_8 Register (Address = 0x3E) [Reset = 0x0000]

Return to the Summary Table.

Figure 6-114. DWC_FLAG_VS1_8 Register

15	14	13	12	11	10	9	8
HIGH_FLAG_VS1	HIGH_FLAG_VS2	HIGH_FLAG_VS3	HIGH_FLAG_VS4	HIGH_FLAG_VS5	HIGH_FLAG_VS6	HIGH_FLAG_VS7	HIGH_FLAG_VS8
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b
7	6	5	4	3	2	1	0
LOW_FLAG_VS1	LOW_FLAG_VS2	LOW_FLAG_VS3	LOW_FLAG_VS4	LOW_FLAG_VS5	LOW_FLAG_VS6	LOW_FLAG_VS7	LOW_FLAG_VS8
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 6-120. DWC_FLAG_VS1_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	HIGH_FLAG_VS1	R	0b	Digital window comparator high flag for VS1.
14	HIGH_FLAG_VS2	R	0b	Digital window comparator high flag for VS2.
13	HIGH_FLAG_VS3	R	0b	Digital window comparator high flag for VS3.
12	HIGH_FLAG_VS4	R	0b	Digital window comparator high flag for VS4.
11	HIGH_FLAG_VS5	R	0b	Digital window comparator high flag for VS5.
10	HIGH_FLAG_VS6	R	0b	Digital window comparator high flag for VS6.
9	HIGH_FLAG_VS7	R	0b	Digital window comparator high flag for VS7.
8	HIGH_FLAG_VS8	R	0b	Digital window comparator high flag for VS8.
7	LOW_FLAG_VS1	R	0b	Digital window comparator low flag for VS1.
6	LOW_FLAG_VS2	R	0b	Digital window comparator low flag for VS2.
5	LOW_FLAG_VS3	R	0b	Digital window comparator low flag for VS3.

Table 6-120. DWC_FLAG_VS1_8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	LOW_FLAG_VS4	R	0b	Digital window comparator low flag for VS4.
3	LOW_FLAG_VS5	R	0b	Digital window comparator low flag for VS5.
2	LOW_FLAG_VS6	R	0b	Digital window comparator low flag for VS6.
1	LOW_FLAG_VS7	R	0b	Digital window comparator low flag for VS7.
0	LOW_FLAG_VS8	R	0b	Digital window comparator low flag for VS8.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application

7.1.1 Multichannel Lithium-ion cell formation and test

After the cell assembly process, each Li-ion battery goes through gradual charging, during which it forms a solid electrolyte interphase (SEI) layer, which is critical for its long-term functionality. If this process is not well controlled, the battery can lose up to 50% of its capacity. Therefore, test equipment must provide precise constant-current and constant-voltage charging and discharging to control the thickness of the SEI layer. This can bring down capacity losses to below 5%.

Figure 7-1 shows application schematic using the ADS93x8V8I. The ADS93x8V8I enables solution for 8-cell battery formation and testing applications, providing simultaneous, high-precision monitoring of all battery cells in real-time. With 8 dedicated voltage channels and 8 current channels, this 24-bit ADC enables comprehensive characterization of each cell during charge/discharge cycles at 125kSPS per channel. The integrated zero-drift programmable gain amplifiers deliver ±0.01% full-scale current measurement accuracy, critical for precise battery testing and quality control. The device no-cycle-latency architecture enable immediate fault detection and fast closed-loop control, essential for protecting cells against over-current, over-voltage, or thermal events during formation cycles. Multiple configurable input ranges accommodate various shunt resistor configurations and cell voltage levels, while the 140dB common-mode rejection ratio ensures accurate high-side current sensing. By integrating 8 instrumentation amplifiers, 8 difference amplifiers, and a 16-channel SAR ADC in a single 8mm x 8mm package, the ADS9308V8I significantly reduces BOM cost, simplifies PCB layout, and enables compact automated battery test equipment design.

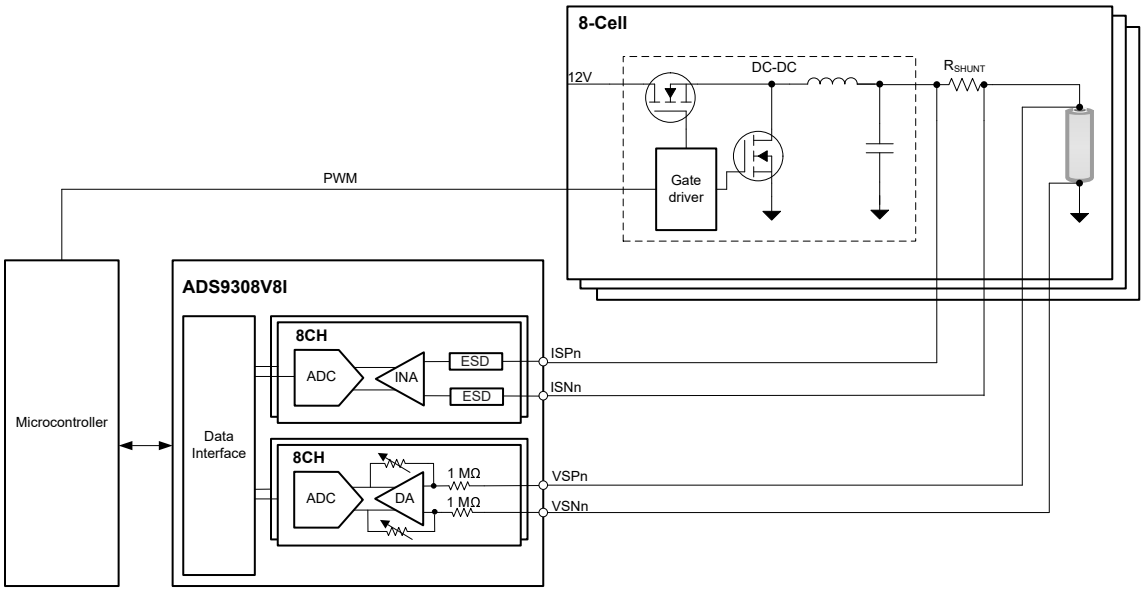


Figure 7-1. Multichannel Battery Cell Testing using the ADS9308V8I

7.2 Power Supply Recommendations

The ADS93x8V8I has three separate power supplies: AVDD_5V, AVDD_1V8, and IOVDD. There is no requirement for a specific power-up sequence. IOVDD powers the digital IOVDD. When using a 1.8V rail for IOVDD, AVDD_1V8 can be shorted with IOVDD with a 100Ω ferrite bead. Figure 7-2 illustrates the decoupling capacitor connections for the respective power supplies. Make sure each power-supply pin has separate 0.1µF decoupling capacitors.

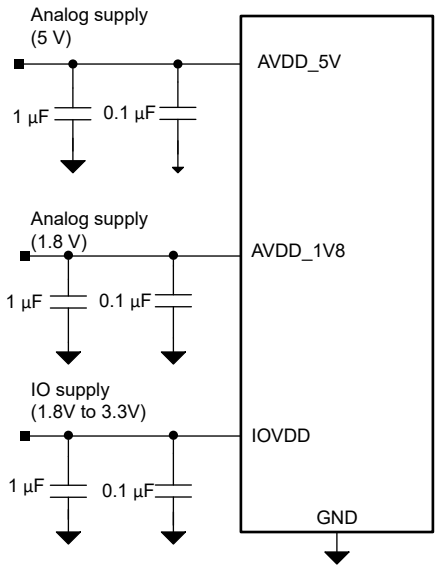


Figure 7-2. Power-Supply Decoupling

7.3 Layout

7.3.1 Layout Guidelines

Figure 7-3 illustrates a board layout example for the ADS9308V8I. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources.

For best performance, filter the internal reference noise by connecting a 4.7µF ceramic bypass capacitor to the REFIO pin, and connect 1µF ceramic capacitors directly between REFCAPA and REFM pins, and between the REFCAPB and REFM pins. Place 1µF reference decoupling capacitors close to the device REFCAP and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

Use 0.1µF ceramic bypass capacitors in close proximity to the AVDD_5V, AVDD_1V8, and IOVDD power-supply pins. Avoid placing vias between the power-supply pins and the bypass capacitors.

ADVANCE INFORMATION

7.3.2 Layout Example

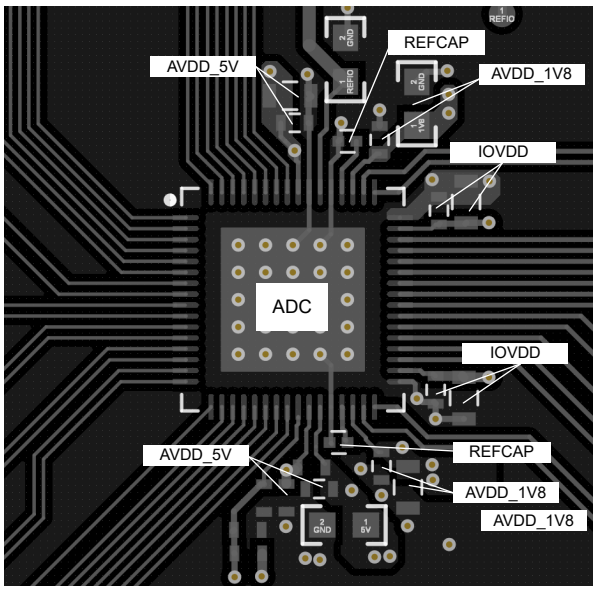


Figure 7-3. Example Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* datasheet
- Texas Instruments, *AN-2029 Handling & Process Recommendations* application note

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

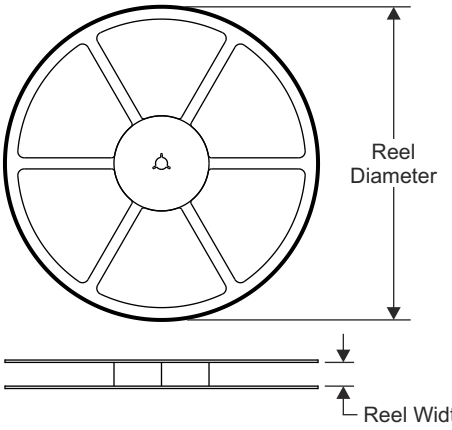
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

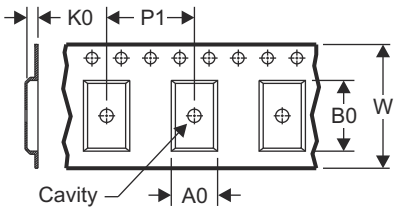
ADVANCE INFORMATION

10.1 Tape and Reel Information

REEL DIMENSIONS

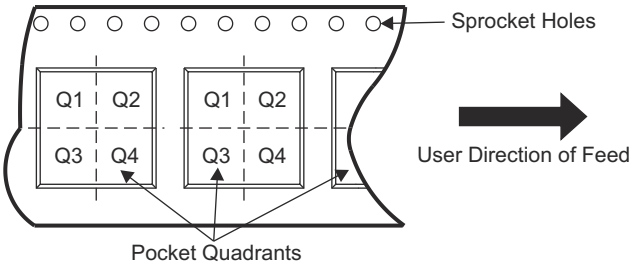


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

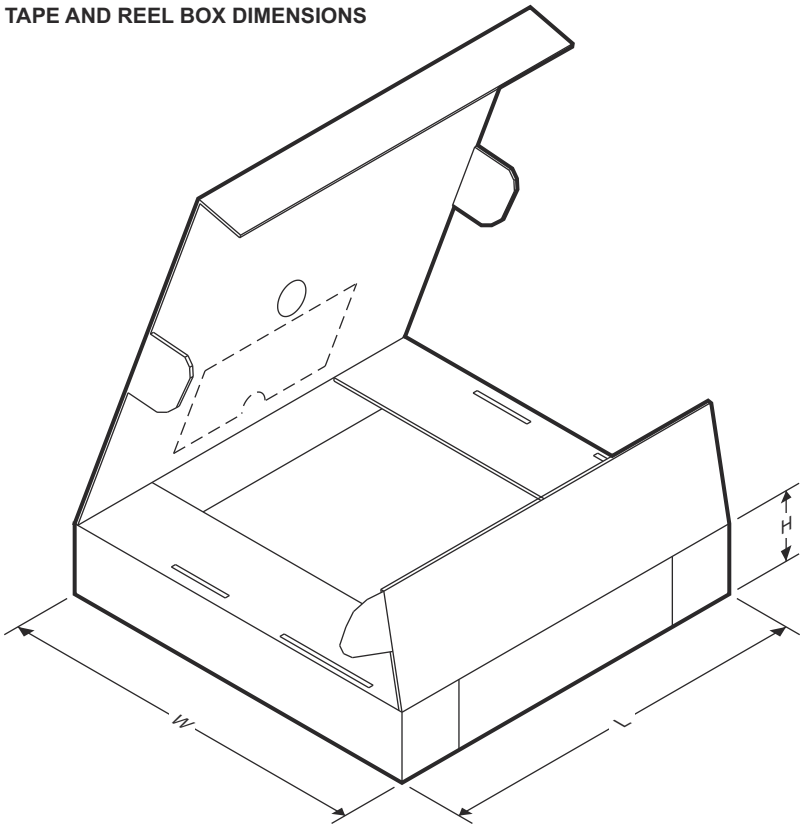
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
P9308V8IRSKR	VQFN	RSK	64	3500	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS

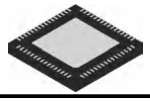


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
P9308V8IRSKR	VQFN	RSK	64	3500	360.0	360.0	36.0

ADVANCE INFORMATION

10.2 Mechanical Data

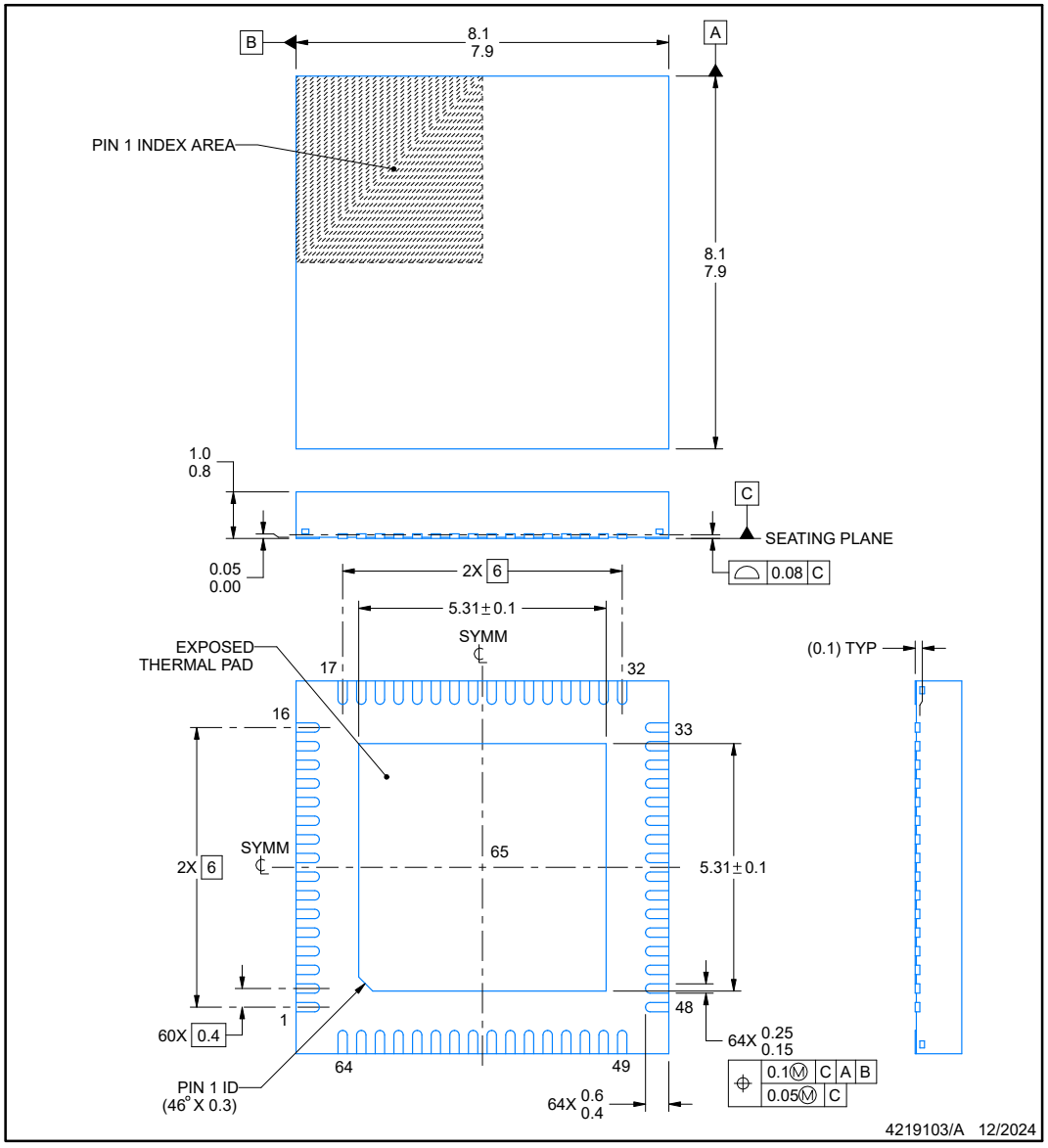
RSK0064B



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



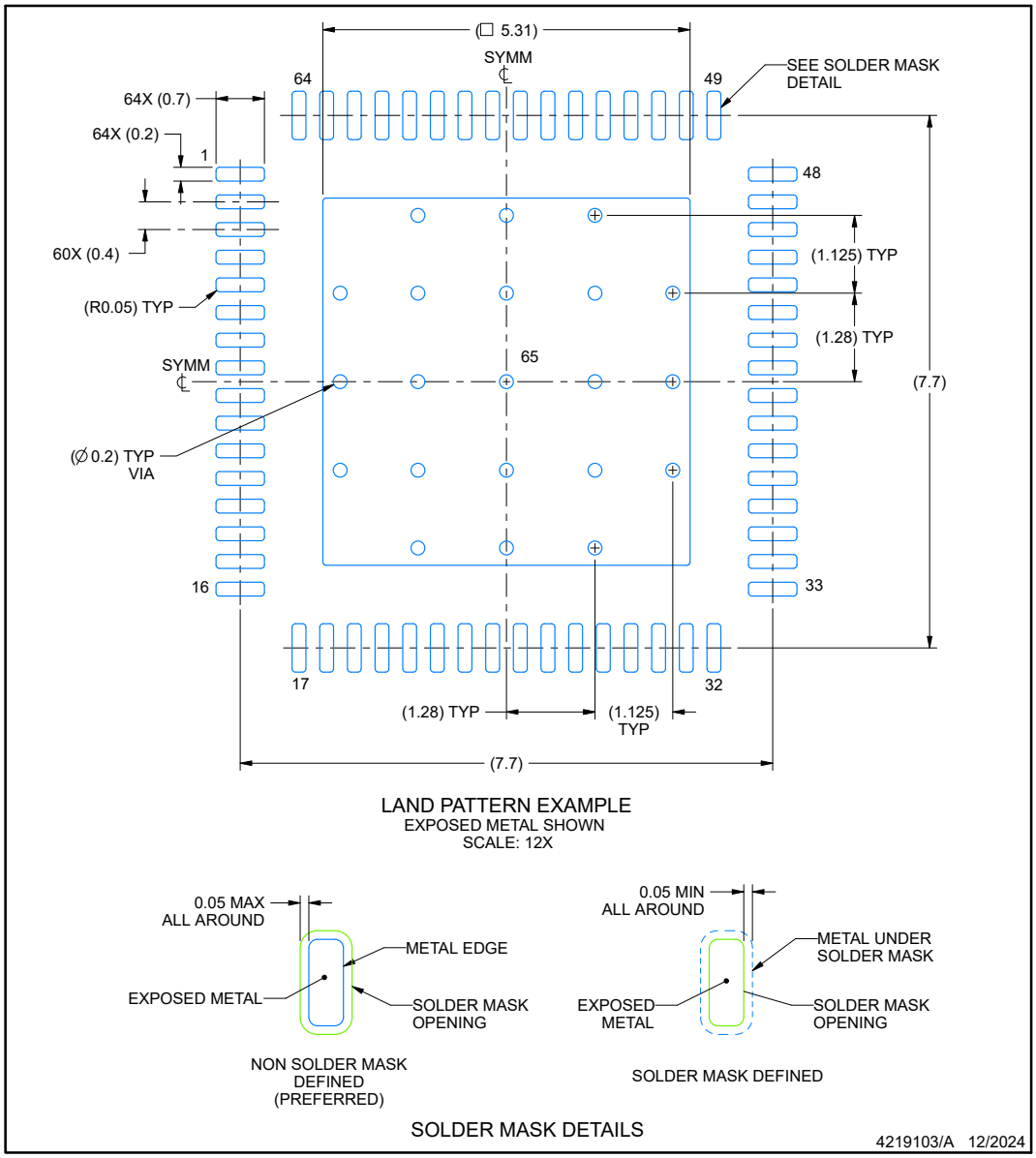
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RSK0064B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

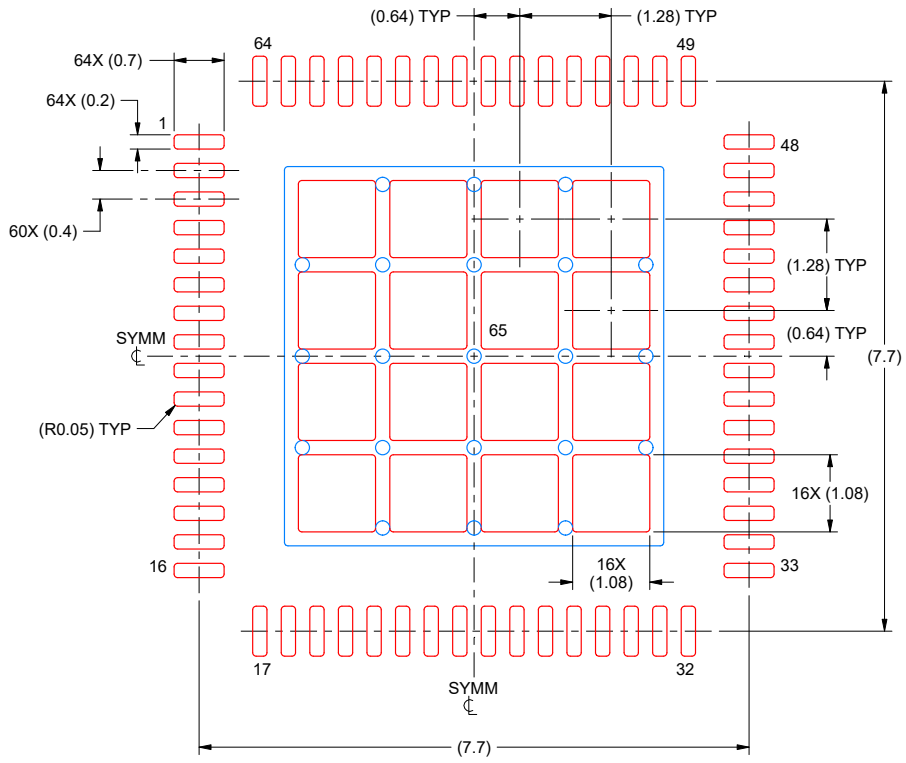
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RSK0064B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 65
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219103/A 12/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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