

AFEx3004W 10-Bit, 12-Bit, Quad Voltage and Current Output, 10-Bit ADC, Smart AFEs in DSBGA Package

1 Features

- Programmable voltage or current outputs with flexible configuration:
 - Voltage outputs:
 - 1LSB DNL
 - Gains of 1 ×, 1.5 ×, 2 ×, 3 ×, and 4 ×
 - Current outputs:
 - 1LSB INL and DNL (8-bit)
 - Unipolar and bipolar output range options from 25µA to 250µA
- 10-bit ADC input
 - 2LSB INL, 1LSB DNL
- Programmable comparator mode for all channels
- High-impedance output when VDD is off
- High-impedance or resistive pull-down power-down modes
- 50MHz SPI-compatible interface
- Automatically detects I²C, SPI, or PMBus® Interface
 - 1.62V V_{IH} with V_{DD} = 5.5V
- General-purpose input/output (GPIO) configurable to multiple functions
- Predefined waveform generation: sine wave, triangular, sawtooth
- User-programmable nonvolatile memory (NVM)
- Internal, external, or power-supply as reference
- Wide operating range:
 - Power supply: 1.8V to 5.5V
 - Temperature range: –40°C to +125°C
- Tiny package: 16-pin DSBGA (1.76mm × 1.76mm)

2 Applications

- [Optical module](#)
- [Standard notebook PC](#)

3 Description

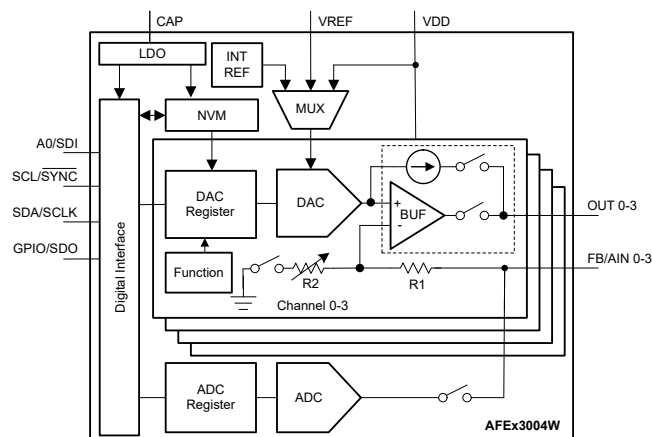
The 10-bit AFE53004W and 12-bit AFE63004W (AFEx3004W) is a family of 4-channel, ultra-low power smart analog-front-end (AFE) devices. These devices feature one shared 10-bit analog-to-digital converter (ADC) with four independent channels. Each channel is independently configurable as a buffered voltage output digital-to-analog converter (DAC), programmable current output DAC, or an input to the shared ADC. The devices support Hi-Z power-down mode and Hi-Z output during power-off conditions. The analog outputs provide a force-sense option for use as a programmable comparator and current sink. The multifunction GPIO, function generation, and NVM enable these smart AFEs for *processor-less* applications and design reuse. These devices automatically detect I²C, PMBus, and SPI, and contain an internal reference.

The flexibility and the feature set of the smart AFE combined with tiny package and ultra low-operating power make these devices an excellent choice for small, battery-operated systems.

Device Information

PART NUMBER	RESOLUTION	PACKAGE ⁽¹⁾
AFE53004W	10-bit	YBH (DSBGA, 16)
AFE63004W	12-bit	

(1) For more information, see [Section 11](#).



Simplified Block Diagram



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4 Pin Configuration and Functions

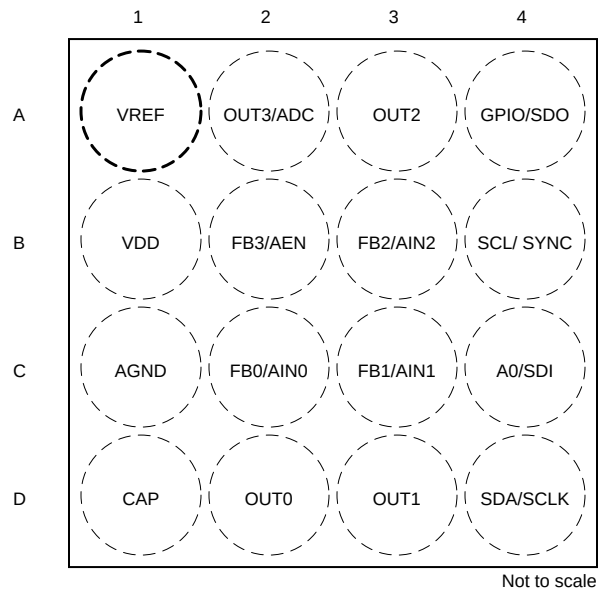


Figure 4-1. YBH Package, 16-Pin DSBGA (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	VREF	Power	External reference input. Connect a capacitor (approximately 0.1µF) between VREF and AGND. Use a pullup resistor to VDD when the external reference is not used. Do not ramp up this pin before VDD. If an external reference is used, ensure that the reference ramps up after VDD.
A2	OUT3/ADC	Output	Analog output from DAC channel 3 in voltage- or current-output mode. Input to ADC channel 3 in ADC mode.
A3	OUT2	Output	Analog output from DAC channel 2. Not connected in ADC mode; leave floating.
A4	GPIO/SDO	Input/ Output	General-purpose input/output configurable as LDAC, PD, PROTECT, RESET, SDO, and STATUS. For STATUS and SDO, connect the pin to the IO voltage with an external pullup resistor. If unused, connect the GPIO pin to VDD or AGND using an external resistor. This pin is able to ramp up before VDD.
B1	VDD	Power	Supply voltage.
B2	FB3/AEN	Input	Voltage feedback pin for channel 3. In voltage-output mode, connect to OUT3 for closed-loop amplifier output. In current-output mode, keep the FB3 pin unconnected to minimize leakage current. In ADC mode, connect to VDD with a pullup resistor.
B3	FB2/AIN2	Input	Voltage feedback pin for channel 2. In voltage-output mode, connect to OUT2 for closed-loop amplifier output. In current-output mode, keep the FB2 pin unconnected to minimize leakage current. In ADC mode, input to ADC channel 2.
B4	SCL/ SYNC	Output	I ² C serial interface clock or SPI chip select input. Connect this to the IO voltage using an external pullup resistor. This pin is able to ramp up before VDD.
C1	AGND	Ground	Ground reference point for all circuitry on the device.
C2	FB0/AIN0	Input	Voltage feedback pin for channel 0. In voltage-output mode, connect to OUT0 for closed-loop amplifier output. In current-output mode, keep the FB0 pin unconnected to minimize leakage current. In ADC mode, input to ADC channel 0.
C3	FB1/AIN1	Input	Voltage feedback pin for channel 1. In voltage-output mode, connect to OUT1 for closed-loop amplifier output. In current-output mode, keep the FB1 pin unconnected to minimize leakage current. In ADC mode, input to ADC channel 1.
C4	A0/SDI	Input	Address configuration pin for I ² C or serial data input for SPI. For A0, connect this pin to VDD, AGND, SDA, or SCL for address configuration (Section 6.5.2.2.1). For SDI, this pin need not be pulled up or pulled down. This pin is able to ramp up before VDD.
D1	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5µF) between CAP and AGND.
D2	OUT0	Output	Analog output from DAC channel 0. Not connected in ADC mode; leave floating.
D3	OUT1	Output	Analog output from DAC channel 1. Not connected in ADC mode; leave floating.
D4	SDA/SCLK	Input/ Output	Bidirectional I ² C serial data bus or SPI clock input. Connect this pinto the IO voltage using an external pullup resistor in I ² C mode. This pin is able to ramp up before VDD.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage, V _{DD} to AGND	−0.3	6	V
	Digital inputs to AGND	−0.3	V _{DD} + 0.3	V
	V _{OUTX} or A _{INX} or V _{FBX} to AGND	−0.3	V _{DD} + 0.3	V
V _{REF}	External reference, V _{REF} to AGND	−0.3	V _{DD} + 0.3	V
	Current into any pin except the OUTx, VDD, and AGND pins	−10	10	mA
T _J	Junction temperature	−40	150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Positive supply voltage to ground (AGND)	1.7		5.5	V
V _{REF}	External reference to ground (AGND)	1.7		V _{DD}	V
V _{IH}	Digital input high voltage, 1.7V < V _{DD} ≤ 5.5V	1.62			V
V _{IL}	Digital input low voltage			0.4	V
C _{CAP}	External capacitor on CAP pin	0.5		15	μF
T _A	Ambient temperature	−40		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AFE53004W	UNIT
		YBH (DSBGA)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	81.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	20.3	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	20.3	°C/W

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

5.5 Electrical Characteristics, Voltage Output

all minimum and maximum values at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and typical values at $T_A = 25^{\circ}\text{C}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, DAC reference tied to V_{DD} , gain = 1 \times , DAC output pin (OUT) loaded with resistive load ($R_L = 5\text{k}\Omega$ to AGND) and capacitive load ($C_L = 200\text{pF}$ to AGND), and digital inputs at V_{DD} or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	AFE63004W	12			Bits
		AFE53004W	10			
INL	Integral nonlinearity ⁽¹⁾	AFE63004W	–5		5	LSB
		AFE53004W	–1.25		1.25	
DNL	Differential nonlinearity ⁽¹⁾		–1		1	LSB
	Zero-code error ⁽⁴⁾	Code 0d into DAC, external reference, $V_{DD} = 5.5\text{V}$		6	12	mV
		Code 0d into DAC, internal V_{REF} , gain = 4 \times , $V_{DD} = 5.5\text{V}$		6	15	
	Zero-code error temperature coefficient ⁽⁴⁾			± 10		$\mu\text{V}/^{\circ}\text{C}$
	Offset error ^{(4) (6)}	$1.7\text{V} \leq V_{DD} < 2.7\text{V}$, V_{FB} pin shorted to V_{OUT} , DAC code: 32d for 12-bit resolution	–0.75	0.3	0.75	%FSR
		$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, V_{FB} pin shorted to V_{OUT} , DAC code: 32d for 12-bit resolution	–0.5	0.25	0.5	
	Offset-error temperature coefficient ⁽⁴⁾	V_{FB} pin shorted to V_{OUT} , DAC code: 32d for 12-bit resolution, 8d for 10-bit resolution		± 0.0003		%FSR/ $^{\circ}\text{C}$
	Gain error ⁽⁴⁾	Between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution	–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient ⁽⁴⁾	Between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution		± 0.0008		%FSR/ $^{\circ}\text{C}$
	Full-scale error ^{(4) (6)}	$1.7\text{V} \leq V_{DD} < 2.7\text{V}$, DAC at full-scale	–1		1	%FSR
		$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, DAC at full-scale	–0.5		0.5	
	Full-scale-error temperature coefficient ⁽⁴⁾	DAC at full-scale		± 0.0008		%FSR/ $^{\circ}\text{C}$
OUTPUT						
	Output voltage	Reference tied to V_{DD}	0		V_{DD}	V
C_L	Capacitive load ⁽²⁾	$R_L = \text{infinite}$, phase margin = 30°			200	pF
		Phase margin = 30°			1000	
	Short-circuit current	$V_{DD} = 1.7\text{V}$, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		15		mA
		$V_{DD} = 2.7\text{V}$, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		50		
		$V_{DD} = 5.5\text{V}$, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		60		
	Output-voltage headroom ⁽²⁾	To V_{DD} (DAC output unloaded, internal reference = 1.21V), $V_{DD} \geq 1.21\text{V} \times \text{gain} + 0.2\text{V}$	0.2			V
		To V_{DD} and to AGND (DAC output unloaded, external reference at V_{DD} (gain = 1 \times), the V_{REF} pin is not shorted to V_{DD})	0.8			
		To V_{DD} and to AGND ($I_{LOAD} = 10\text{mA}$ at $V_{DD} = 5.5\text{V}$, $I_{LOAD} = 3\text{mA}$ at $V_{DD} = 2.7\text{V}$, $I_{LOAD} = 1\text{mA}$ at $V_{DD} = 1.8\text{V}$), external reference at V_{DD} (gain = 1 \times), the V_{REF} pin is not shorted to V_{DD})	10			
Z_O	V_{FB} dc output impedance ⁽³⁾	DAC output enabled, internal reference (gain = 1.5 \times or 2 \times) or external reference at V_{DD} (gain = 1 \times), the V_{REF} pin is not shorted to V_{DD}	400	500	600	k Ω
		DAC output enabled, internal V_{REF} , gain = 3 \times or 4 \times	325	400	485	

5.5 Electrical Characteristics, Voltage Output (continued)

all minimum and maximum values at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and typical values at $T_A = 25^{\circ}\text{C}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, DAC reference tied to VDD, gain = 1 \times , DAC output pin (OUT) loaded with resistive load ($R_L = 5\text{k}\Omega$ to AGND) and capacitive load ($C_L = 200\text{pF}$ to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio (dc)	Internal V_{REF} , gain = 2 \times , DAC at midscale, $V_{DD} = 5\text{V} \pm 10\%$		0.25		mV/V
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, $V_{DD} = 5.5\text{V}$		20		μs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, $V_{DD} = 5.5\text{V}$, internal V_{REF} , gain = 4 \times		25		
	Slew rate	$V_{DD} = 5.5\text{V}$		0.3		V/ μs
	Power-on glitch magnitude	At start-up (DAC output disabled)		75		mV
		At start-up (DAC output disabled), $R_L = 100\text{k}\Omega$		200		
	Output-enable glitch magnitude	DAC output disabled to enabled (DAC registers at zero scale), $R_L = 100\text{k}\Omega$		250		mV
V_n	Output noise voltage (peak to peak)	$f = 0.1\text{Hz}$ to 10Hz , DAC at midscale, $V_{DD} = 5.5\text{V}$		50		μV_{PP}
		Internal V_{REF} , gain = 4 \times , $f = 0.1\text{Hz}$ to 10Hz , DAC at midscale, $V_{DD} = 5.5\text{V}$		90		
	Output noise density	$f = 1\text{kHz}$, DAC at midscale, $V_{DD} = 5.5\text{V}$		0.35		$\mu\text{V}/\sqrt{\text{Hz}}$
		Internal V_{REF} , gain = 4 \times , $f = 1\text{kHz}$, DAC at midscale, $V_{DD} = 5.5\text{V}$		0.9		
	Power supply rejection ratio (ac) ⁽³⁾	Internal V_{REF} , gain = 4 \times , 200mV 50Hz or 60Hz sine wave superimposed on power supply voltage, DAC at midscale		-68		dB
	Code change glitch impulse	$\pm 1\text{LSB}$ change around midscale (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	$\pm 1\text{LSB}$ change around midscale (including feedthrough)		15		mV
POWER						
I_{DD}	Current flowing into VDD ^{(4) (5)}	Normal operation, DACs at full scale, digital pins static, external reference at V_{DD} but the V_{REF} pin is not shorted to V_{DD}		35	50	$\mu\text{A}/\text{ch}$

(1) Measured with DAC output unloaded. For external reference and internal reference $V_{DD} \geq 1.21 \times \text{gain} + 0.2\text{V}$, between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution.

(2) Specified by design and characterization, not production tested.

(3) Specified with 200mV headroom with respect to reference value when internal reference is used.

(4) Measured with DAC output unloaded.

(5) The total power consumption is calculated by $I_{DD} \times (\text{total number of channels powered on}) + (\text{sleep-mode current})$.

(6) When a DAC channel is configured in IOUT mode for long term and then switched to VOUT mode, the VOUT mode can show parametric drift.

5.6 Electrical Characteristics, Current Output

all minimum and maximum values at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ and typical values at $T_A = 25^\circ\text{C}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, $\pm 250\mu\text{A}$ output range, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		8			Bits
INL	Integral nonlinearity	DAC codes between 0d and 255d	–1		1	LSB
DNL	Differential nonlinearity	DAC codes between 0d and 255d	–1		1	LSB
	Offset error	DAC output ranges: $\pm 25\mu\text{A}$, $\pm 50\mu\text{A}$, $\pm 125\mu\text{A}$, and $\pm 250\mu\text{A}$; DAC at midscale		± 1		%FSR
	Gain error	DAC output ranges: $\pm 25\mu\text{A}$, $\pm 50\mu\text{A}$, $\pm 125\mu\text{A}$, and $\pm 250\mu\text{A}$; DAC codes between 0d and 255d		± 1.3		%FSR
OUTPUT						
	Output compliance voltage ⁽¹⁾	DAC output ranges: $\pm 25\mu\text{A}$, $\pm 50\mu\text{A}$, $\pm 125\mu\text{A}$, and $\pm 250\mu\text{A}$; to V_{DD} and to AGND	400			mV
Z_O	I_{OUT} dc output impedance ⁽²⁾	DAC at midscale, DAC output kept at $V_{DD}/2$	60			M Ω
	Power supply rejection ratio (dc)	DAC at midscale, all bipolar ranges, V_{DD} changed from 4.5V to 5.5V		0.23		LSB/V
DYNAMIC PERFORMANCE						
t_{sett}	Output current settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 1 LSB at 8-bit resolution, $V_{DD} = 5.5\text{V}$, common-mode voltage at OUTx pin is $V_{DD}/2$		60		μs
V_n	Output noise current (peak to peak)	0.1Hz to 10Hz, DAC at midscale, $V_{DD} = 5.5\text{V}$, $\pm 250\mu\text{A}$ output range		150		nA _{pp}
	Output noise density	$f = 1\text{kHz}$, DAC at midscale, $V_{DD} = 5.5\text{V}$, $\pm 250\mu\text{A}$ output range		1		nA/ $\sqrt{\text{Hz}}$
	Power supply rejection ratio (ac) ⁽³⁾	$\pm 250\mu\text{A}$ output range, 200mV 50Hz or 60Hz sine wave superimposed on power-supply voltage, DAC at midscale		0.65		LSB/V
POWER						
I_{DD}	Current flowing into VDD ^{(3) (4)}	Normal operation, DACs at full scale, $\pm 25\mu\text{A}$ output range, digital pins static		42	50	$\mu\text{A}/\text{ch}$
		Normal operation, DACs at full scale, $\pm 50\mu\text{A}$ output range, digital pins static		56	70	
		Normal operation, DACs at full scale, $\pm 125\mu\text{A}$ output range, digital pins static		98	120	
		Normal operation, DACs at full scale, $\pm 250\mu\text{A}$ output range, digital pins static		167	200	

(1) Measured between DAC codes 0d and 255d.

(2) Specified by design and characterization, not production tested.

(3) The current flowing into V_{DD} does not account for the load current sourced or sunk on the OUTx pins. V_{REF} pin is connected to V_{DD} .

(4) The total power consumption is calculated by $I_{DD} \times (\text{total number of channels powered on}) + (\text{sleep-mode current})$.

5.7 Electrical Characteristics, Comparator Mode

all minimum and maximum values at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and typical values at $T_A = 25^{\circ}\text{C}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, DAC reference tied to VDD, gain = $1 \times$ in voltage output mode, DAC output pin (OUT) loaded with resistive load ($R_L = 5\text{k}\Omega$ to AGND) and capacitive load ($C_L = 200\text{pF}$ to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Offset error ^{(1) (2)}	$1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$; DAC at midscale, comparator input at Hi-Z, and DAC operating with external reference.	-6	0	6	mV
	Offset error time drift ⁽¹⁾	$V_{DD} = 5.5\text{V}$, external reference, $T_A = 125^{\circ}\text{C}$, FB in Hi-Z mode, DAC at full scale and V_{FB} at 0V or DAC at zero scale and V_{FB} at 1.84V, drift specified for 10 years of continuous operation		4		mV
OUTPUT						
	Input voltage	V_{REF} connected to V_{DD} , V_{FB} resistor network connected to ground	0		V_{DD}	V
		V_{REF} connected to V_{DD} , V_{FB} resistor network disconnected from ground	0	$V_{DD} \times (1/3 - 1/100)$		
V_{OL}	Logic low output voltage	$I_{LOAD} = 100\mu\text{A}$, output in open-drain mode		0.1		V
DYNAMIC PERFORMANCE						
t_{resp}	Output response time	DAC at midscale with 10-bit resolution, FB input at Hi-Z, and transition step at FB node is $(V_{DAC} - 2\text{LSB})$ to $(V_{DAC} + 2\text{LSB})$, transition time measured between 10% and 90% of output, output current of $100\mu\text{A}$, comparator output configured in push-pull mode, load capacitor at DAC output is 25pF		10		μs

(1) Specified by design and characterization, not production tested.

(2) This specification does not include the total unadjusted error (TUE) of the DAC.

5.8 Electrical Characteristics, ADC Input

all minimum and maximum values at $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ and typical values at $T_A = 25^{\circ}\text{C}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, reference tied to VDD, gain = $1 \times$, and digital inputs at VDD or AGND (unless otherwise noted) capacitive load ($C_L = 200\text{pF}$ to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		10			Bits
INL	Integral nonlinearity ^{(1) (2)}		-2		2	LSB
DNL	Differential nonlinearity ^{(1) (2)}		-1		1	LSB
	Offset error ^{(1) (2) (3)}	$1.7\text{V} \leq V_{DD} < 5.5\text{V}$	-5	0	+5	mV
		$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$	-5	0	+5	
	Gain error ^{(1) (2) (3)}		-1		1	%FSR
INPUT						
	Input voltage range	External $V_{REF} = V_{DD}$, V_{FB} attenuation is 1	0		V_{DD}	V
DYNAMIC PERFORMANCE						
	Data rate ⁽²⁾	ADC averaging setting is 4 samples	1406		2008	SPS
	Sampling capacitor			10		pF

(1) For external reference and internal reference $V_{DD} \geq 1.21 \times \text{gain} + 0.2\text{V}$, between end-point codes: 8d to 1016d for 10-bit resolution

(2) Specified by design and characterization, not production tested.

(3) Measured at analog input at mid-scale, Hi-Z input configuration, and with external reference.

5.9 Electrical Characteristics, General

all minimum and maximum values at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and typical values at $T_A = 25^{\circ}\text{C}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, DAC reference tied to VDD, gain = $1 \times$ in voltage output mode or $\pm 250\mu\text{A}$ output range in current output mode, DAC output pin (OUT) loaded with resistive load ($R_L = 5\text{k}\Omega$ to AGND) in voltage-output mode and capacitive load ($C_L = 200\text{pF}$ to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
	Initial accuracy	$T_A = 25^{\circ}\text{C}$	1.1979	1.212	1.224	V
	Reference output temperature coefficient ^{(1) (2)}				50	ppm/ $^{\circ}\text{C}$
EXTERNAL REFERENCE						
	V_{REF} input impedance ^{(1) (3)}			192		k Ω -ch
EEPROM						
	Endurance ⁽¹⁾	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		20000		Cycles
		$T_A = 125^{\circ}\text{C}$		1000		
	Data retention ⁽¹⁾	$T_A = 25^{\circ}\text{C}$		50		Years
	EEPROM programming write cycle time ⁽¹⁾				200	ms
	Device boot-up time ⁽¹⁾	Time taken from power valid ($V_{DD} \geq 1.7\text{V}$) to output valid state (output state as programmed in EEPROM), 0.5 μF capacitor on the CAP pin		5		ms
DIGITAL INPUTS						
	Digital feedthrough	Voltage output mode, DAC output static at midscale, fast mode plus, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER						
I_{DD}	Current flowing into VDD	Sleep mode, internal reference powered down, external reference at 5.5V			28	μA
I_{DD}	Current flowing into VDD ⁽¹⁾	Sleep mode, internal reference enabled, additional current through internal reference		10		μA
I_{DD}	Current flowing into VDD ⁽¹⁾	All channels enabled, internal reference enabled, additional current through internal reference per channel		12.5		μA
HIGH-IMPEDANCE OUTPUT						
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	DAC in Hi-Z output mode, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$		10		nA
		$V_{DD} = 0\text{V}$, $V_{OUT} \leq 1.5\text{V}$, decoupling capacitor between V_{DD} and AGND = 0.1 μF		200		nA
		$V_{DD} = 0\text{V}$, $1.5\text{V} < V_{OUT} \leq 5.5\text{V}$, decoupling capacitor between V_{DD} and AGND = 0.1 μF		500		nA
		100k Ω between V_{DD} and AGND, $V_{OUT} \leq 1.25\text{V}$, series resistance of 10k Ω at OUT pin		± 2		μA

(1) Specified by design and characterization, not production tested.

(2) Measured at -40°C and $+125^{\circ}\text{C}$ and calculated the slope.

(3) Impedances for the DAC channels are connected in parallel.

5.10 Timing Requirements, I²C Standard Mode

all input signals are timed from VIL to 70% of $V_{\text{pull-up}}$, $1.7\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, and $1.7\text{V} \leq V_{\text{pull-up}} \leq V_{\text{DD}}$

		MIN	NOM	MAX	UNIT
f _{SCL}	SCL frequency			100	kHz
t _{BUF}	Bus free time between stop and start conditions	4.7			μs
t _{HDSTA}	Hold time after repeated start	4			μs
t _{SUSTA}	Repeated start setup time	4.7			μs
t _{SUSTO}	Stop condition setup time	4			μs
t _{HDDAT}	Data hold time	0			ns
t _{SUDAT}	Data setup time	250			ns
t _{LOW}	SCL clock low period	4700			ns
t _{HIGH}	SCL clock high period	4000			ns
t _F	Clock and data fall time			300	ns
t _R	Clock and data rise time			1000	ns
t _{VDDAT}	Data valid time, R = 360Ω, C _{trace} = 23pF, C _{probe} = 10pF			3.45	μs
t _{VDACK}	Data valid acknowledge time, R = 360Ω, C _{trace} = 23pF, C _{probe} = 10pF			3.45	μs

5.11 Timing Requirements, I²C Fast Mode

all input signals are timed from VIL to 70% of $V_{\text{pull-up}}$, $1.7\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, and $1.7\text{V} \leq V_{\text{pull-up}} \leq V_{\text{DD}}$

		MIN	NOM	MAX	UNIT
f _{SCL}	SCL frequency			400	kHz
t _{BUF}	Bus free time between stop and start conditions	1.3			μs
t _{HDSTA}	Hold time after repeated start	0.6			μs
t _{SUSTA}	Repeated start setup time	0.6			μs
t _{SUSTO}	Stop condition setup time	0.6			μs
t _{HDDAT}	Data hold time	0			ns
t _{SUDAT}	Data setup time	100			ns
t _{LOW}	SCL clock low period	1300			ns
t _{HIGH}	SCL clock high period	600			ns
t _F	Clock and data fall time			300	ns
t _R	Clock and data rise time			300	ns
t _{VDDAT}	Data valid time, R = 360Ω, C _{trace} = 23pF, C _{probe} = 10pF			0.9	μs
t _{VDACK}	Data valid acknowledge time, R = 360Ω, C _{trace} = 23pF, C _{probe} = 10pF			0.9	μs

5.12 Timing Requirements, I²C Fast Mode Plus

all input signals are timed from VIL to 70% of $V_{\text{pull-up}}$, $1.7\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, and $1.7\text{V} \leq V_{\text{pull-up}} \leq V_{\text{DD}}$

		MIN	NOM	MAX	UNIT
f _{SCL}	SCL frequency			1	MHz
t _{BUF}	Bus free time between stop and start conditions	0.5			μs
t _{HDSTA}	Hold time after repeated start	0.26			μs
t _{SUSTA}	Repeated start setup time	0.26			μs
t _{SUSTO}	Stop condition setup time	0.26			μs
t _{HDDAT}	Data hold time	0			ns
t _{SUDAT}	Data setup time	50			ns
t _{LOW}	SCL clock low period	0.5			μs
t _{HIGH}	SCL clock high period	0.26			μs
t _F	Clock and data fall time			120	ns
t _R	Clock and data rise time			120	ns
t _{VDDAT}	Data valid time, R = 360Ω, C _{trace} = 23pF, C _{probe} = 10pF			0.45	μs
t _{VDACK}	Data valid acknowledge time, R = 360Ω, C _{trace} = 23pF, C _{probe} = 10pF			0.45	μs

5.13 Timing Requirements, SPI Write Operation

all input signals are specified with $t_r = t_f = 1\text{V/ns}$ (10% to 90% of V_{IO}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$, $1.7\text{V} \leq V_{IO} \leq 5.5\text{V}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			50	MHz
t_{SCLKHIGH}	SCLK high time	9			ns
t_{SCLKLOW}	SCLK low time	9			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{\text{CS}}$ to SCLK falling edge setup time	18			ns
t_{CSH}	SCLK falling edge to $\overline{\text{CS}}$ rising edge	10			ns
t_{CSHIGH}	$\overline{\text{CS}}$ high time	50			ns
t_{DACWAIT}	Sequential DAC update wait time (time between subsequent LDAC falling edges) for same channel	2			μs
$t_{\text{BCASTWAIT}}$	Broadcast DAC update wait time (time between subsequent LDAC falling edges)	2			μs

5.14 Timing Requirements, SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with $t_r = t_f = 1\text{V/ns}$ (10% to 90% of V_{IO}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$, $1.7\text{V} \leq V_{IO} \leq 5.5\text{V}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, and $\text{FSDO} = 0$

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			1.25	MHz
t_{SCLKHIGH}	SCLK high time	350			ns
t_{SCLKLOW}	SCLK low time	350			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	400			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	400			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	1			μs
t_{SDODLY}	SCLK rising edge to SDO falling edge, $I_{OL} \leq 5\text{mA}$, $C_L = 20\text{pF}$.			300	ns

5.15 Timing Requirements, SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with $t_r = t_f = 1\text{V/ns}$ (10% to 90% of V_{IO}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$, $1.7\text{V} \leq V_{IO} \leq 5.5\text{V}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, and $\text{FSDO} = 1$

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			2.5	MHz
t_{SCLKHIGH}	SCLK high time	175			ns
t_{SCLKLOW}	SCLK low time	175			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	300			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	300			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	1			μs
t_{SDODLY}	SCLK rising edge to SDO falling edge, $I_{OL} \leq 5\text{mA}$, $C_L = 20\text{pF}$.			300	ns

5.16 Timing Requirements, GPIO

all input signals are specified with $t_r = t_f = 1\text{V/ns}$ (10% to 90% of V_{IO}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$, $1.7\text{V} \leq V_{IO} \leq 5.5\text{V}$, $1.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

		MIN	NOM	MAX	UNIT
$t_{GPIHIGH}$	GPI high time	2			μs
t_{GPILOW}	GPI low time	2			μs
t_{GPAWGD}	$\overline{\text{LDAC}}$ falling edge to DAC update delay			2	μs
$t_{CS2LDAC}$	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	1			μs
$t_{STP2LDAC}$	I ² C stop bit rising edge to $\overline{\text{LDAC}}$ falling edge	1			μs
t_{LDACW}	$\overline{\text{LDAC}}$ low time	2			μs

5.17 Timing Diagrams

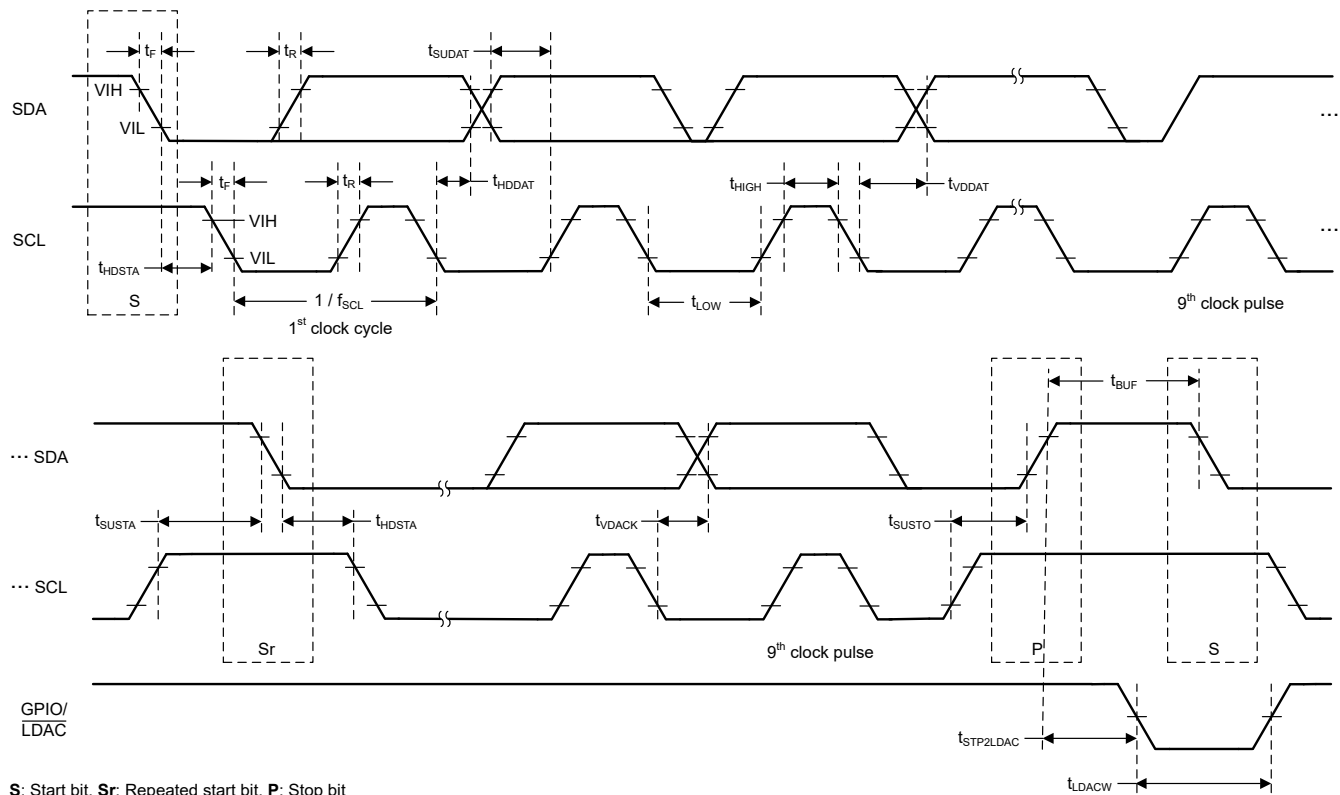


Figure 5-1. I²C Timing Diagram

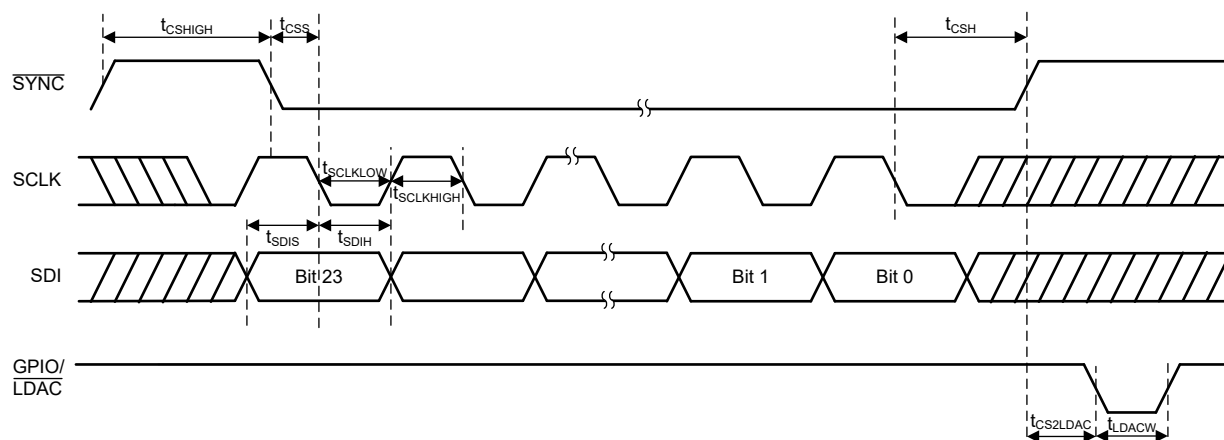


Figure 5-2. SPI Write Timing Diagram

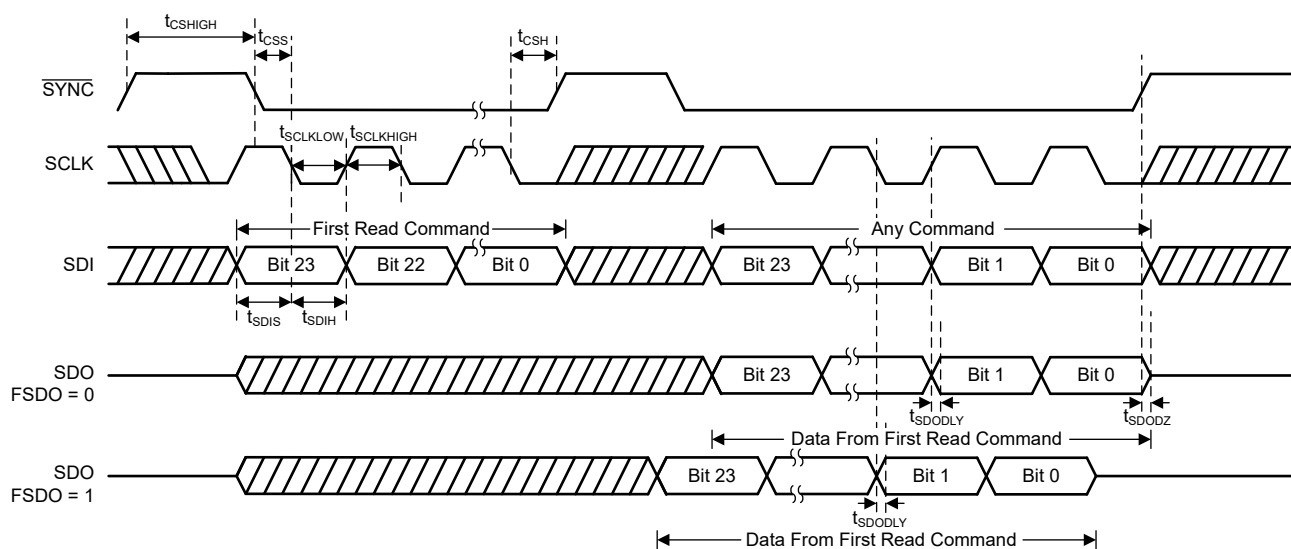


Figure 5-3. SPI Read Timing Diagram

5.18 Typical Characteristics: Voltage Output

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, external reference = 5.5V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

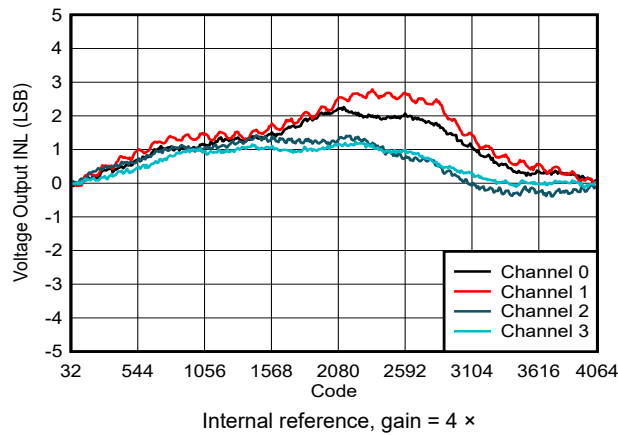


Figure 5-4. Voltage Output INL vs Digital Input Code

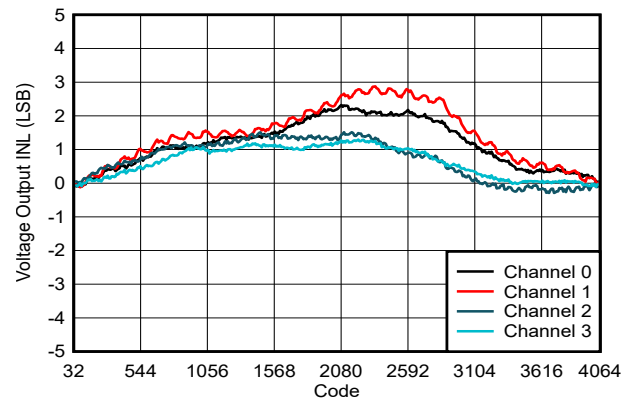


Figure 5-5. Voltage Output INL vs Digital Input Code

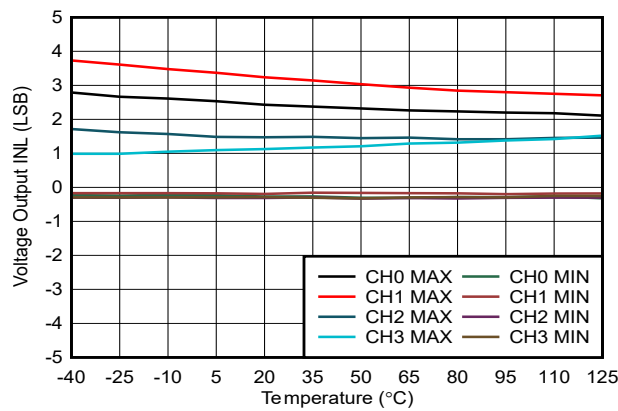


Figure 5-6. Voltage Output INL vs Temperature

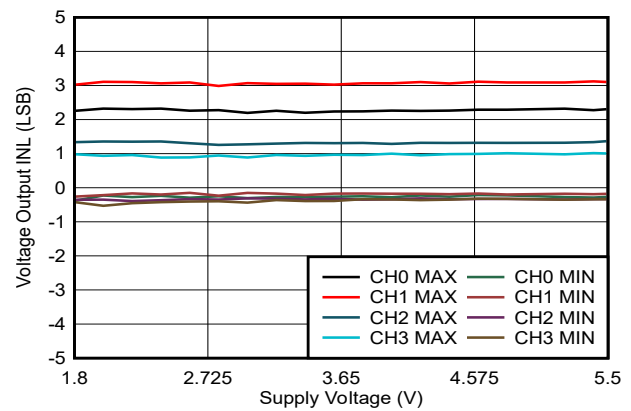


Figure 5-7. Voltage Output INL vs Supply Voltage

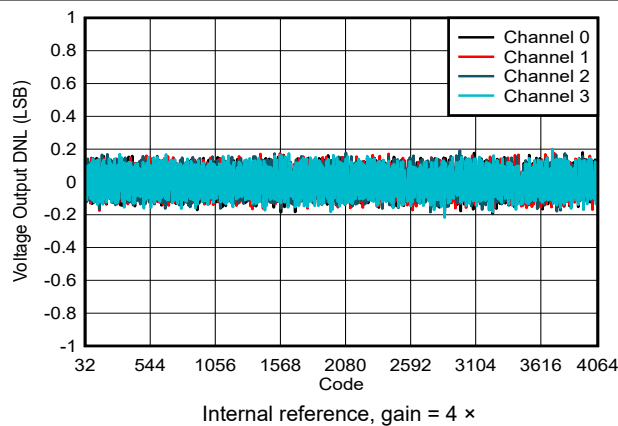


Figure 5-8. Voltage Output DNL vs Digital Input Code

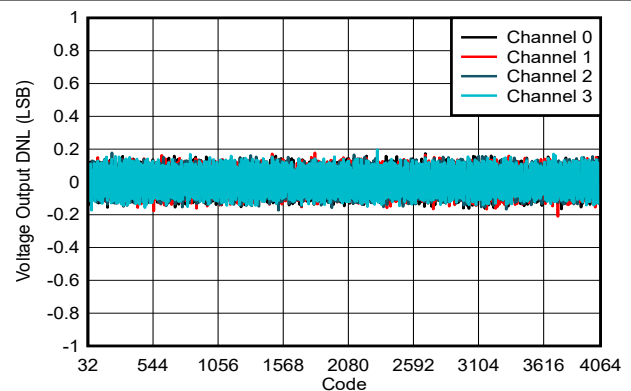


Figure 5-9. Voltage Output DNL vs Digital Input Code

5.18 Typical Characteristics: Voltage Output (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, external reference = 5.5V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

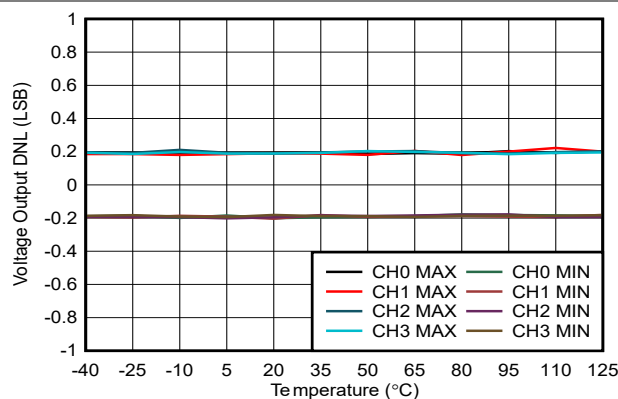


Figure 5-10. Voltage Output DNL vs Temperature

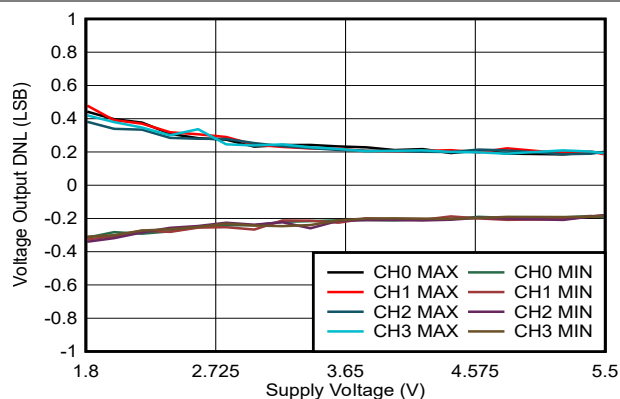


Figure 5-11. Voltage Output DNL vs Supply Voltage

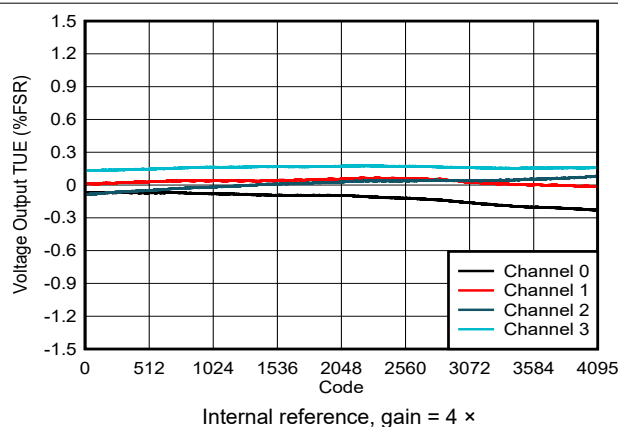


Figure 5-12. Voltage Output TUE vs Digital Input Code

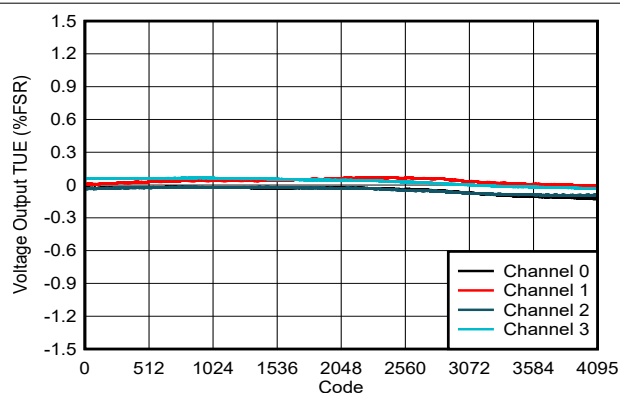


Figure 5-13. Voltage Output TUE vs Digital Input Code

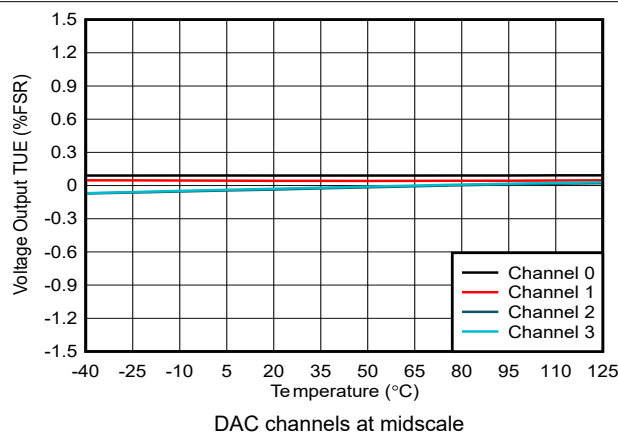


Figure 5-14. Voltage Output TUE vs Temperature

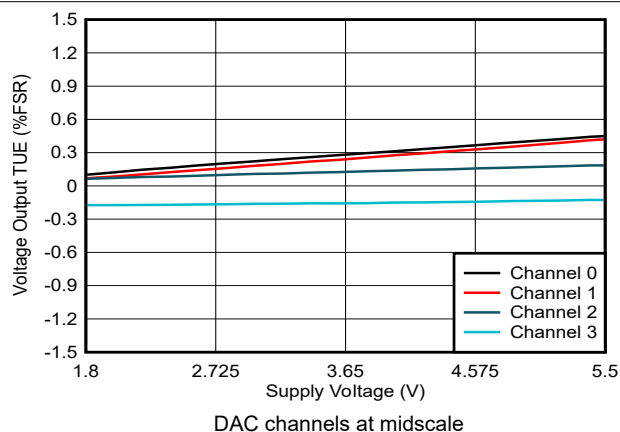


Figure 5-15. Voltage Output TUE vs Supply Voltage

5.18 Typical Characteristics: Voltage Output (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, external reference = 5.5V, gain = 1 \times , 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

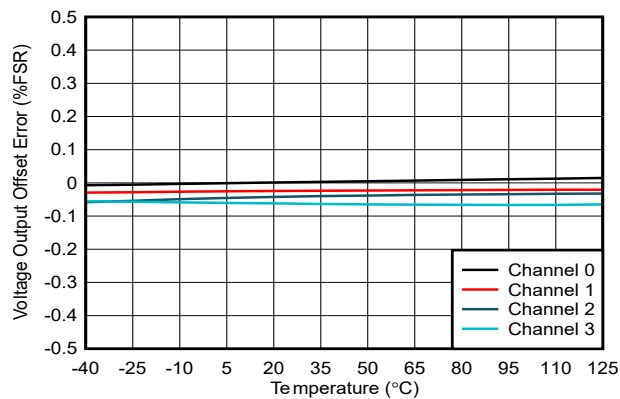


Figure 5-16. Voltage Output Offset Error vs Temperature

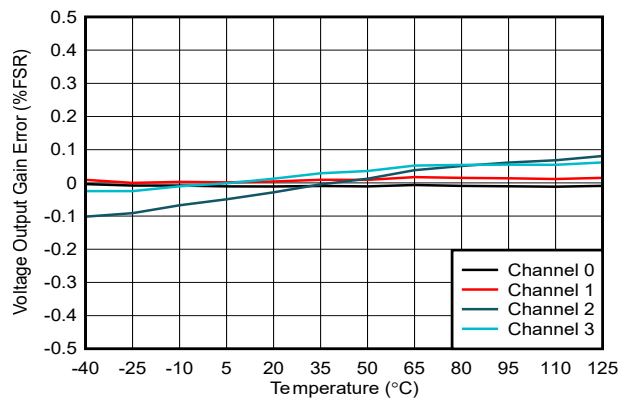


Figure 5-17. Voltage Output Gain Error vs Temperature

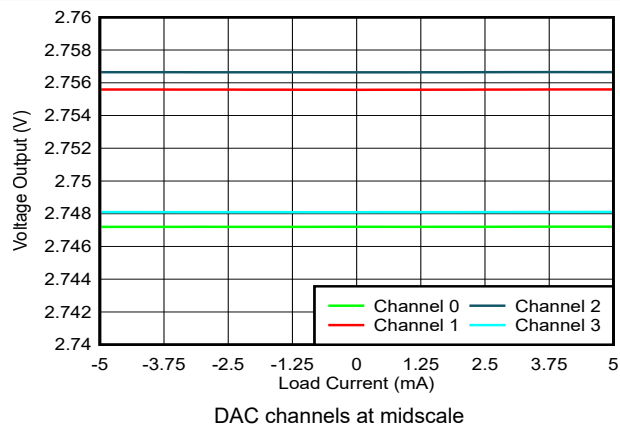


Figure 5-18. Voltage Output vs Load Current

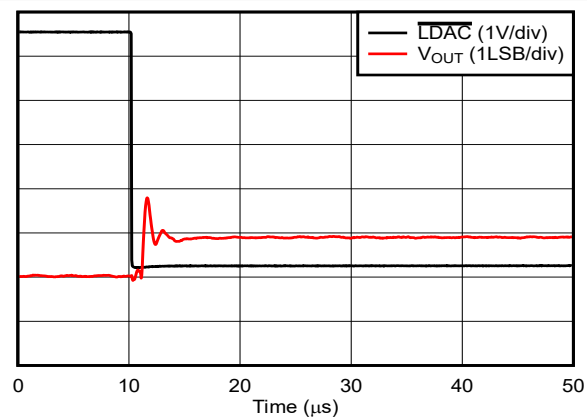


Figure 5-19. Voltage Output Code-to-Code Glitch - Rising Edge

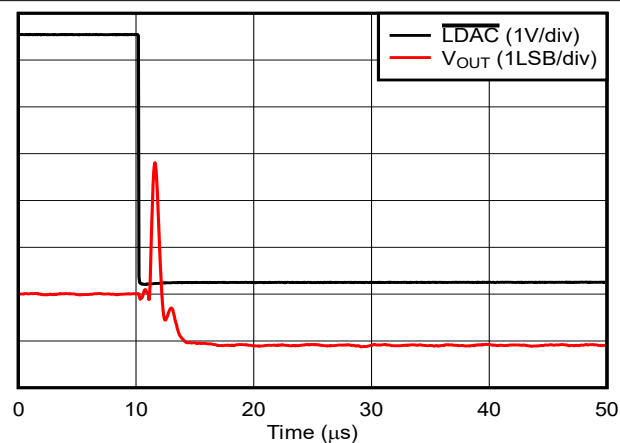


Figure 5-20. Voltage Output Code-to-Code Glitch: Falling Edge

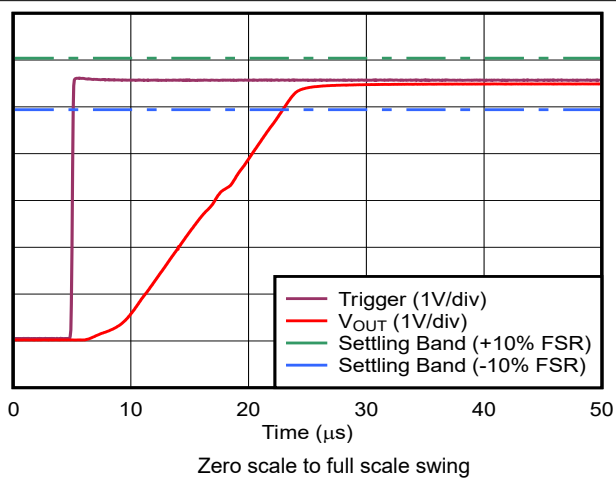


Figure 5-21. Voltage Output Setting Time: Rising Edge

5.18 Typical Characteristics: Voltage Output (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, external reference = 5.5V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

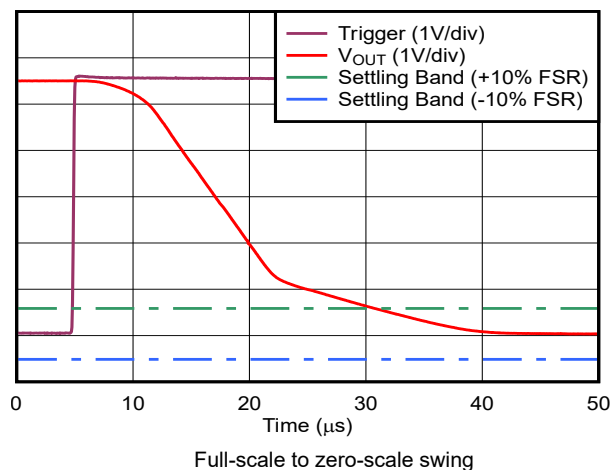


Figure 5-22. Voltage Output Setting Time: Falling Edge

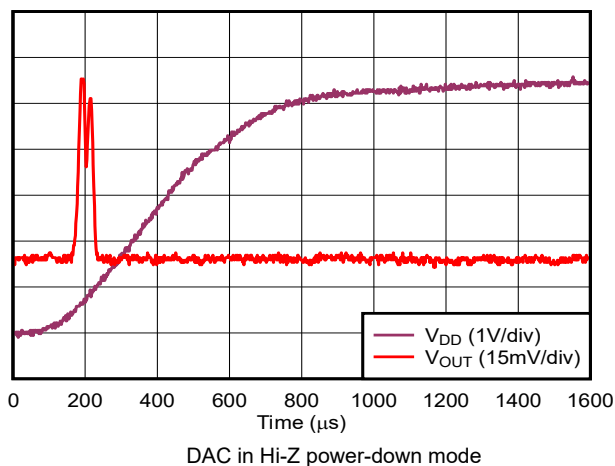


Figure 5-23. Voltage Output Power-On Glitch

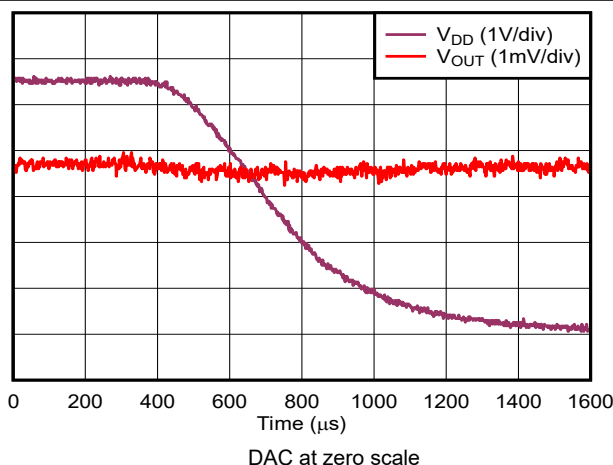


Figure 5-24. Voltage Output Power-Off Glitch

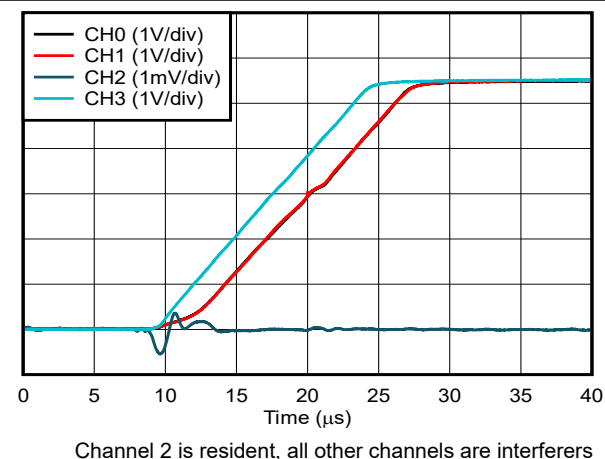


Figure 5-25. Voltage Output Channel-to-Channel Crosstalk

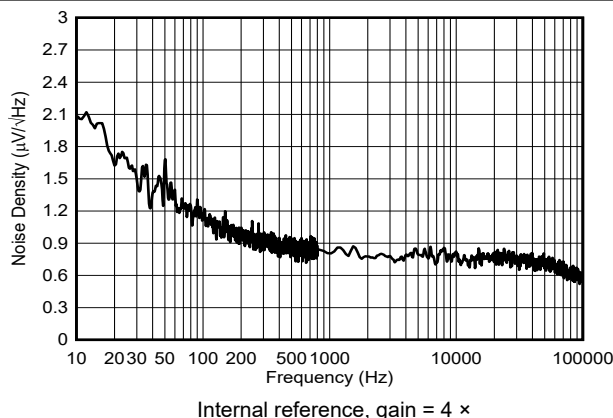


Figure 5-26. Voltage Output Noise Density

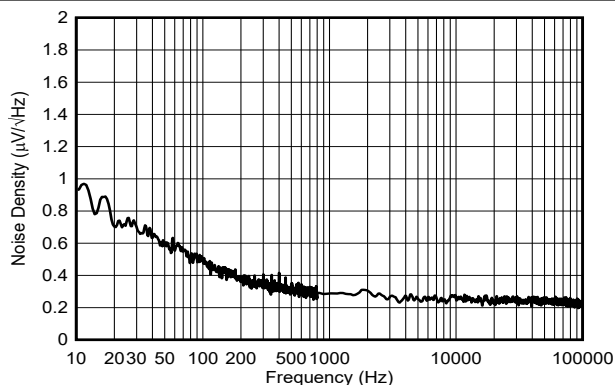


Figure 5-27. Voltage Output Noise Density

5.18 Typical Characteristics: Voltage Output (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, external reference = 5.5V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

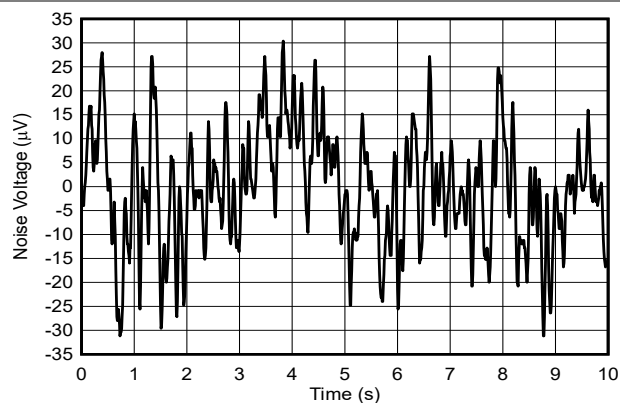


Figure 5-28. Voltage Output Flicker Noise

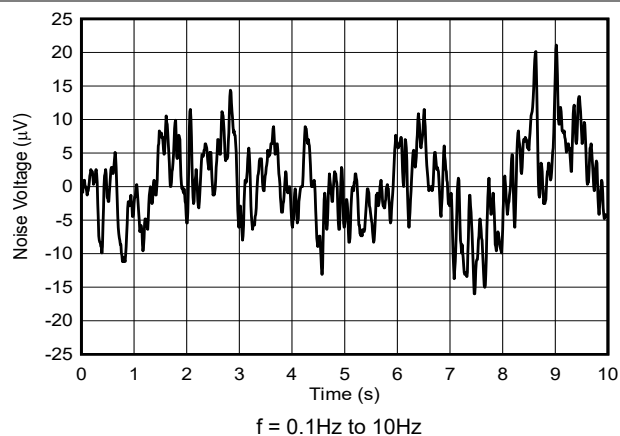


Figure 5-29. Voltage Output Flicker Noise

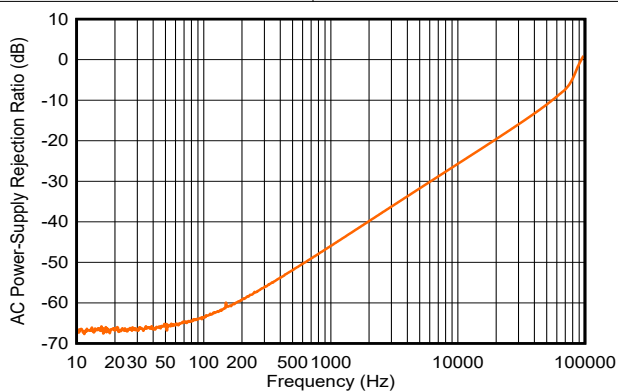


Figure 5-30. Voltage Output AC PSRR vs Frequency

5.19 Typical Characteristics: Current Output

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, output range: $\pm 250\mu\text{A}$ (unless otherwise noted)

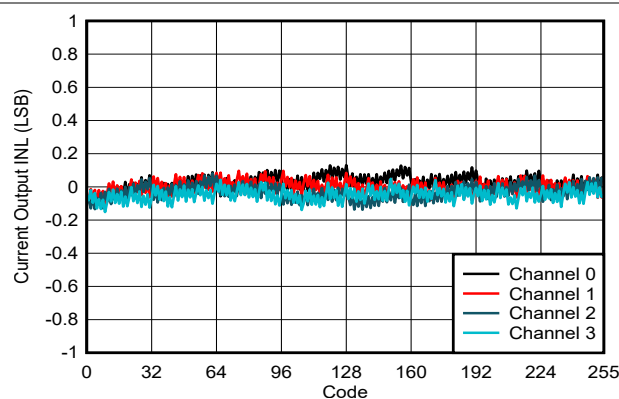


Figure 5-31. Current Output INL vs Digital Input Code

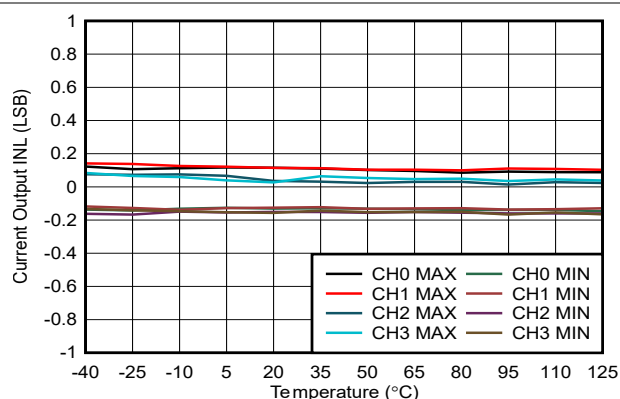


Figure 5-32. Current Output INL vs Temperature

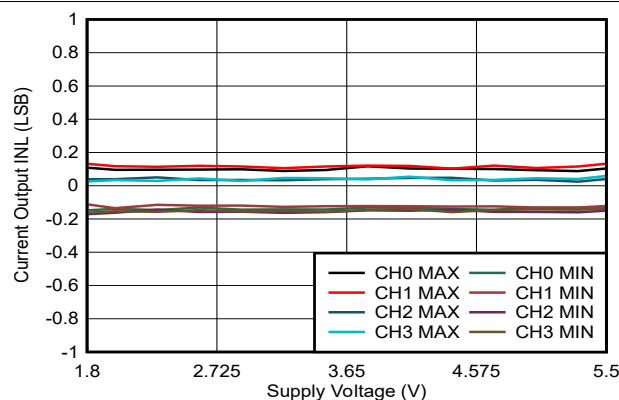


Figure 5-33. Current Output INL vs Supply Voltage

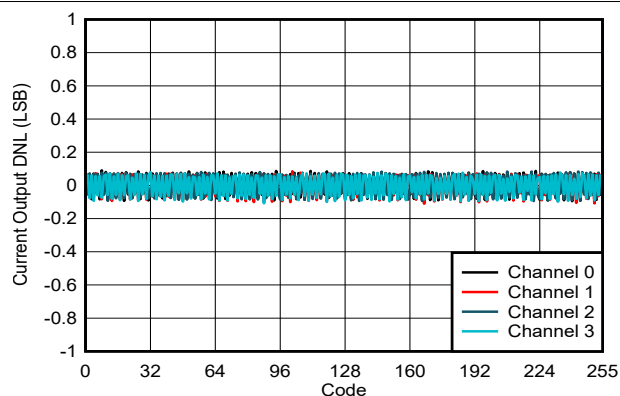


Figure 5-34. Current Output DNL vs Digital Input Code

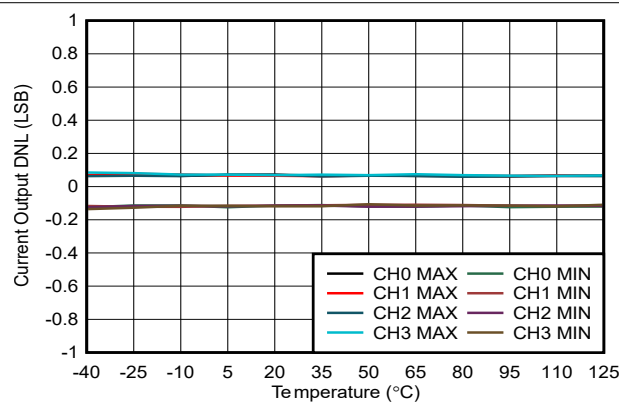


Figure 5-35. Current Output DNL vs Temperature

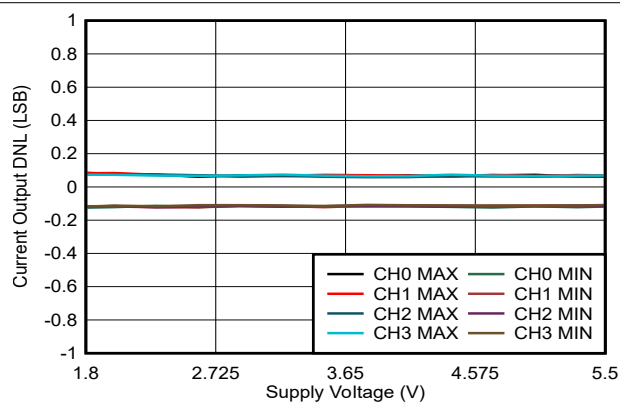


Figure 5-36. Current Output DNL vs Supply Voltage

5.19 Typical Characteristics: Current Output (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, output range: $\pm 250\mu\text{A}$ (unless otherwise noted)

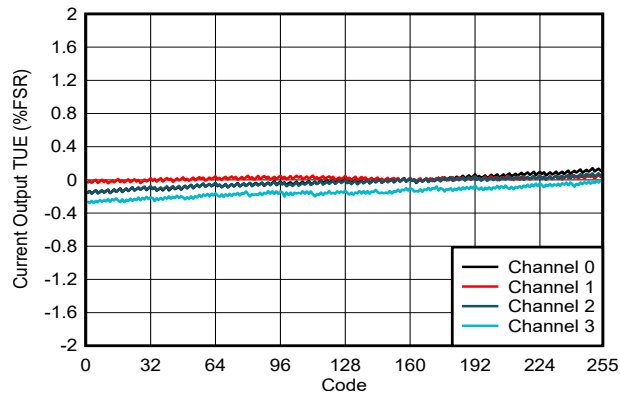


Figure 5-37. Current Output TUE vs Digital Input Code

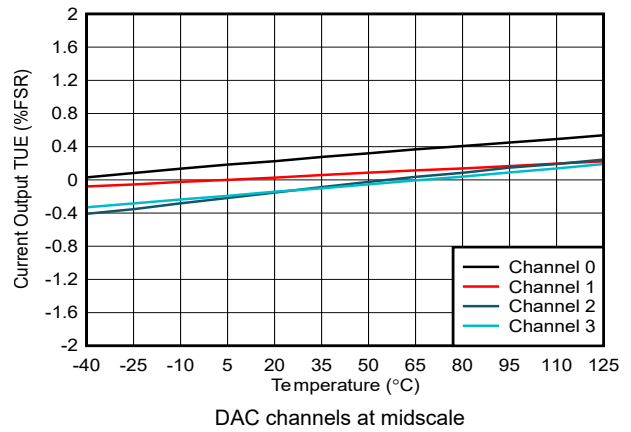


Figure 5-38. Current Output TUE vs Temperature

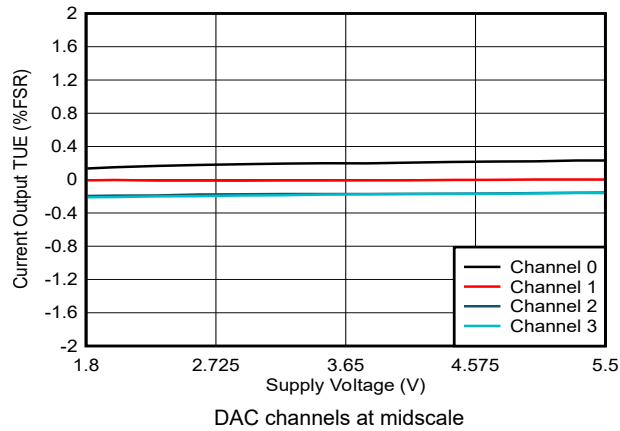


Figure 5-39. Current Output TUE vs Supply Voltage

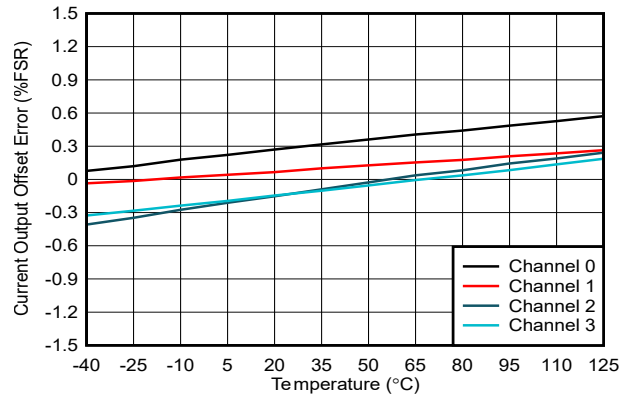


Figure 5-40. Current Output Offset Error vs Temperature

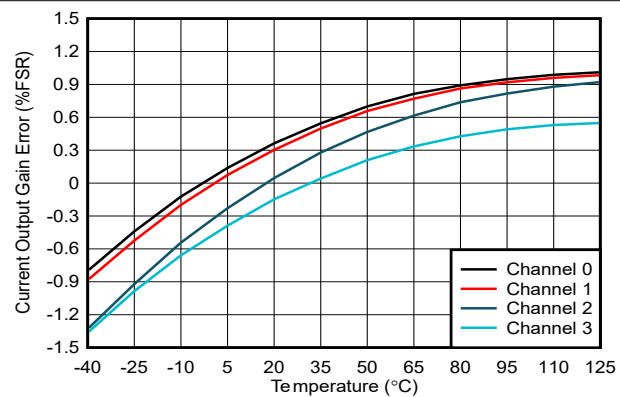


Figure 5-41. Current Output Gain Error vs Temperature

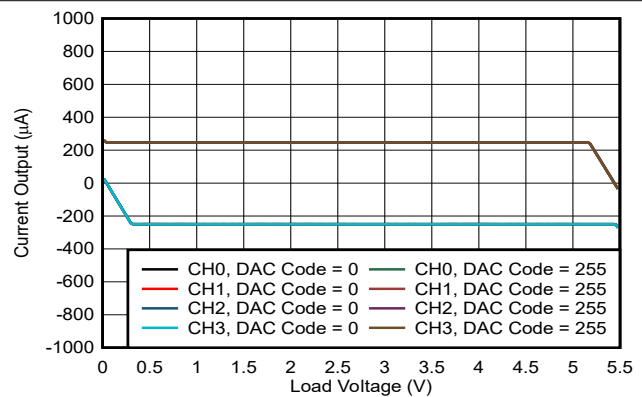


Figure 5-42. Current Output vs Load Voltage

5.19 Typical Characteristics: Current Output (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, output range: $\pm 250\mu\text{A}$ (unless otherwise noted)

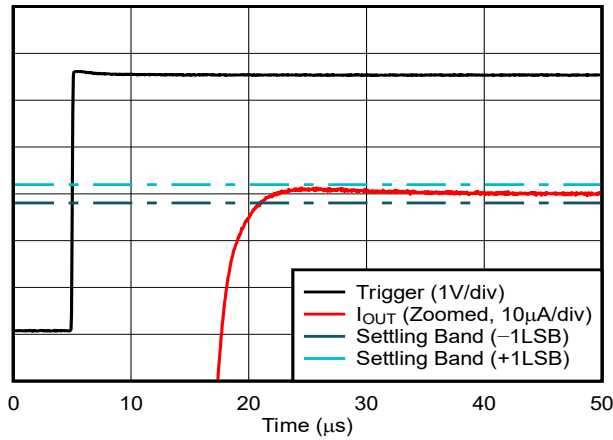


Figure 5-43. Current Output Settling Time: Rising Edge (1/4 to 3/4 scale)

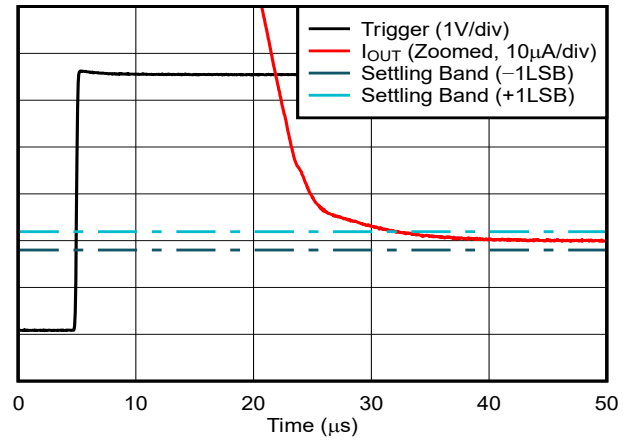


Figure 5-44. Current Output Settling Time: Falling Edge (3/4 to 1/4 scale)

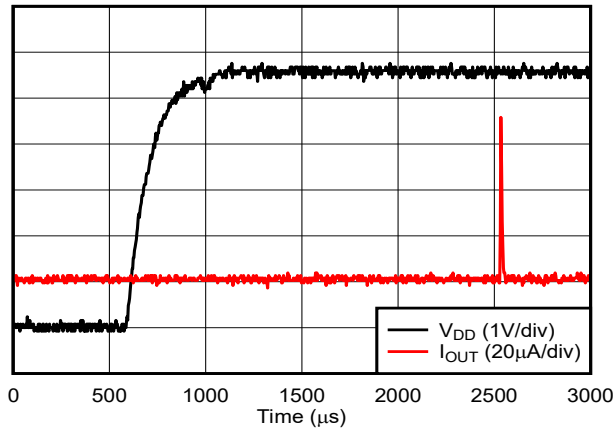


Figure 5-45. Current Output Power-On Glitch

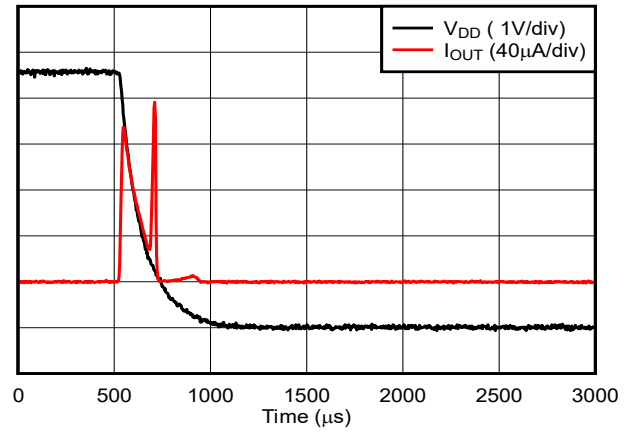


Figure 5-46. Current Output Power-Off Glitch

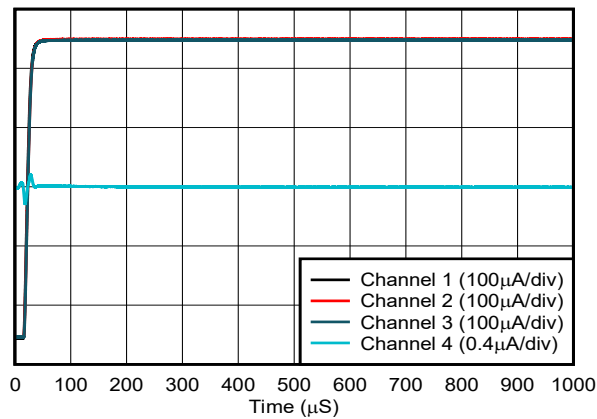


Figure 5-47. Current Output Channel-to-Channel Crosstalk

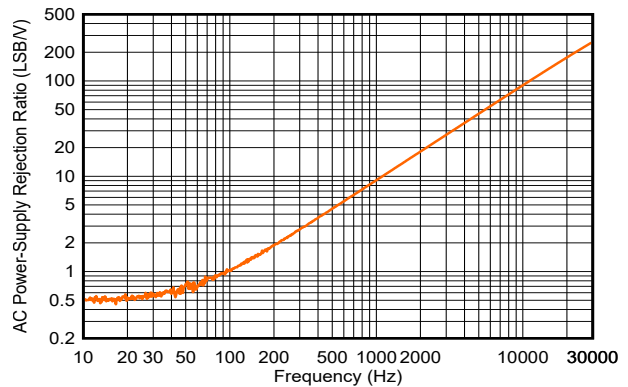


Figure 5-48. Current Output AC PSRR vs Frequency

5.19 Typical Characteristics: Current Output (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, output range: $\pm 250\mu\text{A}$ (unless otherwise noted)

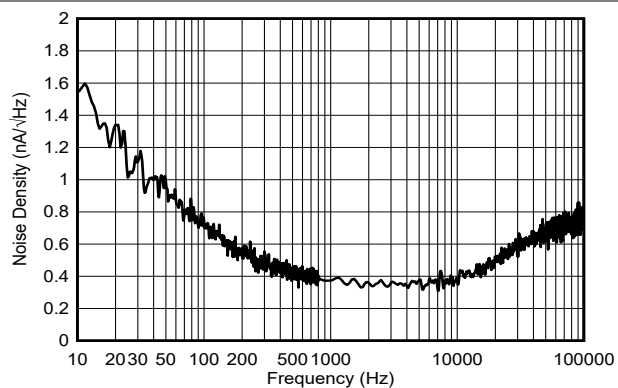


Figure 5-49. Current Output Noise Density

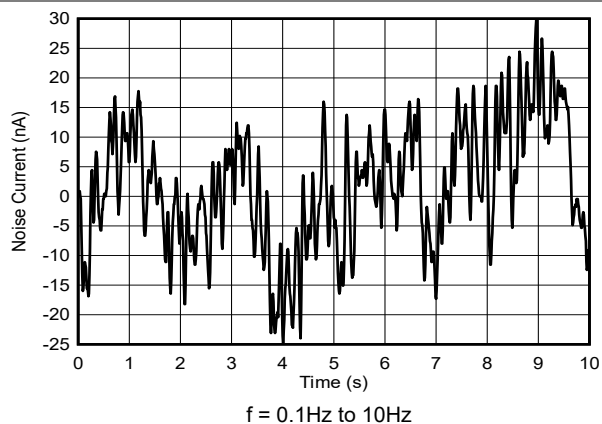


Figure 5-50. Current Output Flicker Noise

5.20 Typical Characteristics: ADC

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, external reference = 5.5V, gain = 1 ×, 10-bit resolution, and Hi-Z input (unless otherwise noted)

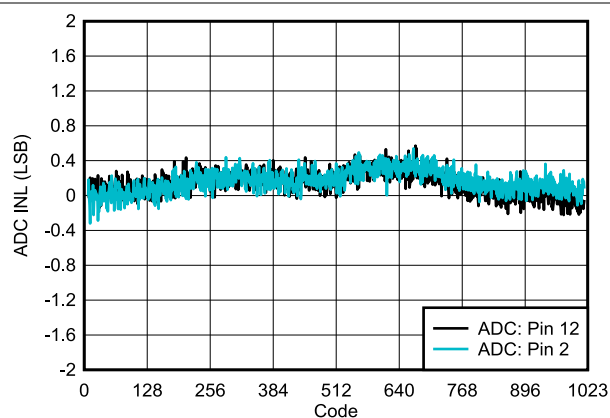


Figure 5-51. ADC INL vs Digital Output Code

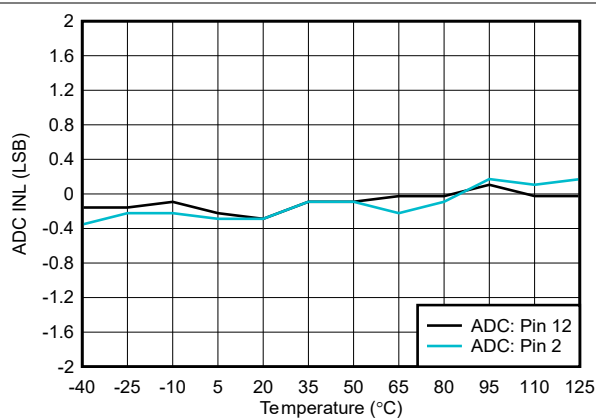


Figure 5-52. ADC INL vs Temperature

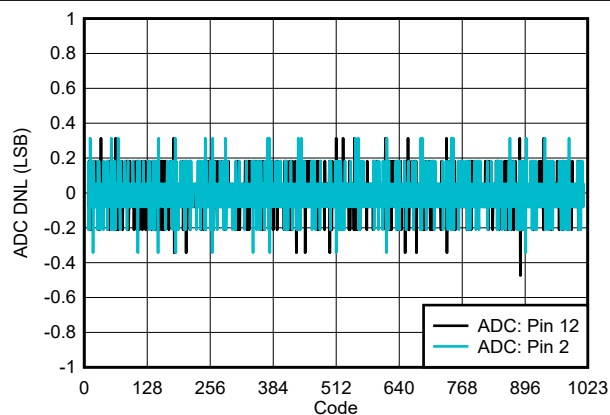


Figure 5-53. ADC DNL vs Digital Output Code

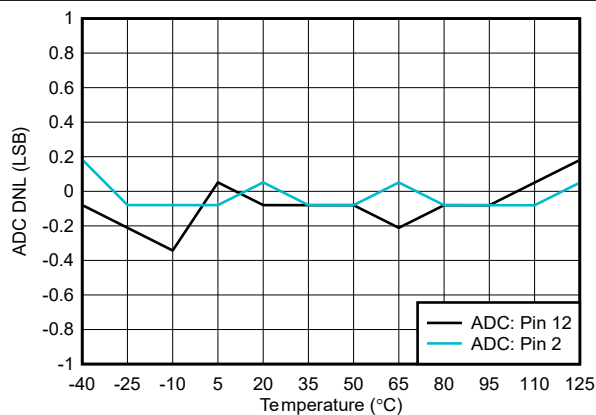


Figure 5-54. ADC DNL vs Temperature

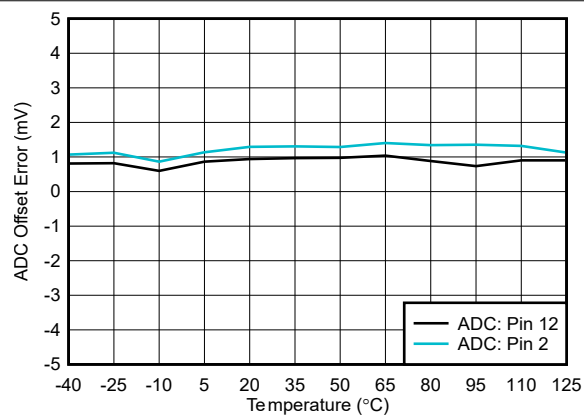


Figure 5-55. ADC Offset Error vs Temperature

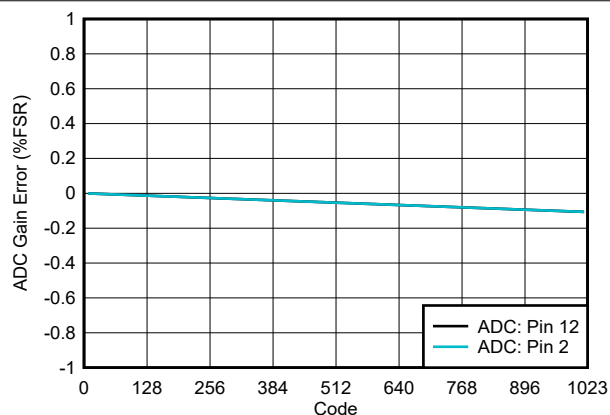


Figure 5-56. ADC Gain Error vs Digital Output Code

5.20 Typical Characteristics: ADC (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, external reference = 5.5V, gain = 1 ×, 10-bit resolution, and Hi-Z input (unless otherwise noted)

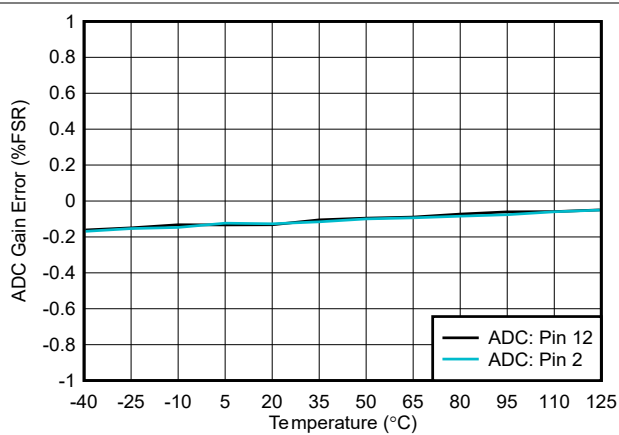
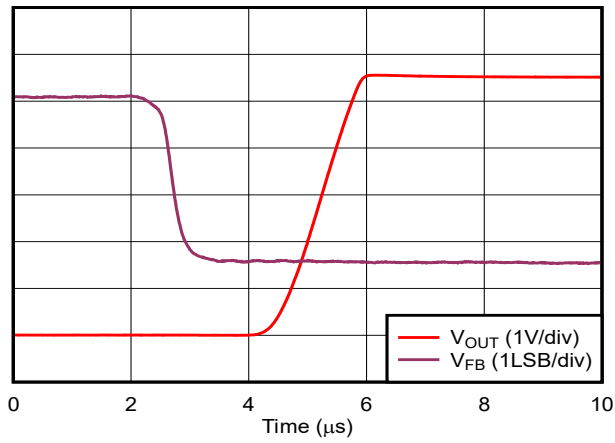


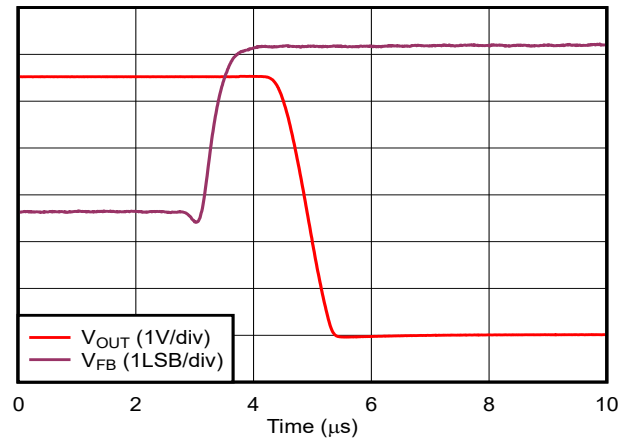
Figure 5-57. ADC Gain Error vs Temperature

5.21 Typical Characteristics: Comparator

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, external reference = 5.5V, gain = 1x, 12-bit resolution, FBx pin in Hi-Z mode, and DAC outputs unloaded (unless otherwise noted)



**Figure 5-58. Comparator Response Time:
Low-to-High Transition**



**Figure 5-59. Comparator Response Time:
High-to-Low Transition**

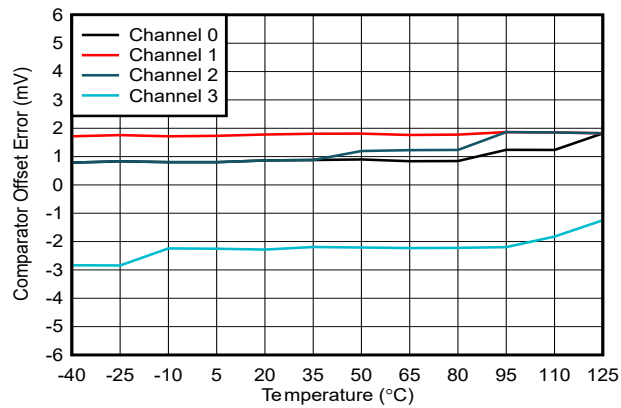


Figure 5-60. Comparator Offset Error vs Temperature

5.22 Typical Characteristics: General

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{V}$, and DAC outputs unloaded (unless otherwise noted)

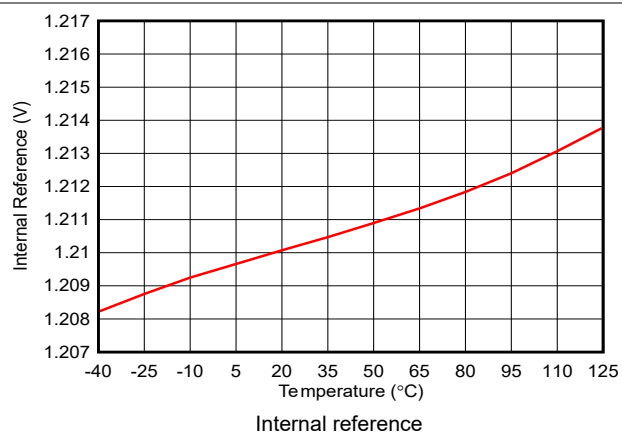


Figure 5-61. Internal Reference vs Temperature

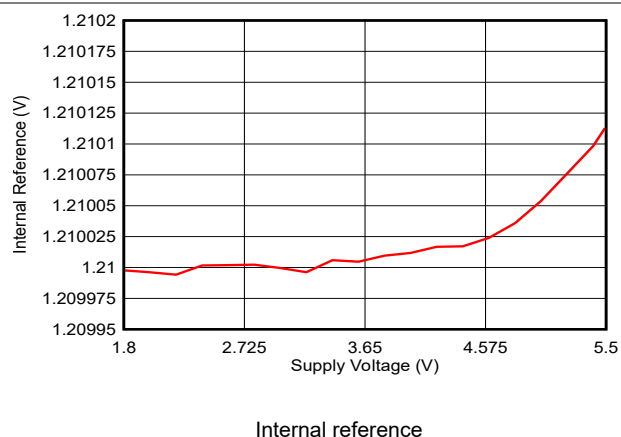


Figure 5-62. Internal Reference vs Supply Voltage

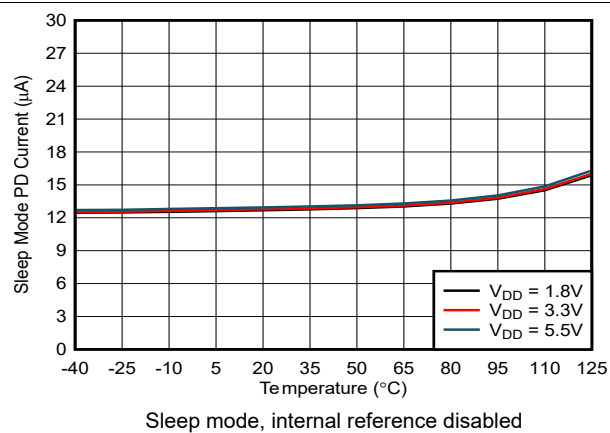


Figure 5-63. Power-Down Current vs Temperature

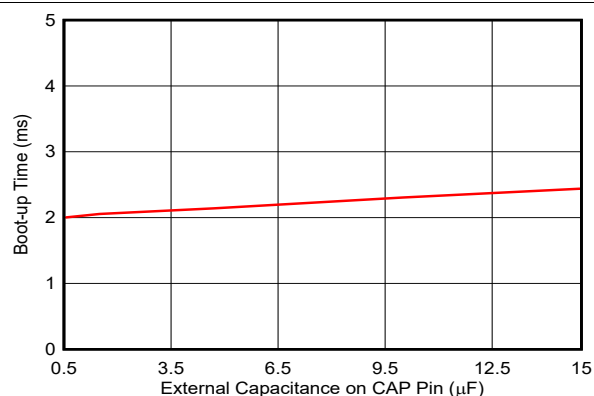


Figure 5-64. Boot-up Time vs Capacitance on CAP pin

6 Detailed Description

6.1 Overview

The 10-bit AFE53004W and 12-bit AFE63004W (AFEx3004W) are a pin-compatible family of four channel smart analog-front-end (AFE) devices which presents a unique combination of analog and digital features in a single tiny WCSP. The AFE analog channels are independently configurable as 10-bit (AFE53004W) or 12-bit (AFE63004W) buffered voltage outputs, 8-bit unipolar or bipolar current outputs, or analog inputs muxed to the 10-bit analog-to-digital converter (ADC). These smart AFEs contain nonvolatile memory (NVM), an internal reference, automatically detectable SPI or I²C interface, PMBus-compatibility in I²C mode, force-sense output, and a general-purpose input. These devices support Hi-Z power-down modes by default, which can be configured to 10k Ω -GND or 100k Ω -GND using the NVM, and the analog outputs are Hi-Z when VDD is off. The AFEx3004W have a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The AFEx3004W operate with either an internal reference, external reference, or with a power supply as the reference, and provide a full-scale output of 1.8V to 5.5V.

The AFEx3004W devices support I²C standard mode (100Kbps), fast mode (400Kbps), and fast mode plus (1Mbps). The I²C interface can be configured with four target addresses using the A0 pin. These devices also support specific PMBus commands such as *turn on/off*, *margin high or low*, and more. The SPI mode supports a three-wire interface by default with up to a 50MHz SCLK input. The GPIO input can be configured as SDO in the NVM for SPI read capability. The GPIO input can alternatively be configured as the $\overline{\text{LDAC}}$, $\overline{\text{PD}}$, $\overline{\text{STATUS}}$, $\overline{\text{FAULT-DUMP}}$, $\overline{\text{RESET}}$, or $\overline{\text{PROTECT}}$ function.

The AFEx3004W also include digital slew rate control, and support standard waveform generation such as *sine and cosine*, *triangular*, and *sawtooth* waveforms. These devices can generate pulse-width modulation (PWM) output with the combination of the triangular or sawtooth waveform and the FB pin. The force-sense outputs of the analog channels can be used as programmable comparators. The comparator mode allows programmable hysteresis, latching comparator, window comparator, and fault-dump to the NVM.

6.2 Functional Block Diagram

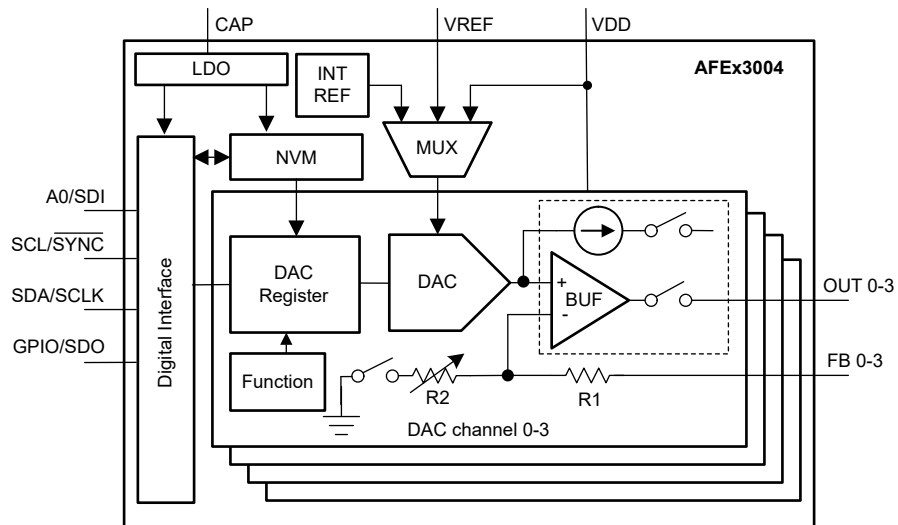


Figure 6-1. Disabled ADC Device Functional Diagram

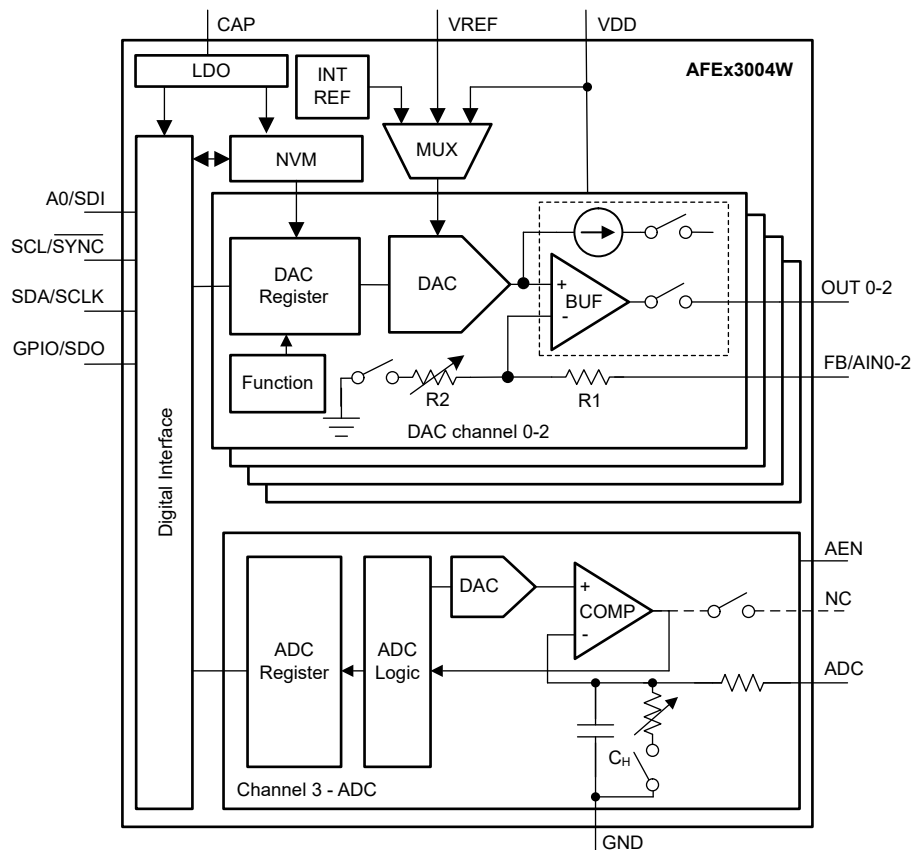


Figure 6-2. Enabled ADC Device Functional Diagram

6.3 Feature Description

6.3.1 Smart Analog-Front-End Converter (AFE) Architecture

The AFE53004W DAC channels consist of a string architecture with a voltage-output amplifier and an external FB pin and voltage-to-current converter. Section 6.2 shows the DAC architecture within the block diagram, which operates from a 1.8V to 5.5V power supply. The AFE has an internal voltage reference of 1.21V. There is an option to select an external reference on the VREF pin, the power supply as a reference, or the internal reference with configurable gain options. The voltage output mode uses one of these three reference options and is independently configurable for each DAC channel. The current output mode uses an internal band gap to generate the current outputs. Both the voltage- and current-output modes support multiple programmable output ranges.

The AFE53004W contains a 10-bit successive-approximation register (SAR) ADC on channel 3. Any other analog channel can be configured as an ADC input if channel 3 is configured in ADC mode. The ADC reference is independently configurable per channel with the same reference options available in the DAC configuration. The figure below shows the AFE architecture with enabled ADC.

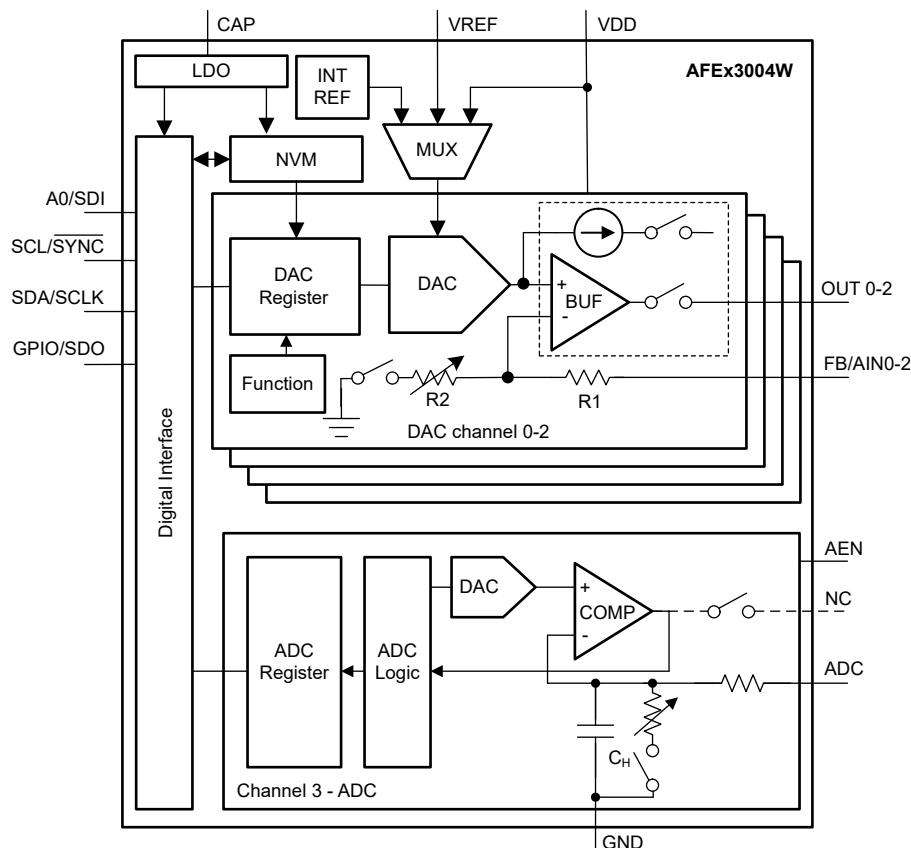


Figure 6-3. Enabled ADC Device Functional Diagram

The AFE53004W devices support Hi-Z output when VDD is off, maintaining very low leakage current at the output pins with up to 1.25V of forced voltage. The analog output pin also starts up in high-impedance mode by default. To change the power-up mode to 10kΩ-GND or 100kΩ-GND, program the corresponding VOUT-PDN-X field in the COMMON-CONFIG register and load these bits in the device NVM.

The AFE53004W devices support an independent programmable comparator mode for each channel. The respective FBx pins act as the inputs for the comparator. The AFE architecture supports inversion of the comparator output using register settings. The comparator outputs can be push-pull or open-drain. The comparator mode supports programmable hysteresis using *margin-high* and *margin-low* register fields, latching comparator, and window comparator. The comparator outputs are accessible internally by the device.

The AFEx3004W devices include a *smart* feature set to enable processor-less operation and high-integration. The NVM enables a predictable start-up. The GPIO triggers the analog output without the I²C interface in the absence of a processor or when the processor or software fails. The integrated functions and the FBx pin enable PWM output for control applications. The FBx pin enables this device to be used as a programmable comparator. The AFE also features digital slew-rate control.

6.3.2 Digital Input/Output

The AFEx3004W have four digital IO pins that include I²C, SPI, PMBus, and GPIO interfaces. These devices automatically detect I²C and SPI protocols at the first successful communication after power-on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I²C interface uses the A0 pin to select from among four address options. The SPI interface is a 3-wire interface by default. No readback capability is available in this mode. The GPIO pin can be configured in the register map and then programmed in to the NVM as the SDO pin. The SPI readback mode is slower than the write mode. The programming interface pins are:

- I²C: SCL, SDA, A0
- SPI: SCLK, SDI, $\overline{\text{SYNC}}$, SDO/GPIO

The GPIO can be configured as multiple functions other than SDO. These are $\overline{\text{LDAC}}$, $\overline{\text{PD}}$, $\overline{\text{STATUS}}$, $\overline{\text{PROTECT}}$, $\overline{\text{FAULT-DUMP}}$, and $\overline{\text{RESET}}$. All the digital pins are open-drain when used as outputs. Therefore, all the output pins must be pulled up to the desired IO voltage using external resistors.

6.3.3 Nonvolatile Memory (NVM)

The AFEx3004W contain nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, as shown in the highlighted gray cells in the *Register Map* section, can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. The NVM-PROG is an autoresetting bit. The default values for all the registers in the AFEx3004W are loaded from NVM as soon as a POR event is issued.

The AFEx3004W also implement NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 for the device to start an NVM-reload operation. After completion, the device autoresets the NVM-RELOAD bit to 0. During the NVM write or reload operation, all read/write operations to the device are blocked. The *Electrical Characteristics: General* section provides the timing specification for the NVM write cycle. The processor must wait for the specified duration before resuming any read or write operation on the SPI or I²C interface.

6.4 Device Functional Modes

6.4.1 Voltage-Output Mode

The voltage-output mode for each AFE channel can be entered by selecting the power-up option in the VOUT-PDN-X fields in the COMMON-CONFIG register and simultaneously powering down the current output option for the respective channels using the IOUT-PDN-X bits in the same register. Short the OUTx and FBx pins of respective channels externally for closed-loop amplifier output. An open FBx pin saturates the amplifier output. To achieve the desired voltage output, select the correct reference option, select the amplifier gain for the required output range, and program the DAC code in the DAC-X-DATA register of the respective channels.

6.4.1.1 Voltage Reference and DAC Transfer Function

There are three voltage reference options possible with the AFE53004W: internal reference, external reference, and the power supply as reference, as shown in Figure 6-4. The DAC transfer function in the voltage-output and comparator modes changes based on the voltage reference selection.

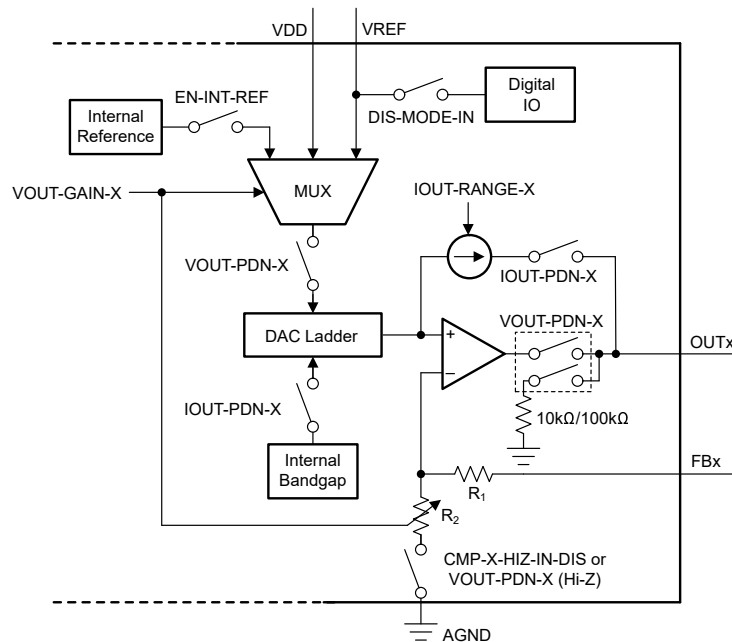


Figure 6-4. Voltage Reference Selection and Power-Down Logic

6.4.1.1.1 Internal Reference

The AFE53004W contain an internal reference that is disabled by default. To enable the internal reference, write 1 to bit EN-INT-REF in the COMMON-CONFIG register. The internal reference generates a fixed 1.21V voltage (typical). Use the VOUT-GAIN-X bit in the DAC-X-VOUT-CMP-CONFIG register to achieve gains of 1.5 ×, 2 ×, 3 ×, or 4 × for the DAC output voltage (V_{OUT}). Equation 1 shows DAC transfer function using the internal reference.

$$V_{OUT} = \frac{DAC_DATA}{2^N} \times V_{REF} \times GAIN \quad (1)$$

where:

- N is the resolution in bits, 12 (AFE63004W) or 10 (AFE53004W).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA bit in the DAC-X-DATA register. DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21V (typical).
- GAIN = 1.5 ×, 2 ×, 3 ×, or 4 ×, based on VOUT-GAIN-X bits.

6.4.1.1.2 External Reference

By default, the AFE53004W operate from an external reference input. The external reference option can also be selected by configuring the VOUT-GAIN-X field in the DAC-X-VOUT-CMP-CONFIG register appropriately. Write 1 to the DIS-MODE-IN bit in the DEVICE-MODE-CONFIG register to minimize I_{DD} . The external reference can be between 1.7V and VDD. Equation 2 shows DAC transfer function when the external reference is used. The gain at the output stage of the DAC is always 1 × in the external reference mode.

Note

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

$$V_{OUT} = \frac{DAC_DATA}{2^N} \times V_{REF} \quad (2)$$

where:

- N is the resolution in bits, 12 (AFE63004W) or 10 (AFE53004W).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA field in the DAC-X-DATA register. DAC_DATA ranges from 0 to $2^N - 1$.
- V_{REF} is the external reference voltage.

6.4.1.1.3 Power-Supply as Reference

The AFE53004W can operate with the power-supply pin (VDD) as a reference. Equation 3 shows DAC transfer function when the power-supply pin is used as reference. The gain at the output stage is always 1x.

$$V_{OUT} = \frac{DAC_DATA}{2^N} \times V_{DD} \quad (3)$$

where:

- N is the resolution in bits, 10 (AFE63004W) or 12 (AFE53004W).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA bit in the DAC-X-DATA register.
- DAC_DATA ranges from 0 to $2^N - 1$.
- V_{DD} is used as the DAC reference voltage.

6.4.2 Current-Output Mode

To enter current-output mode for each AFE channel, disable the respective IOUT-PDN-X bits in the COMMON-CONFIG register, and set the respective VOUT-PDN-X bits in the same register to Hi-Z power-down mode. Select the desired current-output range by writing to the IOUT-RANGE-X bit in the DAC-X-IOUT-MISC-CONFIG register. To minimize leakage in current-output mode, disconnect the FBx pin. For the best power-on glitch performance, program the NVM with IOUT mode using the smallest output range before powering on the output channel, and then immediately program the DAC code and desired output range. The transfer function of the output current is shown in the following equation:

$$I_{OUT} = \frac{DAC_DATA \times (I_{MAX} - I_{MIN})}{2^8} + I_{MIN} \quad (4)$$

where:

- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA bits specified in Section 7.8 or the DAC-X-DATA-8BIT bits specified in Section 7.21. DAC_DATA ranges from 0 to 255.
- I_{MAX} is the signed maximum current in the IOUT-RANGE-X setting specified in Section 7.5.
- I_{MIN} is the signed minimum current in the IOUT-RANGE-X setting specified in Section 7.5.

6.4.3 Analog-to-Digital Converter (ADC) Mode

The AFEx3004W have an integrated ADC. The analog channels can be converted to independent ADC inputs, as shown in Figure 6-5. The main ADC channel is ADC3, whereas the other inputs are multiplexed to ADC3. ADC3 must be configured as a comparator and the FB3/AIN3 pin must be connected to VDD using a pullup resistor when any channel is selected as ADC. The transfer function of the ADC is given in Equation 5.

$$\text{ADC_DATA} = \left(\text{INTEGER} \right) \left(\frac{V_{\text{IN}}}{V_{\text{FS}}} \right) \times 2^{10} \quad (5)$$

where

- ADC_DATA is the output of the ADC read back in the register map. ADC_DATA is limited to $(2^{10}-1)$.
- V_{IN} is the input voltage at the AINx pin.
- V_{FS} is the full-scale input voltage as provided in Table 6-1.
- (INTEGER) denotes integer division.

Follow these steps to configure and read data from ADC channel x:

1. Configure the full-scale voltage using VOUT-GAIN-X for the corresponding channel in the DAC-X-VOUT-CMP-CONFIG register.
2. Configure DAC channel 3 as comparator by writing 1 to the CMP-X-EN bit in the DAC-3-VOUT-CMP-CONFIG register. Only Hi-Z input is allowed in channel 3.
3. Configure DAC channel-x as comparator by writing 1 to the CMP-X-EN bit in the DAC-X-VOUT-CMP-CONFIG register.
4. Select the number of averages, ADC channel, and then trigger the ADC conversion using the ADC-CONFIG-TRIG register.
5. Read the ADC data using the ADC-DATA register. The data are valid when the ADC-DRDY bit is 1.
6. Repeat steps 4 and 5 for every ADC readback.

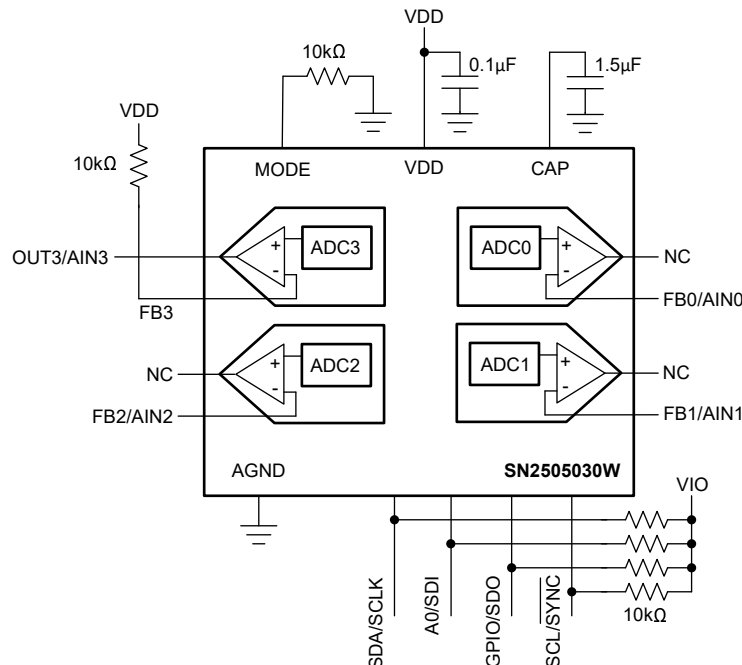


Figure 6-5. ADC Interface

Table 6-1. Full Scale Analog Input (V_{FS})

REFERENCE (VREF)	GAIN	V_{FS} (HI-Z INPUT MODE)	V_{FS} (FINITE IMPEDANCE INPUT MODE)
Power supply	1 ×	VDD / 3	VDD
External	1 ×	VREF / 3	VREF
Internal	1.5 ×	$(VREF \times GAIN) / 3$	$VREF \times GAIN$
	2 ×	$(VREF \times GAIN) / 3$	$VREF \times GAIN$
	3 ×	$(VREF \times GAIN) / 6$	$(VREF \times GAIN) / 2$
	4 ×	$(VREF \times GAIN) / 6$	$(VREF \times GAIN) / 2$

6.4.4 Comparator Mode

All the AFE channels can be configured as programmable comparators in the voltage-output mode. To enter the comparator mode for a channel, write 1 to the CMP-X-EN bit in the respective DAC-X-VOUT-CMP-CONFIG register. The comparator output can be configured as push-pull or open-drain using the CMP-X-OD-EN bit. To enable the comparator output on the output pin, write 1 to the CMP-X-OUT-EN bit. To invert the comparator output, write 1 to the CMP-X-INV-EN bit. The FBx pin has a finite impedance. By default, the FBx pin is in the high-impedance mode. To disable high-impedance on the FBx pin, write 1 to the CMP-X-HIZ-IN-DIS bit. [Table 6-2](#) shows the comparator output at the pin for different bit settings.

Note

In the Hi-Z input mode, the comparator input range is limited to:

- For GAIN = 1x, 1.5x, or 2x: $V_{FB} \leq (V_{REF} \times GAIN) / 3$
- For GAIN = 3x, or 4x: $V_{FB} \leq (V_{REF} \times GAIN) / 6$

Any higher input voltage is clipped.

Table 6-2. Comparator Output Configuration

CMP-X-EN	CMP-X-OUT-EN	CMP-X-OD-EN	CMP-X-INV-EN	CMPX-OUT PIN
0	X	X	X	Comparator not enabled
1	0	X	X	No output
1	1	0	0	Push-pull output
1	1	0	1	Push-pull and inverted output
1	1	1	0	Open-drain output
1	1	1	1	Open-drain and inverted output

[Figure 6-6](#) shows the interface circuit when all the DAC channels are configured as comparators. The programmable comparator operation is as shown in [Figure 6-7](#). Individual comparator channels can be configured in no-hysteresis, with-hysteresis, and window-comparator modes using the CMP-X-MODE bit in the respective DAC-X-CMP-MODE-CONFIG register, as shown in [Table 6-3](#).

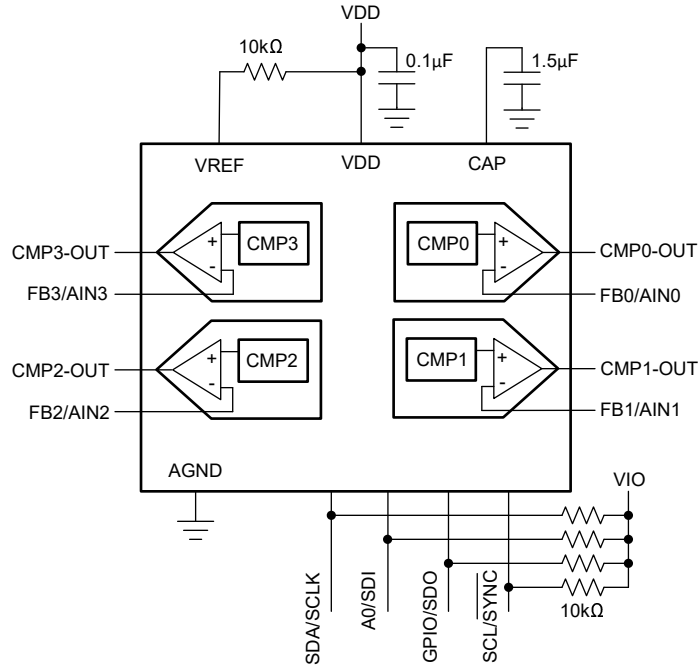


Figure 6-6. Comparator Interface

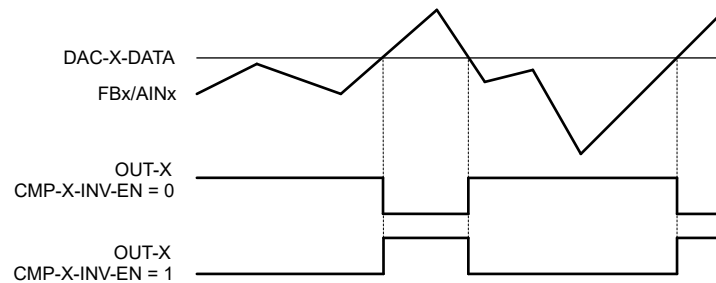


Figure 6-7. Programmable Comparator Operation

Table 6-3. Comparator Mode Selection

CMP-X-MODE BIT FIELD	COMPARATOR CONFIGURATION
00	Normal comparator mode. No hysteresis or window operation.
01	Hysteresis comparator mode. DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers set the hysteresis.
10	Window comparator mode. DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers set the window bounds.
11	Invalid setting

6.4.4.1 Programmable Hysteresis Comparator

Comparator mode provides hysteresis when the CMP-X-MODE bit is set to 01b, as shown in Table 6-3. The hysteresis is provided by the DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers, as shown in Figure 6-8.

When the DAC-X-MARGIN-HIGH is set to full-code or the DAC-X-MARGIN-LOW is set to zero-code, the comparator works as a latching comparator that is, the output is latched after the threshold is crossed. The latched output can be reset by writing to the corresponding RST-CMP-FLAG-X bit in the COMMON-DAC-TRIG register. Figure 6-9 shows the behavior of a latching comparator with active low output and Figure 6-10 shows the behavior of a latching comparator with active high output.

Note

The value of the DAC-X-MARGIN-HIGH register must be greater than the value of the DAC-X-MARGIN-LOW register. The comparator output in the hysteresis mode can only be noninverting that is, the CMP-X-INV-EN bit in the DAC-X-VOULT-CMP-CONFIG register must be set to 0. In latching mode, for the reset to take effect, the input voltage must be within DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW.

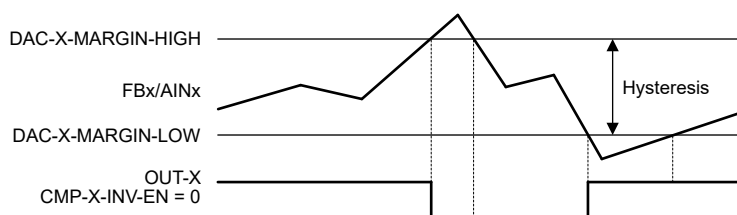


Figure 6-8. Programmable Hysteresis Without Latching Output

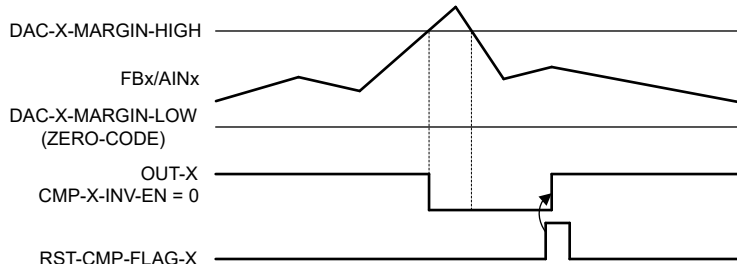


Figure 6-9. Latching Comparator With Active Low Output

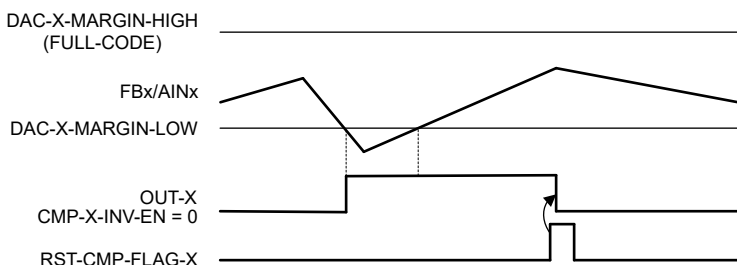


Figure 6-10. Latching Comparator With Active High Output

6.4.4.2 Programmable Window Comparator

Window comparator mode is enabled by setting the CMP-X-MODE bit to 10b, as shown in [Table 6-3](#). The window bounds are set by the DAC-X-MARGIN-HIGH and the DAC-X-MARGIN-LOW registers, as shown in [Figure 6-11](#). The output of the window comparator for a given channel is indicated by the respective WIN-CMP-X bit in the CMP-STATUS register. The comparator output (WIN-CMP-X) can be latched by writing 1 to the WIN-LATCH-EN bit in the COMMON-CONFIG register. After being latched, the comparator output can be reset using the corresponding RST-CMP-FLAG-X bit in the COMMON-DAC-TRIG register. For the reset to take effect, the input must be within the window bounds.

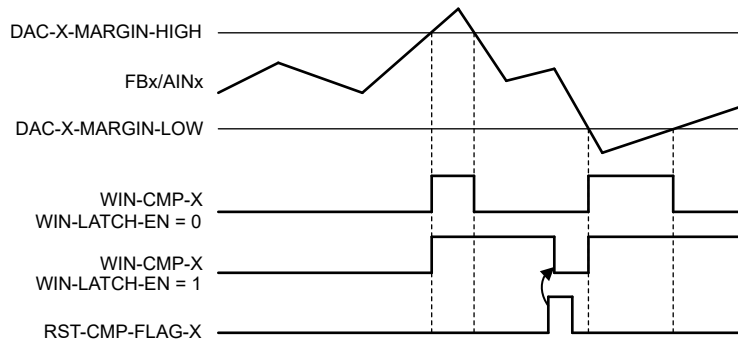


Figure 6-11. Window Comparator Operation

A single comparator is used per channel to check both the *margin-high* and *margin-low* limits of the window. Therefore, the window comparator function has a finite response time as specified in the *Electrical Characteristics: Comparator Mode* section. Also, the static behavior of the WIN-CMP-X bit is not reflected at the output pins. Set the CMP-X-OUT-EN bit to 0. The WIN-CMP-X bit must be read digitally using the communication interface. This bit can also be mapped to the GPIO pin, as shown in [Table 6-20](#).

Note

- The value of the DAC-X-MARGIN-HIGH register must be greater than that of the DAC-X-MARGIN-LOW register.
- Set the SLEW-RATE-X bit to 0000b (no-slew) and LOG-SLEW-EN-X bit to 0b in the DAC-X-FUNC-CONFIG register to get the best response time from the window comparator.
- The CMP-X-OUT-EN bit in the DAC-X-VOUT-CMP-CONFIG register can be set to 0b to eliminate undesired toggling of the OUT pin.

6.4.5 Programmable Slew-Rate Control

When the DAC data registers are written, the voltage on DAC output immediately transitions to the new code following the slew rate and settling time specified in the *Electrical Characteristics*.

The slew rate control feature allows the user to control the rate at which the output voltage changes. When this feature is enabled (using the SLEW-RATE-X[3:0] bits), the DAC output changes from the current code to the code in the DAC-X-MARGIN-HIGH or DAC-X-MARGIN-LOW registers (when margin high or low commands are issued to the DAC) using the step size and time-period per step set in CODE-STEP-X and SLEW-RATE-X bits in the DAC-X-FUNC-CONFIG register:

- SLEW-RATE-X defines the time-period per step at which the digital slew updates.
- CODE-STEP-X defines the number of LSBs by which the output value changes at each update, for the corresponding channels.

Table 6-4 and Table 6-5 show different settings available for CODE-STEP-X and SLEW-RATE-X. With the default slew rate control setting of no-slew, the output changes immediately at a rate limited by the output drive circuitry and the attached load.

When the slew rate control feature is used, the output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output as shown in Figure 6-12. Do not write to CODE-STEP-X, SLEW-RATE-X, or DAC-X-DATA during the output slew operation. Equation 6 provides the equation for the calculating the slew time (t_{SLEW}).

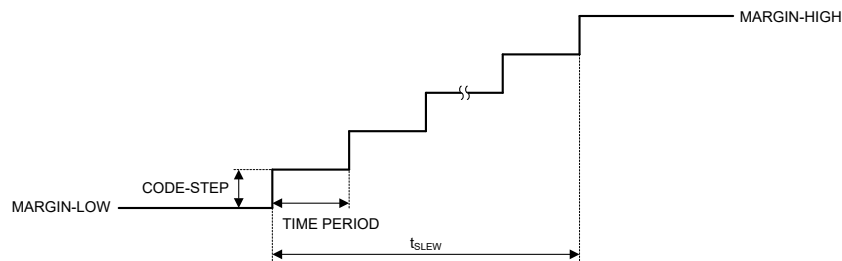


Figure 6-12. Programmable Slew-Rate Control

$$t_{\text{SLEW}} = \text{SLEW_RATE} \times \text{CEILING}\left(\frac{\text{MARGIN_HIGH} - \text{MARGIN_LOW}}{\text{CODE_STEP}} + 1\right) \quad (6)$$

where:

- SLEW_RATE is the SLEW-RATE-X setting as specified in Table 6-5.
- CODE_STEP is the CODE-STEP-X setting as specified in Table 6-4.
- MARGIN_HIGH is the decimal value of the DAC-X-MAGIN-HIGH bits specified in the DAC-X-MARGIN-HIGH register.
- MARGIN_LOW is the decimal value of the DAC-X-MAGIN-LOW bits specified in the DAC-X-MARGIN-LOW register.

Table 6-4. Code Step

REGISTER	CODE-STEP-X[2]	CODE-STEP-X[1]	CODE-STEP-X[0]	CODE STEP SIZE
DAC-X-FUNC-CONFIG	0	0	0	1 LSB (default)
	0	0	1	2 LSB
	0	1	0	3 LSB
	0	1	1	4 LSB
	1	0	0	6 LSB
	1	0	1	8 LSB
	1	1	0	16 LSB
	1	1	1	32 LSB

Table 6-5. Slew Rate

REGISTER	SLEW-RATE-X[3]	SLEW-RATE-X[2]	SLEW-RATE-X[1]	SLEW-RATE-X[0]	TIME PERIOD (PER STEP)
DAC-X-FUNC-CONFIG	0	0	0	0	No slew (default)
	0	0	0	1	4µs
	0	0	1	0	8µs
	0	0	1	1	12µs
	0	1	0	0	18µs
	0	1	0	1	27.04µs
	0	1	1	0	40.48µs
	0	1	1	1	60.72µs
	1	0	0	0	91.12µs
	1	0	0	1	136.72µs
	1	0	1	0	239.2µs
	1	0	1	1	418.64µs
	1	1	0	0	732.56µs
	1	1	0	1	1282µs
	1	1	1	0	2563.96µs
	1	1	1	1	5127.92µs

6.4.6 Fault-Dump Mode

The AFE53004W provides a feature to save a few registers into the NVM when the FAULT-DUMP bit is triggered or the GPIO mapped to fault-dump (as shown in [Table 6-19](#)) is triggered. This feature is useful in system-level fault management to capture the state of the device or system just before a fault is triggered, to allow diagnosis after the fault has occurred. The registers saved when fault-dump is triggered are:

- CMP-STATUS[7:0]
- DAC-0-DATA[15:8]
- DAC-1-DATA[15:8]
- DAC-2-DATA[15:8]
- DAC-3-DATA[15:8]
- ADC-DATA [15:0]

Note

When the fault-dump cycle is in progress, any change in the data can corrupt the final outcome. Make sure the comparator and the DAC codes are stable during the NVM write cycle.

[Table 6-6](#) shows the storage format of the registers in the NVM.

Table 6-6. Fault-Dump NVM Storage Format

NVM ROWS	B31-B24	B23-B16	B15-B8	B7-B0
Row1	CMP-STATUS[7:0]	ADC-DATA[15:0]		Don't care
Row2	DAC-0-DATA[15:8]	DAC-1-DATA[15:8]	DAC-2-DATA[15:8]	DAC-3-DATA[15:8]

The data captured in the NVM after the fault dump can be read in a specific sequence:

1. Set the EE-READ-ADDR bit to 0b in the COMMON-CONFIG register, to select row1 of the NVM.
2. Trigger the read of the selected NVM row by writing 1 to the READ-ONE-TRIG in the COMMON-TRIGGER register; this bit autoresets. This action copies that data from the selected NVM row to SRAM addresses 0x9D (LSB 16 bits from the NVM) and 0x9E (MSB 16 bits from the NVM).
3. To read the SRAM data:
 - a. Write 0x009D to the SRAM-CONFIG register.
 - b. Read the data from the SRAM-DATA register to get the LSB 16 bits.
 - c. Write 0x009E to the SRAM-CONFIG register.

- d. Read the data from the SRAM-DATA register again to get the MSB bits.
4. Set the EE-READ-ADDR bit to 1b in the COMMON-CONFIG register, to select row2 of the NVM. Repeat steps 2 and 3.

6.4.7 High-Impedance Output and $\overline{\text{PROTECT}}$ Input

All the DAC output channels remain in high-impedance (Hi-Z) when VDD is off. Figure 6-13 shows a simplified schematic of AFEx3004W used in a voltage margining application. The series resistor R_S is needed in voltage-output mode, but is optional in current-output mode. Almost all linear regulators and DC/DC converters have a feedback voltage of $\leq 1.25\text{V}$. The low-leakage currents at the outputs are maintained for V_{FB} of $\leq 1.25\text{V}$. Thus, for all practical purposes, the DAC outputs appear as Hi-Z when VDD of the DAC is off in voltage margining and scaling applications. This feature allows for seamless integration of the AFEx3004W into a system without any need for additional power-supply sequencing for the DAC.

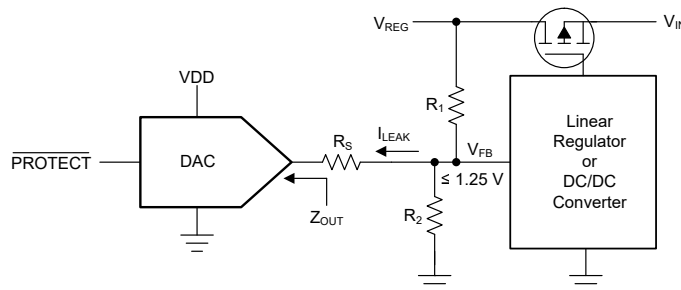


Figure 6-13. High-Impedance (Hi-Z) Output and $\overline{\text{PROTECT}}$ Input

The DAC channels power down to Hi-Z at boot up. The outputs can power up with a preprogrammed code that corresponds to the nominal output of the DC/DC converter or the linear regulator. This feature allows for smooth power up and power down of the DAC without impacting the feedback loop of the DC/DC converter or the linear regulator.

The GPIO pin of the AFEx3004W can be configured as a $\overline{\text{PROTECT}}$ function; see also Table 6-19. $\overline{\text{PROTECT}}$ takes the DAC outputs to a predictable state with a slewed or direct transition. This function is useful in systems where a fault condition (such as a brownout), a subsystem failure, or a software crash requires that the DAC outputs reach a predefined state without the involvement of a processor. The detected event can be fed to the GPIO pin that is configured as the $\overline{\text{PROTECT}}$ input. The $\overline{\text{PROTECT}}$ function is also triggered using the $\overline{\text{PROTECT}}$ bit in the COMMON-TRIGGER register. Configure the behavior of the $\overline{\text{PROTECT}}$ function in the $\overline{\text{PROTECT-CONFIG}}$ field in the DEVICE-MODE-CONFIG register; see also Table 6-7.

Note

- After the $\overline{\text{PROTECT}}$ function is triggered, the write functionality is disabled on the communication interface until the function is completed.
- The $\overline{\text{PROTECT-FLAG}}$ bit in the CMP-STATUS register is set to 1 when the $\overline{\text{PROTECT}}$ function is triggered. To poll this bit, read the CMP-STATUS register. After the $\overline{\text{PROTECT}}$ function is complete, a read command on the CMP-STATUS register resets the $\overline{\text{PROTECT-FLAG}}$ bit.

Table 6-7. $\overline{\text{PROTECT}}$ Function Configuration

PROTECT-CONFIG FIELD	FUNCTION
00	Switch to Hi-Z power-down (no slew).
01	Switch to DAC code stored in NVM (no slew) and then switch to Hi-Z power-down.
10	Slew to margin-low code and then switch to Hi-Z power-down.
11	Slew to margin-high code and then switch to Hi-Z power-down.

6.4.8 PMBus Compatibility Mode

The PMBus protocol is an I²C-based communication standard for power-supply management. PMBus contains standard command codes tailored to power supply applications. The AFE53004W implement some PMBus commands such as *Turn Off*, *Turn On*, *Margin Low*, *Margin High*, *Communication Failure Alert Bit (CML)*, as well as *PMBUS revision*. Figure 6-14 shows typical PMBus connections. The EN-PMBUS bit in the INTERFACE-CONFIG register must be set to 1 to enable the PMBus protocol.

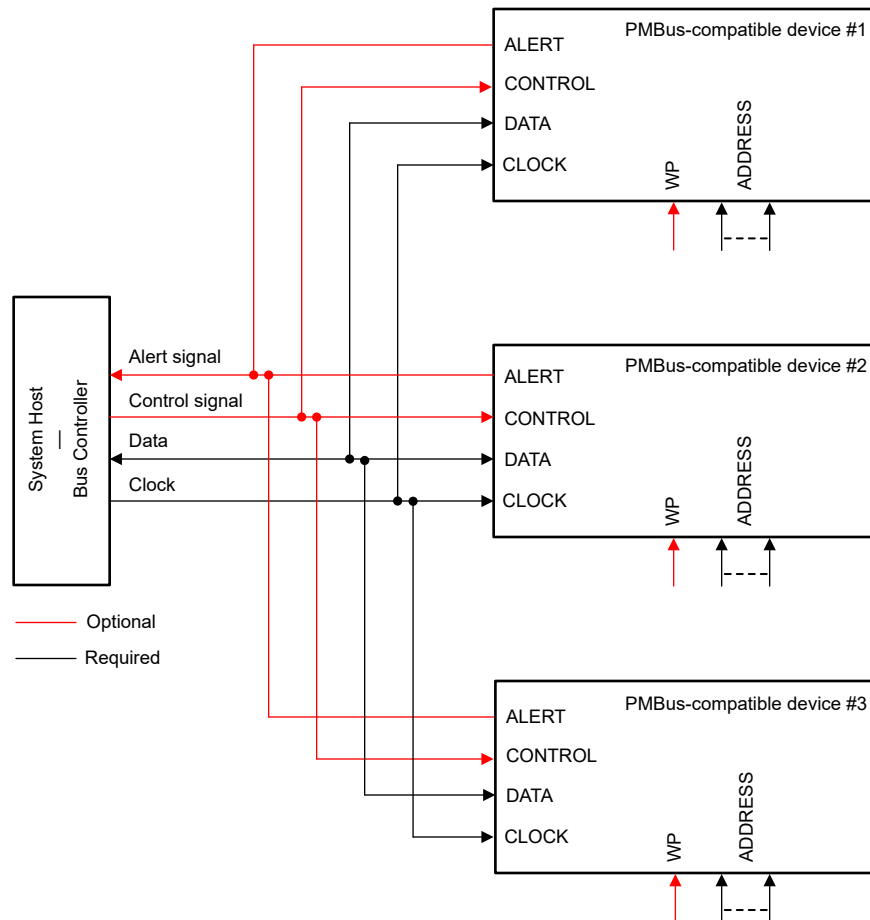


Figure 6-14. PMBus Connections

Similar to I²C, PMBus is a variable length packet of 8-bit data bytes, each with a receiver acknowledge, wrapped between a start and stop bit. The first byte is always a 7-bit *target address* followed by a *write* bit, sometimes called the *even address* that identifies the intended receiver of the packet. The second byte is an 8-bit *command* byte, identifying the PMBus command being transmitted using the respective command code. After the command byte, the transmitter either sends data associated with the command to write to the receiver command register (from least significant byte to most significant byte, as shown in [Table 6-8](#)), or sends a new start bit indicating the desire to read the data associated with the command register from the receiver. Then the receiver transmits the data following the same least significant byte first format (see [Table 6-9](#)).

Table 6-8. PMBus Update Sequence

MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte Section 6.5.2.2.1				Command byte Section 6.5.2.2.2				Data byte - LSDB				Data byte - MSDB (Optional)			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

Table 6-9. PMBus Read Sequence

S	MSB	...	R/W (0)	ACK	MSB	...	LSB	ACK	Sr	MSB	...	R/W (1)	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK			
	ADDRESS BYTE Section 6.5.2.2.1				COMMAND BYTE Section 6.5.2.2.2				Sr	ADDRESS BYTE Section 6.5.2.2.1				LSDB				MSDB (Optional)						
From Controller				Target	From Controller				Target	From Controller				Target	From Target				Controller	From Target				Controller

The AFEx3004W I²C interface implements some of the PMBus commands. [Table 6-10](#) shows the supported PMBus commands that are implemented in AFEx3004W. The DAC uses DAC-X-MARGIN-LOW, DAC-X-MARGIN-HIGH bits, SLEW-RATE-X, and CODE-STEP-X bits for PMBUS-OPERATION-CMD-X. To access multiple channels, write the PMBus page address as specified in the *Register Names* table in the *Register Map* section to the PMBUS-PAGE register first, followed by a write to the channel-specific register.

Table 6-10. PMBus Operation Commands

REGISTER	PMBUS-OPERATION-CMD-X[15:8]	DESCRIPTION
PMBUS-OP-CMD-X	00h	Turn off
	80h	Turn on
	94h	Margin low
	A4h	Margin high

The AFEx3004W also implement PMBus features such as group command protocol and communication time-out failure. The CML bit in the PMBUS-CML register indicates a communication fault in the PMBus. This bit is reset by writing 1.

To get the PMBus version, read the PMBUS-VERSION register.

6.4.9 Function Generation

The AFE53004W implement a continuous function or waveform generation feature. These devices can generate a triangular wave, sawtooth wave, and sine wave independently for every channel.

6.4.9.1 Triangular Waveform Generation

Figure 6-15 shows that the triangular waveform uses the DAC-X-MARGIN-LOW (FUNCTION-MIN) and DAC-X-MARGIN-HIGH (FUNCTION-MAX) registers for minimum and maximum levels, respectively. The frequency of the waveform depends on the min and max levels, CODE-STEP and SLEW-RATE settings as shown in Equation 7. An external RC load with a time-constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-X and SLEW-RATE-X settings are available in the DAC-X-FUNC-CONFIG register. Writing 0b000 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register selects triangular waveform.

$$f_{\text{TRIANGLE}} = \frac{1}{2 \times \text{TIME_STEP} \times \text{CEILING}\left(\frac{\text{FUNCTION_MAX} - \text{FUNCTION_MIN}}{\text{CODE_STEP}}\right)} \quad (7)$$

where:

- TIME_STEP is the SLEW-RATE-X setting as specified in Table 6-5.
- CODE_STEP is the CODE-STEP-X setting as specified in Table 6-4.
- FUNCTION_MAX is the decimal value of DAC-X-MAGIN-HIGH bits specified in the DAC-X-MARGIN-HIGH register.
- FUNCTION_MIN is the decimal value of the DAC-X-MAGIN-LOW bits specified in the DAC-X-MARGIN-LOW register.

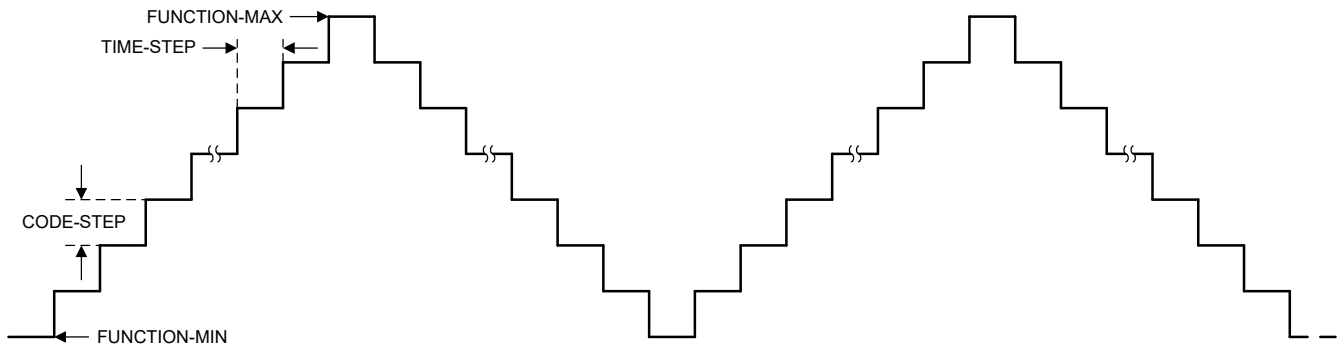


Figure 6-15. Triangle Waveform

6.4.9.2 Sawtooth Waveform Generation

Figure 6-16 shows the sawtooth and the inverse sawtooth waveforms use the DAC-X-MARGIN-LOW (FUNCTION-MIN) and DAC-X-MARGIN-HIGH (FUNCTION-MAX) registers for minimum and maximum levels, respectively. The frequency of the waveform depends on the min and max levels, CODE-STEP and SLEW-RATE settings as shown in Equation 8. An external RC load with a time constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-X and SLEW-RATE-X settings are available in the DAC-X-FUNC-CONFIG register. Write 0b001 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register to select sawtooth waveform, and write 0b010 to select inverse sawtooth waveform.

$$f_{\text{SAWTOOTH}} = \frac{1}{\text{TIME_STEP} \times \text{CEILING}\left(\frac{\text{FUNCTION_MAX} - \text{FUNCTION_MIN}}{\text{CODE_STEP}} + 1\right)} \quad (8)$$

where:

- TIME_STEP is the SLEW-RATE-X setting as specified in Table 6-5.
- CODE_STEP is the CODE-STEP-X setting as specified in Table 6-4.
- FUNCTION_MAX is the decimal value of the DAC-X-MARGIN-HIGH bits specified in the DAC-X-MARGIN-HIGH register.
- FUNCTION_MIN is the decimal value of the DAC-X-MARGIN-LOW bits specified in the DAC-X-MARGIN-LOW.

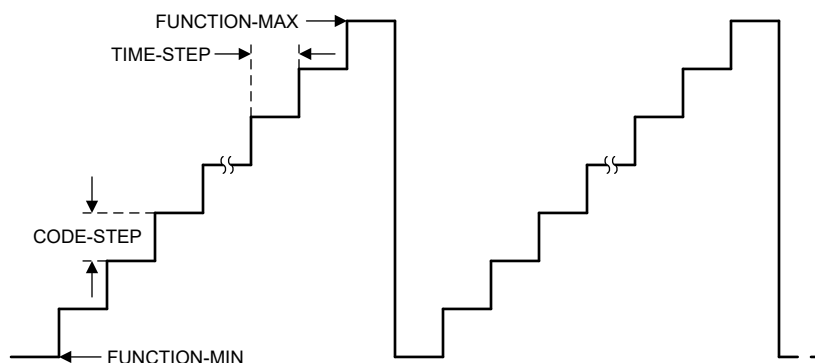


Figure 6-16. Sawtooth Waveform

6.4.9.3 Sine Waveform Generation

The sine wave function uses 24 preprogrammed points per cycle. The frequency of the sine wave depends on the SLEW-RATE settings as shown in Equation 9:

$$f_{\text{SINE_WAVE}} = \frac{1}{24 \times \text{SLEW_RATE}} \quad (9)$$

where SLEW_RATE is the SLEW-RATE-X setting as specified in Table 6-5.

An external RC load with a time constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The SLEW-RATE-X setting is available in the DAC-X-FUNC-CONFIG register. Writing 0b100 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register selects sine wave. The codes for the sine wave are fixed. Use the gain settings at the output amplifier for changing the full-scale output using the internal reference option. The gain settings are accessible through the VOUT-GAIN-X bits in the DAC-X-VOUT-CMP-CONFIG register. Table 6-11 shows the list of hard-coded discrete points for the sine wave with 12-bit resolution and Figure 6-17 shows the pictorial representation of the sine wave. There are four phase settings available for the sine wave that are selected using the PHASE-SEL-X bit in the DAC-X-FUNC-CONFIG register.

Table 6-11. Sine Wave Data Points

SEQUENCE	12-BIT VALUE	SEQUENCE	12-BIT VALUE
0 (0° phase start)	0x800	12	0x800
1	0x9A8	13	0x658
2	0xB33	14	0x4CD
3	0xC87	15	0x379
4	0xD8B	16 (240° phase start)	0x275
5	0xE2F	17	0x1D1
6 (90° phase start)	0xE66	18	0x19A
7	0xE2F	19	0x1D1
8 (120° phase start)	0xD8B	20	0x275
9	0xC87	21	0x379
10	0xB33	22	0x4CD
11	0x9A8	23	0x658

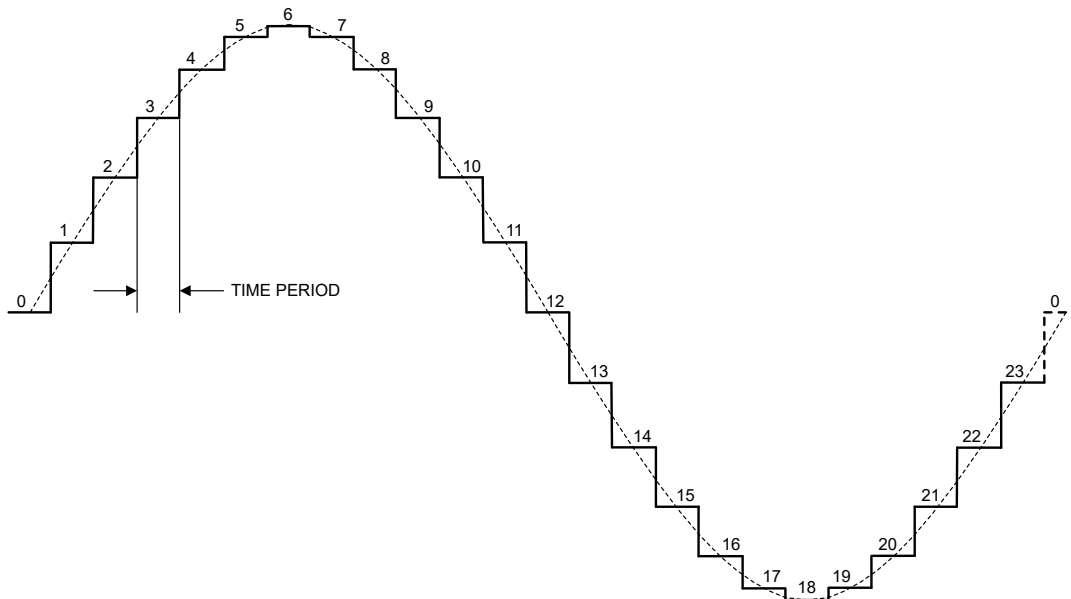


Figure 6-17. Sine Wave Generation

6.4.10 Device Reset and Fault Management

This section provides the details of power-on-reset (POR), software reset, and other diagnostics and fault-management features of AFE53004W.

6.4.10.1 Power-On Reset (POR)

The AFE53004W family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the AFE53004W is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels (as indicated in Figure 6-18) to discharge the internal capacitors and reset the device at power up. To initiate a POR, ensure that V_{DD} is less than 0.7V for at least 1ms. When V_{DD} drops to less than 1.65V, but remains greater than 0.7V (shown as the undefined region), the device does not always reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65V, a POR does not occur.

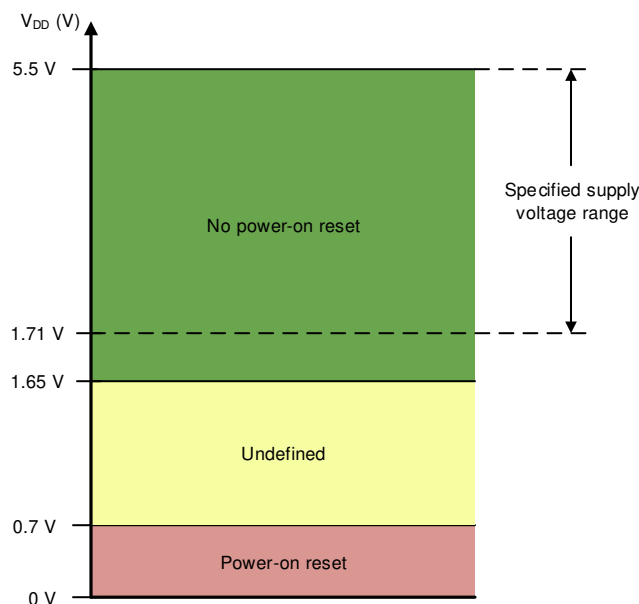


Figure 6-18. Threshold Levels for V_{DD} POR Circuit

6.4.10.2 External Reset

An external reset to the device can be triggered through the GPIO pin or through the register map. To initiate a device software reset event, write the reserved code 1010b to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event. The GPIO pin can be configured as a $\overline{\text{RESET}}$ pin as shown in Table 6-19. This configuration must be programmed into the NVM so that the setting is not cleared after the device reset. The $\overline{\text{RESET}}$ input must be a low pulse. The device starts the boot-up sequence after the falling edge of the $\overline{\text{RESET}}$ input. The rising edge of the $\overline{\text{RESET}}$ input does not have any effect.

6.4.10.3 Register-Map Lock

The AFE53004W implement a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. However, the software reset function through the COMMON-TRIGGER register is not blocked when using I²C interface. To bypass the DEV-LOCK setting, write 0101b to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

6.4.10.4 NVM Cyclic Redundancy Check (CRC)

The AFE53004W implement a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in AFE53004W:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of internal NVM bits. The CRC feature is implemented by storing a 16-Bit CRC (CRC-16-CCITT) along with the NVM data each time NVM program operation (write or reload) is performed and during the device start up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM. The alarm bits are set only at boot-up.

6.4.10.4.1 NVM-CRC-FAIL-USER Bit

A logic 1 on NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see [Section 6.4.10.2](#)) command, or cycle power to the DAC. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

6.4.10.4.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset (see [Section 6.4.10.2](#)) command or cycle power to the DAC. A permanent failure in the NVM makes the device unusable.

6.4.11 Power-Down Mode

The AFE53004W output amplifier and internal reference can be independently powered down through the EN-INT-REF, VOUT-PDN-X, and IOUT-PDN-X bits in the COMMON-CONFIG register, as shown in [Figure 6-4](#). At power up, the DAC output and the internal reference are disabled by default. In power-down mode, the DAC outputs (OUTx pins) are in a high-impedance state. To change this state to 10kΩ-AGND or 100kΩ-AGND in the voltage-output mode (at power up), use the VOUT-PDN-X bits. The power-down state for current-output mode is always high-impedance.

The DAC power-up state can be programmed to any state (power-down or normal mode) using the NVM. [Table 6-12](#) shows the DAC power-down bits. The individual channel power-down bits or the global device power-down function can be mapped to the GPIO pin using the GPIO-CONFIG register.

Table 6-12. DAC Power-Down Bits

REGISTER	VOUT-PDN-X[1]	VOUT-PDN-X[0]	IOUT-PDN-X	DESCRIPTION
COMMON-CONFIG	0	0	1	Power up VOUT-X.
	0	1	1	Power down VOUT-X with 10kΩ to AGND. Power down IOUT-X to Hi-Z.
	1	0	1	Power down VOUT-X with 100kΩ to AGND. Power down IOUT-X to Hi-Z.
	1	1	1	Power down VOUT-X to Hi-Z. Power down IOUT-X to Hi-Z (default).
	1	1	0	Power down VOUT-X to Hi-Z. Power up IOUT-X.

6.5 Programming

The AFE53004W are programmed through either a 3-wire SPI or 2-wire I²C interface. A 4-wire SPI mode is enabled by mapping the GPIO pin as SDO. The SPI readback operates at a lower SCLK than the standard SPI write operation. The type of interface is determined based on the first protocol to communicate after device power up. After the interface type is determined, the device ignores any change in the type while the device is on. The interface type can be changed after a power cycle.

6.5.1 SPI Programming Mode

To initiate an SPI access cycle for the AFE53004W, assert the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, is a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for AFE53004W is 24 bits long. Therefore, ensure that the $\overline{\text{SYNC}}$ stays low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. By default, the SDO pin is not enabled (three-wire SPI). In the three-wire SPI mode, if the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDI signals are blocked, and SDO becomes Hi-Z to allow data readback from other devices connected on the bus.

Table 6-13 and Figure 6-19 describe the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

Table 6-13. SPI Read/Write Access Cycle

BIT	FIELD	DESCRIPTION
23	R/W	Identifies the communication as a read or write command to the address register: R/W = 0 sets a write operation. R/W = 1 sets a read operation
22-16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are <i>Don't care</i> values.

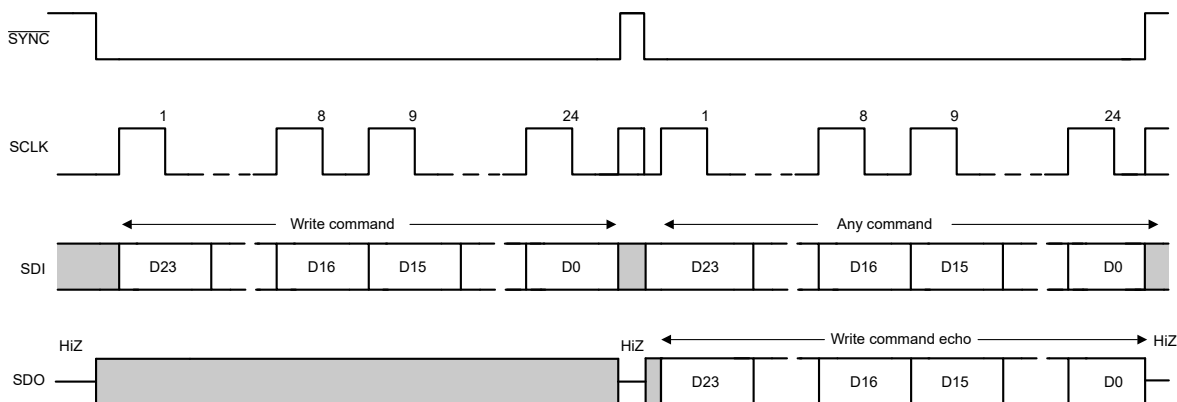


Figure 6-19. SPI Write Cycle

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. This configuration is called four-wire SPI. A read operation is initiated by issuing a read command access cycle. After the read command, issue a second access cycle to get the requested data. Table 6-14 and Figure 6-20 show the output data format. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit; see also Figure 5-3.

Table 6-14. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/W	Echo R/W from previous access cycle
22-16	A[6:0]	Echo register address from previous access cycle
15-0	DI[15:0]	Readback data requested on previous access cycle

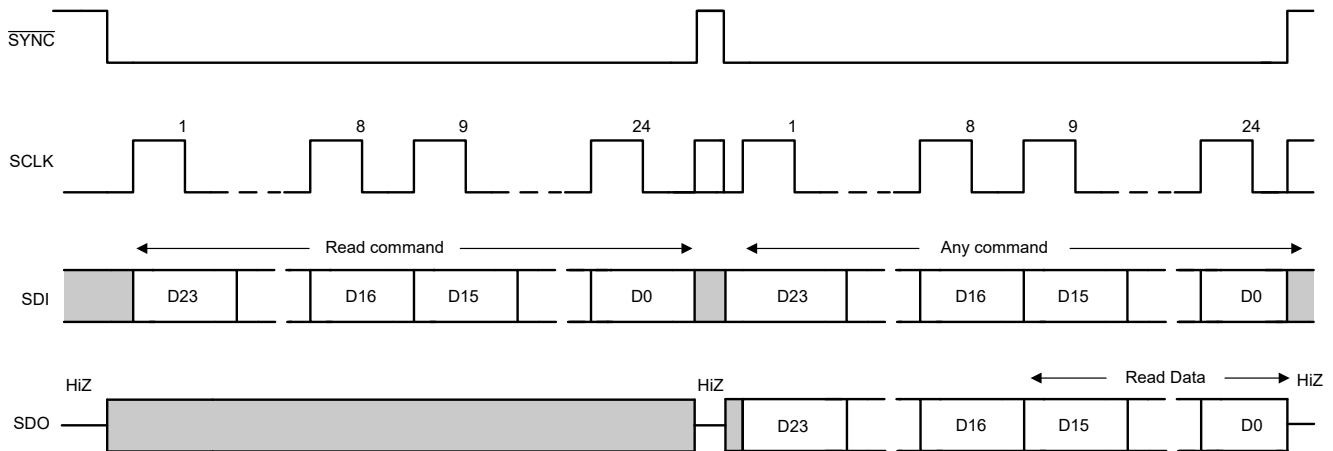


Figure 6-20. SPI Read Cycle

The daisy-chain operation is also enabled with the SDO pin. In daisy-chain mode, multiple devices are connected in a *chain* with the SDO pin of one device is connected to SDI pin of the following device; see [Figure 6-21](#). The SPI host drives the SDI pin of the first device in the chain. The SDO pin of the last device in the chain is connected to the POCI pin of the SPI host. In four-wire SPI mode, if the access cycle contains multiples of 24 clock edges, only the last 24 bits are used by the device first device in the chain. If the access cycle contains clock edges that are not in multiples of 24, the SPI packet is ignored by the device. [Figure 6-22](#) describes the packet format for the daisy-chain write cycle.

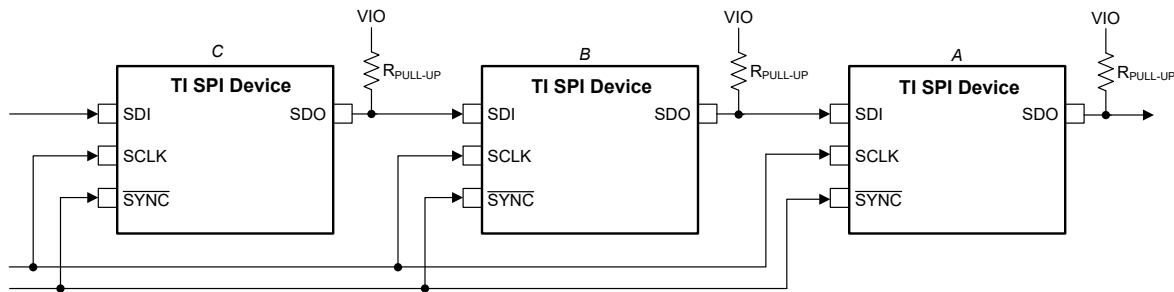


Figure 6-21. SPI Daisy-Chain Connection

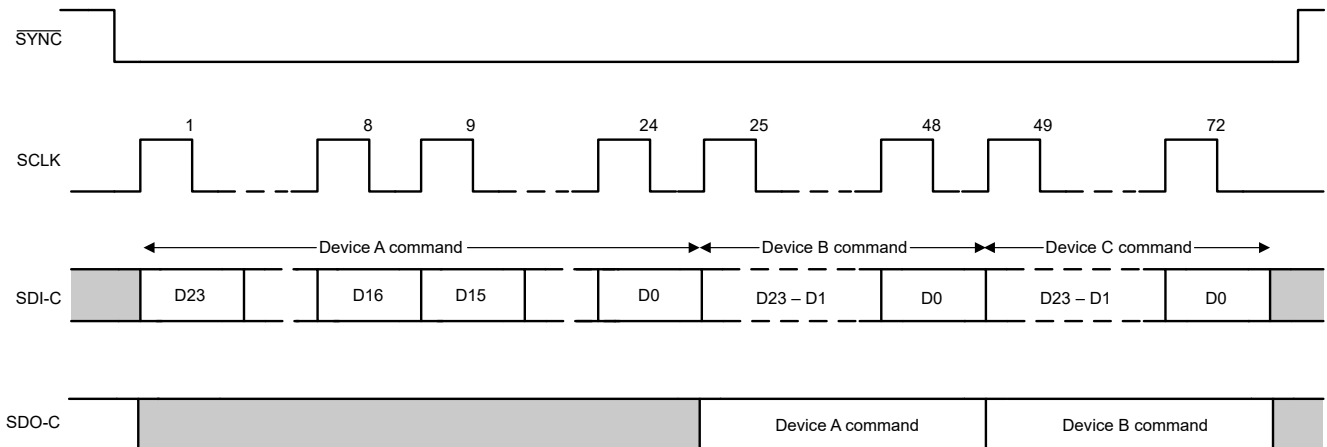


Figure 6-22. SPI Daisy-Chain Write Cycle

6.5.2 I²C Programming Mode

The AFE53004W devices have a 2-wire serial interface (SCL and SDA), and one address pin (A0), as shown in the pin diagram in the *Pin Configuration and Functions* section. The I²C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA and SCL.

The I²C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I²C bus is typically a microcontroller or digital signal processor (DSP). The AFE53004W family operates as a target on the I²C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

Typically, the AFE53004W family operates as a target receiver. A controller writes to the AFE53004W, a target receiver. However, if a controller requires the AFE53004W internal register data, the AFE53004W operate as a target transmitter. In this case, the controller reads from the AFE53004W. According to I²C terminology, read and write refer to the controller.

The AFE53004W family supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3mA; similar to the case of standard and fast modes. The AFE53004W family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle, as shown in [Figure 6-23](#).

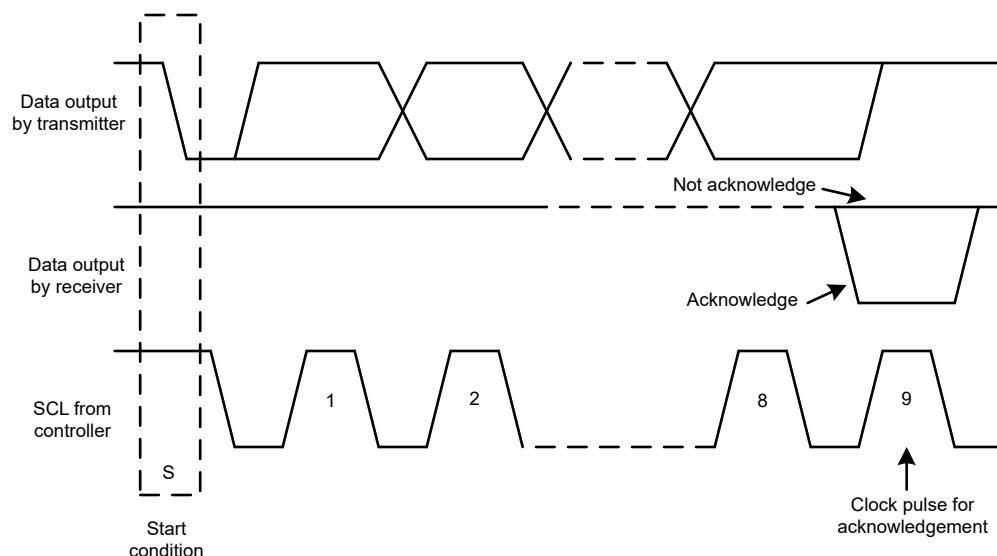


Figure 6-23. Acknowledge and Not Acknowledge on the I²C Bus

6.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in [Figure 6-24](#). All I²C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/W) on the SDA line. During all transmissions, the controller makes sure that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in [Figure 6-25](#). All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle, as shown in [Figure 6-23](#). When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit (R/W bit 0) or receive (R/W bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue as long as necessary.
4. To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high, as shown in [Figure 6-24](#). This action releases the bus and stops the communication link with the addressed target. All I²C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.

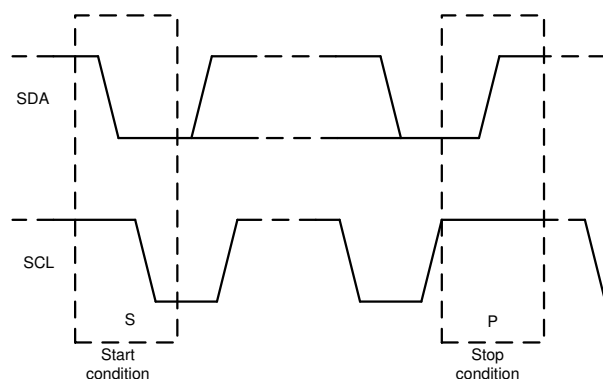


Figure 6-24. Start and Stop Conditions

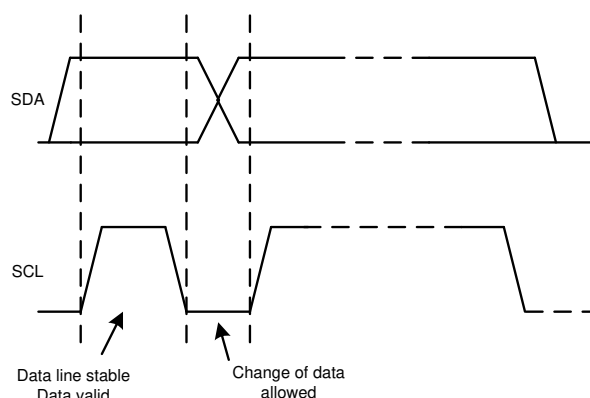


Figure 6-25. Bit Transfer on the I²C Bus

6.5.2.2 I²C Update Sequence

For a single update, the AFE53004W require a start condition, a valid I²C address byte, a command byte, and two data bytes, as listed in [Table 6-15](#).

Table 6-15. Update Sequence

MSB	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte Section 6.5.2.2.1				Command byte Section 6.5.2.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the AFE53004W family acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in [Figure 6-26](#). These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C address byte selects the AFE53004W.

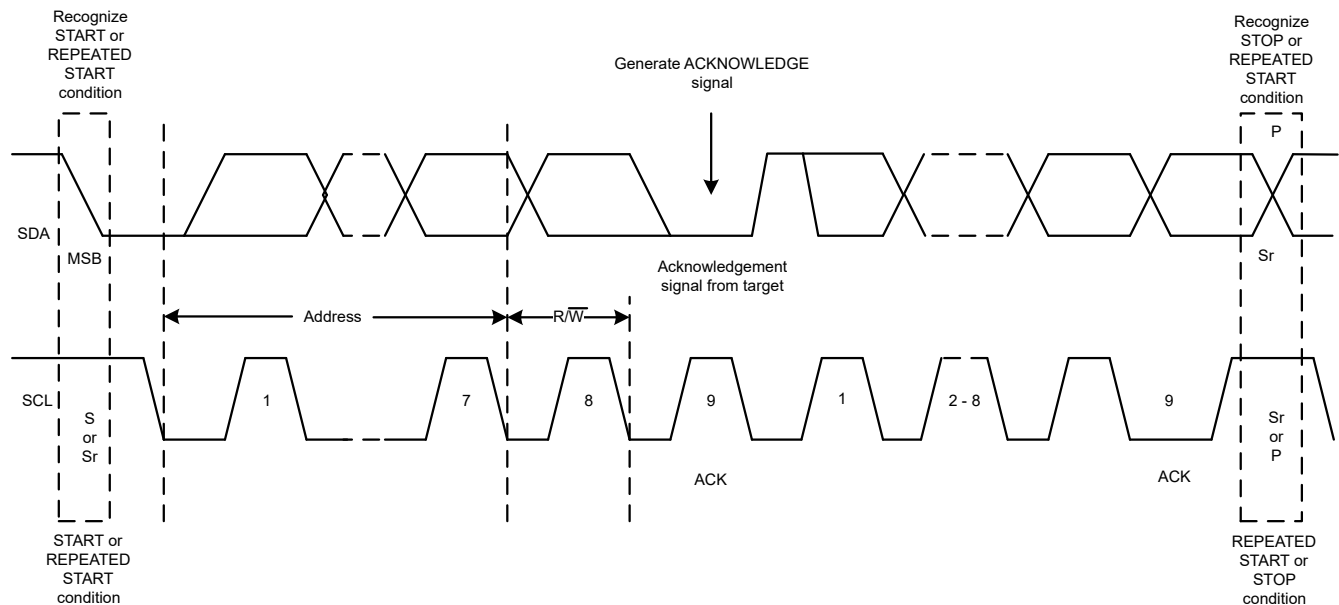


Figure 6-26. I²C Bus Protocol

The command byte sets the operating mode of the selected AFE53004W device. For a data update to occur when the operating mode is selected by this byte, the AFE53004W device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The AFE53004W device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400kHz), the maximum DAC update rate is limited to 10kSPS. Using fast mode plus (clock = 1MHz), the maximum DAC update rate is limited to 25kSPS. When a stop condition is received, the AFE53004W device releases the I²C bus and awaits a new start condition.

6.5.2.2.1 Address Byte

The address byte, as shown in [Table 6-16](#), is the first byte received from the controller device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to [Table 6-17](#).

Table 6-16. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
General address	1	0	0	1	See Table 6-17 (target address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

Table 6-17. Address Format

TARGET ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

The AFEx3004W supports broadcast addressing, which is used for synchronously updating or powering down multiple AFEx3004W devices. When the broadcast address is used, the AFEx3004W responds regardless of the address pin state. Broadcast is supported only in write mode.

6.5.2.2.2 Command Byte

The *Register Names* table in the *Register Map* section lists the command byte in the ADDRESS column.

6.5.2.3 I²C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the $\overline{R/\overline{W}}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the $\overline{R/\overline{W}}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

The broadcast address cannot be used for reading.

Table 6-18. Read Sequence

S	MSB	...	R/W (0)	ACK	MSB	...	LSB	ACK	Sr	MSB	...	R/W (1)	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
	ADDRESS BYTE Section 6.5.2.2.1				COMMAND BYTE Section 6.5.2.2.2				Sr	ADDRESS BYTE Section 6.5.2.2.1				MSDB				LSDB			
	From Controller			Target	From Controller			Target		From Controller			Target	From Target			Controller	From Target			Controller

6.5.3 General-Purpose Input/Output (GPIO) Modes

Together with I²C and SPI, the AFEx3004W also support a GPIO that can be configured in the NVM for multiple functions. This pin allows for updating the DAC output channels and reading status bits without using the programming interface, thus enabling processor-less operation. In the GPIO-CONFIG register, write 1 to the GPI-EN bit to set the GPIO pin as an input, or write 1 to the GPO-EN bit to set the pin as output. There are global and channel-specific functions mapped to the GPIO pin. For channel-specific functions, select the channels using the GPI-CH-SEL field in the GPIO-CONFIG register. [Table 6-19](#) lists the functional options available for the GPIO as input and [Table 6-20](#) lists the options for the GPIO as output. Some of the GP input operations are edge-triggered after the device boots up. After the power supply ramps up, the device registers the GPI level and executes the associated command. This feature allows the user to configure the initial output state at power-on. By default, the GPIO pin is not mapped to any operation. When the GPIO pin is mapped to a specific input function, the corresponding software bit functionality is disabled to avoid a race condition. When used as a $\overline{\text{RESET}}$ input, the GPIO pin must transmit an active-low pulse for triggering a device reset. All other constraints of the functions are applied to the GPIO-based trigger.

Note

Pull the GPIO pin to high or low when not used. When the GPIO pin is used as $\overline{\text{RESET}}$, the configuration must be programmed into the NVM. Otherwise, the setting is cleared after the device resets.

Table 6-19. General-Purpose Input Function Map

REGISTER	BIT FIELD	VALUE	CHANNELS	GPIO EDGE / LEVEL	FUNCTION
GPIO-CONFIG	GPI-CONFIG	0010	All	Falling-edge	Trigger FAULT-DUMP
				Rising-edge	No effect
		0011	As per GPI-CH-SEL	Falling-edge	IOUT power-down
				Rising-edge	IOUT power-up
		0100	As per GPI-CH-SEL	Falling-edge	VOUT power-down. Pulldown resistor as per the VOUT-PDN-X setting
				Rising-edge	VOUT power-up
		0101	All	Falling-edge	Trigger PROTECT function
				Rising-edge	No effect
		0111	All	Falling-edge	Trigger CLR function
				Rising-edge	No effect
		1000	As per GPI-CH-SEL. Both the SYNC-CONFIG-X and the GPI-CH-SEL must be configured for every channel.	Falling-edge	Trigger LDAC function
				Rising-edge	No effect
		1001	As per GPI-CH-SEL	Falling-edge	Stop function generation
				Rising-edge	Start function generation
		1010	As per GPI-CH-SEL	Falling-edge	Trigger margin-low
				Rising-edge	Trigger margin-high
		1011	All	Low pulse	Trigger device RESET. The RESET configuration must be programmed into the NVM.
				Rising-edge	No effect
		1100	All	Falling-edge	Allows NVM programming
				Rising-edge	Blocks NVM programming
		1101	All	Falling-edge	Allows register map update
				Rising-edge	Blocks register map write except a write to the DEV-UNLOCK field through I ² C or SPI and the RESET fields through I ² C
		Others	N/A	N/A	Not applicable

Table 6-20. General-Purpose Output (STATUS) Function Map

REGISTER	BIT FIELD	VALUE	FUNCTION
GPIO-CONFIG	GPO-CONFIG	0001	NVM-BUSY
		0100	DAC-0-BUSY
		0101	DAC-1-BUSY
		0110	DAC-2-BUSY
		0111	DAC-3-BUSY
		1000	WIN-CMP-0
		1001	WIN-CMP-1
		1010	WIN-CMP-2
		1011	WIN-CMP-3
		Others	Not applicable

7 Register Map

Table 7-1. Register Map

REGISTER ⁽¹⁾	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)								
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
NOP	NOP																
DAC-X-MARGIN-HIGH	DAC-X-MARGIN-HIGH												x				
DAC-X-MARGIN-LOW	DAC-X-MARGIN-LOW												x				
DAC-X-VOUT-CMP-CONFIG	x			VOUT-GAIN-X				x					CMP-X-OD-EN	CMP-X-OUT-EN	CMP-X-HIZ-IN-DIS	CMP-X-INV-EN	CMP-X-EN
DAC-X-IOUT-MISC-CONFIG	x			IOUT-X-RANGE				x									
DAC-X-CMP-MODE-CONFIG	x				CMP-X-MODE			x									
DAC-X-FUNC-CONFIG	CLR-SEL-X	SYNC-CONFIG-X	BRD-CONFIG-X	FUNC-GEN-CONFIG-BLOCK-X													
DAC-X-DATA	DAC-X-DATA												x				
ADC-CONFIG-TRIG	RESERVED		ADC-EN	ADC-AVG		ADC-MUX-SEL			RESERVED			x				ADC-TRIG	
ADC-DATA	ADC-DATA										x		ADC-MUX-READBACK			ADC-DRDY	
COMMON-CONFIG	WIN-LATCH-EN	DEV-LOCK	EE-READ-ADDR	EN-INT-REF	VOUT-PDN-3		IOUT-PDN-3	VOUT-PDN-2		IOUT-PDN-2	VOUT-PDN-1		IOUT-PDN-1	VOUT-PDN-0		IOUT-PDN-0	
COMMON-TRIGGER	DEV-UNLOCK				RESET				LDAC	CLR	x	FAULT-DUMP	PROTECT	READ-ONE-TRIG	NVM-PROG	NVM-RELOAD	
COMMON-DAC-TRIG	RST-CMP-FLAG-0	TRIG-MAR-LO-0	TRIG-MAR-HI-0	START-FUNC-0	RST-CMP-FLAG-1	TRIG-MAR-LO-1	TRIG-MAR-HI-1	START-FUNC-1	RST-CMP-FLAG-2	TRIG-MAR-LO-2	TRIG-MAR-HI-2	START-FUNC-2	RST-CMP-FLAG-3	TRIG-MAR-LO-3	TRIG-MAR-HI-3	START-FUNC-3	
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	x	DAC-BUSY-3	DAC-BUSY-2	DAC-BUSY-1	DAC-BUSY-0	NVM-BUSY	DEVICE-ID								
CMP-STATUS	x							PROTECT-FLAG	WIN-CMP-3	WIN-CMP-2	WIN-CMP-1	WIN-CMP-0	CMP-FLAG-3	CMP-FLAG-2	CMP-FLAG-1	CMP-FLAG-0	
GPIO-CONFIG	GF-EN	x	GPO-EN	GPO-CONFIG				GPI-CH-SEL				GPI-CONFIG				GPI-EN	
DEVICE-MODE-CONFIG	RESERVED		DIS-MODE-IN	RESERVED			PROTECT-CONFIG		RESERVED			x					
INTERFACE-CONFIG	x			TIMEOUT-EN	x			EN-PMBUS	x					FSDO-EN	x	SDO-EN	
SRAM-CONFIG	x								SRAM-ADDR								
SRAM-DATA	SRAM-DATA																
DAC-X-DATA-8BIT	DAC-X-DATA-8BIT								x								
BRDCAST-DATA	BRDCAST-DATA												x				
PMBUS-PAGE	PMBUS-PAGE								NA								
PMBUS-OP-CMD	PMBUS-OPERATION-CMD-X								NA								
PMBUS-CML	x						CML	x	NA								
PMBUS-VERSION	PMBUS-VERSION								NA								

(1) The highlighted gray cells indicate the register bits or fields that are stored in the NVM.

Table 7-2. Register Names

I ² C/SPI ADDRESS	PMBUS PAGE ADDR	PMBUS REGISTER ADDR	REGISTER NAME	SECTION
00h	FFh	D0h	NOP	Section 7.1
01h	00h	25h	DAC-0-MARGIN-HIGH	Section 7.2
02h	00h	26h	DAC-0-MARGIN-LOW	Section 7.3
03h	FFh	D1h	DAC-0-VOOUT-CMP-CONFIG	Section 7.4
04h	FFh	D2h	DAC-0-IOUT-MISC-CONFIG	Section 7.5
05h	FFh	D3h	DAC-0-CMP-MODE-CONFIG	Section 7.6
06h	FFh	D4h	DAC-0-FUNC-CONFIG	Section 7.7
07h	01h	25h	DAC-1-MARGIN-HIGH	Section 7.2
08h	01h	26h	DAC-1-MARGIN-LOW	Section 7.3
09h	FFh	D5h	DAC-1-VOOUT-CMP-CONFIG	Section 7.4
0Ah	FFh	D6h	DAC-1-IOUT-MISC-CONFIG	Section 7.5
0Bh	FFh	D7h	DAC-1-CMP-MODE-CONFIG	Section 7.6
0Ch	FFh	D8h	DAC-1-FUNC-CONFIG	Section 7.7
0Dh	02h	25h	DAC-2-MARGIN-HIGH	Section 7.2
0Eh	02h	26h	DAC-2-MARGIN-LOW	Section 7.3
0Fh	FFh	D9h	DAC-2-VOOUT-CMP-CONFIG	Section 7.4
10h	FFh	DAh	DAC-2-IOUT-MISC-CONFIG	Section 7.5
11h	FFh	DBh	DAC-2-CMP-MODE-CONFIG	Section 7.6
12h	FFh	DCh	DAC-2-FUNC-CONFIG	Section 7.7
13h	03h	25h	DAC-3-MARGIN-HIGH	Section 7.2
14h	03h	26h	DAC-3-MARGIN-LOW	Section 7.3
15h	FFh	DDh	DAC-3-VOOUT-CMP-CONFIG	Section 7.4
16h	FFh	DEh	DAC-3-IOUT-MISC-CONFIG	Section 7.5
17h	FFh	DFh	DAC-3-CMP-MODE-CONFIG	Section 7.6
18h	FFh	E0h	DAC-3-FUNC-CONFIG	Section 7.7
19h	00h	21h	DAC-0-DATA	Section 7.8
1Ah	01h	21h	DAC-1-DATA	Section 7.8
1Bh	02h	21h	DAC-2-DATA	Section 7.8
1Ch	03h	21h	DAC-3-DATA	Section 7.8
1Dh	FFh	E1h	ADC-CONFIG-TRIG	Section 7.9
1Eh	FFh	E2h	ADC-DATA	Section 7.10
1Fh	FFh	E3h	COMMON-CONFIG	Section 7.11

Table 7-2. Register Names (continued)

I ² C/SPI ADDRESS	PMBUS PAGE ADDR	PMBUS REGISTER ADDR	REGISTER NAME	SECTION
20h	FFh	E4h	COMMON-TRIGGER	Section 7.12
21h	FFh	E5h	COMMON-DAC-TRIG	Section 7.13
22h	FFh	E6h	GENERAL-STATUS	Section 7.14
23h	FFh	E7h	CMP-STATUS	Section 7.15
24h	FFh	E8h	GPIO-CONFIG	Section 7.16
25h	FFh	E9h	DEVICE-MODE-CONFIG	Section 7.17
26h	FFh	EAh	INTERFACE-CONFIG	Section 7.18
2Bh	FFh	EFh	SRAM-CONFIG	Section 7.19
2Ch	FFh	F0h	SRAM-DATA	Section 7.20
40h	NA	NA	DAC-0-DATA-8BIT	Section 7.21
41h	NA	NA	DAC-1-DATA-8BIT	Section 7.21
42h	NA	NA	DAC-2-DATA-8BIT	Section 7.21
43h	NA	NA	DAC-3-DATA-8BIT	Section 7.21
50h	FFh	F1h	BRDCAST-DATA	Section 7.22
NA	All pages	00h	PMBUS-PAGE	Section 7.23
NA	00h	01h	PMBIS-OP-CMD-0	Section 7.24
NA	01h	01h	PMBUS-OP-CMD-1	Section 7.24
NA	02h	01h	PMBUS-OP-CMD-2	Section 7.24
NA	03h	01h	PMBUS-OP-CMD-3	Section 7.24
NA	All pages	78h	PMBUS-CML	Section 7.25
NA	All pages	98h	PMBUS-VERSION	Section 7.26

Table 7-3. Access Type Codes

Access Type	Code	Description
x	x	Don't care
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1 NOP Register (address = 00h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D0h

Figure 7-1. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R-0h															

Table 7-4. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R	0000h	No operation

7.2 DAC-X-MARGIN-HIGH Register (address = 01h, 07h, 0Dh, 13h) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 25h

Figure 7-2. DAC-X-MARGIN-HIGH Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-MARGIN-HIGH[11:0] DAC-X-MARGIN-HIGH[9:0] DAC-X-MARGIN-HIGH[7:0]												x			
R/W-000h														x-0h	

Table 7-5. DAC-X-MARGIN-HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-X-MARGIN-HIGH[11:0] DAC-X-MARGIN-HIGH[9:0] DAC-X-MARGIN-HIGH[7:0]	R/W	000h	Margin-high code for DAC output Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: AFE53004W VOUT: {DAC-X-MARGIN-HIGH[11:0]} AFE63004W VOUT: {DAC-X-MARGIN-HIGH[9:0], X, X} IOUT: {DAC-X-MARGIN-HIGH[7:0], X, X, X, X} x = Don't care bits.
3-0	x	x	0	Don't care bits

7.3 DAC-X-MARGIN-LOW Register (address = 02h, 08h, 0Eh, 14h) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 26h

Figure 7-3. DAC-X-MARGIN-LOW Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-MARGIN-LOW[11:0] DAC-X-MARGIN-LOW[9:0] DAC-X-MARGIN-LOW[7:0]												x			
R/W-000h														x-0h	

Table 7-6. DAC-X-MARGIN-LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-X-MARGIN-LOW[11:0] DAC-X-MARGIN-LOW[9:0] DAC-X-MARGIN-LOW[7:0]	R/W	000h	Margin-low code for DAC output Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: AFE53004W VOUT: {DAC-X-MARGIN-LOW[11:0]} AFE63004W VOUT: {DAC-x-MARGIN-LOW[9:0], x, x} IOUT: {DAC-X-MARGIN-LOW[7:0], x, x, x} x = Don't care bits.
3-0	x	x	0	Don't care

7.4 DAC-X-VOUT-CMP-CONFIG Register (address = 03h, 09h, 0Fh, 15h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D1h, D5h, D9h, DDh

Figure 7-4. DAC-X-VOUT-CMP-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x			VOUT-GAIN-X			x			CMP-X-OD-EN		CMP-X-OUT-EN	CMP-X-HIZ-IN-DIS	CMP-X-INV-EN	CMP-X-EN	
x-0h			R/W-0h			x-0h			R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-7. DAC-X-VOUT-CMP-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	x	x	0h	Don't care
12-10	VOUT-GAIN-X	R/W	0h	Voltage reference in DAC or ADC mode. 000: Gain = 1x, external reference on VREF pin 001: Gain = 1x, VDD as reference 010: Gain = 1.5x, internal reference 011: Gain = 2x, internal reference 100: Gain = 3x, internal reference 101: Gain = 4x, internal reference Others: Invalid
9-5	x	x	0h	Don't care
4	CMP-X-OD-EN	R/W	0	0: Set OUTx pin as push-pull 1: Set OUTx pin as open-drain in comparator mode (CMP-X-EN = 1 and CMP-X-OUT-EN = 1)
3	CMP-X-OUT-EN	R/W	0	0: Generate comparator output but consume internally 1: Bring comparator output to the respective OUTx pin
2	CMP-X-HIZ-IN-DIS	R/W	0	0: FBx input has high-impedance. Input voltage range is limited. 1: FBx input is connected to resistor divider and has finite impedance. Input voltage range is same as full-scale.
1	CMP-X-INV-EN	R/W	0	0: Do not invert the comparator output 1: Invert the comparator output
0	CMP-X-EN	R/W	0	Set to 1 for comparator or ADC mode. 0: Disable comparator mode 1: Enable comparator mode. Current-output must be in power-down. Voltage-output mode must be enabled.

7.5 DAC-X-IOUT-MISC-CONFIG Register (address = 04h, 0Ah, 10h, 16h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D2h, D6h, DAh, DEh

Figure 7-5. DAC-X-IOUT-MISC-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x			IOUT-RANGE-X					x							
x-0h			R/W-0h					x-0h							

Table 7-8. DAC-X-IOUT-MISC-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	x	x	0h	Don't care
12-9	IOUT-RANGE-X	R/W	0000	0000: 0μA to 25μA 0001: 0μA to 50μA 0010: 0μA to 125μA 0011: 0μA to 250μA 0100: 0μA to –24μA 0101: 0μA to –48μA 0110: 0μA to –120μA 0111: 0μA to –240μA 1000: –25μA to +25μA 1001: –50μA to +50μA 1010: –125μA to +125μA 1011: –250μA to +250μA Others: Invalid
8-0	x	x	000h	Don't care

7.6 DAC-X-CMP-MODE-CONFIG Register (address = 05h, 0Bh, 11h, 17h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D3h, D7h, DBh, DFh

Figure 7-6. DAC-X-CMP-MODE-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x				CMP-X-MODE		x									
x-0h				R/W-0h				x-0h							

Table 7-9. DAC-X-CMP-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	x	x	00h	Don't care
11-10	CMP-X-MODE	R/W	00	00: No hysteresis or window function 01: Hysteresis provided using DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers 10: Window comparator mode with DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers setting window bounds 11: Invalid
9-0	x	x	000h	Don't care

7.7 DAC-X-FUNC-CONFIG Register (address = 06h, 0Ch, 12h, 18h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D4h, D8h, DCh, E0h

Figure 7-7. DAC-X-FUNC-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR-SEL-X	SYNC-CONFIG-X	BRD-CONFIG-X	FUNC-GEN-CONFIG-BLOCK												
R/W-0h	R/W-0h	R/W-0h	R/W-000h												

Table 7-10. DAC-X-FUNC-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CLR-SEL-X	R/W	0	0: Clear DAC-X to zero-scale 1: Clear DAC-X to mid-scale
14	SYNC-CONFIG-X	R/W	0	0: DAC-X output updates immediately after a write command 1: DAC-X output updates with LDAC pin falling-edge or when the LDAC bit in the COMMON-TRIGGER register is set to 1
13	BRD-CONFIG-X	R/W	0	0: Do not update DAC-X with broadcast command 1: Update DAC-X with broadcast command

Table 7-11. Linear-Slew Mode: FUNC-GEN-CONFIG-BLOCK Field Descriptions

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-X	R/W	0	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-X	R/W	0	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-X	R/W	0	0: Enable linear slew
6-4	CODE-STEP-X	R/W	0	CODE-STEP for linear slew mode: 000: 1-LSB 001: 2-LSB 010: 3-LSB 011: 4-LSB 100: 6-LSB 101: 8-LSB 110: 16-LSB 111: 32-LSB
3-0	SLEW-RATE-X	R/W	0	SLEW-RATE for linear slew mode: 0000: No slew for margin-high and margin-low. Invalid for waveform generation. 0001: 4μs/step 0010: 8μs/step 0011: 12μs/step 0100: 18μs/step 0101: 27.04μs/step 0110: 40.48μs/step 0111: 60.72μs/step 1000: 91.12μs/step 1001: 136.72μs/step 1010: 239.2μs/step 1011: 418.64μs/step 1100: 732.56μs/step 1101: 1282μs/step 1110: 2563.96μs/step 1111: 5127.92μs/step

Table 7-12. Logarithmic-Slew Mode: FUNC-GEN-CONFIG-BLOCK Field Descriptions

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-X	R/W	0	00: 0° 01: 120° 10: 240° 11: 90°
10 - 8	FUNC-CONFIG-X	R/W	0	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-X	R/W	0	1: Enable logarithmic slew. In logarithmic slew mode, the DAC output moves from the DAC-X-MARGIN-LOW code to the DAC-X-MARGIN-HIGH code, or vice versa, in 3.125% steps. When slewing in the positive direction, the next step is (1 + 0.03125) times the current step. When slewing in the negative direction, the next step is (1 – 0.03125) times the current step. When DAC-X-MARGIN-LOW is 0, the slew starts from code 1. The time interval for each step is defined by RISE-SLEW-X and FALL-SLEW-X.
6-4	RISE-SLEW-X	R/W	0	SLEW-RATE for logarithmic slew mode (DAC-X-MARGIN-LOW to DAC-X-MARGIN-HIGH): 000: 4μs/step 001: 12μs/step 010: 27.04μs/step 011: 60.72μs/step 100: 136.72μs/step 101: 418.64μs/step 110: 1282μs/step 111: 5127.92μs/step
3-1	FALL-SLEW-X	R/W	0	SLEW-RATE for logarithmic slew mode (DAC-X-MARGIN-HIGH to DAC-X-MARGIN-LOW): 000: 4μs/step 001: 12μs/step 010: 27.04μs/step 011: 60.72μs/step 100: 136.72μs/step 101: 418.64μs/step 110: 1282μs/step 111: 5127.92μs/step
0	x	x	0	Don't care

7.8 DAC-X-DATA Register (address = 19h, 1Ah, 1Bh, 1Ch) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 21h

Figure 7-8. DAC-X-DATA Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-DATA[11:0] DAC-X-DATA[9:0] DAC-X-DATA[7:0]												x			
R/W-000h												x-0h			

Table 7-13. DAC-X-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-X-DATA[11:0] DAC-X-DATA[9:0] DAC-X-DATA[7:0]	R/W	000h	Data for DAC output Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: AFE53004W VOUT: {DAC-X-DATA[11:0]} AFE63004W VOUT: {DAC-X-DATA[9:0], x, x} IOUT: {DAC-X-DATA[7:0], x, x,x, x} x = Don't care bits.
3-0	x	x	0h	Don't care

7.9 ADC-CONFIG-TRIG Register (address = 1Dh) [reset = 0000h]

Figure 7-9. ADC-CONFIG-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		ADC-EN	ADC-AVG	ADC-MUX-SEL		RESERVED		x		ADC-TRIG					
R/W-0h		R/W-0h	R/W-0h	R/W-0h		R/W-0h		x-0h		W-0h					

Table 7-14. ADC-CONFIG-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0	Always write 000b.
13	ADC-EN	R/W	0	0: ADC disabled. 1: ADC enabled.
12 - 11	ADC-AVG	R/W	00	Number of ADC samples to be averaged: 00: 4 01: 8 10: 16 11: 32
10 - 8	ADC-MUX-SEL	R/W	000	000: ADC0 in Hi-Z input mode. 001: ADC1 in Hi-Z input mode. 010: ADC2 in Hi-Z input mode. 011: ADC3 in Hi-Z input mode. 100: ADC0 in finite-impedance input mode. 101: ADC1 in finite-impedance input mode. 110: ADC2 in finite-impedance input mode. 111: Invalid.
7 - 5	RESERVED	R/W	0h	Always write 110b.
4 - 1	x	x	0h	Don't care.
0	ADC-TRIG	W	0	0: Don't care. 1: Trigger ADC. This bit is auto-resetting. <div style="text-align: center;">Note</div> <div>Before setting the ADC-TRIG bit:</div> <ul style="list-style-type: none"> Set ADC-EN to 1. Configure the reference and gain for channel-3. Configure channel-3 as a comparator. Configure reference and gain for desired channel. Configure channel-3 as a comparator.

7.10 ADC-DATA Register (address = 1Eh) [reset = 0000h]

Figure 7-10. ADC-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC-DATA[9:0]										x	ADC-MUX-READBACK			ADC-DRDY	
R-0h										x-0h		R-0h			R-0h

Table 7-15. ADC-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	ADC-DATA[9:0]	R	000h	Data readback from ADC Data are in straight-binary format. MSB left-aligned.
5-4	x	x	00	Don't care.
3 - 1	ADC-MUX-READBACK	R	0h	000: ADC0 in Hi-Z input mode. 001: ADC1 in Hi-Z input mode. 010: ADC2 in Hi-Z input mode. 011: ADC3 in Hi-Z input mode. 100: ADC0 in finite-impedance input mode. 101: ADC1 in finite-impedance input mode. 110: ADC2 in finite-impedance input mode. 111: Invalid.
0	ADC-DRDY	R	0	0: ADC conversion in progress. ADC-DATA is invalid. 1: ADC conversion complete. ADC-DATA is valid.

7.11 COMMON-CONFIG Register (address = 1Fh) [reset = 0FFFh]

PMBus page address = FFh, PMBus register address = E3h

Figure 7-11. COMMON-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIN-LATCH-EN	DEV-LOCK	EE-READ-ADDR	EN-INT-REF	VOUT-PDN-3	IOUT-PDN-3	VOUT-PDN-2	IOUT-PDN-2	VOUT-PDN-1	IOUT-PDN-1	VOUT-PDN-0	IOUT-PDN-0				
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-11b	R/W-1b	R/W-11b	R/W-1b	R/W-11b	R/W-1b	R/W-11b	R/W-1b	R/W-11b	R/W-11b	R/W-11b	R/W-1b

Table 7-16. COMMON-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	WIN-LATCH-EN	R/W	0	0: Non-latching window-comparator output 1: Latching window-comparator output
14	DEV-LOCK	R/W	0	0: Device not locked. 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	EE-READ-ADDR	R/W	0	0: Fault-dump read enable at address 0x00 1: Fault-dump read enable at address 0x01
12	EN-INT-REF	R/W	0	0: Disable internal reference. 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11-10, 8-7, 5-4, 2-1	VOUT-PDN-X	R/W	11	00: Power-up VOUT-X 01: Power-down VOUT-X with 10kΩ to AGND 10: Power-down VOUT-X with 100kΩ to AGND 11: Power-down VOUT-X with Hi-Z to AGND
9, 6, 3, 0	IOUT-PDN-X	R/W	1	0: Power-up IOUT-X 1: Power-down IOUT-X

7.12 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E4h

Figure 7-12. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET			LDAC	CLR	x	FAULT-DUMP	PROTECT	READ-ONE-TRIG	NVM-PROG	NVM-RELOAD	
R/W-0h				R/W-0h			R/W-0h	R/W-0h	x-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-17. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W	0000	0101: Device unlocking password. To unlock device, write this unlock password first, followed by a write 0 to the DEV-LOCK bit in the COMMON-CONFIG register. Others: Don't care
11 - 8	RESET	W	0000	1010: POR reset triggered. This bit self-resets. Others: Don't care
7	LDAC	R/W	0	0: LDAC operation not triggered 1: LDAC operation triggered if the respective SYNC-CONFIG-X bit in the DAC-X-FUNC-CONFIG register is 1. This bit self-resets.
6	CLR	R/W	0	0: DAC registers and outputs unaffected 1: DAC registers and outputs set to zero-code or mid-code based on the respective CLR-SEL-X bit in the DAC-X-FUNC-CONFIG register. This bit self-resets.
5	x	x	0	Don't care
4	FAULT-DUMP	R/W	0	0: Fault-dump is not triggered 1: Triggers fault-dump sequence. This bit self-resets.
3	PROTECT	R/W	0	0: PROTECT function not triggered 1: Trigger PROTECT function. This bit is self-resetting.
2	READ-ONE-TRIG	R/W	0	0: Fault-dump read not triggered 1: Read one row of NVM for fault-dump. This bit self-resets.
1	NVM-PROG	R/W	0	0: NVM write not triggered 1: NVM write triggered. This bit self-resets.
0	NVM-RELOAD	R/W	0	0: NVM reload not triggered 1: Reload data from NVM to register map. This bit self-resets.

7.13 COMMON-DAC-TRIG Register (address = 21h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E5h

Figure 7-13. COMMON-DAC-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET-CMP-FLAG-0	TRIG-MAR-LO-0	TRIG-MAR-HI-0	START-FUNC-0	RESET-CMP-FLAG-1	TRIG-MAR-LO-1	TRIG-MAR-HI-1	START-FUNC-1	RESET-CMP-FLAG-2	TRIG-MAR-LO-2	TRIG-MAR-HI-2	START-FUNC-2	RESET-CMP-FLAG-3	TRIG-MAR-LO-3	TRIG-MAR-HI-3	START-FUNC-3
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 7-18. COMMON-DAC-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15, 11, 7, 3	RESET-CMP-FLAG-X	W	0	0: Latching-comparator output unaffected 1: Reset latching-comparator and window-comparator output. This bit self-resets.
14, 10, 6, 2	TRIG-MAR-LO-X	W	0	0: Don't care 1: Trigger margin-low command. This bit self-resets.
13, 9, 5, 1	TRIG-MAR-HI-X	W	0	0: Don't care 1: Trigger margin-high command. This bit self-resets.
12, 8, 4, 0	START-FUNC-X	R/W	0	0: Stop function generation 1: Start function generation as per FUNC-GEN-CONFIG-X in the DAC-X-FUNC-CONFIG register.

7.14 GENERAL-STATUS Register (address = 22h) [reset = 00h, DEVICE-ID, VERSION-ID]

PMBus page address = FFh, PMBus register address = E6h

Figure 7-14. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	x	DAC-3-BUSY	DAC-2-BUSY	DAC-1-BUSY	DAC-0-BUSY	x	DEVICE-ID						VERSION-ID	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	x-0h	R						R-0h	

Table 7-19. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP 1: Indicates a failure in OTP loading. A software reset or power-cycle can bring the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get original state. A software reset brings the device out of this temporary error condition.
13	x	R	0	Don't care
12	DAC-3-BUSY	R	0	0: DAC-3 channel can accept commands 1: DAC-3 channel does not accept commands
11	DAC-2-BUSY	R	0	0: DAC-2 channel can accept commands 1: DAC-2 channel does not accept commands
10	DAC-1-BUSY	R	0	0: DAC-1 channel can accept commands 1: DAC-1 channel does not accept commands
9	DAC-0-BUSY	R	0	0: DAC-0 channel can accept commands 1: DAC-0 channel does not accept commands
8	x	R	0	Don't care
7-2	DEVICE-ID	R	AFE63004W:09h AFE53004W: Ah	Device identifier.
1-0	VERSION-ID	R	00	Version identifier.

7.15 CMP-STATUS Register (address = 23h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E7h

Figure 7-15. CMP-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x							PROTECT-FLAG	WIN-CMP-3	WIN-CMP-2	WIN-CMP-1	WIN-CMP-0	CMP-FLAG-3	CMP-FLAG-2	CMP-FLAG-1	CMP-FLAG-0
x-0h							R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-20. CMP-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	x	x	0	Don't care
8	PROTECT-FLAG	R	0	0: PROTECT operation not triggered. 1: PROTECT function is completed or in progress. This bit resets to 0 when read.
7, 6, 5, 4	WIN-CMP-X	R	0	Window comparator output from respective channels. The output is latched or unlatched based on the WINDOW-LATCH-EN setting in the COMMON-CONFIG register.
3, 2, 1, 0	CMP-FLAG-X	R	0	Synchronized comparator output from respective channels.

7.16 GPIO-CONFIG Register (address = 24h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E8h

Figure 7-16. GPIO-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GF-EN	x	GPO-EN	GPO-CONFIG				GPI-CH-SEL			GPI-CONFIG			GPI-EN		
R/W-0h	x-0h	R/W-0h	R/W-0h				R/W-0h			R/W-0h			R/W-0h		R/W-0h

Table 7-21. GPIO-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GF-EN	R/W	0	0: Glitch filter disabled for GP input. This setting provides faster response. 1: Glitch filter enabled for GPI. This setting introduces additional propagation delay but provides robustness.
14	x	x	0	Don't care.
13	GPO-EN	R/W	0	0: Disable output mode for GPIO pin. 1: Enable output mode for GPIO pin.
12 - 9	GPO-CONFIG	R/W	0000	STATUS function setting. The GPIO pin is mapped to the following register bits as output: 0001: NVM-BUSY 0100: DAC-0-BUSY 0101: DAC-1-BUSY 0110: DAC-2-BUSY 0111: DAC-3-BUSY 1000: WIN-CMP-0 1001: WIN-CMP-1 1010: WIN-CMP-2 1011: WIN-CMP-3 Others: NA

Table 7-21. GPIO-CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8 - 5	GPI-CH-SEL	R/W	0000	Each bit corresponds to a DAC channel. 0b is <i>disabled</i> and 1b is <i>enabled</i> . GPI-CH-SEL[0]: Channel 0 GPI-CH-SEL[1]: Channel 1 GPI-CH-SEL[2]: Channel 2 GPI-CH-SEL[3]: Channel 3 Example: when GPI-CH-SEL is 0101, both channel-0 and channel-2 are enabled and both channel-1 and channel-3 are disabled.
4 - 1	GPI-CONFIG	R/W	0000	GPIO pin input configuration. Global settings act on the entire device. Channel-specific settings are dependent on the channel selection by the GPI-CH-SEL bits: 0010: $\overline{\text{FAULT-DUMP}}$ (global). GPIO falling edge triggers fault dump, GPIO = 1 has no effect. 0011: IOUT power up-down (channel-specific). GPIO falling edge triggers power down, GPIO rising edge triggers power up. 0100: VOUT power up-down (channel-specific). The output load is as per the VOUT-PDN-X setting. GPIO falling edge triggers $\overline{\text{ECT}}$ input (global). GPIO falling edge asserts $\overline{\text{PROTECT}}$ function, GPIO = 1 has no effect. 0111: $\overline{\text{CLR}}$ input (global). GPIO = 0 asserts $\overline{\text{CLR}}$ function, GPIO = 1 has no effect. 1000: $\overline{\text{LDAC}}$ input (channel-specific). GPIO falling edge asserts $\overline{\text{LDAC}}$ function, GPIO = 1 has no effect. Both the SYNC-CONFIG-X and the GPI-CH-SEL must be configured for every channel. 1001: Start and stop function generation (channel-specific). GPIO falling edge stops function generation. GPIO rising edge starts function generation. 1010: Trigger margin high-low (channel-specific). GPIO falling edge triggers margin low. GPIO rising edge triggers margin high. 1011: $\overline{\text{RESET}}$ input (global). The falling edge of the GPIO pin asserts the $\overline{\text{RESET}}$ function. The $\overline{\text{RESET}}$ input must be a pulse. The GPIO rising edge brings the device out of reset. The $\overline{\text{RESET}}$ configuration must be programmed into the NVM. Otherwise the setting is cleared after the device reset. 1100: NVM write protection (global). GPIO falling edge allows NVM programming. GPIO rising edge blocks NVM programming. 1101: Register-map lock (global). GPIO falling edge allows update to the register map. GPIO rising edge blocks any register map update except a write to the DEV-UNLOCK field through I ² C or SPI and to the RESET field through I ² C. Others: Invalid
0	GPI-EN	R/W	0	0: Disable input mode for GPIO pin. 1: Enable input mode for GPIO pin.

7.17 DEVICE-MODE-CONFIG Register (address = 25h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E9h

Figure 7-17. DEVICE-MODE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DIS-MODE-IN		RESERVED		PROTECT-CONFIG		RESERVED					x		
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h					x-0h		

Table 7-22. DEVICE-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	00	Always write 0b00
13	DIS-MODE-IN	R/W	0	Write 1 to this bit for low-power consumption.
12-10	RESERVED	R/W	0	Always write 0b000
9-8	PROTECT-CONFIG	R/W	00	00: Switch to Hi-Z power-down (no slew) 01: Switch to DAC code stored in NVM (no slew) and then switch to Hi-Z power-down 10: Slew to margin-low code and then switch to Hi-Z power-down 11: Slew to margin-high code and then switch to Hi-Z power-down
7-5	RESERVED	R/W	0	Always write 0b000
4-0	x	R/W	00h	Don't care

7.18 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

Figure 7-18. INTERFACE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x			TIMEOUT-EN		x		EN-PMBUS		x				FSDO-EN	x	SDO-EN
x-0h			R/W-0h		x-0h		R/W-0h		x-0h				R/W-0h	x-0h	R/W-0h

Table 7-23. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	x	x	0h	Don't care
12	TIMEOUT-EN	R/W	0	0: I ² C timeout disabled 1: I ² C timeout enabled
11-9	x	x	0h	Don't care
8	EN-PMBUS	R/W	0	0: PMBus disabled 1: Enable PMBus
7-3	x	x	00h	Don't care
2	FSDO-EN	R/W	0	0: Fast SDO (FSDO) disabled 1: Fast SDO enabled
1	x	x	0	Don't care
0	SDO-EN	R/W	0	0: SDO disabled 1: SDO enabled on GPIO pin

7.19 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

PMBus page address = FFh, PMBus register address = EFh

Figure 7-19. SRAM-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x								SRAM-ADDR							
x-00h								R/W-00h							

Table 7-24. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	x	x	00h	Don't care
7-0	SRAM-ADDR	R/W	00h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a write to the SRAM.

7.20 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

PMBus page address = FFh, PMBus register address = F0h

Figure 7-20. SRAM-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM-DATA															
R/W-0000h															

Table 7-25. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-DATA	R/W	0000h	16-bit SRAM data. Data are written to or read from the address configured in the SRAM-CONFIG register.

7.21 DAC-X-DATA-8BIT Register (address = 40h, 41h, 42h, 43h) [reset = 0000h]

PMBus page address = Not applicable, PMBus register address = Not applicable

Figure 7-21. DAC-X-DATA-8BIT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-DATA-8BIT[7:0]								x							
R/W-00h								x-00h							

Table 7-26. DAC-X-DATA-8BIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	DAC-X-DATA-8BIT[7:0]	R/W	00h	8-bit data for current output. This register provides faster update rate in the I ² C mode. Data are in straight-binary format.
7-0	x	x	00h	Not applicable

7.22 BRDCAST-DATA Register (address = 50h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = F1h

Figure 7-22. BRDCAST-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRDCAST-DATA[11:0] BRDCAST-DATA[9:0] BRDCAST-DATA[7:0]												x			
R/W-000h												x-0h			

Table 7-27. BRDCAST-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	BRDCAST-DATA[11:0] BRDCAST-DATA[9:0] BRDCAST-DATA[7:0]	R/W	000h	Broadcast code for all DAC channels Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: AFE53004W VOUT: {BRDCAST-DATA[11:0]} AFE63004W VOUT: {BRDCAST-DATA[9:0], X, X} IOUT: {BRDCAST-DATA[7:0], X, X, X, X} X = Don't care bits. The BRD-CONFIG-X bit in the DAC-X-FUNC-CONFIG register must be enabled for the respective channels.
3-0	x	x	0h	Don't care.

7.23 PMBUS-PAGE Register [reset = 0300h]

PMBus page address = X, PMBus register address = 00h

Figure 7-23. PMBUS-PAGE Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-PAGE								x							
R/W-03h								x-00h							

Table 7-28. PMBUS-PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PMBUS-PAGE	R/W	03h	8-bit PMBus page address as specified in the <i>Register Names</i> table in the <i>Register Map</i> section.
7-0	x	x	00h	Not applicable

7.24 PMBUS-OP-CMD-X Register [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 01h

Figure 7-24. PMBUS-OP-CMD-X Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-OPERATION-CMD-X								x							
R/W-00h								x-00h							

Table 7-29. PMBUS-OP-CMD-X Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PMBUS-OPERATION-CMD-X	R/W	00h	PMBus operation commands: 00h: Turn off 80h: Turn on A4h: Margin high, DAC output margins high to DAC-X-MARGIN-HIGH code 94h: Margin low, DAC output margins low to DAC-X-MARGIN-LOW code
7-0	x	x	00h	Not applicable

7.25 PMBUS-CML Register [reset = 0000h]

PMBus page address = X, PMBus register address = 78h

Figure 7-25. PMBUS-CML Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x						CML	x	N/A							
x-00h						R/W-0h	x-0h	x-00h							

Table 7-30. PMBUS-CML Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	x	x	00h	Don't care
9	CML	R/W	0	0: No communication fault 1: PMBus communication fault for write with incorrect number of clocks, read before write command, invalid command address, and invalid or unsupported data value; reset this bit by writing 1.
8	x	x	0h	Don't care
7-0	x	x	00h	Not applicable

7.26 PMBUS-VERSION Register [reset = 2200h]

PMBus page address = X, PMBus register address = 98h

Figure 7-26. PMBUS-VERSION Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-VERSION								X							
R-22h								X-00h							

Table 7-31. PMBUS-VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PMBUS-VERSION	R	22h	PMBus version
7-0	X	X	00h	Not applicable

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The AFEx3004W are quad-channel buffered, force-sense output, voltage-output and current-output smart DACs that include an NVM and internal reference, and are available in a tiny 1.76mm × 1.76mm DSBGA package. The external reference must not exceed V_{DD} , either during transient or steady-state conditions. For the best Hi-Z output performance, use a pullup resistor on the VREF pin to VDD. In case the VDD pin remains floating during the off condition, place a 100kΩ resistor to AGND for proper detection of the VDD pin *off* condition. All the digital outputs are open drain; use external pullup resistors on these pins. The interface protocol is detected at power-on, and the device locks to the protocol as long as V_{DD} is on. In I²C mode, when allocating the I²C addresses in the system, also consider the broadcast address. I²C timeout can be enabled for robustness. SPI mode is three-wire by default. Configure the GPIO pin as SDO in the NVM for SPI readback capability. The SPI clock speed in readback mode is slower than in write mode. Power-down mode sets the DAC outputs in Hi-Z by default. Change the configuration appropriately for different power-down settings. The DAC channels can also power-up with a programmed DAC code in the NVM.

8.2 Typical Application

The AFEx3004W is configurable for use as a programmable current source using an external MOSFET for current values greater than 250 μ A. The force-sense outputs of the AFEx3004W are used to compensate for the gate-source voltage drop caused by temperature, drain current, and aging of the MOSFET. The GPIO pin is used to switch the output current on or off without the need for run-time software. The slew between the on and off values is programmable. [Figure 8-1](#) shows how the AFEx3004W is used as a programmable current source. A resistor, R_{SET}, connected to the source of the MOSFET sets the output current range. This circuit is used in optical modules that require a high current output with a small size.

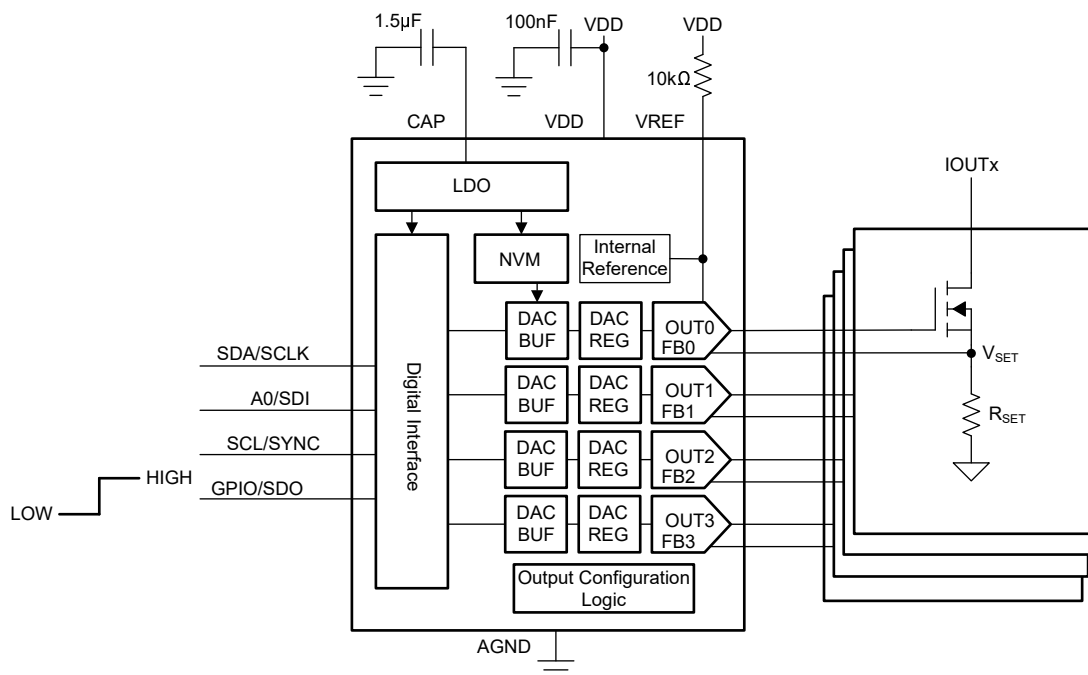


Figure 8-1. Current Source

8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
Current output range	0mA to 200mA
DAC range	0V to 0.6V
R _{SET}	Ω

8.2.2 Detailed Design Procedure

V_{SET} is controlled by the AFEx3004W to adjust the current output. R_{SET} sets the output range of the current source. Choose a small V_{SET} so that the power dissipation across R_{SET} is minimum. Equation 10 calculates R_{SET}.

$$R_{SET} = \frac{V_{SET}}{I_{OUT}} \quad (10)$$

A 0.6V max V_{SET} is used in this example. Equation 11 shows that R_{SET} is calculated to be 3Ω. Choose an R_{SET} with a power rating of at least 120mW.

$$R_{SET} = \frac{0.6V}{200mA} = 3\Omega \quad (11)$$

Equation 12 shows how to calculate the DAC code for a given output voltage, reference, and gain setting.

$$DAC_DATA = \frac{V_{OUT} \times 2^N}{V_{REF} \times GAIN} \quad (12)$$

Equation 13 calculates the DAC code for an output voltage, V_{SET}, of 0.6V, the internal 1.21V reference, and the 1.5 × gain setting.

$$DAC_DATA = \frac{0.6V \times 2^{12}}{1.21V \times 1.5} = 1354d \quad (13)$$

The GPIO pin can be configured as an input to trigger the DACx3x04W output to turn on and off, which turns the current source on and off. Configure the GPIO in the GPIO-CONFIG register. The GPI-EN bit enables the GPIO pin as an input. The GPI-CH-SEL field selects which channels are controlled by the GPI. The GPI-CONFIG field selects the GPI function. Table 6-19 defines the functions for the GPI-CONFIG field. Choose the trigger margin-high or margin-low function if programmable slew is needed, or VOUT power up or down if programmable slew is not needed.

The programmable slew is configured by the CODE-STEP and SLEW-RATE fields in the DAC-X-FUNC-CONFIG Register. The programmable slew is only available when toggling between two values stored in the DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW Registers. Section 6.4.5 discusses how to set the programmable slew. This application example uses a SLEW-RATE of 8μV/s and a CODE-STEP of 8LSB to achieve a 1.36ms slew time.

The pseudo code for this application example is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Set gain setting to 1.5x internal reference (1.8V) (repeat for all channels)
WRITE DAC-0-VOUT-CMP-CONFIG(0x3), 0x08, 0x00
//Power-up voltage output on all channels and enable the internal reference
WRITE COMMON-CONFIG(0x1F), 0x12, 0x49
//Configure GPI for Margin-High, Low trigger for all channels
WRITE GPIO-CONFIG(0x24), 0x01, 0xF5
//Set slew rate and code step (repeat for all channels)
//CODE_STEP: 8 LSB, SLEW_RATE: 8μs/step
WRITE DAC-0-FUNC-CONFIG(0x06), 0x00, 0x52
//Write DAC margin high code (repeat for all channels)
//For a 1.8V output range, the 12-bit hex code for 0.6V is 0x54A. with 16-bit left alignment,
this becomes 0x54A0
WRITE DAC-0-MARGIN-HIGH(0x01), 0x54, 0xA0
//Write DAC margin low code (repeat for all channels)
//The 12-bit hex code for 0V is 0x000. with 16-bit left alignment, this
becomes 0x0000
WRITE DAC-0-MARGIN-LOW(0x02), 0x00, 0x00
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

8.2.3 Application Curve

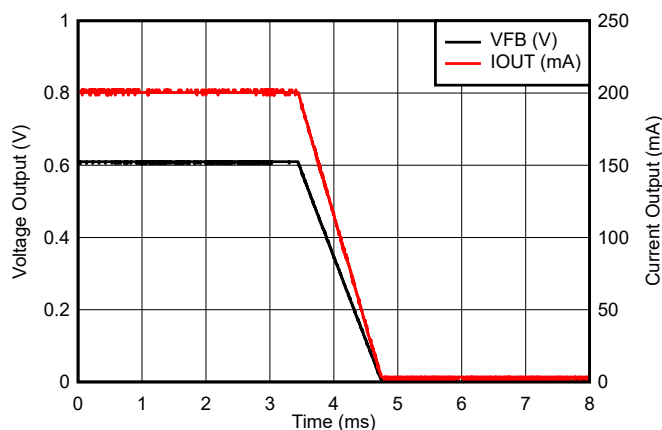


Figure 8-2. IOUT and VFB On-to-Off Transition

8.3 Power Supply Recommendations

The AFEx3004W family of devices does not require specific power-supply sequencing. These devices require a single power supply, V_{DD} . However, ensure that the external voltage reference is applied after V_{DD} . Use a $0.1\mu\text{F}$ decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value approximately $1.5\mu\text{F}$ for the CAP pin.

8.4 Layout

8.4.1 Layout Guidelines

The AFEx3004W pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

8.4.2 Layout Example

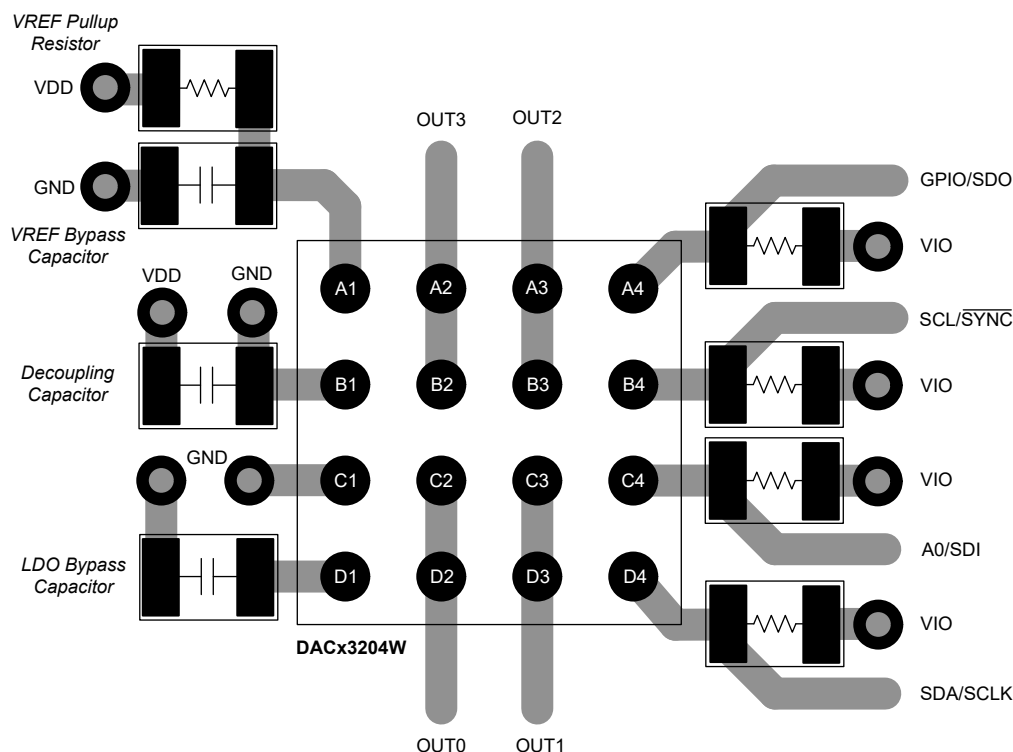


Figure 8-3. Layout Example

Note: The ground and power planes have been omitted for clarity.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and system integration assistance are listed below.

9.1 Documentation Support

Note

TI is transitioning to use more inclusive terminology. Some language can be different than what is expected for certain technology areas.

9.1.1 Related Documentation

The following EVM user's guide is available: [DAC63004 Evaluation Module user's guide](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

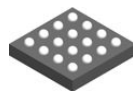
10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

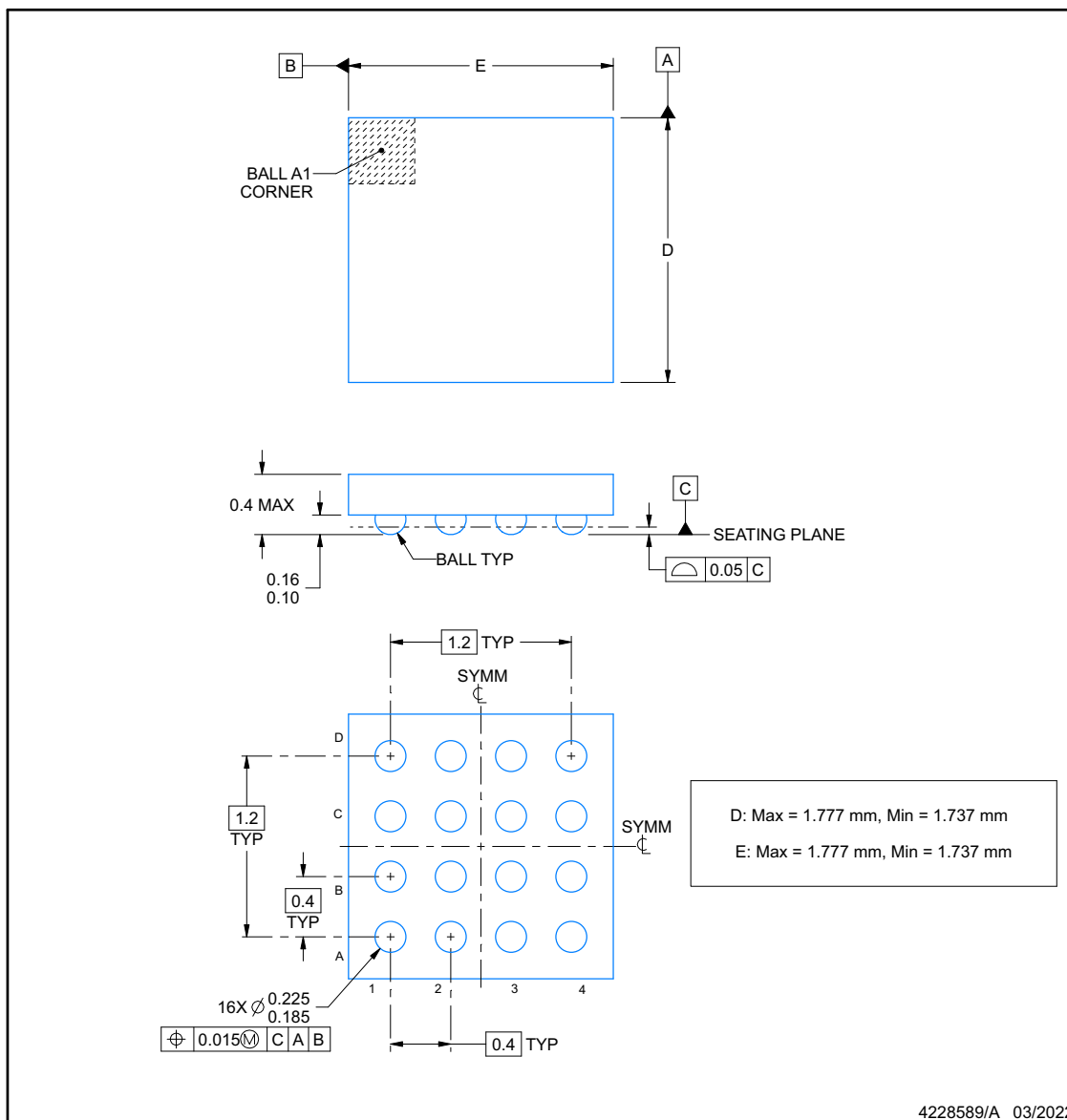
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



YBH0016-C03

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY

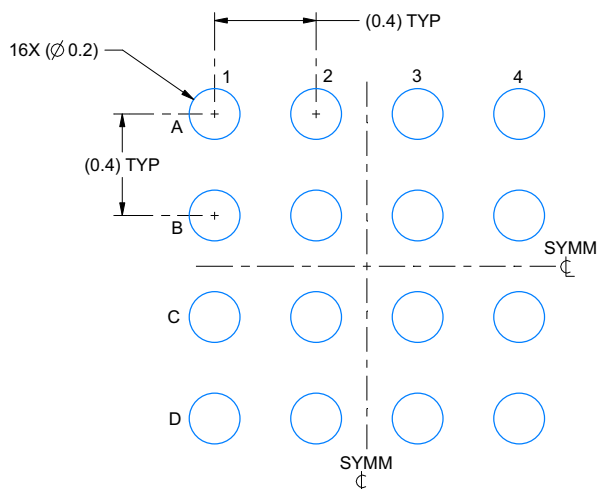


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

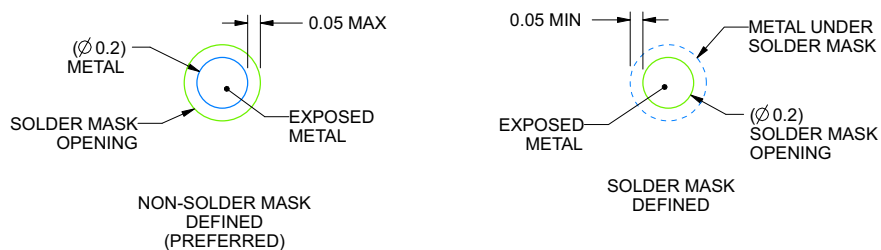
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT**YBH0016-C03****DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4228589/A 03/2022

NOTES: (continued)

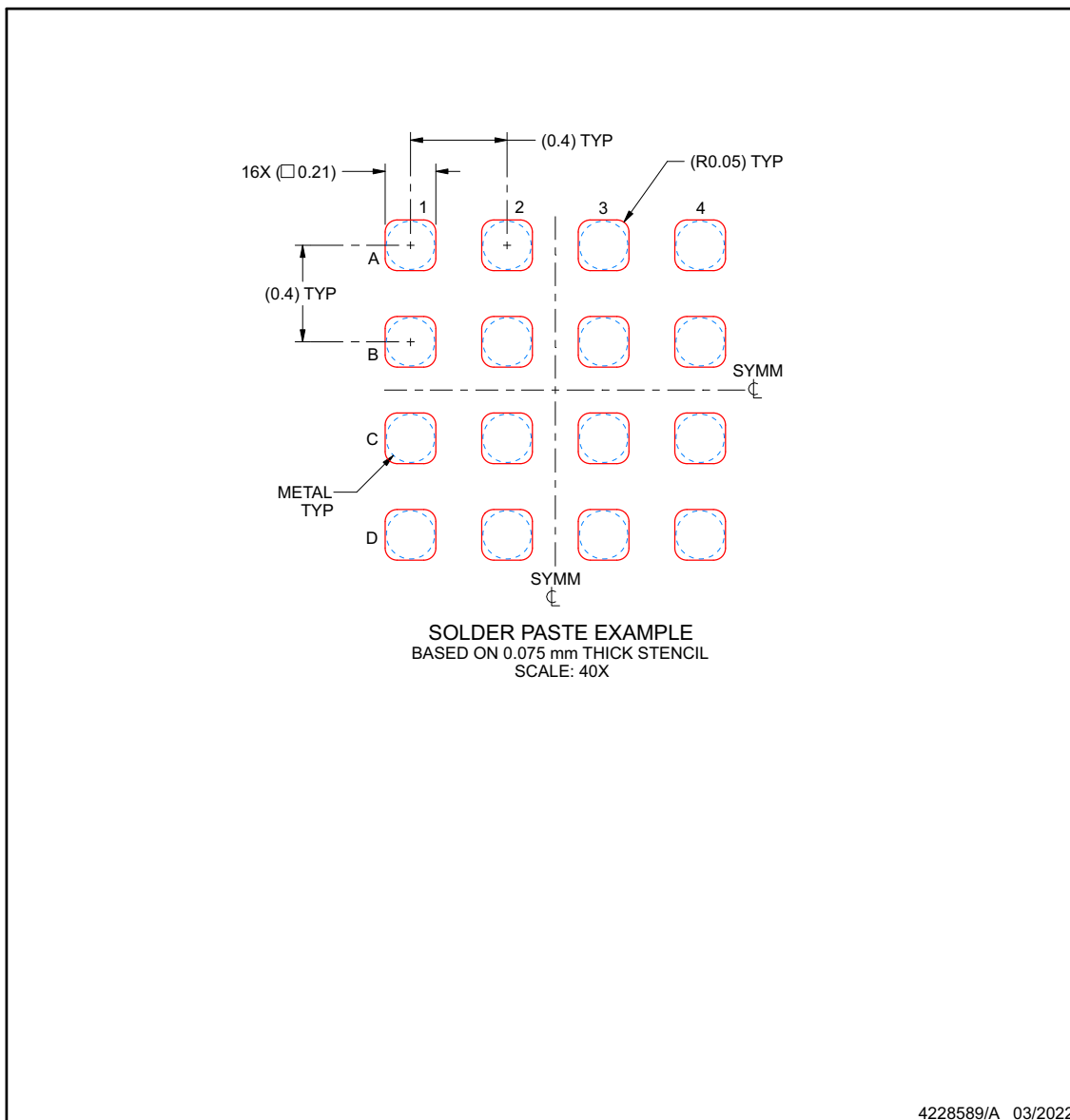
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBH0016-C03

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE53004YBHR	Active	Production	DSBGA (YBH) 16	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	AFE 53004

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE53004YBHR	DSBGA	YBH	16	3000	180.0	8.4	1.94	1.94	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE53004YBHR	DSBGA	YBH	16	3000	182.0	182.0	20.0

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