

bq2425x 2A Single-Input I²C, Stand-Alone Switched-Mode Li-Ion Battery Charger With Power-Path Management

1 Features

- High-Efficiency Switched-Mode Charger With Separate Power Path
- Startup System From Deeply Discharged or Missing Battery
- USB Charging Compliant
 - Selectable Input Current Limit of 100 mA, 500 mA, 900 mA, 1.5 A, and 2 A
- BC1.2 Compatible D+, D– Detection
- In Host Mode (After I²C Communication Starts and Before Watchdog Timer Times Out)
 - Programmable Battery Charge Voltage, V_{BATREG}
 - Programmable Charge Current (I_{CHG})
 - Programmable Input Current Limit (I_{LIM})
 - Programmable Input Voltage-Based Dynamic Power Management Threshold, (V_{IN_DPM})
 - Programmable Input Overvoltage Protection Threshold (V_{OVP})
 - Programmable Safety Timer
- Resistor Programmable Defaults for:
 - I_{CHG} up to 2 A With Current Monitoring Output (ISET)
 - I_{LIM} up to 2 A With Current Monitoring Output (ILIM)
 - V_{IN_DPM} (VDPM)
- Watchdog Timer Disable Bit
- Integrated 4.9 V, 50 mA LDO
- Complete System-Level Protection
 - Input UVLO, Input Overvoltage Protection (OVP), Battery OVP, Sleep Mode, V_{IN_DPM}
 - Input Current Limit
 - Charge Current Limit
 - Thermal Regulation
 - Thermal Shutdown
 - Voltage-Based, JEITA Compatible NTC Monitoring Input
 - Safety Timer
- 22 V Absolute Maximum Input Voltage Rating
- 10.5 V Maximum Operating Input Voltage
- Low $R_{DS(on)}$ Integrated Power FETs for a Charging Rate of up to 2 A
- Open-Drain Status Outputs

- Synchronous Fixed-Frequency PWM Controller Operating at 3 MHz for Small Inductor Support
- AnyBoot Robust Battery Detection Algorithm
- Charge Time Optimizer for Improved Charge Times at Any Given Charge Current
- 2.40-mm x 2.00-mm 30-Ball DSBGA and 4-mm x 4-mm 24-Pin QFN Packages

2 Applications

- Mobile Phones and Smart Phones
- MP3 Players
- Portable Media Players
- Handheld Devices

3 Description

The bq24250, bq24251, and bq24253 are highly integrated single-cell Li-Ion battery chargers and system power-path management devices targeted for space-limited, portable applications with high-capacity batteries. The single-cell charger has a single input that operates from either a USB port or an AC wall adapter for a versatile solution.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------------------------|------------|-------------------|
| bq24250 bq24251 bq24253 | VQFN (24) | 4.00 mm x 4.00 mm |
| | DSBGA (30) | 2.40 mm x 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

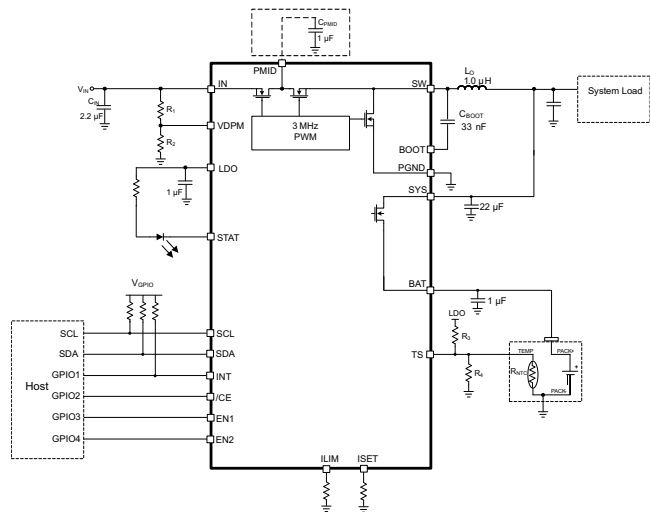


Table of Contents

| | | | |
|--|----|--|----|
| 1 Features | 1 | 9.4 Device Functional Modes | 30 |
| 2 Applications | 1 | 9.5 Programming | 31 |
| 3 Description | 1 | 9.6 Register Maps | 33 |
| 4 Revision History | 2 | 10 Application and Implementation | 39 |
| 5 Description (continued) | 4 | 10.1 Application Information | 39 |
| 6 Device Options | 4 | 10.2 Typical Application | 39 |
| 7 Pin Configuration and Functions | 5 | 11 Power Supply Recommendations | 42 |
| 8 Specifications | 8 | 12 Layout | 42 |
| 8.1 Absolute Maximum Ratings | 8 | 12.1 Layout Guidelines | 42 |
| 8.2 ESD Ratings | 8 | 12.2 Layout Example | 43 |
| 8.3 Recommended Operating Conditions | 8 | 12.3 Thermal Considerations | 44 |
| 8.4 Thermal Information | 9 | 13 Device and Documentation Support | 45 |
| 8.5 Electrical Characteristics | 9 | 13.1 Related Links | 45 |
| 8.6 Typical Characteristics | 14 | 13.2 Trademarks | 45 |
| 9 Detailed Description | 16 | 13.3 Electrostatic Discharge Caution | 45 |
| 9.1 Overview | 16 | 13.4 Glossary | 45 |
| 9.2 Functional Block Diagram | 17 | 14 Mechanical, Packaging, and Orderable Information | 45 |
| 9.3 Feature Description | 18 | 14.1 Package Summary | 46 |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision G (January 2015) to Revision H | Page |
|---|------|
| • Changed 20 V Maximum Input Voltage Rating Feature bullet to 22 V to match Absolute Maximum Ratings table | 1 |
| • Changed Figure 11 and Figure 12 image X-axis labels from "Temperature (fC)" to "Temperature (°C)" | 15 |

| Changes from Revision F (December 2014) to Revision G | Page |
|---|------|
| • Deleted Lead temperature (soldering) spec from Absolute Maximum Ratings table. See Package Option Addendum. | 8 |
| • Changed table heading from Handling Ratings to ESD Ratings. Moved T _{stg} spec to the Absolute Maximum Ratings table | 8 |
| • Changed the test condition of IBAT- Battery discharge current in SYSOFF mode: Removed "(BAT, SW, SYS)" | 9 |
| • Added spec for I _{IN} /I _{LIM} ratio | 11 |

| Changes from Revision E (December 2013) to Revision F | Page |
|--|------|
| • Added <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted the minimum spec for RILIM-SHORT and changed the typical value to 55 ohm and maximum spec to 75 ohm. | 11 |
| • Changed V _{LDO} values to (4.65, 4.85, 5.04) and added description in the second column "bq24250". Added one row below for "bq24251 and bq24253" and added values (4.65, 4.95, 5.25). | 12 |

| Changes from Revision D (July 2013) to Revision E | Page |
|--|------|
| • Changed VDPM pin description from ".....sets a default of 4.36V" to ".....sets a default of 4.68V" | 6 |
| • Changed text string in the V _{IN_DLM} settings description from: "The ISET resistor must be floated in order to avoid an internal fault." to: "The ISET resistor must be connected in order to avoid an unstable charging state." | 20 |
| • Changed text string in the Sleep Mode description from: "...sends a single 256µs pulse is sent on the STAT and INT outputs..." to: "...sends a single 256µs pulse on the STAT and INT outputs..." | 26 |

| | |
|--|----|
| • Changed text string in the Input Over-Voltage Protection description from: "...turns the battery FET, sends a single 256µs pulse is sent on the STAT and INT outputs..." to "...turns the battery FET, sends a single 256µs pulse on the STAT and INT outputs...." | 26 |
| • Added Serial Interface Description | 31 |
| • Changed Register #3 description, B1(4)(5) Name from: "USB_DET_1/EN1" to: "USB_DET_1/EN2" | 35 |
| • Changed Register #3 description, B0(LSB) Name from: "USB_DET_0/EN0" to: "USB_DET_0/EN1" | 35 |
| • Changed Register #3 description, B1(4)(5) and B0(LSB) FUNCTION entries from: "Return USB detection result or pin EN1/EN0 status –" to "Return USB detection result or pin EN2/EN1 status –" ; changed 00 - DCP detected / from: "EN1=0, EN0=0" to: "EN2=0, EN1=0"; changed 01 - CDP detected / from: "EN1=0, EN0=1" to: "EN2=0, EN1=1"; changed 10 - SDP detected / from: "EN1=1, EN0=0" to: "EN2=1, EN1=0"; and changed 11 - Apple/TT or non-standard adaptor detected / from: "EN1=1, EN0=1" to: "EN2=1, EN1=1", respectively. | 35 |

Changes from Revision C (June 2013) to Revision D
Page

| | |
|--|----|
| • Changed VDPM Pin Description regulator reference from "1.23V" to "1.2" | 6 |
| • Changed text string in D+/D- pin description from "...will remain low..." to "...will remain high impedance..." | 7 |
| • Added SCL and SDA to Pin Voltage Range spec in the Absolute Maximum Ratings table | 8 |
| • Changed spec conditions for Output Current (Continuous), from "IN, SW, SYS, BAT" to "IN, SYS, BAT" in ABS Max Ratings table | 8 |
| • Changed Figure 20 | 25 |
| • Added text to NTC Monitor description for clarification. | 28 |
| • Added text to Safety Timer description for clarification. | 28 |
| • Changed Fault Condition from "Input Good" to "Input Fault & LDO Low" in Fault Conditions table. | 29 |
| • Changed Register #2 Reset state from "1010 1100" to "xxxx 1100" | 34 |
| • Changed Register #4 Reset state from "0000 0000" to "1111 1000" | 35 |
| • Changed Bit B7, B6, B5, B4, B3 FUNCTION description from "(default 0)" to "(default 1)" | 35 |
| • Changed Register #4 Footnote (1) text from "...current is 500ma..." to ".....current is external.." | 35 |
| • Changed TS_EN description from "When set to a '1' the TS function is disabled" to "When set to a '0', the TS function is disabled..." | 37 |
| • Added text to TS_STAT description for clarification. | 37 |
| • Changed Register #7, Bit B3 FUNCTION description from "...if TERM is true or EN_PTM is true..." to "if TERM is true or Force PTM s true..." | 38 |

Changes from Revision B (May 2013) to Revision C
Page

| | |
|---|----|
| • Deleted PREVIEW status note from devices bq24250YFF, bq24251YFF, bq24251RGE, and bq24253RGE | 45 |
|---|----|

Changes from Revision A (March 2013) to Revision B
Page

| | |
|---|----|
| • Added PREVIEW status to devices in the Ordering Information table, except the bq24250RGER and bq24250RGET | 45 |
|---|----|

Changes from Original (October 2012) to Revision A
Page

| | |
|--|----|
| • Changed From: Product Brief To: Full data sheet | 1 |
| • Added Typical Characteristics graphs | 14 |
| • Added Typical Characteristics graphs | 15 |
| • Added Typical Characteristics graphs | 16 |
| • Changed Equation (3) | 20 |
| • Changed text in the F/S Mode Protocol section from "...to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0)" to "...to either transmit data to the slave (R/W bit 0) or receive data from the slave | |

(R/W bit 1)" for clarification..... 32

5 Description (continued)

The power-path management feature allows the bq24250, bq24251, and bq24253 to power the system from a high-efficiency DC-DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This reduced charge current allows for proper charge termination and enables the system to run with a defective or absent battery pack. Additionally, this reduced charge current enables instant system turnon even with a totally discharged battery or no battery. The architecture of the power-path management also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This supplementation of current requirements enables the use of a smaller adapter.

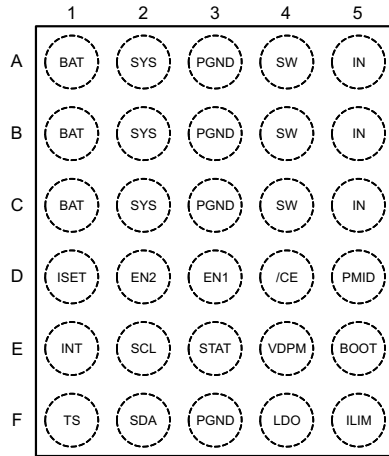
The battery is charged in four phases: trickle charge, precharge, constant current, and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. Additionally, a voltage-based, JEITA compatible battery pack thermistor monitoring input (TS) that monitors battery temperature for safe charging is included.

6 Device Options

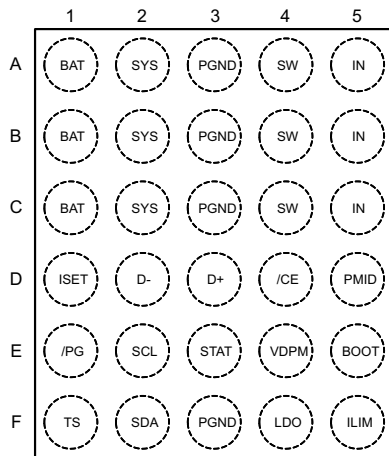
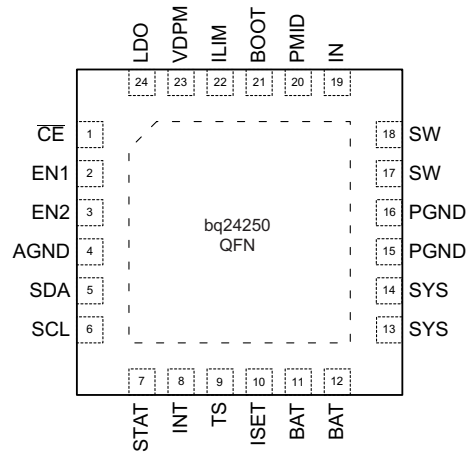
| DEVICE | DEFAULT OVP | D+/D- OR EN1/EN2 | INT OR PG | DEFAULT V _{OREG} | MINSYS | TS PROFILE | I ² C OR STAND ALONE | I ² C ADDRESS |
|---------|-------------|-------------------|------------------------|---------------------------|--------|------------|---------------------------------|--------------------------|
| bq24250 | 10.5V | EN1/EN2 | INT | 4.2V | 3.5V | JEITA | I ² C + SA | 0x6A |
| bq24251 | 10.5V | D+/D- | $\overline{\text{PG}}$ | 4.2V | 3.5V | JEITA | I ² C + SA | 0x6A |
| bq24253 | 10.5V | D+/D- and EN1/EN2 | $\overline{\text{PG}}$ | 4.2V | 3.5V | JEITA | SA Only | N/A |

7 Pin Configuration and Functions

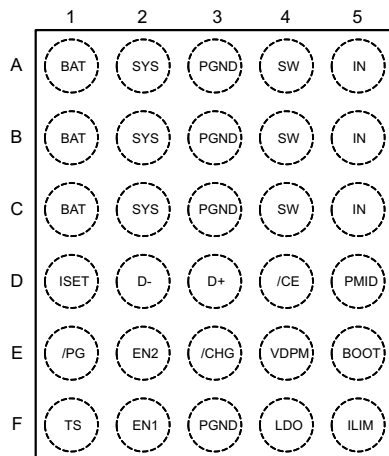
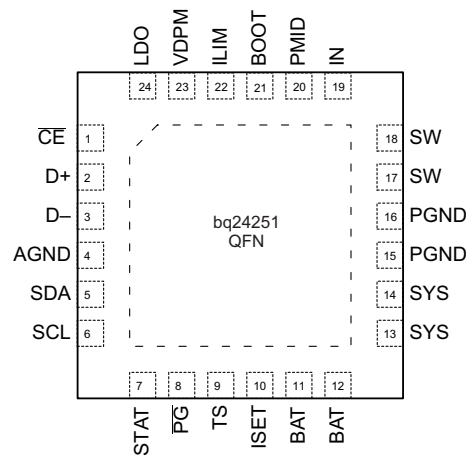
DSBGA/QFN
30 Pins/24 Pins
Top View



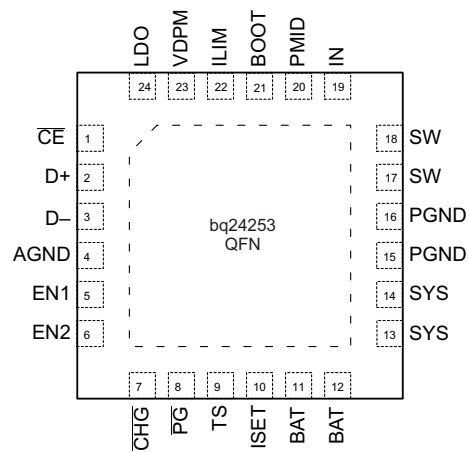
bq24250 DSBGA



bq24251 DSBGA



bq24253 DSBGA



Pin Functions

| NAME | PIN | | | | | | I/O | DESCRIPTION |
|------------------|----------------|-------|----------------|-------|----------------|-------|-----|--|
| | bq24250 | | bq24251 | | bq24253 | | | |
| | YFF | RGE | YFF | RGE | YFF | RGE | | |
| IN | A5,B5,C5 | 19 | A5,B5,C5 | 19 | A5,B5,C5 | 19 | I | Input power supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to PGND with >2μF ceramic capacitor |
| PMID | D5 | 20 | D5 | 20 | D5 | 20 | I | Connection between blocking FET and high-side FET. |
| SW | A4, B4, C4 | 17–18 | A4, B4, C4 | 17–18 | A4, B4, C4 | 17–18 | O | Inductor Connection. Connect to the switching side of the external inductor. |
| BOOT | E5 | 21 | E5 | 21 | E5 | 21 | I | High Side MOSFET Gate Driver Supply. Connect a 0.033μF ceramic capacitor (voltage rating > 15V) from BOOT to SW to supply the gate drive for the high side MOSFETs. |
| PGND | A3, B3, C3, F3 | 15–16 | A3, B3, C3, F3 | 15–16 | A3, B3, C3, F3 | 15–16 | | Ground terminal. Connect to the ground plane of the circuit. |
| SYS | A2, B2, C2 | 13–14 | A2, B2, C2 | 13–14 | A2, B2, C2 | 13–14 | I | System Voltage Sense and switched-mode power supply (SMPS) output filter connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with >20μF. |
| BAT | A1, B1, C1 | 11–12 | A1, B1, C1 | 11–12 | A1, B1, C1 | 11–12 | I/O | Battery Connection. Connect to the positive terminal of the battery. Additionally, bypass BAT with a >1μF capacitor. |
| TS | F1 | 9 | F1 | 9 | F1 | 9 | I | Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from LDO to GND. The NTC is connected from TS to GND. The TS function provides 4 thresholds for JEITA or PSE compatibility. See the <i>NTC Monitor</i> section for more details on operation and selecting the resistor values. |
| VDPM | E4 | 23 | E4 | 23 | E4 | 23 | I | Input DPM Programming Input. Connect a resistor divider between IN and GND with VDPM connected to the center tap to program the Input Voltage based Dynamic Power Management threshold (V_{IN_DPM}). The input current is reduced to maintain the supply voltage at V_{IN_DPM} . The reference for the regulator is 1.2V. Short pin to GND if external resistors are not desired—this sets a default of 4.68V for the input DPM threshold. |
| ISET | D1 | 10 | D1 | 10 | D1 | 10 | I | Charge Current Programming Input. Connect a resistor from ISET to GND to program the fast charge current. The charge current is programmable from 300mA to 2A. |
| ILIM | F5 | 22 | F5 | 22 | F5 | 22 | I | Input Current Limit Programming Input. Connect a resistor from ILIM to GND to program the input current limit for IN. The current limit is programmable from 0.5A to 2A. ILIM has no effect on the USB input. If an external resistor is not desired, short to GND for a 2A default setting. |
| \overline{CE} | D4 | 1 | D4 | 1 | D4 | 1 | I | Charge Enable Active-Low Input. Connect CE to a high logic level to place the battery charger in standby mode. |
| EN1 | D3 | 2 | – | – | F2 | 5 | I | Input Current Limit Configuration Inputs. Use EN1, and EN2 to control the maximum input current and enable USB compliance. See Table 1 for programming details. |
| EN2 | D2 | 3 | – | – | E2 | 6 | I | |
| \overline{CHG} | – | – | – | – | E3 | 7 | O | Charge Status Open Drain Output. \overline{CHG} is pulled low when a charge cycle starts and remains low while charging. \overline{CHG} is high impedance when the charging terminates and when no supply exists. \overline{CHG} does not indicate recharge cycles. |

Pin Functions (continued)

| NAME | PIN | | | | | | I/O | DESCRIPTION |
|------------------------|---------|-----|---------|-----|---------|-----|-----|---|
| | bq24250 | | bq24251 | | bq24253 | | | |
| | YFF | RGE | YFF | RGE | YFF | RGE | | |
| $\overline{\text{PG}}$ | – | – | E1 | 8 | E1 | 8 | O | Power Good Open Drain Output. $\overline{\text{PG}}$ is pulled low when a valid supply is connected to IN. A valid supply is between $V_{\text{BAT}}+V_{\text{SLP}}$ and V_{OVP} . If no supply is connected or the supply is out of this range, $\overline{\text{PG}}$ is high impedance. |
| STAT | E3 | 7 | E3 | 7 | – | – | O | Status Output. STAT is an open-drain output that signals charging status and fault interrupts. STAT pulls low during charging. STAT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 256 μ s pulse is sent out as an interrupt for the host. STAT is enabled/disabled using the EN_STAT bit in the control register. STAT will indicate recharge cycles. Connect STAT to a logic rail using an LED for visual indication or through a 10k Ω resistor to communicate with the host processor. |
| INT | E1 | 8 | – | – | – | – | O | Status Output. INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 256 μ s pulse is sent out as an interrupt for the host. INT will indicate recharge cycles. Connect INT to a logic rail through a 10k Ω resistor to communicate with the host processor. |
| SCL | E2 | 6 | E2 | 6 | – | – | I | I ² C Interface Clock. Connect SCL to the logic rail through a 10k Ω resistor. |
| SDA | F2 | 5 | F2 | 5 | – | – | I/O | I ² C Interface Data. Connect SDA to the logic rail through a 10k Ω resistor. |
| D+ | – | – | D3 | 2 | D3 | 2 | I | BC1.2 compatible D+/D– Based Adapter Detection. Detects DCP, SDP, and CDP. Also complies with the unconnected dead battery provision clause. D+ and D– are connected to the D+ and D– outputs of the USB port at power up. Also includes the detection of Apple™ and TomTom™ adapters where a 500mA input current limit is enabled. The $\overline{\text{PG}}$ pin will remain high impedance until the detection has completed. |
| D– | – | – | D2 | 3 | D2 | 3 | I | |
| LDO | F4 | 24 | F4 | 24 | F4 | 24 | O | LDO output. LDO is regulated to 4.9V and drives up to 50mA. Bypass LDO with a 1 μ F ceramic Capacitor. LDO is enabled when $V_{\text{UVLO}} < V_{\text{IN}} < 18\text{V}$. |
| AGND | – | 4 | – | 4 | – | 4 | | Analog Ground for QFN only. Connect to the thermal pad and the ground plane of the circuit. |

8 Specifications

8.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|------|-----|------|
| Pin Voltage Range (with respect to GND) | IN | -0.3 | 22 | V |
| | SW | -0.7 | 12 | V |
| | BOOT | -0.3 | 20 | V |
| | LDO, STAT, INT, /CHG, /PG, EN1, EN2, EN3, /CE, D+, D-, ILIM, ISET, VDPM, TS, SCL, SDA | -0.3 | 7 | V |
| | SYS, BAT | -0.3 | 5 | V |
| BOOT relative to SW | | -0.3 | 7 | V |
| Output Current (Continuous) | IN | | 2 | A |
| | SYS, BAT | | 4 | |
| Output Sink Current | STAT, /CHG, /PG | | 5 | mA |
| Operating free-air temperature range | | -40 | 85 | °C |
| Junction temperature, T _J | | -40 | 125 | °C |
| Input Power | IN | | 15 | W |
| Storage temperature, T _{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

All voltages are with respect to PGND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages

| | | MIN | MAX | UNIT |
|---------------------|--|------|-------------------|------|
| V _{IN} | IN voltage range | 4.35 | 18 ⁽¹⁾ | V |
| | IN operating voltage range | 4.35 | 10.5 | |
| I _{IN} | Input current | | 2 | A |
| I _{CHG} | Current in charge mode, BAT | | 2 | A |
| I _{DISCHG} | Current in discharge mode, BAT | | 4 | A |
| R _{ISET} | Charge current programming resistor range | 75 | | Ω |
| R _{ILIM} | Input current limit programming resistor range | 105 | | Ω |
| P _{IN} | Input Power | | 12 | W |
| T _J | Operating junction temperature range | 0 | 125 | °C |

- (1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. Small routing loops for the power nets in layout minimize switching noise.

8.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | YFF (30 PINS) | RGE (24 PINS) | UNIT |
|-------------------------------|--|------------------|------------------|------|
| R _{θJA} | Junction-to-ambient thermal resistance | 76.5 | 32.9 | °C/W |
| R _{θJctop} | Junction-to-case (top) thermal resistance | 0.2 | 32.8 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 44 | 10.6 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 1.6 | 0.3 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 43.4 | 10.7 | °C/W |
| R _{θJcbot} | Junction-to-case (bottom) thermal resistance | N/A | 2.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

8.5 Electrical Characteristics

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT} + V_{SLP}$, $T_J = 0^{\circ}\text{C} - 125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---|---|----------------------------|---|----------------------------|------|
| INPUT CURRENTS | | | | | | |
| I _{IN} | Supply current from IN | V _{DPM} < V _{IN} < V _{OVP} AND V _{IN} > V _{BAT} + V _{SLP} PWM switching, CE Enable | | 13 | | mA |
| | | V _{DPM} < V _{IN} < V _{OVP} AND V _{IN} > V _{BAT} + V _{SLP} PWM switching, CE Disable | | | 5 | |
| | | V _{IN} = 5.5V, 0°C < T _J < 85°C, High-Z Mode | | 170 | 225 | μA |
| I _{BAT} | Battery discharge current in high impedance mode, (BAT, SW, SYS) | 0°C < T _J < 85°C, V _{BAT} = 4.2 V, V _{IN} = 0V or 5V, High-Z Mode | | 16 | 22 | μA |
| | Battery discharge current in SYSOFF mode | 0°C < T _J < 85°C, V _{BAT} = 4.2 V, V _{IN} < UVLO, SYSOFF Mode | | | 1 | |
| POWER-PATH MANAGEMENT | | | | | | |
| V _{SYSREG} | System Regulation Voltage | MINSYS stage (no DPM or DPPM) | -1% | 3.52 | 1% | V |
| | | MINSYS stage (DPM or DPPM active) | -1.50% | V _{MINSYS} - 200mV | 1.50% | |
| | | BATREG stage | | V _{BAT} + I _{CHG} R _{on} | | |
| | | SYSREG stage | V _{BATREG} + 2.1% | V _{BATREG} + 3.1% | V _{BATREG} + 4.1% | |
| V _{SPLM} | Enter supplement mode voltage threshold | V _{BAT} = 3.6V | | V _{BAT} - 40mV | | V |
| I _{SPLM} | Exit supplement mode current threshold | V _{BAT} = 3.6V | | 20 | | mA |
| t _{DGL(SC1)} | Deglintch Time, OUT Short Circuit during Discharge or Supplement Mode | Measured from (V _{BAT} - V _{SYS}) = 300 mV | | 740 | | μs |
| t _{REC(SC1)} | Recovery Time, OUT Short Circuit during Discharge or Supplement Mode | | | 64 | | ms |
| BATTERY CHARGER | | | | | | |
| R _{ON(BAT-SYS)} | Internal battery charger MOSFET on-resistance | Measured from BAT to SYS, V _{BAT} = 4.2V (WCSP) | | 20 | 30 | mΩ |
| | | Measured from BAT to SYS, V _{BAT} = 4.2V (QFN) | | 30 | 40 | |

Electrical Characteristics (continued)
 $V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT} + V_{SLP}$, $T_J = 0^{\circ}\text{C} - 125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|--|--------|----------------------------|-------|-------|
| V _{BATREG} | I ² C host mode | Operating in voltage regulation, Programmable Range | 3.5 | | 4.44 | V |
| | SA mode or I ² C default mode | | | 4.2 | | |
| | Voltage Regulation Accuracy | T _J = 25°C | | -0.5% | | 0.5% |
| T _J = 0°C to 125°C | | | -0.75% | | 0.75% | |
| I _{CHG} | Fast Charge Current Range | V _{LOWV} ≤ V _{BAT} < V _{BAT(REG)} | 500 | | 2000 | mA |
| | Fast Charge Current Accuracy | I ² C mode | | -7% | 7% | |
| I _{CHG-LOW} | Low Charge Current Setting | Set via I ² C | 297 | 330 | 363 | mA |
| K _{ISET} | Programmable Fast Charge Current Factor | $I_{CHG} = \frac{K_{ISET}}{R_{ISET}}$ | 232.5 | 250 | 267.5 | AΩ |
| V _{ISET} | Maximum ISET pin voltage (in regulation) | | | 0.42 | | V |
| R _{ISET-SHORT} | Short circuit resistance threshold | | 45 | 55 | 75 | Ω |
| V _{LOWV} | Pre-charge to fast charge threshold | Rising | 2.9 | 3 | 3.1 | V |
| | Hysteresis for V _{LOWV} | Battery voltage falling | | 100 | | mV |
| I _{PRECHG} | Pr-charge current (V _{BATUVLO} < V _{BAT} < V _{LOWV}) | I _{pre-chg} is a percentile of the external fast charge settings. | 8 | 10 | 12 | % |
| t _{DGL(LOWV)} | Deglitch time for pre-charge to fast charge transition | | | 32 | | ms |
| V _{BAT_UVLO} | Battery Under voltage lockout threshold | V _{BAT} rising | 2.37 | 2.5 | 2.63 | V |
| | Battery UVLO hysteresis | | | 200 | | mV |
| V _{BATSHRT} | Trickle charge to pre-charge threshold | | 1.9 | 2 | 2.1 | V |
| | Hysteresis for VBATSHRT | Battery voltage falling | | 100 | | mV |
| I _{BATSHRT} | Trickle charge mode charge current (V _{BAT} < V _{BATSHRT}) | | 25 | 35 | 50 | mA |
| t _{DGL(BATSHRT)} | Deglitch time for trickle charge to pre-charge transition | | | 256 | | us |
| I _{TERM} | Termination Current Threshold | Termination current on SA only | | 10 | | %ICHG |
| | Termination Current Threshold Tolerance | | -10% | | 10% | |
| t _{DGL(TERM)} | Deglitch time for charge termination | Both rising and falling, 2-mV over-drive, t _{RISE} , t _{FALL} = 100 ns | | 64 | | ms |
| V _{RCH} | Recharge threshold voltage | Below V _{BATREG} | 70 | 115 | 160 | mV |
| t _{DGL(RCH)} | Deglitch time | V _{BAT} falling below V _{RCH} , t _{FALL} = 100 ns | | 32 | | ms |
| BATTERY DETECTION | | | | | | |
| V _{BATREG_HI} | Battery Detection High Regulation Voltage | Same as V _{BATREG} | | V _{BATREG} | | V |
| V _{BATREG_LO} | Battery Detection Low Regulation Voltage | 360 mV offset from V _{BATREG} | | V _{BATREG} -480mV | | V |
| V _{BATDET_HI} | Battery detection comparator | V _{BATREG} = V _{BATREG_HI} | | V _{BATREG} -120mV | | V |
| V _{BATDET_LO} | Battery detection comparator | V _{BATREG} = V _{BATREG_LO} | | V _{BATREG} +120mV | | V |
| I _{DETECT} | Battery Detection Current Sink | Always on during battery detection | | 7.5 | | mA |
| t _{DETECT} | Battery detection time | For both V _{BATREG_HI} and V _{BATREG_LO} | | 32 | | ms |
| Tsafe | Safety Timer Accuracy | | -10% | | +10% | |

Electrical Characteristics (continued)
 $V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT} + V_{SLP}$, $T_J = 0^{\circ}\text{C} - 125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|---|---------------------|---------------|---------------------|----------------|
| INPUT PROTECTION | | | | | | |
| I_{IN} | Input current limiting | $I_{IN_LIMIT} = 100\text{ mA}$ | 90 | 95 | 100 | mA |
| | | $I_{IN_LIMIT} = 150\text{ mA}$ | 135 | 142.5 | 150 | |
| | | $I_{IN_LIMIT} = 500\text{ mA}$ | 450 | 475 | 500 | |
| | | $I_{IN_LIMIT} = 900\text{ mA}$ | 810 | 860 | 910 | |
| | | $I_{IN_LIMIT} = 1500\text{ mA}$ | 1400 | 1475 | 1550 | |
| | | $I_{IN_LIMIT} = 2000\text{ mA}$ | 1850 | 1950 | 2050 | |
| | $I_{IN_LIMIT} = \text{External}$ | $I_{LIM} = \frac{K_{ILIM}}{R_{ILIM}}$ | | | | |
| I_{LIM} | Maximum input current limit programmable range for IN input | | 500 | | 2000 | mA |
| K_{ILIM} | Maximum input current factor for IN input | $I_{LIM} = 500\text{ mA to } 2.0\text{ A}$ | 240 | 270 | 300 | A Ω |
| V_{ILIM} | Maximum ILIM pin voltage (in regulation) | | | 0.42 | | V |
| I_{IN} / I_{ILIM} | Ratio between input current and the ILIM pin current in external control or stand alone mode | External ILIM control or stand alone | | 540 | | A/A |
| $R_{ILIM-SHORT}$ | Short circuit resistance threshold | | | 55 | 75 | Ω |
| V_{IN_DPM} | V_{IN_DPM} threshold range | SA mode | 4.2 | | 10 | V |
| | | I ² C mode | 4.2 | | 4.76 | |
| | V_{IN_DPM} threshold for USB Input in SA mode | USB100, USB150, USB500, USB900, current limit selected. Also I ² C register default. | 4.27 | 4.36 | 4.45 | |
| | V_{IN_DPM} threshold with adaptor current limit and VDPM shorted to GND | Must set to external resistor settings via the EN1/EN2 pins or the I ² C register interface. | $V_{IN_DPM} - 2\%$ | V_{IN_DPM} | $V_{IN_DPM} + 2\%$ | |
| | V_{IN_DPM} threshold Accuracy | Both I ² C and SA mode | -2% | | 2% | |
| V_{REF_DPM} | DPM regulation voltage | External resistor setting only | 1.15 | 1.2 | 1.25 | V |
| V_{DPM_SHRT} | V_{IN_DPM} short threshold | If VDPM is shorted to ground, V_{IN_DPM} threshold will use internal default value | | 0.3 | | V |
| V_{UVLO} | IC active threshold voltage | V_{IN} rising | 3.15 | 3.35 | 3.5 | V |
| | IC active hysteresis | V_{IN} falling from above V_{UVLO} | | 175 | | mV |
| V_{SLP} | Sleep-mode entry threshold, $V_{IN-VBAT}$ | $2.0\text{ V} \leq V_{BAT} \leq V_{BATREG}$, V_{IN} falling | 0 | 50 | 100 | mV |
| | Sleep-mode exit hysteresis, $V_{IN-VBAT}$ | $2.0\text{ V} \leq V_{BAT} \leq V_{BATREG}$ | 40 | 100 | 160 | mV |
| $t_{DGL(SLP)}$ | Deglintch time for IN rising above $V_{IN} + V_{SLP_EXIT}$ | Rising voltage, 2-mV over drive, $t_{RISE} = 100\text{ ns}$ | | 32 | | ms |
| V_{OVP} | Input supply OVP threshold voltage | IN rising | Input OVP -200mV | Input OVP | Input OVP +200mV | V |
| | VOVP hysteresis | IN falling from V_{OVP} | | 100 | | mV |
| $t_{DGL(OVP)}$ | Deglintch time for IN Rising above VOVP | IN rising voltage, $t_{RISE} = 100\text{ ns}$ | | 32 | | ms |
| V_{BOVP} | Battery OVP threshold voltage | V_{BAT} threshold over V_{BATREG} to turn off charger during charge | 102.5 | 105 | 107.5 | % V_{BATREG} |
| | VBOVP hysteresis | Lower limit for V_{BAT} falling from above V_{BOVP} | | 1 | | % V_{BATREG} |
| $t_{DGL(BOVP)}$ | BOVP Deglintch | Battery entering/exiting BOVP | | 1 | | ms |

Electrical Characteristics (continued)

 $V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT} + V_{SLP}$, $T_J = 0^{\circ}\text{C} - 125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|--|--|--|-------|------|--------------------|---|
| PWM CONVERTER | | | | | | | |
| $R_{ON(BLK)}$ | Internal blocking MOSFET on-resistance | Measured from IN to PMID (WCSP & QFN) | | 60 | 100 | m Ω | |
| $R_{ON(HS)}$ | Internal high-side MOSFET on-resistance | Measured from PMID to SW (WCSP & QFN) | | 100 | 150 | m Ω | |
| $R_{ON(LS)}$ | Internal low-side MOSFET on-resistance | Measured from SW to PGND (WCSP & QFN) | | 110 | 165 | m Ω | |
| I_{CbC} | Cycle-by-cycle current limit | VSYS shorted | 2.6 | 3.2 | 3.8 | A | |
| f_{OSC} | Oscillator frequency | | 2.7 | 3 | 3.3 | MHz | |
| D_{MAX} | Maximum duty cycle | | | 95% | | | |
| D_{MIN} | Minimum duty cycle | | 0% | | | | |
| T_{SHTDWN} | Thermal trip | | | 150 | | $^{\circ}\text{C}$ | |
| | Thermal hysteresis | | | 10 | | | |
| T_{REG} | Thermal regulation threshold | Charge current begins to cut off | | 125 | | | |
| LDO (LINEAR DROPOUT) | | | | | | | |
| V_{LDO} | LDO Output Voltage | bq24250 | $V_{IN} = 5.5\text{ V}$, $I_{LDO} = 0$ to 50 mA | 4.65 | 4.85 | 5.04 | V |
| | | bq24251 and bq24253 | | 4.65 | 4.95 | 5.25 | |
| I_{LDO} | Maximum LDO Output Current | | | 50 | | mA | |
| V_{DO} | LDO Dropout Voltage ($V_{IN} - V_{LDO}$) | $V_{IN} = 5.0\text{ V}$, $I_{LDO} = 50\text{ mA}$ | | 200 | 300 | mV | |
| BATTERY-PACK NTC MONITOR (1) | | | | | | | |
| V_{HOT} | High temperature threshold | V_{TS} falling | 29.6 | 30 | 30.4 | % V_{LDO} | |
| $V_{HYS(HOT)}$ | Hysteresis on high threshold | V_{TS} rising | | 1 | | | |
| V_{WARM} | Warm temperature threshold | V_{TS} falling | 37.9 | 38.3 | 38.7 | | |
| $V_{HYS(WARM)}$ | Hysteresis on warm temperature threshold | V_{TS} rising | | 1 | | | |
| V_{COOL} | Cool temperature threshold | V_{TS} rising | 56.1 | 56.5 | 56.9 | | |
| $V_{HYS(COOL)}$ | Hysteresis on cool temperature threshold | V_{TS} falling | | 1 | | | |
| V_{COLD} | Low temperature threshold | V_{TS} rising | 59.6 | 60 | 60.4 | | |
| $V_{HYS(COLD)}$ | Hysteresis on low threshold | V_{TS} falling | | 1 | | | |
| V_{FRZ} | Freeze temperature threshold | V_{TS} rising | 62 | 62.5 | 63 | | |
| $V_{HYS(FRZ)}$ | Hysteresis on freeze threshold | V_{TS} falling | | 1 | | | |
| V_{TS_DIS} | TS disable threshold | | 70 | | 73 | | |
| $t_{DGL(TS)}$ | Deglitch time on TS change | | | 32 | | ms | |
| INPUTS (EN1, EN2, EN2, \overline{CE}, CE1, CE2, BATREG, SCL, SDA, DBP) | | | | | | | |
| V_{IH} | Input high threshold | | 1 | | | V | |
| V_{IL} | Input low threshold | | | | 0.4 | V | |
| STATUS OUTPUTS (\overline{CHG}, \overline{PG}, STAT, INT, BATRDY) | | | | | | | |
| V_{OL} | Low-level output saturation voltage | $I_O = 5\text{ mA}$, sink current | | | 0.4 | V | |
| I_{IH} | High-level leakage current | Hi-Z and 5V applies | | | 1 | μA | |
| TIMERS | | | | | | | |
| t_{SAFETY} | 45 min safety timer | | | 2700 | | s | |
| | 6 hr safety timer | | | 21600 | | | |
| | 9 hr safety timer | | | 32400 | | | |
| $t_{WATCH-DOG}$ | Watch dog timer | | | 50 | | s | |

Electrical Characteristics (continued)
 $V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT} + V_{SLP}$, $T_J = 0^{\circ}\text{C} - 125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|------------------------|-------|------|-------|------------------|
| D+/D– DETECTION | | | | | | |
| I_{DP_SRC} | D+ current source for DCD | DCD | 7 | | 13 | μA |
| R_{DM_DWN} | D– pull-down resistance for DCD | DCD | 14.25 | | 24.8 | $\text{k}\Omega$ |
| V_{DP_LOW} | D+ low comparator threshold for DCD | DCD | 0.85 | 0.9 | 0.95 | V |
| V_{DP_SRC} | D+ source voltage for Primary Detection | Primary Detection | 0.5 | 0.6 | 0.7 | V |
| $I_{DP_SRC_PD}$ | D+ source voltage output current for Primary Detection | Primary Detection | 200 | | | μA |
| I_{DM_SINK} | D– sink current for Primary Detection | Primary Detection | 50 | 100 | 150 | μA |
| V_{DAT_REF} | Primary Detection threshold | Primary Detection | 250 | 325 | 400 | mV |
| V_{LGC} | Primary Detection threshold | Primary Detection | 0.85 | 0.9 | 0.95 | V |
| V_{DM_SRC} | D- source voltage for Secondary Detection | Secondary Detection | 0.5 | 0.6 | 0.7 | V |
| $I_{DM_SRC_PD}$ | D- source voltage output current for Secondary Detection | Secondary Detection | 200 | | | μA |
| I_{DP_SINK} | D+ sink current for Secondary Detection | Secondary Detection | 50 | 100 | 150 | μA |
| V_{DAT_REF} | Secondary Detection threshold | Secondary Detection | 250 | 325 | 400 | mV |
| V_{ATT_LO} | Apple/TomTom detection low threshold | Apple/TomTom Detection | 1.8 | 1.85 | 1.975 | V |
| V_{ATT_HI} | Apple/TomTom detection high threshold | Apple/TomTom Detection | 3.2 | 3.5 | 3.8 | V |
| C_I | Input Capacitance | D–, switch open | | 4.5 | | pF |
| | | D+, switch open | | 4.5 | | |
| I_{D_LKG} | Leakage Current into D+/D– | D–, switch open | –1 | | 1 | μA |
| | | D+, switch open | –1 | | 1 | |

8.6 Typical Characteristics

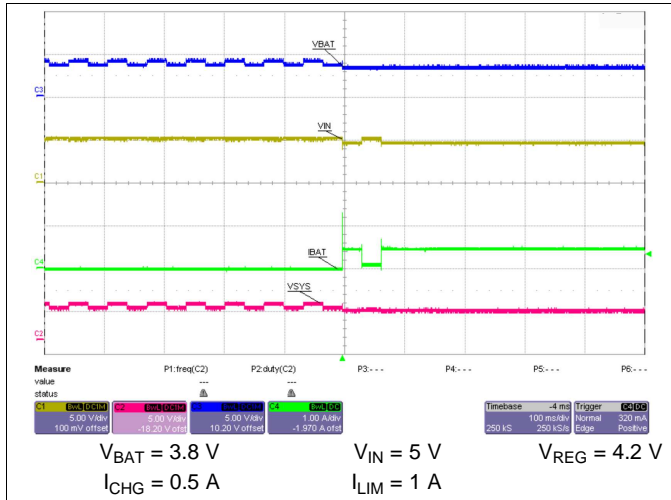


Figure 1. Battery Detection

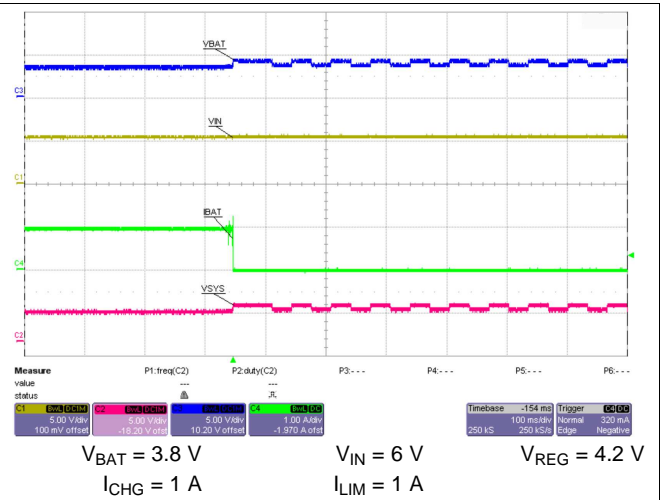


Figure 2. Battery Removal

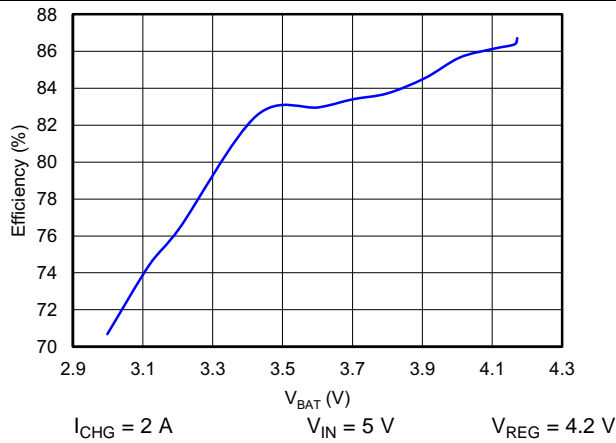


Figure 3. Efficiency vs Battery Voltage

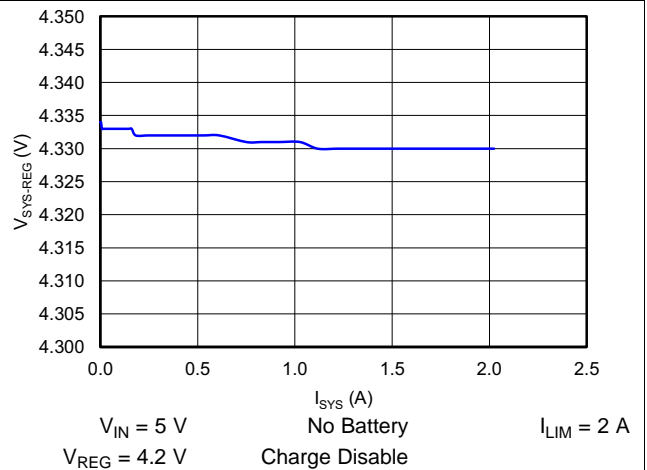


Figure 4. System Voltage Regulation vs Load Current

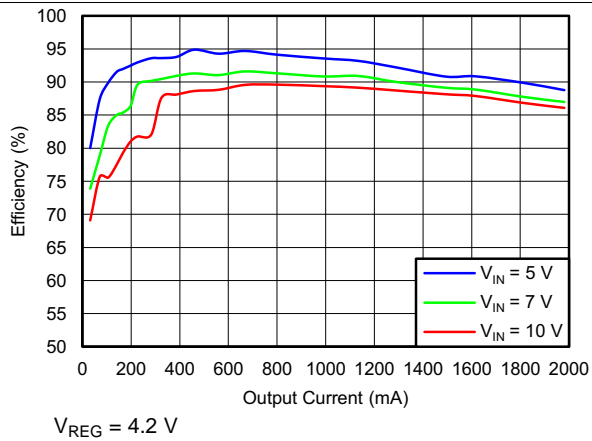


Figure 5. Efficiency vs Output Current

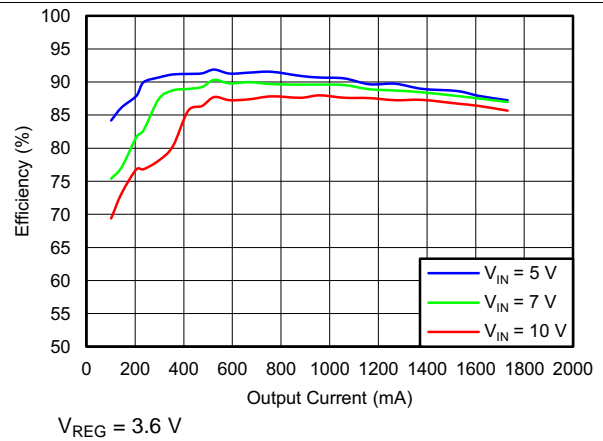
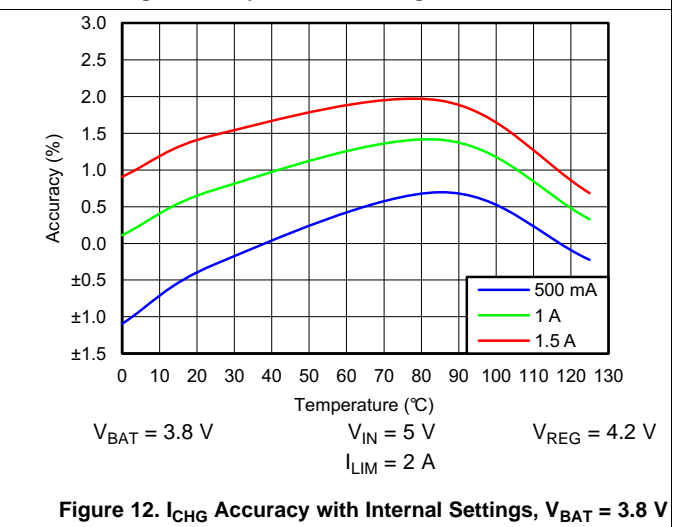
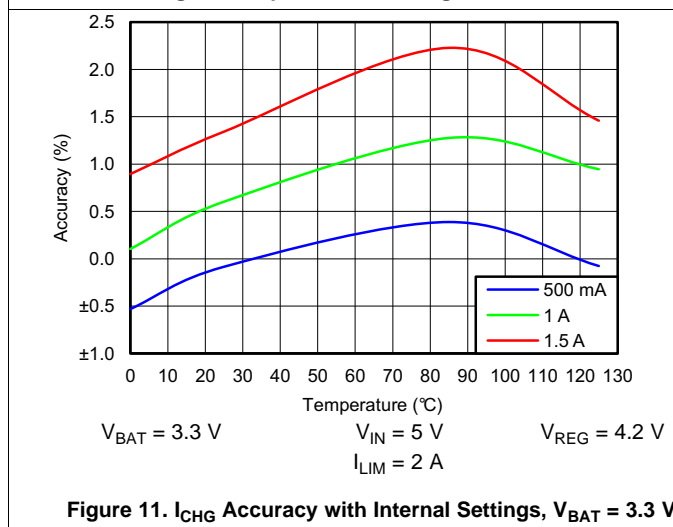
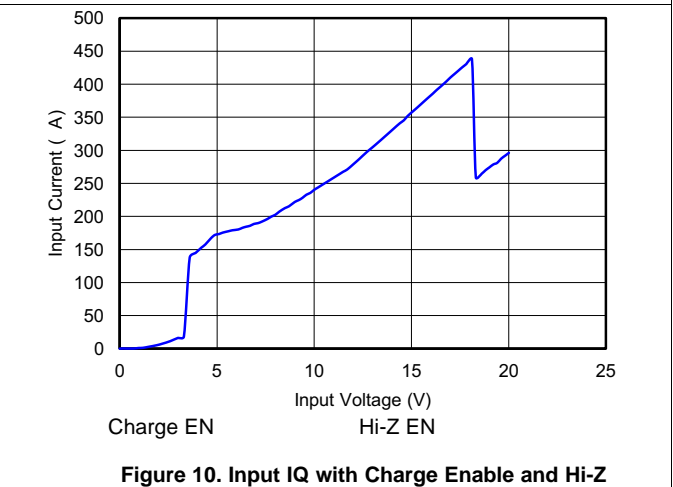
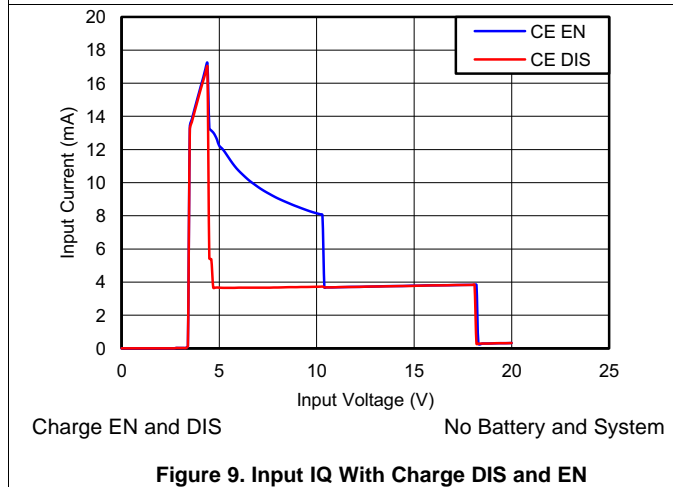
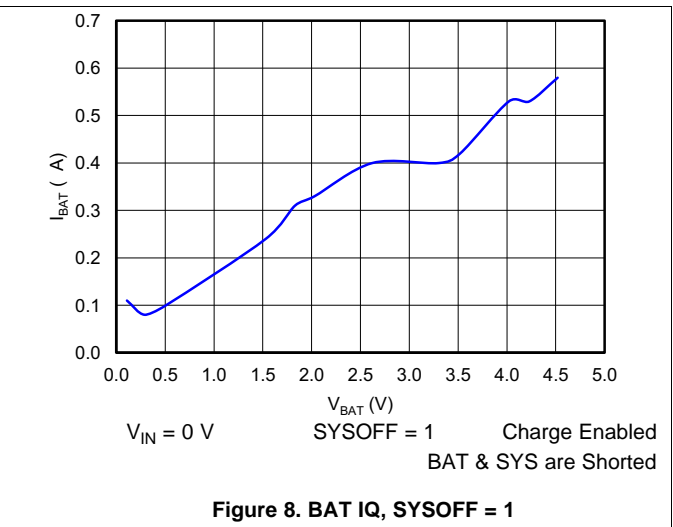
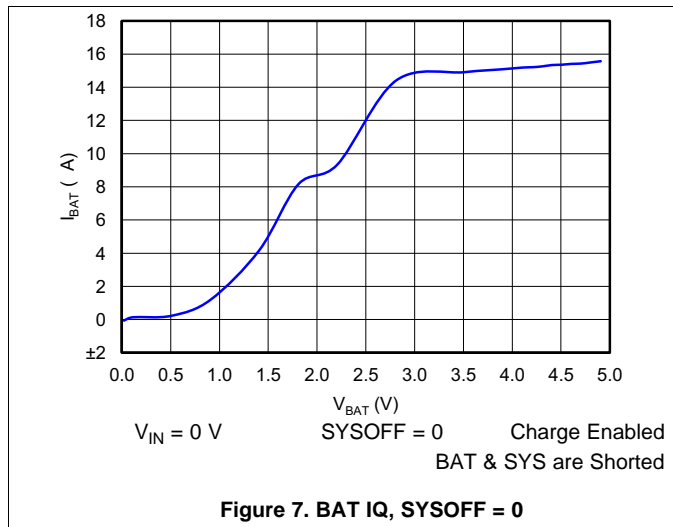
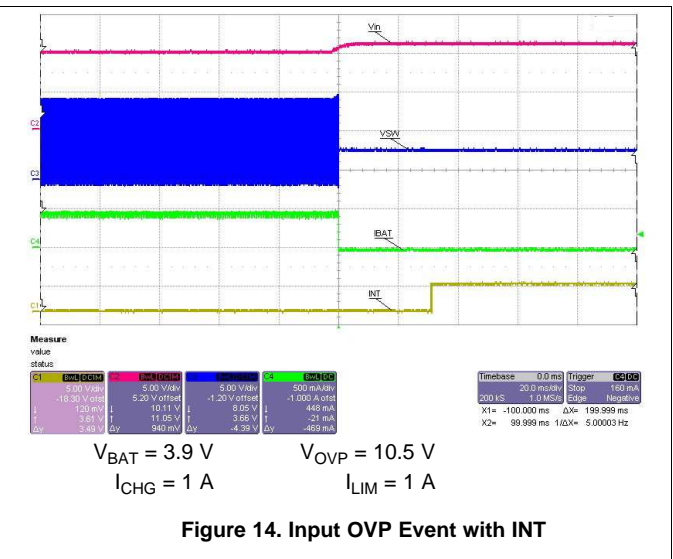
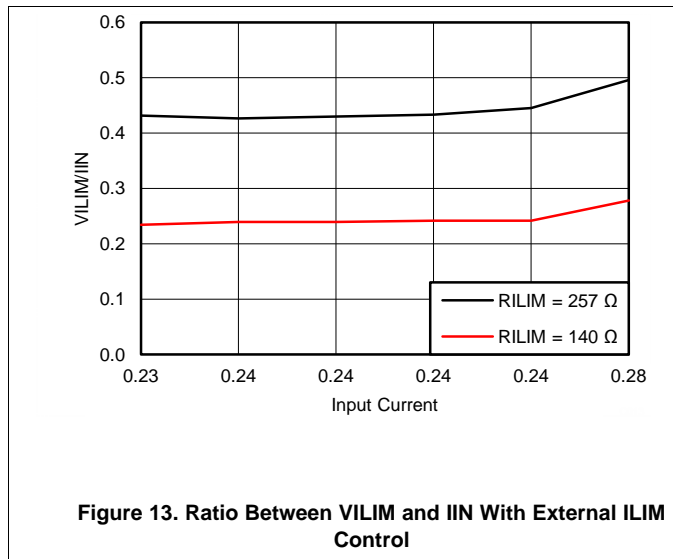


Figure 6. Efficiency vs Output Current

Typical Characteristics (continued)



Typical Characteristics (continued)



9 Detailed Description

9.1 Overview

The bq24250 is a highly-integrated, single-cell, Li-Ion battery charger with integrated current sense resistors targeted for space-limited, portable applications with high-capacity batteries. The single-cell charger has a single input that operates from either a USB port or AC wall adapter for a versatile solution.

The bq24250 device has two modes of operation: 1) I2C mode, and 2) standalone mode. In I2C mode, the host adjusts the charge parameters and monitors the status of the charger operation. In standalone mode, the external resistor sets the input-current limit, and charge current limit. Standalone mode also serves as the default settings when a DCP adapter is present. It enters host mode while the I2C registers are accessed and the watchdog timer has not expired (if enabled). The battery is charged in four phases: trickle charge, pre-charge, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded.

9.3 Feature Description

9.3.1 Charge Profile

The bq2425x family provides a switch-mode buck regulator with output power path and a charge controller to provide optimum performance over the full battery charge cycle. The control loop for the buck regulator has 7 primary feedback loops that can set the duty cycle:

1. Constant Current (CC)
2. Constant Voltage (CV)
3. Minimum System Voltage (MINSYS)
4. Input Current (I_{ILIM})
5. Input Voltage (V_{IN_DPM})
6. Die Temperature
7. Cycle by Cycle Current

The feedback with the minimum duty cycle will be chosen as the active loop. The bq24250, 1, 3 support a precision Li-Ion or Li-Polymer charging system for single-cell applications. The Dynamic Power Path Management (DPPM) feature regulates the system voltage to a minimum of V_{MINSYS} , so that startup is enabled even with a missing or deeply discharged battery. This provides a much better overall user experience in mobile applications. Figure 15 illustrates a typical charge profile while also demonstrating the minimum system output voltage regulation.

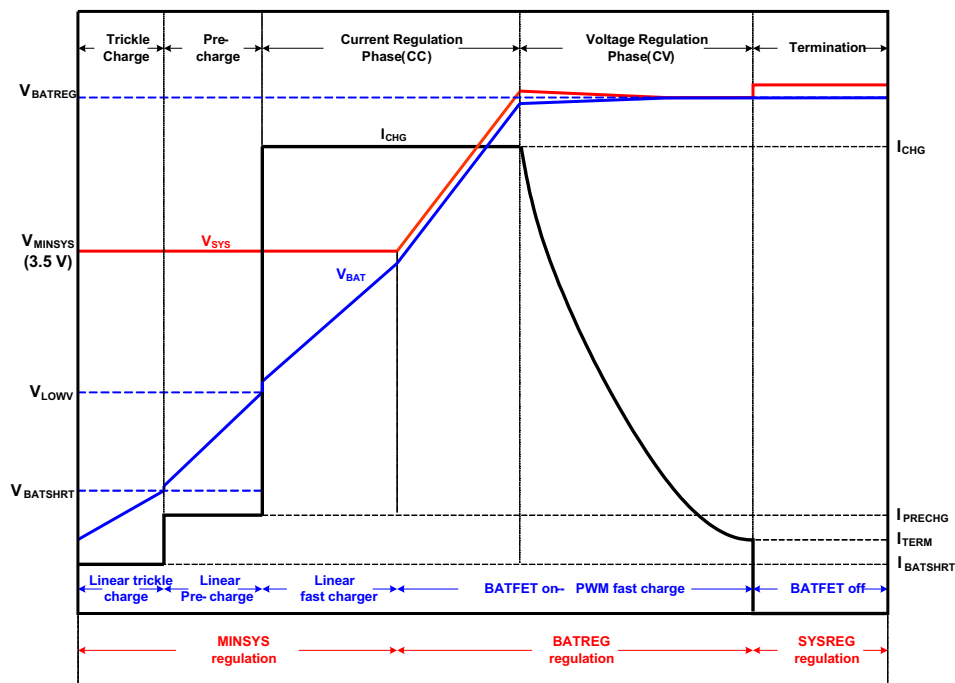
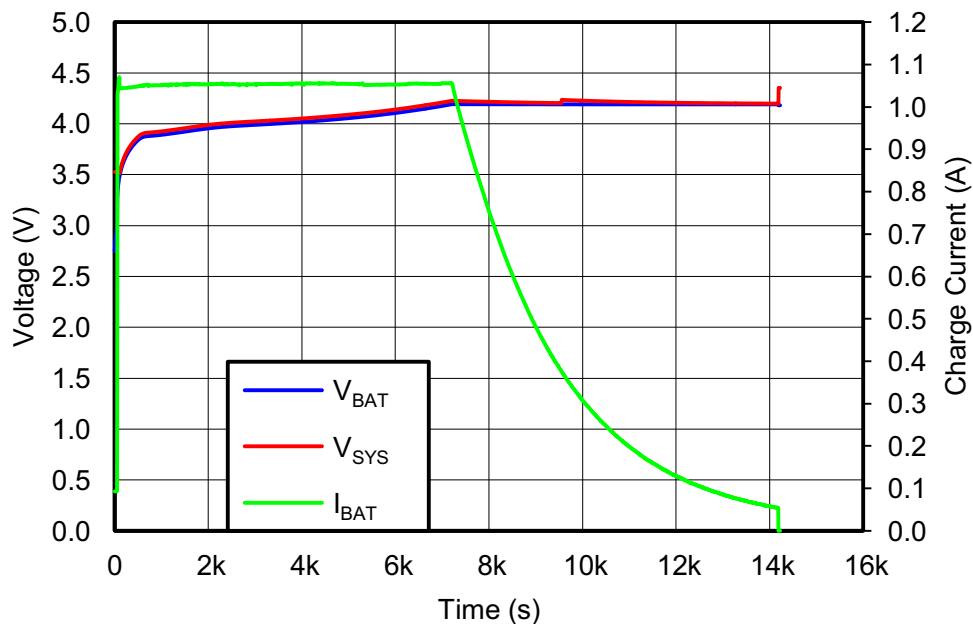


Figure 15. bq24250 Charge Profile and Minimum System Output Voltage Regulation

Figure 16 demonstrates a measured charge profile with the bq2425X while charging a 2700mAh Li-Ion battery at a charge rate of 1A.

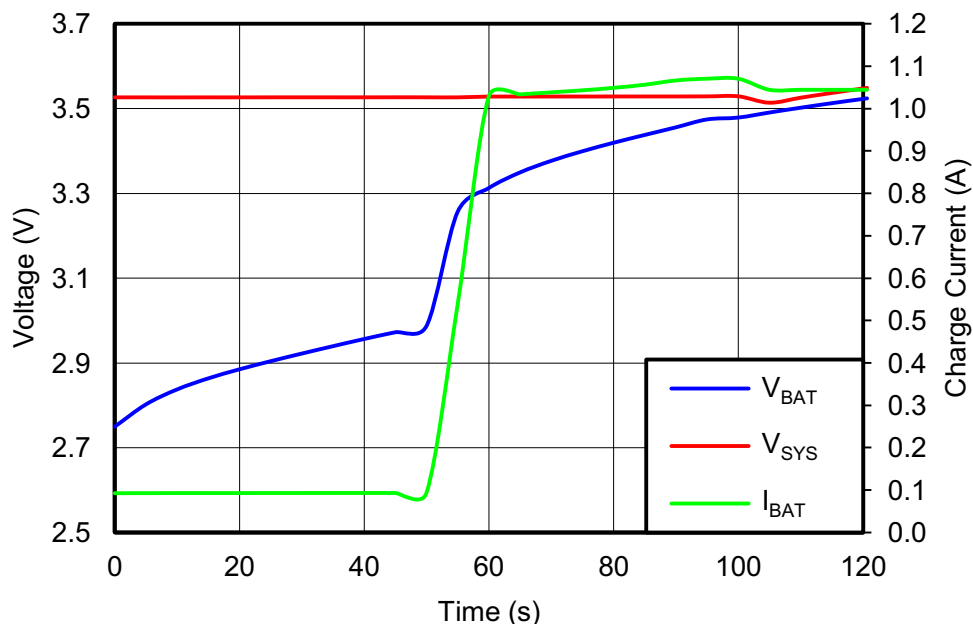
Feature Description (continued)



$I_{CHG} = 1\text{ A}$

Figure 16. bq24250 Charge Profile while Charging a 2700-mAh Battery at a 1A Charge Rate

Figure 17 illustrates the precharge behavior of the above charge profile by narrowing the time axis to 0 – 120 seconds.



$I_{CHG} = 1\text{ A}$

Figure 17. bq24250 Charge Profile While Charging a 2700-mAh Battery at a 1A Charge During Precharge

Feature Description (continued)

9.3.2 EN1 and EN2 Pins

The bq24250 is I²C and Stand Alone part. The EN1 and EN2 pins are available in this IC spin to support USB 2.0 compliance. These pins are used for Input Current Limit Configuration I. Set EN1 and EN2 to control the maximum input current and enable USB compliance. See [Table 1](#) below for programming details.

The bq24251 is also an I²C and Stand Alone part. The EN1 and EN2 are not available for this spin but the D+/D- are available to support the BC1.2 D+/D- Based Adapter Detection. It detects DCP, SDP, and CDP. Also it complies with the unconnected dead battery provision clause. D+ and D- pins are connected to the D+ and D- outputs of the USB port at power up. Also includes the detection of Apple™ and TomTom™ adapters where a 500mA input current limit is enabled. The /PG pin will remain high impedance state until the detection is completed.

The bq24253 is only Stand Alone part. Both of the D+/D- and EN1/EN2 are available for this spin. During power up, the device checks first for the D+/D-. The EN1 and EN2 do not take effect until D+/D- detection routine is over and a change on the status of the EN1 and EN2 occurred.

When the input current limit pins change state, the V_{IN_DPM} threshold changes as well. See [Table 1](#) for the detailed truth table:

Table 1. EN1 and EN2 Truth Table⁽¹⁾

| EN2 | EN1 | Input Current Limit | V _{IN_DPM} Threshold |
|-----|-----|--|-------------------------------|
| 0 | 0 | 500mA | 4.36V |
| 0 | 1 | Externally programmed by ILIM (up to 2.0A) | Externally programmed VDPM |
| 1 | 0 | 100mA | 4.36V |
| 1 | 1 | Input Hi-Z | None |

(1) USB3.0 support available. Contact your local TI representative for details.

9.3.3 External Settings: ISET, ILIM and V_{IN_DPM}

If the external resistor settings are used, the following equations can be followed to configure the charge settings.

The fast charge current resistor (R_{ISET}) can be set by using the following formula:

$$R_{ISET} = \frac{K_{ISET}}{I_{FC}} = \frac{250}{I_{FC}} \quad (1)$$

Where I_{FC} is the desired fast charge current setting in Amperes.

The input current limit resistor (R_{ILIM}) can be set by using the following formula:

$$R_{ILIM} = \frac{K_{ILIM}}{I_C} = \frac{270}{I_C} \quad (2)$$

Where I_C is the desired input current limit in Amperes.

Based on the application diagram reference designators, the resistor R₁ and R₂ can be calculated as follows to set V_{IN_DPM}:

$$V_{IN_DPM} = V_{REF_DPM} \times \frac{R_1 + R_2}{R_2} = 1.2V \times \frac{R_1 + R_2}{R_2} \quad (3)$$

V_{IN_DPM} should be chosen first along with R₁. Choosing R₁ first will ensure that R₂ will be greater than the resistance chosen. This is the case since V_{IN_DPM} should be chosen to be greater than 2x V_{REF_DPM}.

If external resistors are not desired in order to reduce the BOM count, the VDPM and the ILIM pins can be shorted to set the internal defaults. The ISET resistor must be connected in order to avoid an unstable charging state. Note that floating the ILIM pin will result in zero charge current if the external ISET is configured via the I²C register. [Table 2](#) summarizes the settings when the ILIM, ISET, and V_{IN_DPM} pins are shorted to GND:

Table 2. ILIM, VDPM, and ISET Short Behaviors

| PIN SHORTED | BEHAVIOR |
|-------------|--------------------------|
| ILIM | Input current limit = 2A |
| VDPM | $V_{IN_DPM} = 4.68V$ |
| ISET | Fault—Charging Suspended |

9.3.4 BC1.2 D+/D– Detection

The bq24251 and the bq24253 include a fully BC1.2 compatible D+/D– source detection. This detection supports the following types of ports:

- DCP (dedicated charge port)
- CDP (charging downstream port)
- SDP (standard downstream port)
- Apple™/TomTom™ ports

This D+/D– detection algorithm does not support ACA (accessory charge adapter) identification, but the input current will default to 500mA when a charge port is attached to the ACA and bq24251/3 is connected to the OTG port.

The D+/D– detection algorithm is only active when the device is in standalone mode (e.g. the host is not communicating with the device and the watch dog timer has expired). However, when the device is in host mode (e.g. host is communicating via I²C to the device) writing a ‘1’ to register 0x04 bit location 4 (DPDM_EN) forces the device to perform a D+/D– detection. This allows the D+/D– detection to be enabled in both host mode and default mode. The current limit will not be implemented in host mode.

As described previously, the bq24253 is only a Stand Alone part. Both of the D+/D- and EN1/EN2 are available for this spin. The below flow diagram illustrates the behavior of the bq24253 in D+/D- detection and the effect of the EN1/EN2. During power up, the device checks first for the D+/D-. The EN1 and EN2 do not take effect until D+/D- detection routine is over and a change on the status of the EN1 and EN2 occurred.

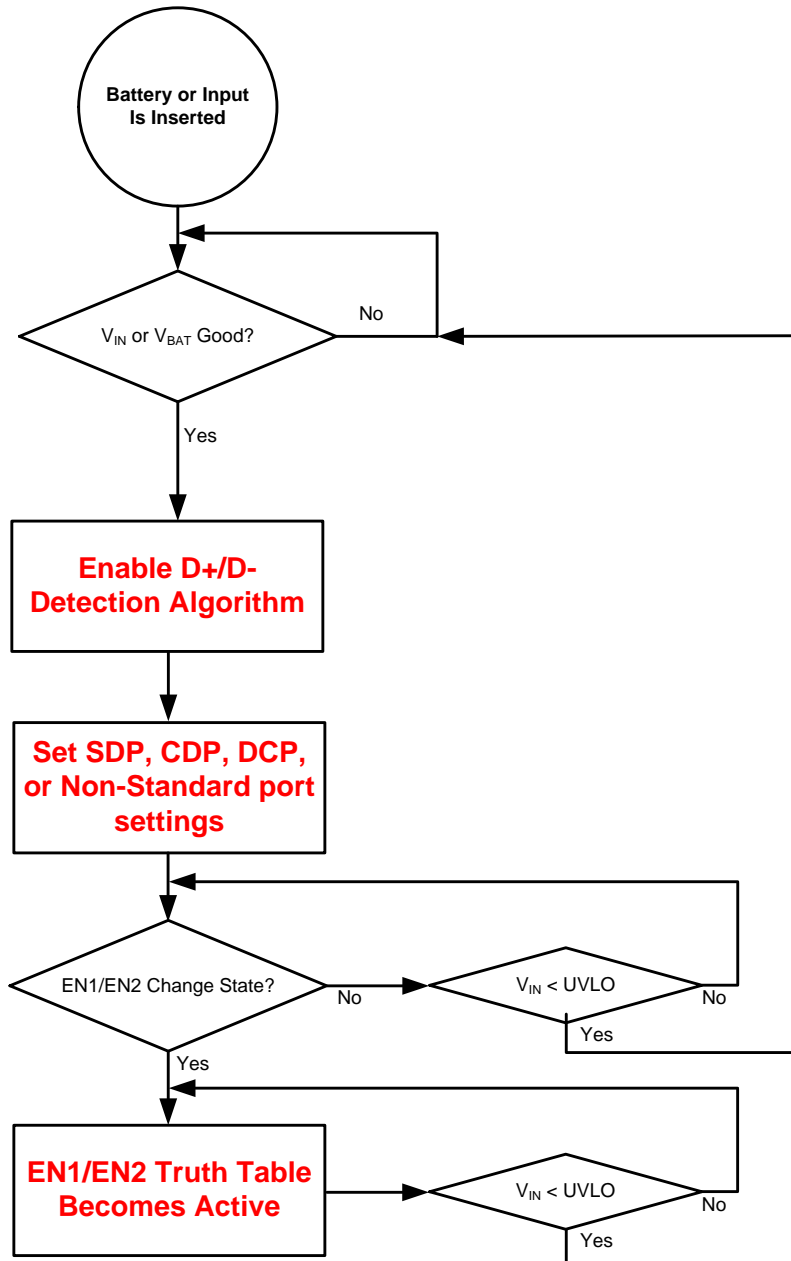


Figure 18. bq24253 D+/D- and EN1/EN2

The D+/D- detection algorithm has 5 primary states. These states are termed the following:

1. Data Contact Detect
2. Primary Detection
3. Secondary Detection
4. Non-standard Adapter Detection (for Apple™ / TomTom™)
5. Detection Configuration

The DCD state determines if the device has properly connected to the D+/D- lines. If the device is not in host mode and VBUS is inserted (or DPDM_EN is true) the device enters the DCD state and enable the appropriate algorithm. If the DCD timer expires, the device enters the Non-standard Adapter Detection (for Apple™ / TomTom™) state. Otherwise it enters the Primary Detection state.

When entering the Primary Detection state, the appropriate algorithm is enabled to determine whether to enter the secondary detection state for DCP and CDP or the secondary detection state for SDP/Non-Standard adapters.

The non-standard adapter detection state for Apple™ / TomTom™ tests for the unique conditions for these non-standard adapters. If the algorithm passes the unique conditions found with these adapters, it proceeds to the Detection Configuration state. Otherwise it reverts back to the primary detection state.

The secondary detection state determines whether the input port is a DCP, CDP, SDP, or other non-standard adapters. If the Primary Detection state indicated that the input port is either a DCP or CDP, the device enables the appropriate algorithm to differentiate between the two. If the Primary Detection state indicated that the input port is either a SDP or non-standard adapter, the device enables the appropriate algorithm to differentiate between these two ports. Once complete, the device continues to the Detection Configuration state.

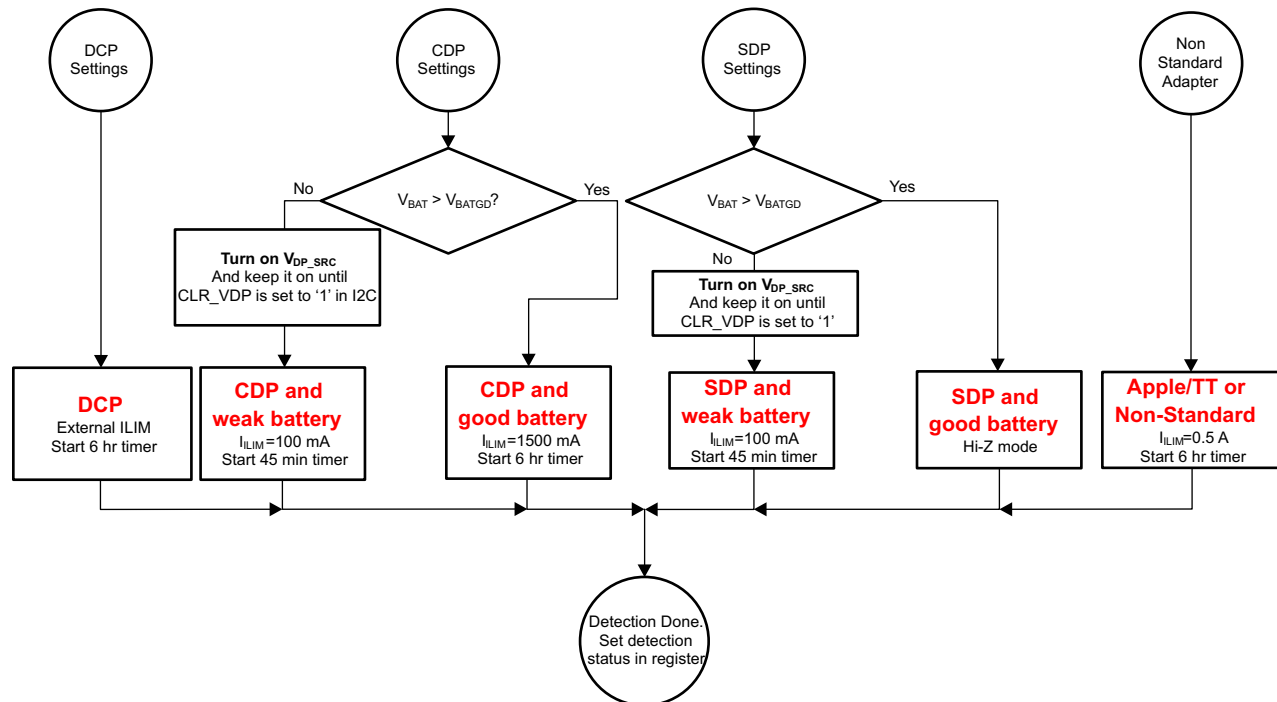


Figure 19. Detection Configuration State

The detection configuration state sets the input current limit of the device along with the charge timer. The exception to the CDP and the SDP settings are due to the Dead Battery Provision (DBP) clause for unconnected devices. This clause states that the device can pull a maximum of 100mA when not connected due to a dead battery. During the battery wakeup time, the device sources a voltage on the D+ pin in order to comply with the DBP clause. Once the battery is good, the system can clear the D+ pin voltage by writing a '1' to address 0x07 bit position 4 (CLR_VDP). The device must connect to the host within 1sec of clearing the D+ pin voltage per the DBP clause.

A summary of the input current limits and timer configurations for each charge port type are found in [Table 3](#).

Table 3. D+/D– Detection Results per Charge Port Type

| CHARGE PORT TYPE | INPUT CURRENT LIMIT | CHARGE TIMER |
|------------------|---------------------|--------------|
| DCP | External ILIM | 6 hours |
| CDP Dead Battery | 100 mA | 45 minutes |
| CDP Good Battery | 1500 mA | 6 hours |
| SDP Dead Battery | 100 mA | 45 minutes |
| SDP Good Battery | Hi-Z | N/A |
| Non-Standard | 500 mA | 6 hours |

9.3.5 Transient Response

The BQ24250/1/3 includes an advanced hybrid switch mode control architecture. When the device is regulating the charge current (fast-charge), a traditional voltage mode control loop is used with a Type-3 compensation network. However, the BQ24250/1/3 switches to a current mode control loop when the device enters voltage regulation. Voltage regulation occurs in three charging conditions: 1) Minimum system voltage regulation (battery below MINSYS), 2) Battery voltage regulation ($I_{BAT} < I_{CHG}$), and 3) Charge Done ($V_{SYS} = V_{BAT} + 3.5\%$). This architecture allows for superior transient performance when regulating the voltage due to the simplification of the compensation when using current mode control. The below transient response plot illustrates a 0A to 2A load step with 4.7ms full cycle and 12% duty cycle. A 3.9V Li-Ion battery is used. The input voltage is set to 5V, charge current is set to 0.5A and the input current is limited to 0.5A. Note that a high line impedance input supply was used to indicate a realistic input scenario (adapter and cable). This is illustrated by the change in V_{IN} seen at the input of the IC.

[Figure 33](#) shows a ringing at both the input voltage and the input current. This is caused by the input current limit speed up comparator.

9.3.6 AnyBoot Battery Detection

The bq2425x family includes a sophisticated battery detection algorithm used to provide the system with the proper status of the battery connection. The AnyBoot battery algorithm also guarantees the detection of voltage based battery protectors that may have a long closure time (due to the hysteresis of the protection switch and the cell capacity). The AnyBoot battery detection algorithm utilizes a dual-voltage based detection methodology where the system rail switches between two primary voltage levels. The period of the voltage level shift is 64ms and therefore the power supply rejection of the down-system electronics detects this shift as essentially DC.

The AnyBoot algorithm has essentially 3 states. The 1st state is used to determine if the device has terminated with a battery attached. If it has terminated due to the battery not being present, then the algorithm moves to the 2nd and 3rd states. The 2nd and 3rd states shift the system voltage level between 4.2V and 3.72V. In each state there are comparator checks to determine if a battery has been inserted. The two states guarantees the detection of a battery even if the voltage of the cell is at the same level of the comparator thresholds. The algorithm will remain in states 2 and 3 until a battery has been inserted. The flow diagram details for the Anyboot algorithm are shown in [Figure 20](#).

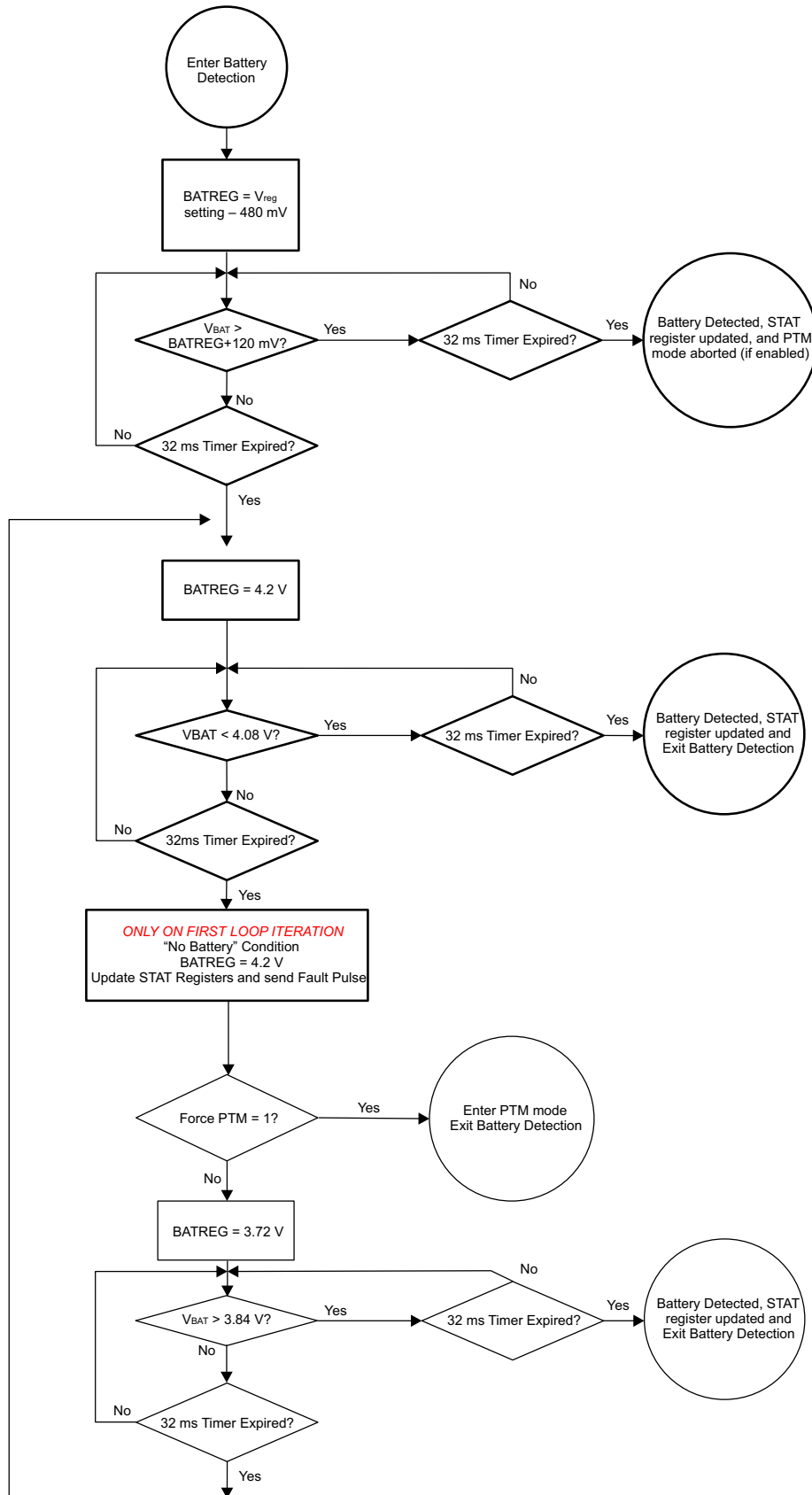


Figure 20. AnyBoot Battery Detection Flow Diagram

9.3.7 Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage decreases. Once the supply drops to VIN_DPM, the input current limit is reduced down to prevent the further drop of the supply. When the IC enters this mode, the charge current is lower than the set. This feature ensures IC compatibility with adapters with different current capabilities without a hardware change.

9.3.8 Sleep Mode

The bq2425x enters the low-power sleep mode if the voltage on VIN falls below sleep-mode entry threshold, VBAT+VSLP, and VIN is higher than the under-voltage lockout threshold, VUVLO. This feature prevents draining the battery during the absence of VIN. When VIN < VBAT+VSLP, the bq2425x turns off the PWM converter, turns on the battery FET, sends a single 256µs pulse on the STAT and INT outputs and the FAULT/STAT bits of the status registers are updated in the I²C. Once VIN > VBAT+VSLP with the hysteresis, the FAULT bits are cleared and the device initiates a new charge cycle.

9.3.9 Input Over-Voltage Protection

The bq2425x provides over-voltage protection on the input that protects downstream circuitry. The built-in input over-voltage protection to protect the device and other components against damage from overvoltage on the input supply (Voltage from VIN to PGND). When VIN > VOVP, the bq2425x turns off the PWM converter, turns on the battery FET, sends a single 256µs pulse on the STAT and INT outputs and the FAULT/STAT bits of the status registers and the battery/supply status registers are updated in the I²C. Once the OVP fault is removed, the FAULT bits are cleared and the device returns to normal operation. The OVP threshold for the bq24250 is programmable from 6.5V to 10.5V using VOVP bits in register #7.

9.3.10 NTC Monitor

The bq24250/1/3 includes the integration of an NTC monitor pin that complies with the JEITA specification (PSE also available upon request). The voltage based NTC monitor allows for the use of any NTC resistor with the use of the circuit shown in Figure 21.

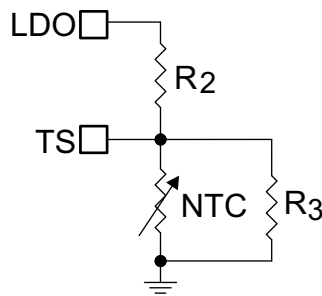


Figure 21. Voltage Based NTC Circuit

The use of R3 is only necessary when the NTC does not have a beta near 3500K. When deviating from this beta, error will be introduced in the actual temperature trip thresholds. The trip thresholds are summarized below which are typical values provided in the specification table.

Table 4. Ratiometric TS Trip Thresholds for JEITA Compliant Charging

| TS THRESHOLDS | V _{TS} /V _{LDO} |
|-------------------|-----------------------------------|
| V _{HOT} | 30.0% |
| V _{WARM} | 38.3% |
| V _{COOL} | 56.5% |
| V _{COLD} | 60% |

When sizing for R2 and R3, it is best to solve two simultaneous equations that ensure the temperature profile of the NTC network will cross the V_{HOT} and V_{COLD} thresholds. The accuracy of the V_{WARM} and V_{COOL} thresholds will depend on the beta of the chosen NTC resistor. The two simultaneous equations are shown below:

$$\%V_{COLD} = \frac{\left(\frac{R_3 R_{NTC}|_{TCOLD}}{R_3 + R_{NTC}|_{TCOLD}} \right)}{\left(\frac{R_3 R_{NTC}|_{TCOLD}}{R_3 + R_{NTC}|_{TCOLD}} \right) + R_2} \times 100$$

$$\%V_{HOT} = \frac{\left(\frac{R_3 R_{NTC}|_{THOT}}{R_3 + R_{NTC}|_{THOT}} \right)}{\left(\frac{R_3 R_{NTC}|_{THOT}}{R_3 + R_{NTC}|_{THOT}} \right) + R_2} \times 100 \quad (4)$$

Where the NTC resistance at the V_{HOT} and V_{COLD} temperatures must be resolved as follows:

$$R_{NTC}|_{TCOLD} = R_0 e^{\beta \left(\frac{1}{TCOLD} - \frac{1}{T_0} \right)}$$

$$R_{NTC}|_{THOT} = R_0 e^{\beta \left(\frac{1}{THOT} - \frac{1}{T_0} \right)} \quad (5)$$

To be JEITA compliant, T_{COLD} must be 0°C and T_{HOT} must be 60°C. If an NTC resistor is chosen such that the beta is 4000K and the nominal resistance is 10kΩ, the following R2 and R3 values result from the above equations:

$$R_2 = 5 \text{ k}\Omega$$

$$R_3 = 9.82 \text{ k}\Omega$$

Figure 22 illustrates the temperature profile of the NTC network with R2 and R3 set to the above values.

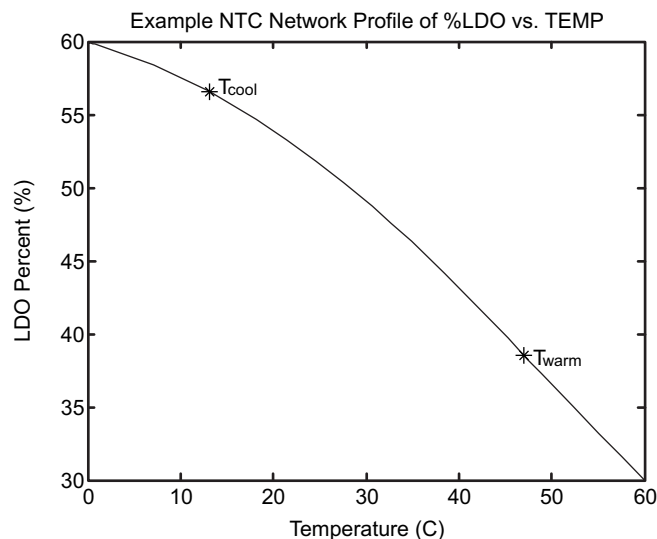


Figure 22. Voltage Based NTC Circuit Temperature Profile

For JEITA compliance, the T_{COOL} and T_{WARM} levels are to be 10°C and 45°C respectively. However, there is some error due to the variation in beta from 3500K. As shown above, the actual temperature points at which the NTC network crosses the V_{COOL} and V_{WARM} are 13°C and 47°C respectively. This error is small but should be considered when choosing the final NTC resistor.

Once the resistors are configured, the internal JEITA algorithm will apply the below profile at each trip point for battery voltage regulation and charge current regulation. In order to ensure continuation of the charge process when an almost-full battery stops charging due to a cold temperature fault, it is recommended that a CE toggle is done on the I2C or CE pin.

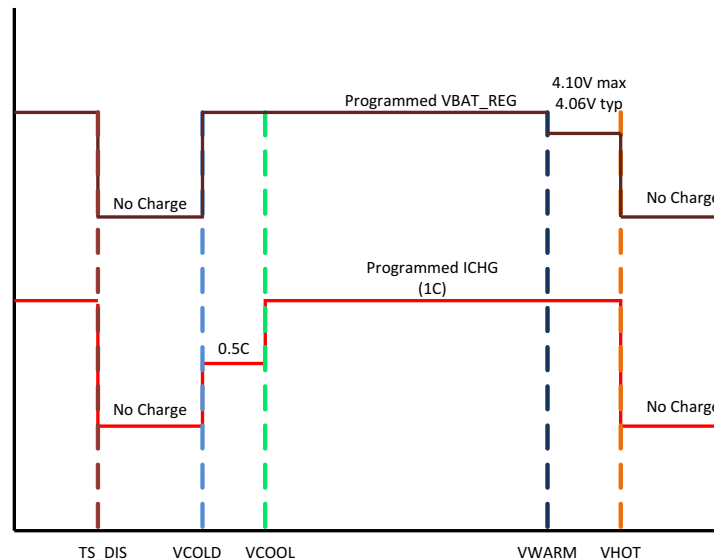


Figure 23. JEITA Profile for Voltage and Current Regulation Loops

9.3.11 Production Test Mode

To aid in end mobile device product manufacturing, the bq2425x includes a Production Test Mode (PTM), where the device is essentially a DC-DC buck converter. In this mode the input current limit to the charger is disabled and the output current limit is limited only by the inductor cycle-by-cycle current (e.g. 3.5A). The PTM mode can be used to test systems with high transient loads such as GSM transmission without the need of a battery being present.

As a means of safety, the Anyboot algorithm will determine if a battery is not present at the output prior to enabling the PTM mode. If a battery is present and the software attempts to enter PTM mode, the device will not enable PTM mode.

9.3.12 Safety Timer

At the beginning of charging process, the bq24250/1/3 starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, the IC enters suspend mode where charging is disabled. The safety timer time is selectable using the I²C interface. A single 256 μ s pulse is sent on the STAT and INT outputs and the FAULT/ bits of the status registers are updated in the I²C. This function prevents continuous charging of a defective battery if the host fails to reset the safety timer. When 2xTMR_EN bit is set to "1", the safety timer runs at a rate 2x slower than normal (the timer is extended) under the following conditions:

- Pre-charge or linear mode (minimum system voltage mode),
- During thermal regulation where the charge current is reduced,
- During TS fault where the charge current is reduced due to temperature rise on the battery, input current limit

The safety timer is suspended during OVP, TS fault where charge is disabled, thermal shut down, and sleep mode. Removing the battery causes the safety timer to be reset and NOT halted/paused.

9.3.13 Watchdog Timer

In addition to the safety timer, the bq24250/1 contains a 50-second watchdog timer that monitors the host through the I2C interface. Once a write is performed on the I2C interface, a watchdog timer is reset and started. The watchdog timer can be disabled by writing "0" on WD_EN bit of register #1. Writing "1" on that bit enables and resets the timer.

If the watchdog timer expires, the IC enters DEFAULT mode where the default charge parameters are loaded and charging continues. The I2C may be accessed again to re-initialize the desired values and restart the watchdog timer as long as the safety timer has not expired. Once the safety timer expires, charging is disabled.

9.3.14 Fault Modes

The bq2425x family includes several hardware fault detections. This allows for specific conditions that could cause a safety concern to be detected. With this feature, the host can be alleviated from monitoring unsafe charging conditions and also allows for a “fail-safe” if the host is not present. The table below summarizes the faults that are detected and the resulting behavior.

| FAULT CONDITION | CHARGER BEHAVIOR | SAFETY TIMER BEHAVIOR |
|-----------------------------|-------------------------------|-----------------------|
| Input OVP | VSYS and ICHG Disabled | Suspended |
| Input UVLO | VSYS and ICHG Disabled | Reset |
| Sleep (VIN < VBAT) | VSYS and ICHG Disabled | Suspended |
| TS Fault (Batter Over Temp) | VSYS Active and ICHG Disabled | Suspended |
| Thermal Shutdown | VSYS and ICHG Disabled | Suspended |
| Timer Fault | VSYS Active and ICHG Disabled | Reset |
| No Battery | VSYS Active and ICHG Disabled | Suspended |
| ISET Short | VSYS Active and ICHG Disabled | Suspended |
| Input Fault & LDO Low | VSYS and ICHG Disabled | Suspended |

9.3.15 Dynamic Power Path Management

The bq24250/1/3 features a SYS output that powers the external system load connected to the battery. This output is active whenever a valid source is connected to IN or BAT. The following discusses the behavior of SYS with a source connected to the supply or a battery source only.

When a valid input source is connected to the input and the charge is enabled, the charge cycle is initiated. In case of VBAT > ~3.5V, the SYS output is connected to VBAT. If the SYS voltage falls to VMINSYS, it is regulated to the VSYSREG threshold to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET is linearly regulated to regulate the charge current into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS.

The dynamic power path management (DPPM) circuitry of the bq24250/1/3 monitors the current limits continuously and if the SYS voltage falls to the VMINSYS voltage, it adjusts charge current to maintain the minimum system voltage and supply the load on SYS. If the charge current is reduced to zero and the load increases further, the bq24250/1/3 enters battery supplement mode. During supplement mode, the battery FET is turned on and the battery supplements the system load.

If the battery is ever 5% above the regulation threshold, the battery OVP circuit shuts the PWM converter off and the battery FET is turned on to discharge the battery to safe operating levels. Battery OVP FAULT is shown in the I2C FAULT registers.

When no input source is available at the input and the battery is connected, the battery FET is turned on similar to supplement mode. The battery must be above VBATUVLO threshold to turn on the SYS output. In this mode, the current is not regulated; however, there is a short circuit current limit. If the short circuit limit is reached, the battery FET is turned off for the deglitch time. After the deglitch time, the battery FET is turned on to test and see if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed. This process is to protect the internal FET from over current.

9.4 Device Functional Modes

9.4.1 I²C Operation (Host Mode / Default Mode)

There are two primary modes of operation when interacting with the charge parameters of the bq24250 and bq24251 chargers: 1) *Host mode* operation where the I²C registers set the charge parameters, and 2) *Default mode* where the register defaults set the charge parameters.

Figure 24 illustrates the behavior of the bq24250 when transitioning between host mode and stand alone mode:

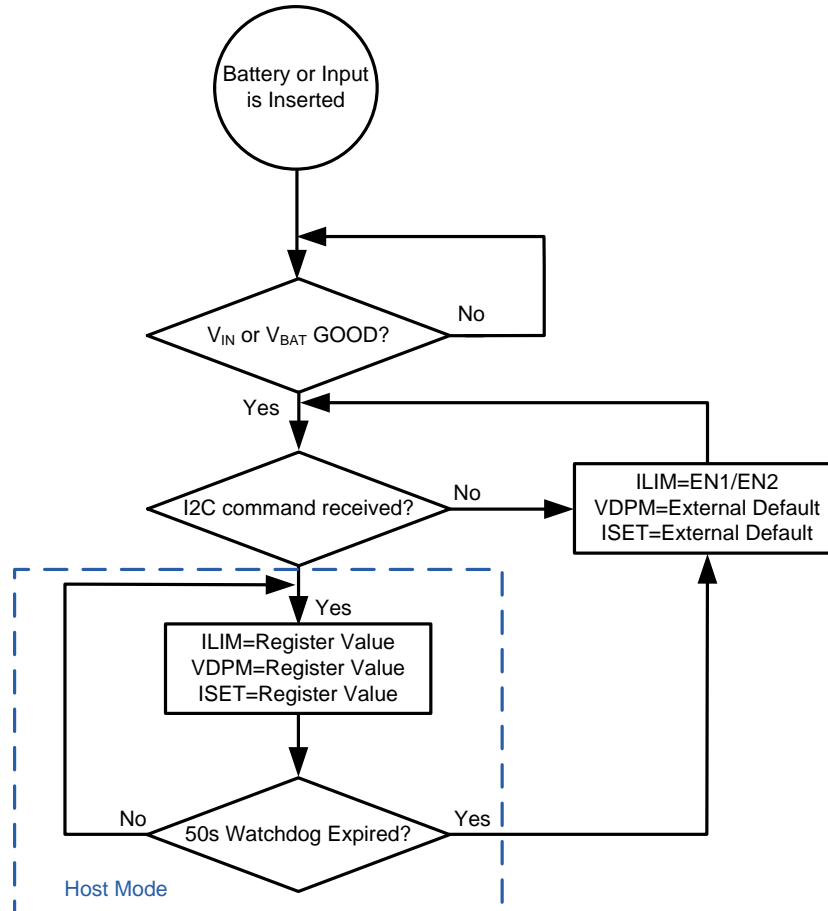


Figure 24. Host Mode and Stand Alone Mode Handoff

Once the battery or input is inserted and above the good thresholds, the device determines if an I²C command has been received in order to discern whether to operate from the I²C registers or the internal register defaults. In stand-alone mode the input current limit is set by the EN1/EN2 pins. If the watch dog timer is enabled, the device will enter stand alone operation once the watchdog timer expires and re-initiate the default charge settings.

9.5 Programming

9.5.1 Serial Interface Description

The bq2425x uses an I²C compatible interface to program charge parameters. I²C™ is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor, see I²C-Bus Specification, Version 5, October 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The bq2425x device works as a slave and supports the following data transfer modes, as defined in the I²C Bus™ Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. The I²C circuitry is powered from IN when a supply is connected.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The bq24250/1 device only supports 7-bit addressing. The device 7-bit address is defined as '1101010' (0x6Ah).

To avoid I²C hang-ups, a timer ($t_{I2C\text{RESET}}$) runs during I2C transactions. If the transaction takes longer than $t_{I2C\text{RESET}}$, any additional commands are ignored and the I2C engine is reset. The timeout is reset with START and repeated START conditions and stops when a valid STOP condition is sent.

9.5.1.1 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 25. All I²C-compatible devices should recognize a start condition.

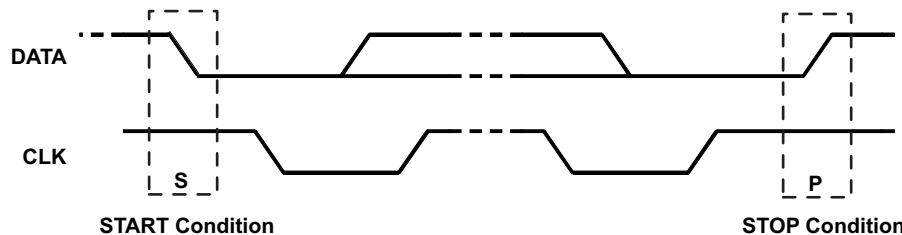


Figure 25. START and STOP Condition

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 26). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 27) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

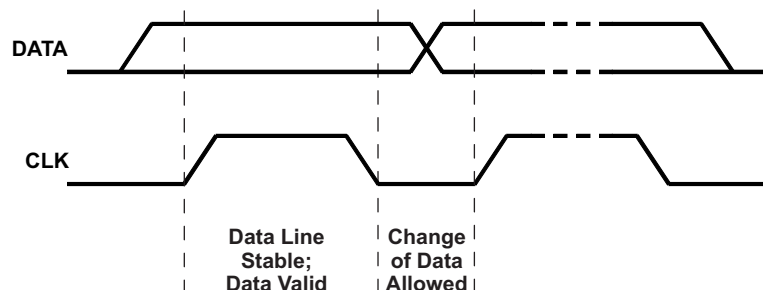


Figure 26. Bit Transfer on the Serial Interface

Programming (continued)

The master generates further SCL cycles to either transmit data to the slave (R/W bit 0) or receive data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 25). This releases the bus and stops the communication link with the addressed slave. All I2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave I2C logic from remaining in a incorrect state. Attempting to read data from register addresses not listed in this section will result in 0xFFh being read out.

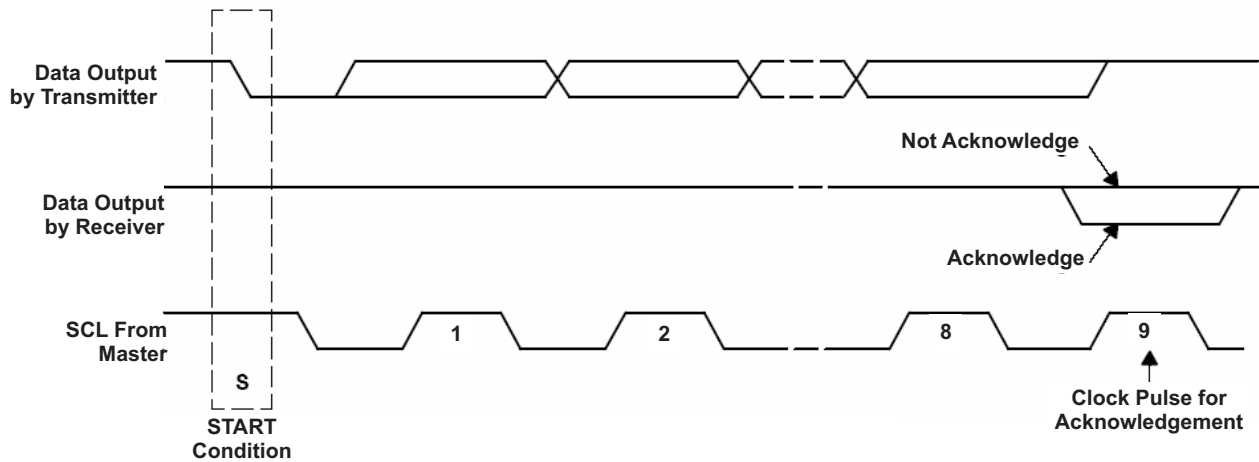


Figure 27. Acknowledge on the I2C Bus

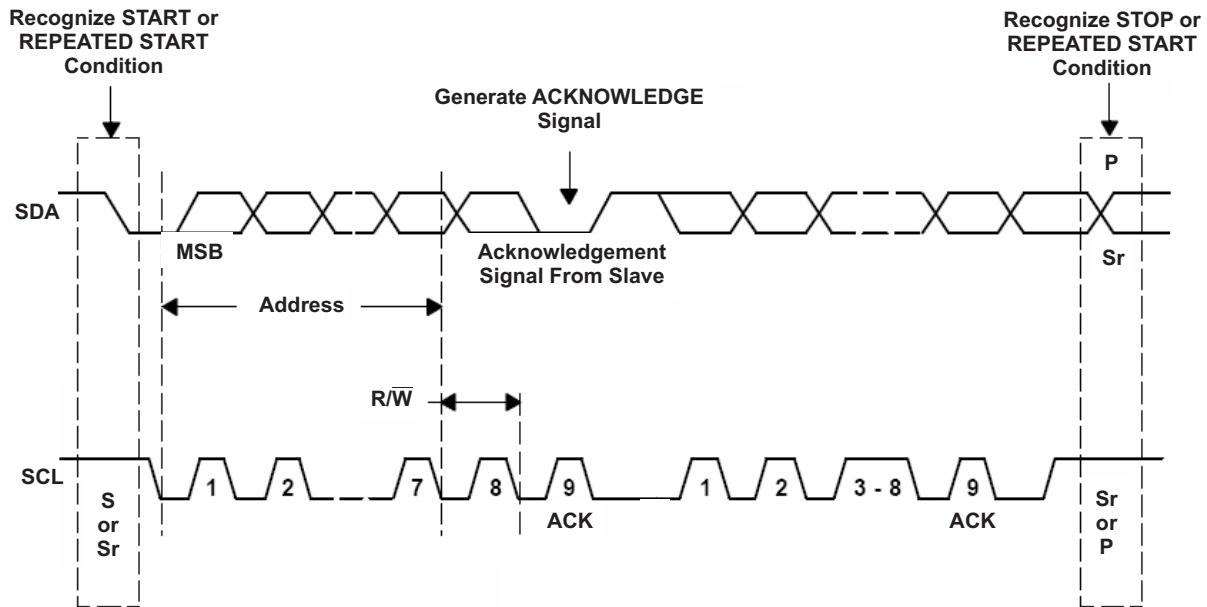


Figure 28. Bus Protocol

9.6 Register Maps

9.6.1 Register #1

Memory location: 00, Reset state: x0xx xxxx

| BIT | NAME | READ/WRITE | FUNCTION |
|---------|----------|------------|--|
| B7(MSB) | WD_FAULT | Read only | Read:0 – No fault 1 – WD timeout if WD enabled |
| B6 | WD_EN | Read/Write | 0 – Disable 1 – Enable (also resets WD timer) |
| B5 | STAT_1 | Read only | 00 – Ready |
| B4 | STAT_0 | Read only | 01 – Charge in progress 10 – Charge done 11 – Fault |
| B3 | FAULT_3 | Read only | 0000 – Normal |
| B2 | FAULT_2 | Read only | 0001 – Input OVP |
| B1 | FAULT_1 | Read only | 0010 – Input UVLO |
| B0(LSB) | FAULT_0 | Read only | 0011 – Sleep 0100 – Battery Temperature (TS) Fault 0101 – Battery OVP 0110 – Thermal Shutdown 0111 – Timer Fault 1000 – No Battery connected 1001 – ISET short 1010 – Input Fault and LDO low |

- **WD_FAULT** – ‘0’ indicates no watch dog fault has occurred, where a ‘1’ indicates a fault has previously occurred.
- **WD_EN** – Enables or disables the internal watch dog timer. A ‘1’ enables the watch dog timer and a ‘0’ disables it. ‘1’ is default for bq24251 only.
- **STAT** – Indicates the charge controller status.
- **FAULT** – Indicates the faults that have occurred. If multiple faults occurred, they can be read by sequentially addressing this register (e.g. reading the register 2 or more times). Once all faults have been read and the device is in a non-fault state, the fault register will show “Normal”. Regarding the "Input Fault & LDO Low" the IC indicates this if LDO is low and at the same time the input is below UVLO or coming out of UVLO with LDO still low.

9.6.2 Register #2

Memory location: 01, Reset state: xxxx 1100

| BIT | NAME | READ/WRITE | FUNCTION |
|----------|--------------------------|------------|---|
| B7(MSB) | Reset | Write only | Write: 1 – Reset all registers to default values 0 – No effect |
| B6 | I _{IN_ILIMIT_2} | Read/Write | 000 – USB2.0 host with 100mA current limit |
| B5 | I _{IN_ILIMIT_1} | Read/Write | 001 – USB3.0 host with 150mA current limit 010 – USB2.0 host with 500mA current limit |
| B4 | I _{IN_ILIMIT_0} | Read/Write | 011 – USB3.0 host with 900mA current limit 100 – Charger with 1500mA current limit 101 – Charger with 2000mA current limit 110 – External ILIM current limit 111- No input current limit with internal clamp at 3A (PTM MODE) |
| B3 | EN_STAT | Read/Write | 0 – Disable STAT function 1 – Enable STAT function |
| B2 | EN_TERM | Read/Write | 0 – Disable charge termination 1 – Enable charge termination |
| B1 | \overline{CE} | Read/Write | 0 – Charging is enabled 1 – Charging is disabled |
| B0 (LSB) | HZ_MODE | Read/Write | 0 – Not high impedance mode 1 – High impedance mode |

- **I_{IN_ILIMIT}** – Sets the input current limit level. When in host mode this register sets the regulation level. However, when in standalone mode (e.g. no I²C writes have occurred after power up or the WD timer has expired) the external resistor setting for I_{ILIM} sets the regulation level.
- **EN_STAT** – Enables and disables the STAT pin. When set to a ‘1’ the STAT pin is enabled and function normally. When set to a ‘0’ the STAT pin is disabled and the open drain FET is in HiZ mode.
- **EN_TERM** – Enables and disables the termination function in the charge controller. When set to a ‘1’ the termination function will be enabled. When set to a ‘0’ the termination function will be disabled. When termination is disabled, there are no indications of the charger terminating (i.e. STAT pin or STAT registers).
- **\overline{CE}** – The charge enable bit which enables or disables the charge function. When set to a ‘0’, the charger operates normally. When set to a ‘1’, the charger is disabled by turning off the BAT FET between SYS and BAT. The SYS pin continues to stay active via the switch mode controller if an input is present.
- **HZ_MODE** – Sets the charger IC into low power standby mode. When set to a ‘1’, the switch mode controller is disabled but the BAT FET remains ON to keep the system powered. When set to a ‘0’, the charger operates normally.

9.6.3 Register #3

Memory location: 02, Reset state: 1000 1111

| BIT | NAME | READ/WRITE | FUNCTION |
|----------|--------------------------|------------|--|
| B7(MSB) | VBATREG_5 ⁽¹⁾ | Read/Write | Battery Regulation Voltage: 640mV (default 1) |
| B6 | VBATREG_4 ⁽¹⁾ | Read/Write | Battery Regulation Voltage: 320mV (default 0) |
| B5 | VBATREG_3 ⁽¹⁾ | Read/Write | Battery Regulation Voltage: 160mV (default 0) |
| B4 | VBATREG_2 ⁽¹⁾ | Read/Write | Battery Regulation Voltage: 80mV (default 0) |
| B3 | VBATREG_1 ⁽¹⁾ | Read/Write | Battery Regulation Voltage: 40mV (default 1) |
| B2 | VBATREG_0 ⁽¹⁾ | Read/Write | Battery Regulation Voltage: 20mV (default 1) |
| B1(4)(5) | USB_DET_1/EN2 | Read Only | Return USB detection result or pin EN2/EN1 status – 00 – DCP detected / EN2=0, EN1=0 01 – CDP detected / EN2=0, EN1=1 10 – SDP detected / EN2=1, EN1=0 11 – Apple/TT or non-standard adaptor detected / EN2=1, EN1=1 |
| B0(LSB) | USB_DET_0/EN1 | Read Only | |

(1) Charge voltage range is 3.5V–4.44V with the offset of 3.5V and step of 20mV (default 4.2V)

- **V_{BATREG}** – Sets the battery regulation voltage
- **USB_DET/EN** – Provides status of the D+/D– detection-results for spins that include the D+/D– pins or the state of EN1/EN2 for spins that include the EN1/EN2 pins

9.6.4 Register #4

Memory location: 03, Reset state: 1111 1000

| BIT | NAME | READ/WRITE | FUNCTION |
|---------|---------------------------|------------|--|
| B7(MSB) | ICHG_4 ^{(1) (2)} | Read/Write | Charge current 800mA – (default 1) |
| B6 | ICHG_3 ^{(1) (2)} | Read/Write | Charge current: 400mA – (default 1) |
| B5 | ICHG_2 ^{(1) (2)} | Read/Write | Charge current: 200mA – (default 1) |
| B4 | ICHG_1 ^{(1) (2)} | Read/Write | Charge current: 100mA – (default 1) |
| B3 | ICHG_0 ^{(1) (2)} | Read/Write | Charge current: 50mA – (default 1) |
| B2 | ITERM_2 ⁽³⁾ | Read/Write | Termination current sense threshold: 100mA (default 0) |
| B1 | ITERM_1 ⁽³⁾ | Read/Write | Termination current sense threshold: 50mA (default 0) |
| B0(LSB) | ITERM_0 ⁽³⁾ | Read/Write | Termination current sense threshold: 25mA (default 0) |

(1) Charge current offset is 500 mA and default charge current is external (maximum is 2.0A)

(2) When all bits are 1's, it is external ISET charging mode

(3) Termination threshold voltage offset is 50mA. The default termination current is 50mA if the charge is selected from I2C. Otherwise, termination is set to 10% of ICHG in external I_{set} mode with +/-10% accuracy.

- **I_{CHG}** – Sets the charge current regulation
- **I_{TERM}** – Sets the current level at which the charger will terminate

9.6.5 Register #5

Memory location: 04, Reset state: xx00 x010

| BIT | NAME | READ/WRITE | FUNCTION |
|---------|-------------------------------------|------------|---|
| B7(MSB) | LOOP_STATUS1 ⁽¹⁾ | Read Only | 00 – No loop is active that slows down timer |
| B6 | LOOP_STATUS0 ⁽¹⁾ | Read Only | 01 – V _{IN-DPM} regulation loop is active 10 – Input current limit loop is active 11 – Thermal regulation loop is active |
| B5 | LOW_CHG | Read/Write | 0 – Normal charge current set by 03h 1 – Low charge current setting 330mA (default 0) |
| B4 | DPDM_EN | Read/Write | 0 – Bit returns to 0 after D+/D- detection is performed 1 – Force D+/D- detection (default 0) |
| B3 | CE_STATUS | Read Only | 0 – CE low 1 – CE high |
| B2 | V _{INDPM_2} ⁽²⁾ | Read/Write | Input V _{IN-DPM} voltage: 320mV (default 0) |
| B1 | V _{INDPM_1} ⁽²⁾ | Read/Write | Input V _{IN-DPM} voltage: 160mV (default 1) |
| B0(LSB) | V _{INDPM_0} ⁽²⁾ | Read/Write | Input V _{IN-DPM} voltage: 80mV (default 0) |

(1) LOOP_STATUS bits show if there are any loop is active that slow down the safety timer. If a status occurs, these bits announce the status and do not clear until read. If more than one occurs, the first one is shown.

(2) V_{IN-DPM} voltage offset is 4.20V and default V_{IN-DPM} threshold is 4.36V.

- **LOOP_STATUS** – Provides the status of the active regulation loop. The charge controller allows for only one loop can regulate at a time.
- **LOW_CHG** – When set to a '1', the charge current is reduced 330mA independent of the charge current setting in register 0x03. When set to '0', the charge current is set by register 0x03.
- **DPDM_EN** – Forces a D+/D- detection routine to be executed once a '1' is written. This is independent of the input being supplied.
- **CE_STATUS** – Provides the status of the $\overline{\text{CE}}$ pin level. If the $\overline{\text{CE}}$ pin is forced high, this bit returns a '1'. If the $\overline{\text{CE}}$ pin is forced low, this bit returns a '0'.
- **V_{INDPM}** – Sets the input VDPM level.

9.6.6 Register #6

Memory location: 05, Reset state: 101x 1xxx

| BIT | NAME | READ/WRITE | FUNCTION |
|---------|----------|------------|--|
| B7(MSB) | 2XTMR_EN | Read/Write | 0 – Timer not slowed at any time 1 – Timer slowed by 2x when in thermal regulation, V_{IN_DPM} or DPPM (default 1) |
| B6 | TMR_1 | Read/Write | Safety Timer Time Limit |
| B5 | TMR_2 | Read/Write | 00 – 0.75 hour fast charge 01 – 6 hour fast charge (default 01) 10 – 9 hour fast charge 11 – Disable safety timers |
| B4 | SYSOFF | Read/Write | 0 – SYSOFF disabled 1 – SYSOFF enabled |
| B3 | TS_EN | Read/Write | 0 – TS function disabled 1 – TS function enabled (default 1) |
| B2 | TS_STAT2 | Read only | TS Fault Mode: 000 – Normal, No TS fault 001 – TS temp > T_{HOT} (Charging suspended for JEITA and Standard TS) 010 – $T_{WARM} < TS \text{ temp} < T_{HOT}$ (Regulation voltage is reduced for JEITA standard) 011 – $T_{COLD} < TS \text{ temp} < T_{COOL}$ (Charge current is reduced for JEITA standard) 100 – TS temp < T_{COLD} (Charging suspended for JEITA and Standard TS) 101 – $T_{FREEZE} < TS \text{ temp} < T_{COLD}$ (Charging at 3.9V and 100mA and only for PSE option only) 110 – TS temp < T_{FREEZE} (Charging suspended for PSE option only) 111 – TS open (TS disabled) |
| B1 | TS_STAT1 | Read only | |
| B0(LSB) | TS_STAT0 | Read only | |

- **2xTMR_EN** – When set to a ‘1’, the 2x Timer function is enabled and allows for the timer to be extended if a condition occurs where the charge current is reduced (i.e. V_{IN_DPM} , thermal regulation, etc.). When set to a ‘0’, this function is disabled and the normal timer will always be executed independent of the current reduce conditions.
- **SYSOFF** – When set to a ‘1’ and the input is removed, the internal battery FET is turned off in order to reduce the leakage from the BAT pin to less than 1 μ A. Note that this disconnects the battery from the system. When set to a ‘0’, this function is disabled.
- **TS_EN** – Enables and disables the TS function. When set to a ‘0’ the TS function is disabled otherwise it is enabled. Only applies to spins that have a TS pin.
- **TS_STAT** – Provides status of the TS pin state for versions that have a TS pin. “100” indicates the TS temp < T_{COLD} and charging suspended for JEITA Standard. In order to ensure continuation of the charge process when an almost-full battery stops charging due to a cold temperature fault, it is recommended that a CE toggle is done on the I2C or CE pin.

9.6.7 Register #7

Memory location: 06, Reset state: 1110 0000

| BIT | NAME | READ/WRITE | FUNCTION |
|---------|------------------|------------|--|
| B7(MSB) | VOVP_2 | Read/Write | OVP voltage: 000 – 6.0V; 001 – 6.5V; 010 – 7.0V; 011 – 8.0V 100 – 9.0V; 101 – 9.5V; 110 – 10.0V; 111 – 10.5V |
| B6 | VOVP_1 | Read/Write | |
| B5 | VOVP_0 | Read/Write | |
| B4 | CLR_VDP | Read/Write | 0 – Keep D+ voltage source on during DBP charging 1 – Turn off D+ voltage source to release D+ line |
| B3 | FORCE_BAT DET | Read/Write | 0 – Enter the battery detection routine only if TERM is true or Force PTM is true 1 – Enter the battery detection routine |
| B2 | FORCE_PTM | Read/Write | 0 – PTM mode is disabled 1 – PTM mode is enabled |
| B1 | N/A | Read/Write | Not available. Keep set to 0. |
| B0(LSB) | N/A | Read/Write | Not available. Keep set to 0. |

- **VOVP** – Sets the OVP level
- **CLR_VDP** – When the D+/D– detection has finished, some cases require the D+ pin to force a voltage of 0.6V. This bit allows the system to clear the voltage prior to any communication on the D+/D– pins. A ‘1’ clears the voltage at the D+ pin if present.
- **FORCE_BATDET** – Forces battery detection and provides status of the battery presence. A logic ‘1’ enables this function.
- **FORCE_PTM** – Puts the device in production test mode (PTM) where the input current limit is disabled. Note that a battery must not be present prior to using this function. Otherwise the function will not be allowed to execute. A logic ‘1’ enables the PTM function.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The bq2425x devices are high-efficiency switched-mode chargers. The device has integrated power FETs that are able to charge at up to a 2-A charging rate, and an integrated 50-mA LDO. In I2C mode (bq24250/1), the device has programmable battery charge voltage (VBATREG), charge current (ICHG), input current limit (ILIM), and input over-voltage protection threshold (VOVP). The charge current and the input current limit are programmed using external resistors (R_{ISET} and R_{ILIM}) connected from the ISET and ILIM pins to ground. The range of these resistors can be found in the datasheet. Both of these currents can be programmed up to 2 A. The device also has complete system-level protection such as input under-voltage lockout (UVLO), input over-voltage protection (OVP), battery OVP, sleep mode, thermal regulation and thermal shutdown, voltage-based NTC monitoring input, and safety timers.

10.2 Typical Application

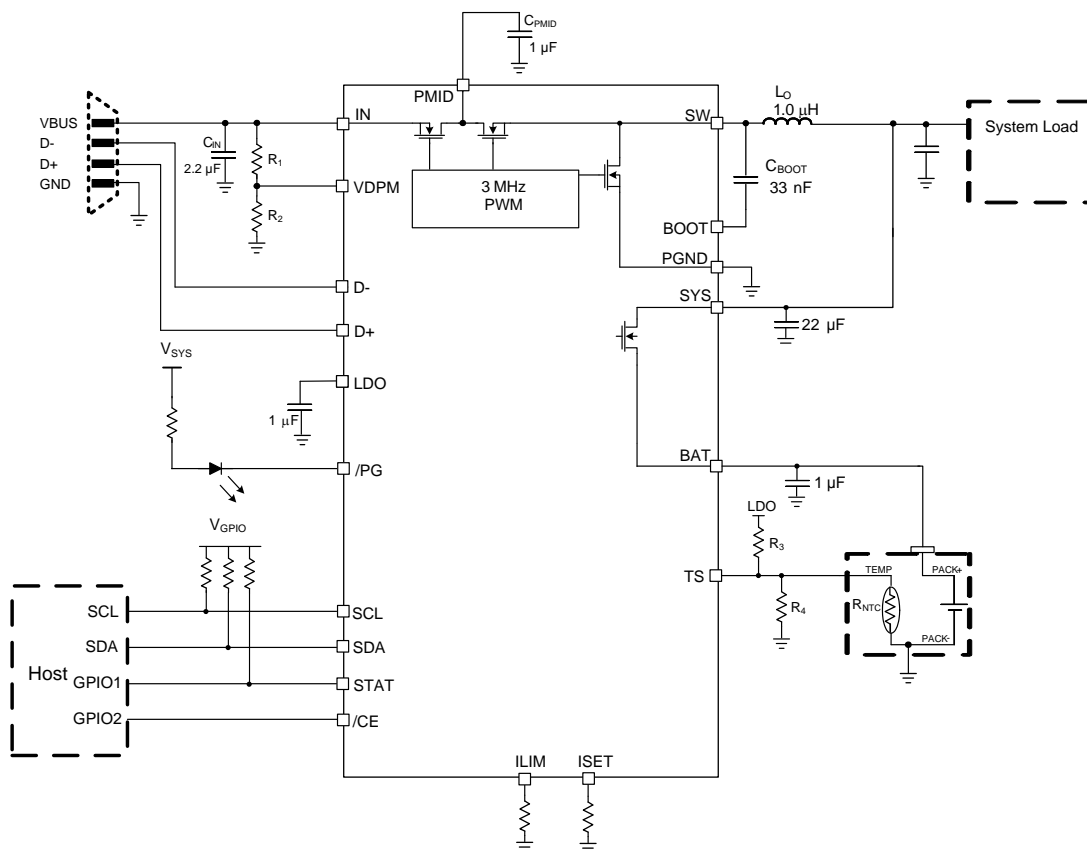


Figure 29. bq24251 Typical Application Circuit

Typical Application (continued)

10.2.1 Design Requirements

Use the following typical application design procedure to select external components values for the bq24251 device.

Table 5. Design Parameters

| SPECIFICATION | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---------------------------|--|------|-----|------|------|
| Input DC voltage, VIN | Recommended input voltage range | 4.35 | | 10.5 | V |
| Input current | Recommended input current range | | | 2 | A |
| Charge current | Fast charge current range | 0.5 | | 2 | A |
| Output regulation voltage | Standalone mode or I2C default mode | | 4.2 | | V |
| Output regulation voltage | I2C host mode: operating in voltage regulation, programmable range | 3.5 | | 4.44 | V |
| LDO | LDO output voltage | | 4.9 | | V |

10.2.2 Detailed Design Procedure

10.2.2.1 Inductor Selection

The inductor selection depends on the application requirements. The bq24250 is designed to operate at around 1 μ H. The value will have an effect on efficiency, and the ripple requirements, stability of the charger, package size, and DCR of the inductor. The 1 μ H inductor provides a good tradeoff between size and efficiency and ripple.

Once the inductance has been selected, the peak current is needed in order to choose the saturation current rating of the inductor. Make sure that the saturation current is always greater than or equal to the calculated I_{PEAK}. The following equation can be used to calculate the current ripple:

$$\Delta I_L = \{VBAT (VIN - VBAT)\}/(VIN \times f_s \times L) \quad (6)$$

Then use current ripple to calculate the peak current as follows:

$$I_{PEAK} = Load \times (1 + \Delta I_L/2) \quad (7)$$

In this design example, the regulation voltage is set to 4.2V, the input voltage is 5V and the inductance is selected to be 1 μ H. The maximum charge current that can be used in this application is 1A and can be set by I2C command. The peak current is needed in order to choose the saturation current rating of the inductor. Using equation 6 and 7, ΔI_L is calculated to be 0.224A and the inductor peak current is 1.112A. A 1 μ F BAT cap is needed and 22 μ F SYS cap is needed on the system trace.

The default settings for external fast charge current and external setting of current limit are chosen to be IFC=500mA and ILIM=1A. R_{ISSET} and R_{LILIM} need to be calculated using equation 1 and 2 in the data sheet.

The fast charge current resistor (R_{ISSET}) can be set as follows:

$$R_{ISSET} = 250/0.5A = 500\Omega$$

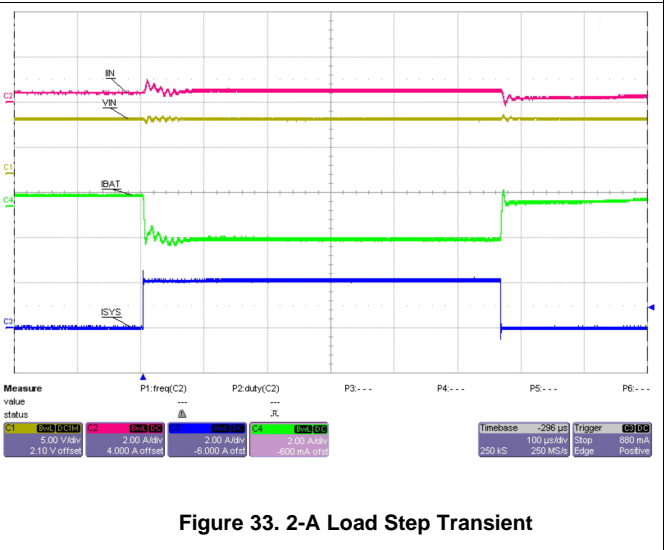
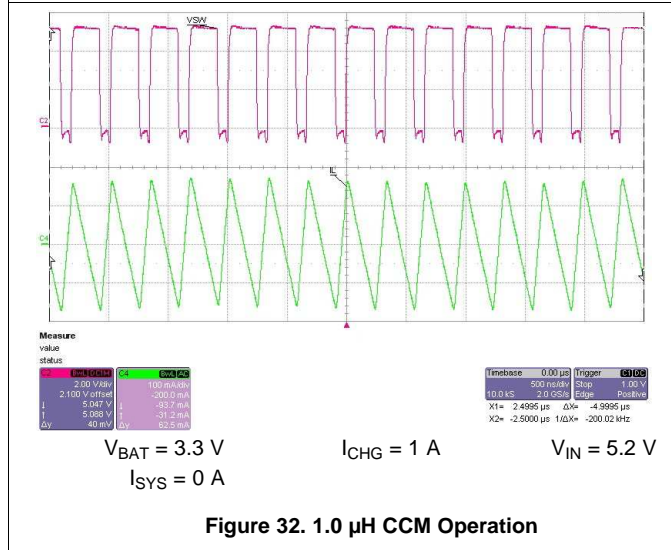
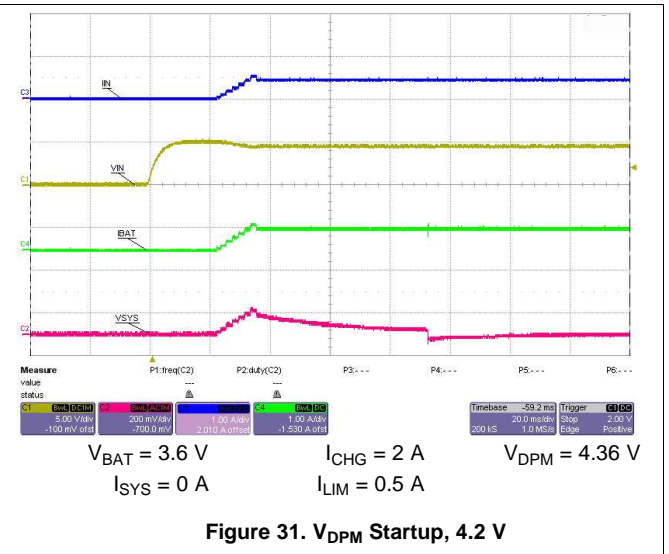
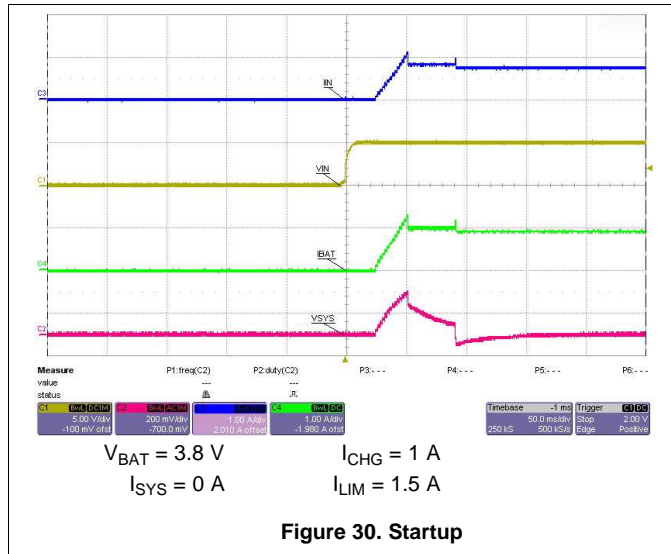
The input current limit resistor (R_{LILIM}) can be set as follows:

$$R_{LILIM} = 270/1A = 270\Omega$$

The external settings of VIN_DPM can be designed by calculating R1 and R2 according to equation 3 in this data sheet and the typical application circuit. VIN_DPM should be chosen first along with R1. VIN_DPM is chosen to be 4.48V and R1 is set to 274K Ω in this design example. Using equation 3, the value of R2 is calculated to be 100K Ω .

In this design example, the application needs to be JEITA compliant. Thus, T_{COLD} must be 0°C and T_{HOT} must be 60°C. If an NTC resistor is chosen such that the beta is 4500K and the nominal resistance is 13K Ω , the calculated R3 and R4 values are 5K Ω and 8.8K Ω respectively. These results are obtained from equation 4 and 5 in this data sheet.

10.2.3 Application Curves



11 Power Supply Recommendations

The devices are designed to operate from an input voltage range between 4.35V and 10.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the bq24250 charger, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

12 Layout

12.1 Layout Guidelines

1. Place the BOOT, PMID, IN, BAT, and LDO capacitors as close as possible to the IC for optimal performance.
2. Connect the inductor as close as possible to the SW pin, and the SYS/CSIN cap as close as possible to the inductor minimizing noise in the path.
3. Place a 1- μ F PMID capacitor as close as possible to the PMID and PGND pins, making the high frequency current loop area as small as possible.
4. The local bypass capacitor from SYS/CSIN to GND must be connected between the SYS/CSIN pin and PGND of the IC. This minimizes the current path loop area from the SW pin through the LC filter and back to the PGND pin.
5. Place all decoupling capacitors close to their respective IC pins and as close as possible to PGND (do not place components such that routing interrupts power-stage currents). All small control signals must be routed away from the high-current paths.
6. To reduce noise coupling, use a ground plane if possible, to isolate the noisy traces from spreading its noise all over the board. Put vias inside the PGND pads for the IC.
7. The high-current charge paths into IN, Micro-USB, BAT, SYS/CSIN, and from the SW pins must be sized appropriately for the maximum charge current to avoid voltage drops in these traces.
8. For high-current applications, the balls for the power paths must be connected to as much copper in the board as possible. This allows better thermal performance because the board conducts heat away from the IC.

12.2 Layout Example

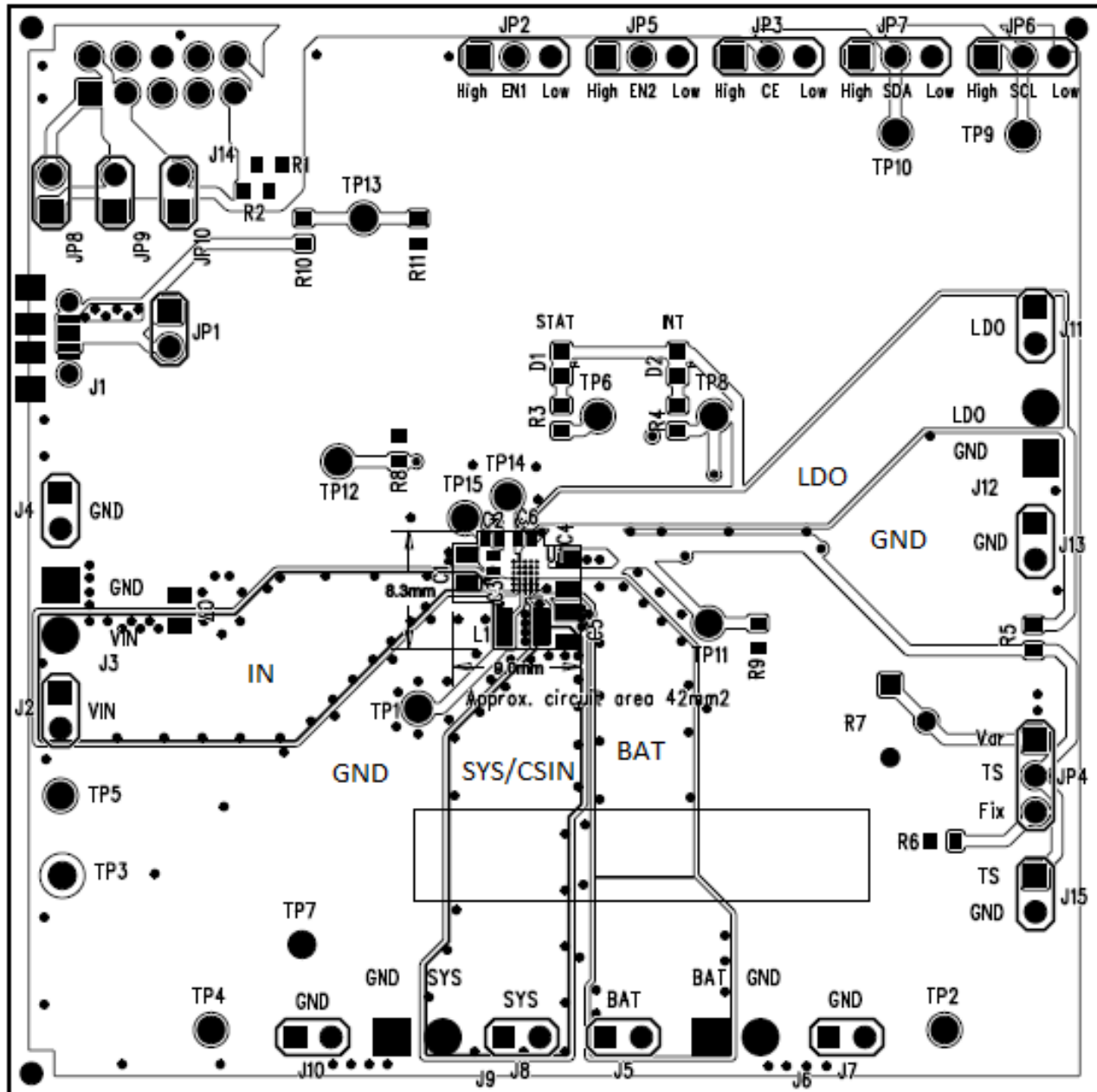


Figure 34. Recommended bq2425x PCB Layout for DSBGA Package

12.3 Thermal Considerations

During the charging process, to prevent overheat of the chip, bq24250/1/3 monitors the junction temperature, T_J , of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, TREG. The charge current is reduced when the junction temperature increases above TREG. Once the charge current is reduced, the system current is reduced while the battery supplements the load to supply the system. This may cause a thermal shutdown of the IC if the die temperature rises too. At any state, if T_J exceeds TSHTDWN, bq2425x suspends charging and disables the buck converter. During thermal shutdown mode, PWM is turned off, all safety timers are suspended, and a single 256 μ s pulse is sent on the STAT and INT outputs and the FAULT/STAT bits of the status registers are updated in the I2C. A new charging cycle begins when T_J falls below TSHTDWN by approximately 10°C.

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| bq24250 | Click here | Click here | Click here | Click here | Click here |
| bq24251 | Click here | Click here | Click here | Click here | Click here |
| bq24253 | Click here | Click here | Click here | Click here | Click here |

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

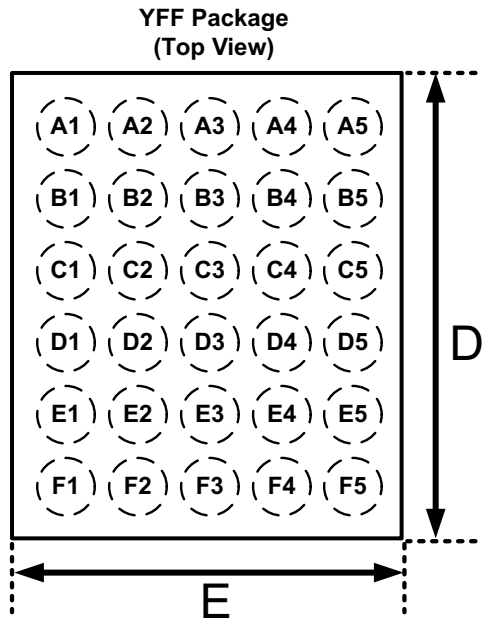
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

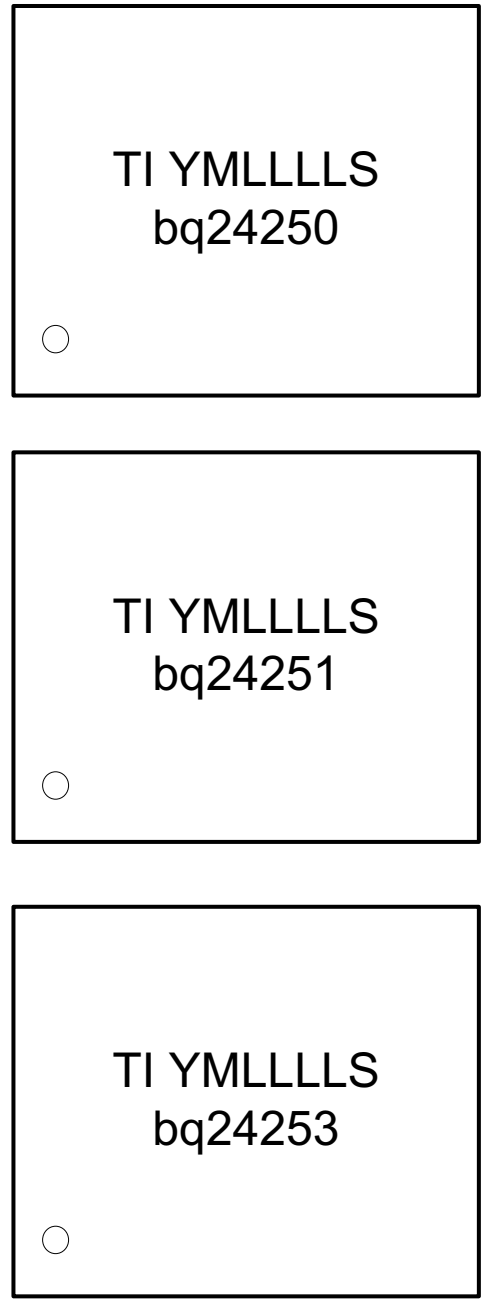
14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 Package Summary



YFF Package Symbol (Top Side Symbol for bq2425x)



0-Pin A1 Marker, TI-TI Letters, YM- Year Month Date Code, LLLL-Lot Trace Code, S-Assembly Site Code

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| BQ24250RGER | Active | Production | VQFN (RGE) 24 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24250RGER.A | Active | Production | VQFN (RGE) 24 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24250RGERG4 | Active | Production | VQFN (RGE) 24 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24250RGERG4.A | Active | Production | VQFN (RGE) 24 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24250RGET | Active | Production | VQFN (RGE) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24250RGET.A | Active | Production | VQFN (RGE) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24250YFFR | Active | Production | DSBGA (YFF) 30 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24250YFFR.A | Active | Production | DSBGA (YFF) 30 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24250YFFT | Active | Production | DSBGA (YFF) 30 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24250YFFT.A | Active | Production | DSBGA (YFF) 30 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24250 |
| BQ24251RGER | NRND | Production | VQFN (RGE) 24 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24251 |
| BQ24251RGER.A | NRND | Production | VQFN (RGE) 24 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24251 |
| BQ24251RGET | NRND | Production | VQFN (RGE) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24251 |
| BQ24251RGET.A | NRND | Production | VQFN (RGE) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24251 |
| BQ24251YFFR | NRND | Production | DSBGA (YFF) 30 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24251 |
| BQ24251YFFR.A | NRND | Production | DSBGA (YFF) 30 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24251 |
| BQ24251YFFT | NRND | Production | DSBGA (YFF) 30 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24251 |
| BQ24251YFFT.A | NRND | Production | DSBGA (YFF) 30 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24251 |
| BQ24253RGER | Active | Production | VQFN (RGE) 24 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24253 |
| BQ24253RGER.A | Active | Production | VQFN (RGE) 24 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24253 |
| BQ24253RGET | Active | Production | VQFN (RGE) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24253 |
| BQ24253RGET.A | Active | Production | VQFN (RGE) 24 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BQ24253 |
| BQ24253YFFR | Active | Production | DSBGA (YFF) 30 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24253 |
| BQ24253YFFR.A | Active | Production | DSBGA (YFF) 30 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24253 |
| BQ24253YFFT | Active | Production | DSBGA (YFF) 30 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24253 |
| BQ24253YFFT.A | Active | Production | DSBGA (YFF) 30 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ24253 |

(1) **Status:** For more details on status, see our [product life cycle](#).

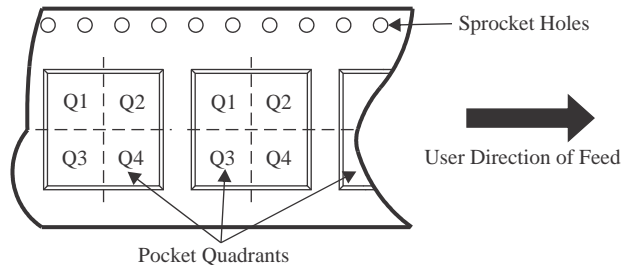
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ24250RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| BQ24250RGERG4 | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| BQ24250RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| BQ24250YFFR | DSBGA | YFF | 30 | 3000 | 180.0 | 8.4 | 2.09 | 2.59 | 0.78 | 4.0 | 8.0 | Q1 |
| BQ24250YFFT | DSBGA | YFF | 30 | 250 | 180.0 | 8.4 | 2.09 | 2.59 | 0.78 | 4.0 | 8.0 | Q1 |
| BQ24251RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| BQ24251RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| BQ24251YFFR | DSBGA | YFF | 30 | 3000 | 180.0 | 8.4 | 2.09 | 2.59 | 0.78 | 4.0 | 8.0 | Q1 |
| BQ24251YFFT | DSBGA | YFF | 30 | 250 | 180.0 | 8.4 | 2.09 | 2.59 | 0.78 | 4.0 | 8.0 | Q1 |
| BQ24253RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| BQ24253RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| BQ24253YFFR | DSBGA | YFF | 30 | 3000 | 180.0 | 8.4 | 2.09 | 2.59 | 0.78 | 4.0 | 8.0 | Q1 |
| BQ24253YFFT | DSBGA | YFF | 30 | 250 | 180.0 | 8.4 | 2.09 | 2.59 | 0.78 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

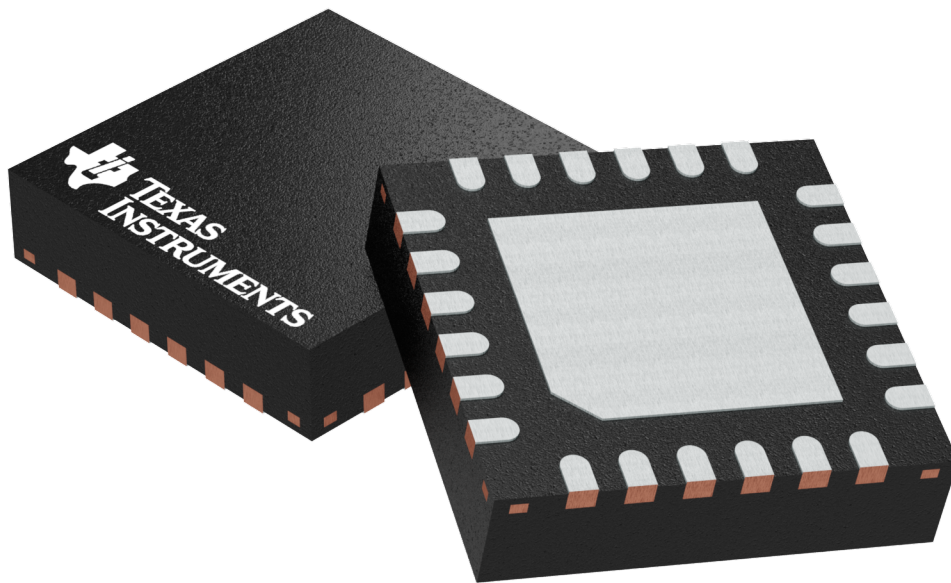
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ24250RGER | VQFN | RGE | 24 | 3000 | 346.0 | 346.0 | 33.0 |
| BQ24250RGERG4 | VQFN | RGE | 24 | 3000 | 346.0 | 346.0 | 33.0 |
| BQ24250RGET | VQFN | RGE | 24 | 250 | 182.0 | 182.0 | 20.0 |
| BQ24250YFFR | DSBGA | YFF | 30 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ24250YFFT | DSBGA | YFF | 30 | 250 | 182.0 | 182.0 | 20.0 |
| BQ24251RGER | VQFN | RGE | 24 | 3000 | 346.0 | 346.0 | 33.0 |
| BQ24251RGET | VQFN | RGE | 24 | 250 | 182.0 | 182.0 | 20.0 |
| BQ24251YFFR | DSBGA | YFF | 30 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ24251YFFT | DSBGA | YFF | 30 | 250 | 182.0 | 182.0 | 20.0 |
| BQ24253RGER | VQFN | RGE | 24 | 3000 | 346.0 | 346.0 | 33.0 |
| BQ24253RGET | VQFN | RGE | 24 | 250 | 182.0 | 182.0 | 20.0 |
| BQ24253YFFR | DSBGA | YFF | 30 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ24253YFFT | DSBGA | YFF | 30 | 250 | 182.0 | 182.0 | 20.0 |

GENERIC PACKAGE VIEW

RGE 24

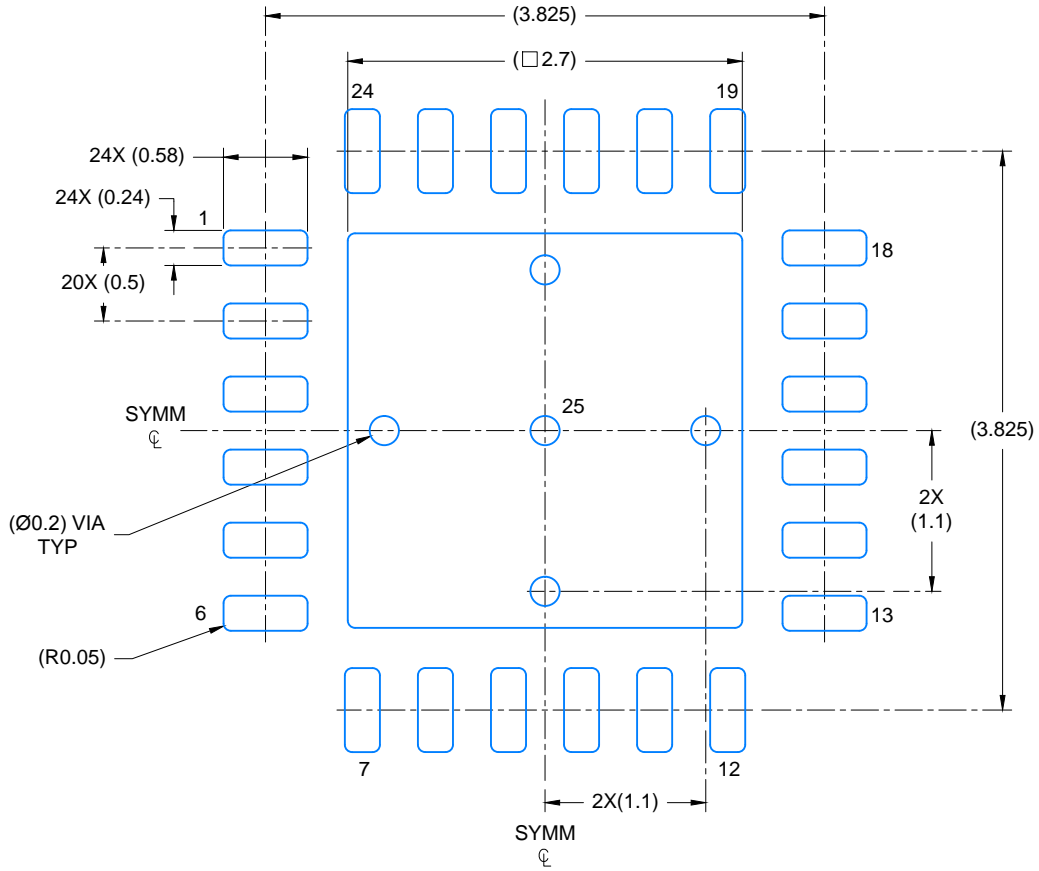
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

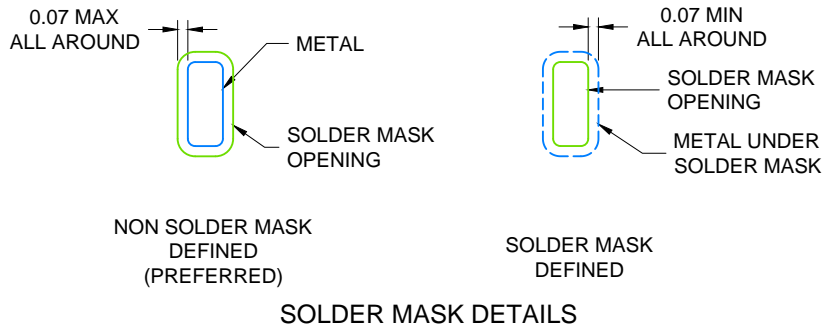


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



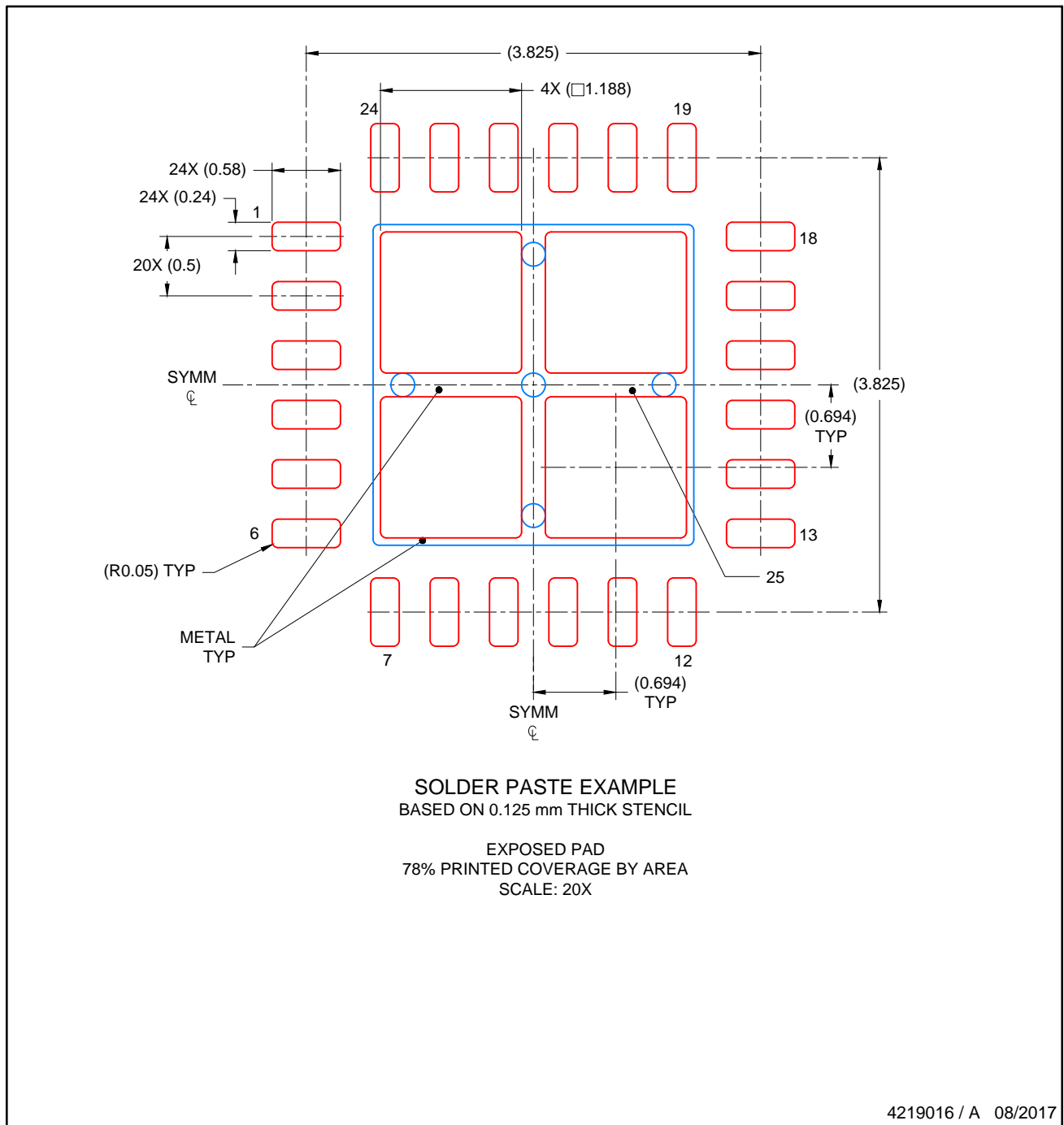
LAND PATTERN EXAMPLE
SCALE: 20X



4219016 / A 08/2017

NOTES: (continued)

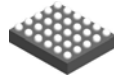
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

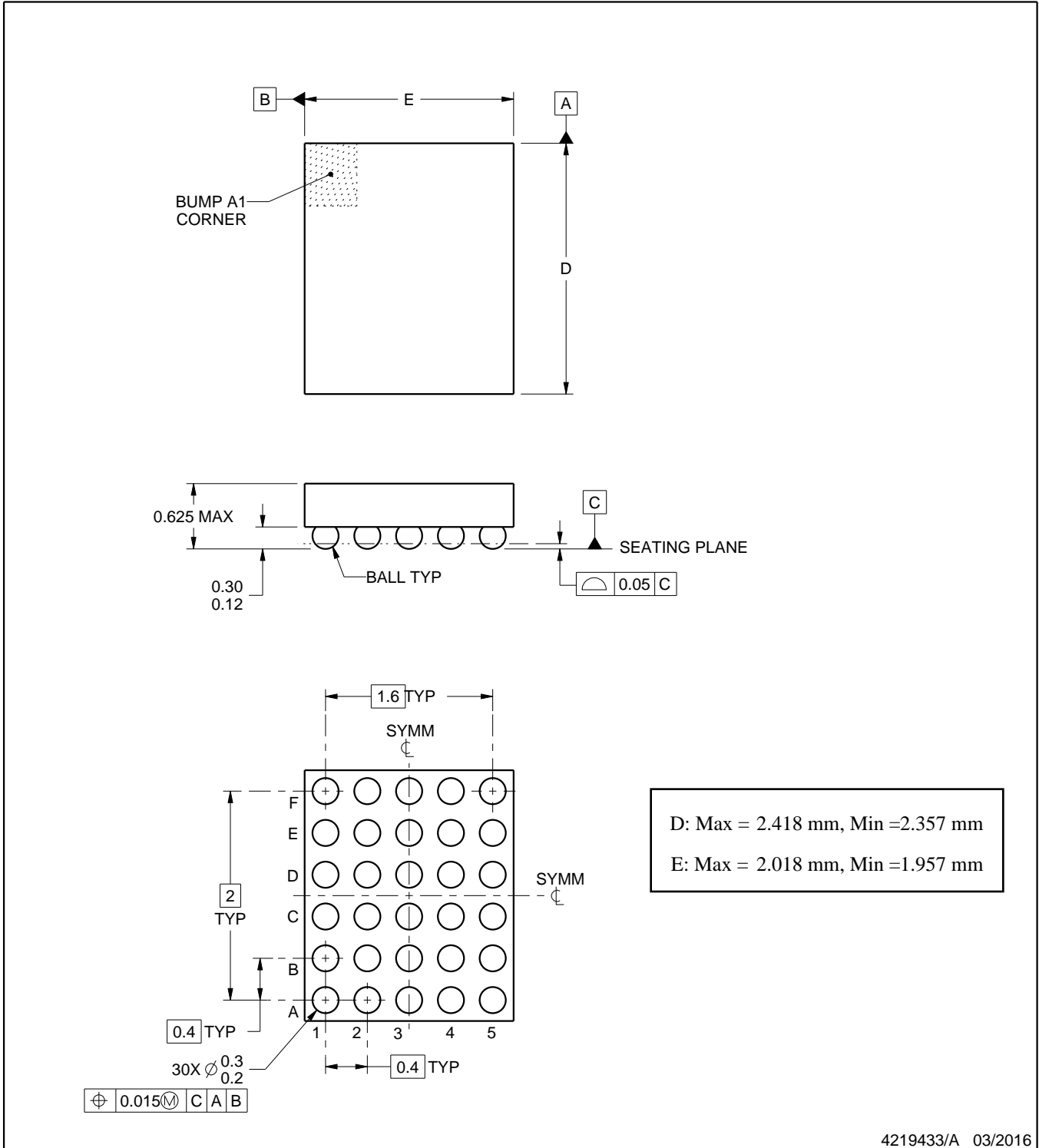
YFF0030



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

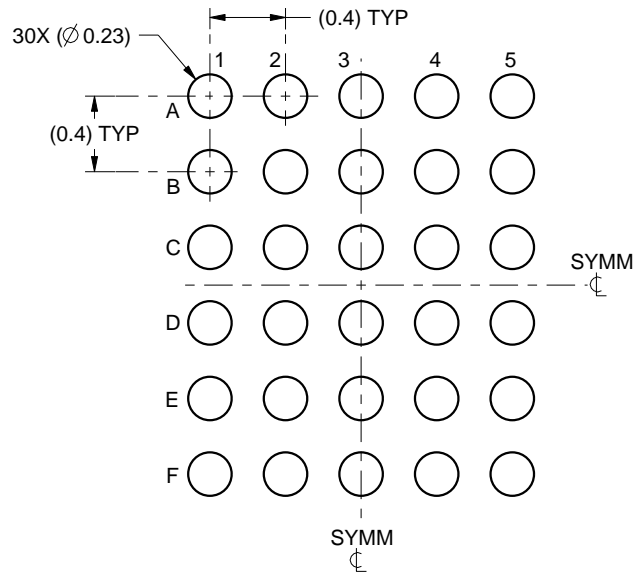
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

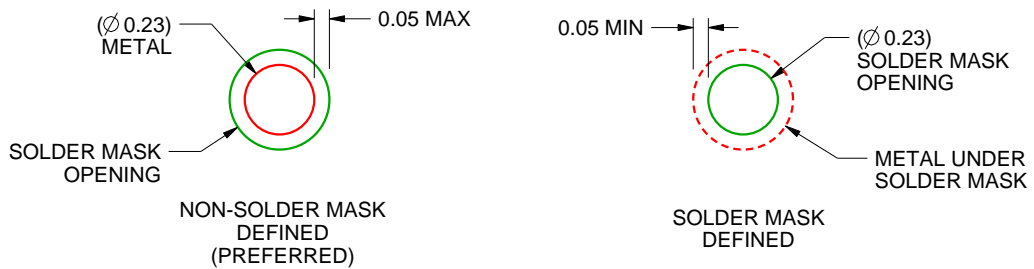
YFF0030

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

4219433/A 03/2016

NOTES: (continued)

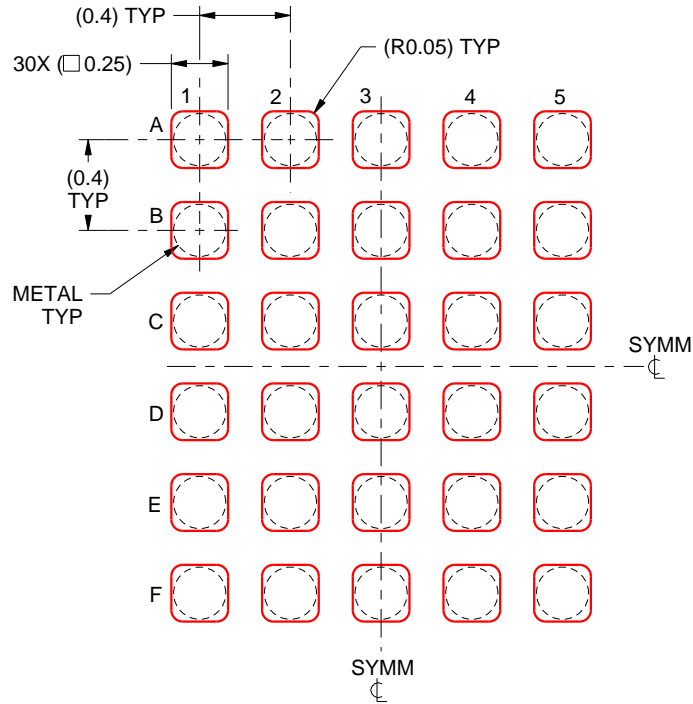
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0030

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219433/A 03/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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