BQ25630 I²C Controlled Single Cell 5A Buck Charger with USB-C Detection

1 Features

- High-efficiency 5A, 1.5MHz, synchronous switch mode buck charger for single cell battery
  - >90% efficiency down to 10mA output current from 5V input
  - Charge current up to 5A in 20mA steps
  - Charge termination from 30 to 1000mA in 10mA steps
  - Highly configurable JEITA profile for safe charging over temperature
- Fully Integrated CC Controller with Dual Role Power (DRP), Try.SNK and Try.SRC
- BATFET control to support shutdown, ship mode and full system reset
  - 1.5µA quiescent current in battery only mode
  - 0.15µA battery leakage current in ship mode
  - 0.1µA battery leakage current in shutdown mode
- Supports USB On-The-Go (OTG) and SRC mode
  - Reverse mode with 3.84V to 9.6V output
  - Programmable current limit up to 3.2A
- Supports a wide range of input sources
  - 3.9V to 18V input operating voltage range with 26V absolute max input voltage
  - Supports USB Type-C inputs, USB BC1.2, HVDCP, and Non-Standard Adapters
  - Supports IINDPM Range from 10mA to 3.2A
  - API (Alternate Power from Input) mode for low power input sources down to 10mA
  - VINDPM automatically tracks battery voltage
  - Input Current Optimizer (ICO) maximizes input power without overloading adapters
- Efficient battery operation with 7mΩ BATFET
- Narrow VDC (NVDC) power path management
  - System instant-on with depleted or no battery
  - Battery supplement when adapter is fully loaded
- Flexible autonomous or I²C-controlled modes
- Integrated 12-bit ADC for voltage, current, and temperature monitoring
- High accuracy
  - ±0.5% charge voltage regulation
  - ±5% charge current regulation
  - ±5% input current regulation
- Safety
  - Liquid detection and corrosion mitigation (Patent Pending)
  - Thermal regulation and thermal shutdown
  - Input/system/battery overvoltage and overcurrent protection
  - Charging safety timer

2 Applications

- Gaming and computer accessories
- Smart phone, tablet
- IP camera, EPOS
- Portable medical equipment

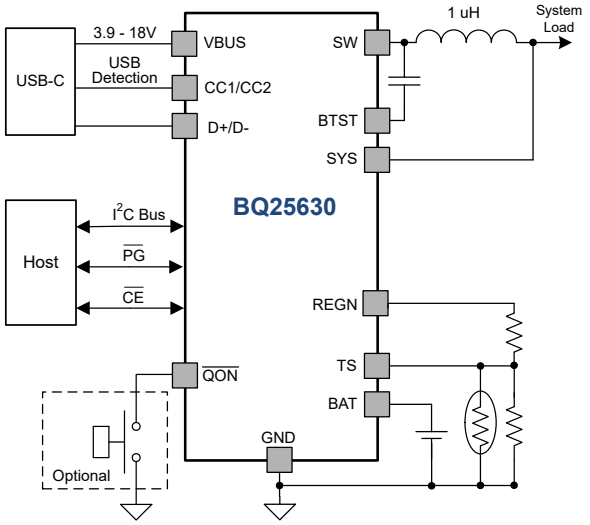
3 Description

The BQ25630 is a highly-integrated 5A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer batteries. The design is highly integrated with built-in current sensing, loop compensation, input reverse-blocking FET (Q1), switching FETs (Q2 and Q3), and battery FET (Q4) between system and battery. The device integrates a USB Type-C controller with Dual-Role Power with Try.SNK and Try.SRC support. The BQ25630 uses NVDC power path management, regulating the system slightly above the battery voltage without dropping below a configurable minimum system voltage. The low impedance power path optimizes efficiency, reduces battery charging time and extends battery life during discharging phase, and the ultra-low 0.15µA ship mode current extends battery shelf life.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
BQ25630	YBG (DSBGA 30)	2.3mm × 2.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



BQ25630 Simplified Application

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4 Description (continued)

The BQ25630 supports a wide range of input sources, including standard USB host port, USB charging port, USB-C adapters, and USB compliant high voltage adapters. The device integrates a USB Type-C controller (CC1/CC2) with USB-C Detection up to 15W and sets the current limit according to the detection result. The device supports Dual-Role Power with Try.SNK and Try.SRC. The device also includes BC1.2 detection using the built-in D+/D- USB adapter detection interface. The BQ25630 is compliant with USB 2.0 and USB 3.0 power specifications for input current and voltage regulation. In addition, the Input Current Optimizer (ICO) supports the detection of maximum power point of the input source without overload. The device also meets USB On-the-Go (OTG) operation power rating specification with constant current limit up to 3.2A.

The power path management regulates the system slightly above battery voltage but does not drop below the programmable minimum system voltage. With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or input voltage limit is reached, the power path management automatically reduces the charge current. If the system load continues to increase, the power path discharges the battery until the system power requirement is met. This supplement mode prevents overloading the input source.

The device initiates and completes a charging cycle without host control. By sensing the battery voltage, the device charges the battery in four different phases: trickle charge, pre-charge, constant current (CC) charge and constant voltage (CV) charge. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset threshold and the battery voltage is higher than the recharge threshold. Termination is supported for TS pin COOL, PRECOOL, NORMAL, WARM and PREWARM temperature zones. When the full battery voltage falls below the programmable recharge threshold, the charger automatically starts a new charging cycle.

The charger provides various safety features for battery charging and system operations, including battery negative temperature coefficient (NTC) thermistor monitoring, charging safety timer and overvoltage and overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds the programmable threshold. Other safety features include battery temperature sensing for charge mode and OTG boost mode, thermal shutdown and input UVLO and over-voltage protection. The device also has an integrated liquid detection and corrosion mitigation feature to protect against port corrosion from moisture. The $\overline{PG}$ output indicates if a good power source is present and above the programmable PG_TH value. The $\overline{INT}$ output immediately notifies the host when a fault occurs or status changes.

The device also provides a 12-bit analog-to-digital converter (ADC) for monitoring charge current and input/battery/system (VBUS, BAT, SYS, TS) voltages. The $\overline{QON}$ pin provides BATFET enable and reset control to exit ship mode and standby mode or initiate a full system reset.

BQ25630 is available in a 30-ball, 2.3mm × 2.4mm DSBGA package.

5 Device Comparison

Table 5-1. Device Comparison

FUNCTION	BQ25630	BQ25638	BQ25898
Input Voltage Range	3.9V - 18V	3.9V - 18V	3.9V - 14V
Maximum Charging Current	5A	5A	4A
USB-C Detection	SNK-Only, SRC-Only, DRP	No	No
D+/D- BC1.2 Support	Yes	No	No
ILIM Pin	No	Yes	Yes
TS Profile	7-Zone Flexible JEITA	7-Zone Flexible JEITA	3-Zone JEITA
Quiescent Battery Current	1.5µA	1.5µA	32µA
Package	2.3x 2.4mm DSBGA 30	2.0x 2.4mm DSBGA 30	2.8x 2.5mm DSBGA 42

6 Pin Configuration and Functions

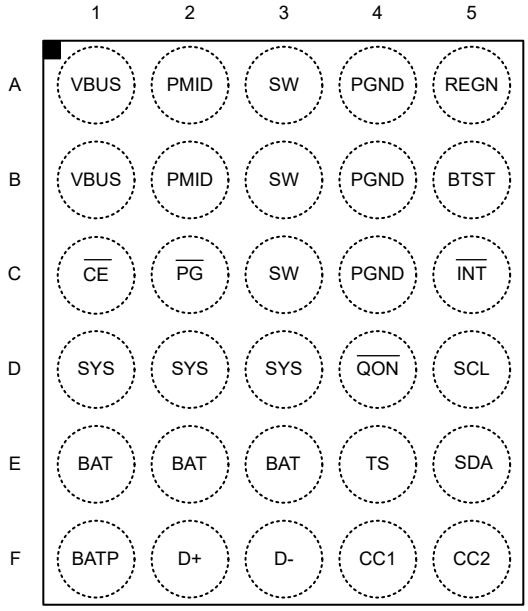


Figure 6-1. BQ25630 Pinout

Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BAT	E1	P	**Positive Terminal of Battery Pack Connection –** The internal BATFET is connected between SYS and BAT. Connect a 10µF ceramic capacitor closely to the BAT pin and GND.
	E2		
	E3		
BATP	F1	AI	**Positive Battery Voltage Sense –** Kelvin connect to positive battery terminal. Place 100Ω series resistance between this pin and the battery positive terminal.
BTST	B5	P	**PWM High-side Driver Supply –** Internally, BTST is connected to the cathode of the boot-strap diode. Connect a 47nF bootstrap capacitor from SW to BTST.
$\overline{CE}$	C1	DI	**Active Low Charge Enable Pin –** Battery charging is enabled when EN_CHG bit is 1 and CE pin is LOW. CE pin must be pulled HIGH or LOW, do not leave floating.
D+	F2	AIO	**Positive USB data line –** D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and non-standard adaptors.
D−	F3	AIO	**Negative USB data line –** D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and non-standard adaptors.
CC1	F4	AIO	**Type-C Configuration Channel 1 –** Used for USB-C connector orientation, connection detection, connection removal, and current capabilities.
CC2	F5	AIO	**Type-C Configuration Channel 2 –** Used for USB-C connector orientation, connection detection, connection removal, and current capabilities.
$\overline{INT}$	C5	DO	**Open Drain Active Low Interrupt Output –** Connect /INT to the logic rail via a 10kΩ resistor. The INT pin sends active low, 256µs pulse to the host to report charger device status and fault.
$\overline{PG}$	C2	DO	**Open Drain Active Low Power Good Indicator –** Connect to the pull up rail via a 2.2kΩ resistor. LOW indicates a valid input source above PG_TH.
PGND	A4	P	**Ground Return**
	B4		
	C4		
PMID	A2	P	**Blocking MOSFET Connection –** Given the total input capacitance, place 1µF on VBUS, and the rest on PMID, as close to the IC as possible. Typical value: 10µF in parallel with 0.1µF ceramic capacitor.
	B2		

Table 6-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
$\overline{QON}$	D4	DI	**BATFET Enable or System Power Reset Control Input –** Pull low to wake up from ship mode or standby mode, or hold low for System Reset. The pin contains an internal pull-up to maintain default high logic.
REGN	A5	P	**Internal Linear Regulator Output –** Internally, REGN is connected to the anode of the boot-strap diode. Connect a 10V or higher rating 4.7µF ceramic capacitor from REGN to power ground. The capacitor must be close to the IC. The REGN LDO output is used for the internal MOSFETs gate driving voltage and for biasing the external TS pin thermistor.
SCL	D5	DI	**I^2C Interface Clock –** Connect SCL to the logic rail through a 10kΩ resistor.
SDA	E5	DIO	**I^2C Interface Data –** Connect SDA to the logic rail through a 10kΩ resistor.
SW	A3	P	**Switching Node Connecting to Output Inductor –** Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 47nF bootstrap capacitor from SW to BTST.
	B3		
	C3		
SYS	D1	P	**Charger Output Voltage to System –** Buck converter output connection point to the system. The internal BATFET is connected between SYS and BAT. Connect 20µF close to the SYS pin.
	D2		
	D3		
TS	E4	AI	**Temperature Qualification Voltage Input –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from TS pin bias reference to TS, then to GND. Charge suspends when TS pin voltage is out of range. Recommend a 103AT-2 10kΩ thermistor.
VBUS	A1	P	**Charger Input Voltage –** The internal n-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1µF ceramic capacitor from VBUS to GND as close as possible to IC.
	B1		

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range (with respect to GND)	VBUS (converter not switching)	–2	26	V
	PMID (converter not switching)	–0.3	26	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SW	–2 (50ns)	21	V
	BATP, $\overline{CE}$, D+, D-, $\overline{INT}$, $\overline{PG}$, $\overline{QON}$, REGN, SCL, SDA, TS	–0.3	6	V
	CC1, CC2	–0.3	26	V
Differential Voltage	BTST-SW	–0.3	6	V
	PMID-VBUS	–0.3	6	V
	SYS-BAT	–0.3	6	V
Output Sink Current	$\overline{INT}$, $\overline{PG}$		6	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	3.9		18	V
V_{BAT}	Battery voltage			4.8	V
I_{VBUS}	Input current			3.2	A
I_{SW}	Output current (SW)			5.0	A
I_{BAT}	Fast charging current			5.0	A
	RMS discharge current (continuously)			7	A
	Peak discharge current (up to 50ms)			9	A
I_{REGN}	Maximum REGN Current, $V_{VBUS} \le 18$ V			20	mA
I_{REGN}	Maximum REGN Current, 18 V $\le V_{VBUS} \le$ 28 V			8.5	mA
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C
L_{SW}	Inductor for the switching regulator	0.68		2.2	µH
C_{VBUS}	VBUS capacitor (without de-rating)	1			µF
C_{PMID}	PMID capacitor (without de-rating)	10			µF
C_{SYS}	SYS capacitor (without de-rating)	20			µF

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
C_{BAT}	BAT capacitor (without de-rating)	10			µF
C_{SYS}	Effective SYS capacitance with NVM_EN_MIN_CSYS=1 (after voltage de-rating)	1.5			µF

7.4 Thermal Information

THERMAL METRIC(1)		BQ25630 YBG (DSBGA) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (BQ25630EVM)	21.4	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_BAT}	Quiescent battery current (BAT, SYS, SW) in battery only mode	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, CC Disabled, system is powered by battery. -40 °C < T_J < 60 °C		1.5	3.1	µA
$I_{Q\_BAT\_SNK}$	Quiescent battery current (BAT, SYS, SW) in battery only mode with CC advertising SNK Only	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, CC advertising SNK Only, system is powered by battery. -40 °C < T_J < 60 °C		2.1	4.0	µA
$I_{Q\_BAT\_SRC}$	Quiescent battery current (BAT, SYS, SW) in battery only mode with CC advertising SRC Only	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, CC advertising SRC Only, system is powered by battery. -40 °C < T_J < 60 °C		25	30	µA
$I_{Q\_BAT\_DRP}$	Quiescent battery current (BAT, SYS, SW) in battery only mode with CC advertising DRP	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, CC advertising DRP, system is powered by battery. -40 °C < T_J < 60 °C		25	30	µA
$I_{Q\_BAT\_ADC}$	Quiescent battery current (BAT, SYS, SW) in battery only mode with ADC Enabled	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC enabled, system is powered by battery. -40 °C < T_J < 60 °C		260		µA
$I_{Q\_BAT\_SD}$	Quiescent battery current (BAT) when the charger is in shutdown mode	VBAT = 4V, No VBUS, BATFET is disabled, I2C disabled, in shutdown mode, ADC disabled, T_J < 60 °C		100	200	nA
$I_{Q\_BAT\_SHIP}$	Quiescent batery current (BAT) when the charger is in ship mode	VBAT = 4V, No VBUS, BATFET is disabled, I2C disabled, in ship mode, ADC disabled, T_J < 60 °C		150	300	nA
$I_{Q\_BAT\_STANDBY}$	Quiescent battery current (BAT) when the charger is in standby mode	VBAT = 4V, CC_DIS=1, No VBUS, BATFET is disabled, I2C enabled, in standby mode, CC disabled, ADC disabled, T_J < 60 °C		1.3	2.5	µA

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q_VBUS}	Quiescent input current (VBUS)	VBUS = 5V, VBAT = 4V, charge disabled, converter switching, ISYS = 0A, PFM enabled, TS float		450		µA
I_{SD_VBUS}	Quiescent input current (VBUS) in HIZ	VBUS = 5V, VBAT = 4V, HIZ mode, ADC disabled, DIS_CC = 1		5	20	µA
		VBUS = 15V, VBAT = 4V, HIZ mode, ADC disabled, DIS_CC = 1		20	35	µA
		VBUS = 5V, VBAT = 4V, HIZ mode, ADC disabled, DIS_CC = 0		5	25	µA
I_{Q_OTG}	Quiescent battery current (BAT, SYS, SW) in boost OTG / SRC mode	VBAT = 4V, VBUS = 5V, OTG mode enabled, converter switching, PFM enabled, I_{VBUS} = 0A, TS float, TS_IGNORE = 1		250		µA
VBUS / VBAT SUPPLY						
V_{VBUS_OP}	VBUS operating range		3.9		18	V
V_{VBUS_UVLO}	VBUS falling to turn off I2C, no battery	VBUS falling	3.0	3.15	3.3	V
V_{VBUS_UVLOZ}	VBUS rising for active I2C, no battery	VBUS rising	3.2	3.35	3.5	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising, VBUS_OVP = 0	6.1	6.5	6.7	V
		VBUS rising, VBUS_OVP = 1	18.5	18.8	19.1	V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS falling, VBUS_OVP = 0	5.8	6.0	6.2	V
		VBUS falling, VBUS_OVP = 1	17.6	17.8	18.3	V
V_{SLEEP}	Sleep mode falling threshold	(VBUS - VBAT), VBUS falling	9	45	85	mV
V_{SLEEPZ}	Sleep mode rising threshold	(VBUS - VBAT), VBUS rising	115	220	340	mV
V_{BAT_UVLOZ}	BAT voltage for active I2C, turn on BATFET, no VBUS	VBAT rising	2.3	2.4	2.5	V
V_{BAT_UVLO}	BAT voltage to turnoff I2C, turn off BATFET, no VBUS	VBAT falling, VBAT_UVLO = 0	2.1	2.2	2.3	V
		VBAT falling, VBAT_UVLO = 1	1.7	1.8	1.9	V
V_{BAT_OTG}	BAT voltage rising threshold to enable OTG mode	VBAT rising, VBAT_OTG_MIN = 00	3.1	3.2	3.3	V
		VBAT rising, VBAT_OTG_MIN = 01	2.9	3.0	3.1	V
		VBAT rising, VBAT_OTG_MIN = 10	2.7	2.8	2.9	V
		VBAT rising, VBAT_OTG_MIN = 11	2.5	2.6	2.7	V
V_{BAT_OTGZ}	BAT voltage falling threshold to disable OTG mode	VBAT falling, VBAT_OTG_MIN = 00	2.9	3.0	3.1	V
		VBAT falling, VBAT_OTG_MIN = 01	2.7	2.8	2.9	V
		VBAT falling, VBAT_OTG_MIN = 10	2.5	2.6	2.7	V
		VBAT falling, VBAT_OTG_MIN = 11	2.3	2.4	2.5	V
POWER-PATH MANAGEMENT						
$V_{SYS\_REG\_ACC}$	Typical system voltage regulation	ISYS = 0A, VBAT > VSYSMIN, Charge Disabled. Offset above VBAT		50		mV
		ISYS = 0A, V_{BAT} < VSYSMIN, Charge Disabled. Offset above VSYSMIN		230		mV
V_{SYSMIN_RNG}	VSYSMIN register range		2.56		4.0	V
$V_{SYSMIN\_REG\_STEP}$	VSYSMIN register step size			80		mV
$V_{SYSMIN\_REG\_ACC}$	Minimum DC system voltage output	ISYS = 0A, V_{BAT} < VSYSMIN = B00h (3.52V), Charge Disabled	3.52	3.75		V
V_{SYS_SHORT}	VSYS short voltage falling threshold to enter forced PFM			0.9		V
V_{SYS_SHORTZ}	VSYS short voltage rising threshold to exit forced PFM			1.1		V

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		3.50		4.80	V
V_{REG_STEP}	Typical charge voltage step			10		mV
V_{REG_ACC}	Charge voltage accuracy	T_J = 25°C, VREG = 4.2V	–0.3		0.3	%
		T_J = -10°C - 65°C, VREG = 4.2V	–0.5		0.5	%
I_{CHG_RANGE}	Typical charge current regulation range		0.08		5.04	A
I_{CHG_STEP}	Typical charge current regulation step			20		mA
I_{CHG_ACC}	Typical charge current accuracy	VBAT = 3.1V or 3.8V, ICHG = 1760mA, T_J = -10°C - 65°C	–5		5	%
		VBAT = 3.1V or 3.8V, ICHG = 1040mA, T_J = -10°C - 65°C	–6		6	%
		VBAT = 3.1V or 3.8V, ICHG = 480mA, T_J = -10°C - 65°C	–10		10	%
I_{PRECHG_RANGE}	Typical pre-charge current range		40		1000	mA
I_{PRECHG_STEP}	Typical pre-charge current step			20		mA
I_{PRECHG_ACC}	Pre-charge current accuracy when V_{BAT} below V_{SYSMIN} setting	VBAT = 2.5V, IPRECHG = 480mA, T_J = -10°C - 65°C	–10		10	%
		VBAT = 2.5V, IPRECHG = 200mA, T_J = -10°C - 65°C	–10		10	%
		VBAT = 2.5V, IPRECHG = 100mA, T_J = -10°C - 65°C	–30		30	%
		VBAT = 2.5V, IPRECHG = 40mA, T_J = -10°C - 65°C	–70		70	%
I_{TERM_RANGE}	Typical termination current range		30		1000	mA
I_{TERM_STEP}	Typical termination current step			10		mA
I_{TERM_ACC}	Termination current accuracy	ITERM = 30mA, T_J = -10°C - 65°C	–70		70	%
		ITERM = 100mA, T_J = -10°C - 65°C	–10		20	%
		ITERM = 200mA, T_J = -10°C - 65°C	–5		15	%
$I_{LIM\_API\_RANGE}$	Typical current limit range in Alternative Power from Input mode		10		100	mA
$I_{LIM\_API\_STEP}$	Typical current limit step in Alternative Power from Input mode			2.5		mA
$I_{LIM\_API\_ACC}$	Typical current limit accuracy in Alternative Power from Input mode	VBUS = 5V, API_ILIM = 100mA	-10		10	%
V_{BAT_SHORTZ}	Battery short voltage rising threshold to start pre-charge	VBAT rising		2.25		V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling, VBAT_UVLO=0		2.05		V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling, VBAT_UVLO=1		1.85		V
I_{BAT_SHORT}	Battery short trickle charging current	VBAT < V_{BAT_SHORTZ}, ITRICKLE = 0, T_J = -10°C - 65°C	6	20	34	mA
		VBAT < V_{BAT_SHORTZ}, ITRICKLE = 1, T_J = -10°C - 65°C	64	80	102	mA
V_{BAT_LOWV}	Battery LOW rising voltage threshold to start fast charge	BATLOWV = 00	2.9	3.0	3.1	V
	Battery LOW falling voltage threshold to start fast charge	BATLOWV = 00	2.7	2.8	2.9	V

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RECHG}	Battery recharge threshold below V_{REG}	VBAT falling, VRECHG = 0		100		mV
		VBAT falling, VRECHG = 1		200		mV
I_{PMID_LOAD}	PMID discharge load current		20			mA
I_{BAT_LOAD}	Battery discharge load current		20			mA
I_{SYS_LOAD}	System discharge load current		20			mA
BATFET						
V_{SUPPZ}	SYS < BAT threshold to exit supplement mode			5		mV
R_{BATFET}	MOSFET on resistance from SYS to BAT			7	12	mΩ
BATTERY PROTECTIONS						
V_{BAT_OVP}	Battery overvoltage rising threshold	As percentage of VREG	103	104	105	%
V_{BAT_OVPZ}	Battery overvoltage falling threshold	As percentage of VREG	101	102	103	%
I_{BATFET_OCP}	BATFET over-current rising threshold		7			A
I_{BAT_PK}	Battery discharging peak current rising threshold	IBAT_PK = 00	3			A
		IBAT_PK = 01	6			A
		IBAT_PK = 10	9			A
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Typical input voltage regulation range		3.8		16.8	V
V_{INDPM_STEP}	Typical input voltage regulation step			40		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM=4.6V	–3		3	%
		VINDPM=8V	–3		3	%
		VINDPM=16V	–2		2	%
$V_{INDPM\_BAT\_TRACK}$	Battery tracking VINDPM accuracy	VBAT = 3.9V, VINDPM_BAT_TRACK=1, VINDPM = 4V	3.95	4.1	4.2	V
I_{INDPM_RANGE}	Typical input current regulation range		0.1		3.2	A
I_{INDPM_STEP}	Typical input current regulation step			10		mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 500mA, VBUS=5V	415	475	500	mA
		IINDPM = 900mA, VBUS=5V	750	825	900	mA
		IINDPM = 1500mA, VBUS=5V	1350	1425	1500	mA
USB TYPE C						
V_{SAFE5V}	USB-C safe operating Voltage at 5V.		4.75		5.5	V
V_{SAFE0V}	USB-C safe operating Voltage at “zero volts.”		0		0.8	V
$V_{CC\_OVP\_TH}$	V_{CC_OVP} comparator threshold, CC_OVP = 0	Rising	3.53		3.63	V
		Falling	3.43		3.53	V
	V_{CC_OVP} comparator threshold, CC_OVP = 1	Rising	5.9		6.1	V
		Falling	5.7		5.9	V
R_D	Pull-down resistor when in SNK or DRP mode		4.6	5.1	5.6	kΩ
Type-C Sink (Rd pull-down)						

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SNK\_DISCONNECT}$	Valid range of thresholds for transition from Attached.SNK to Unattached.SNK when VBUS is 5 V.		0.8		3.67	V
V_{SNK_RDB}	Dead battery Rd clamp	VBAT < VBAT_UVLO, the connected SRC is presenting default (500mA/ 900mA) current capability	0.25		1.5	V
		VBAT < VBAT_UVLO, the connected SRC is presenting medium (1.5A) current capability	0.45		1.5	
		VBAT < VBAT_UVLO, the connected SRC is presenting high (3A) current capability	0.88		2.18	
$V_{SNK\_RD\_RA}$	Voltage across Rd when configured as a SNK to detect a cable presenting Ra	VBAT > VBAT_OTG, CC_MODE = 00b	-0.25		0.2	V
$V_{SNK\_RD\_DEF}$	Voltage across Rd when configured as a SNK to detect a SRC with default (500mA/900mA) current capacity	VBAT > VBAT_OTG, CC_MODE = 00b	0.25		0.61	V
$V_{SNK\_RD\_MED}$	Voltage across Rd when configured as a SNK to detect a SRC with medium (1.5A) current capacity	VBAT > VBAT_OTG, CC_MODE = 00b	0.7		1.16	V
$V_{SNK\_RD\_HI}$	Voltage across Rd when configured as a SNK to detect a SRC with high (3A) current capacity	VBAT > VBAT_OTG, CC_MODE = 00b	1.31		2.04	V
Type-C Source (Rp pull-up)						
$I_{SRC\_RP\_DEF}$	When presenting as a SRC, pull-up current source for default (500mA/900mA) current capacity	RP_VALUE = 00b, CC_MODE = 01b	64	80	96	µA
$I_{SRC\_RP\_MED}$	When presenting as a SRC, pull-up current source for medium (1.5A) current capacity	RP_VALUE = 01b, CC_MODE = 01b	166	180	194	µA
$I_{SRC\_RP\_HI}$	When presenting as a SRC, pull-up current source for high (3A) current capacity	RP_VALUE = 10b, CC_MODE = 01b	304	330	356	µA
LIQUID DETECTION						
V_{LQD}	Rising threshold to detect liquid	VLQD = 1100b		1.600		V
D+ / D- DETECTION						
$V_{D+D-\_0MV\_SRC}$	D+/D- voltage source (0 mV)	I_{D+} < 1mA; DP_DAC = 001 or DM_DAC = 001	-150	0	150	mV
$V_{D+D-\_600MV\_SRC}$	D+/D- voltage source (600 mV)	I_{D+} < 1mA; DP_DAC = 010 or I_{D-} < 1mA; DM_DAC = 010	400	600	800	mV
$V_{D+D-\_650MV\_SRC}$	D+/D- voltage source (650 mV)		638	650	700	mV
$V_{D+D-\_1p2V\_SRC}$	D+/D- voltage source (1.2 V)	I_{D+} < 1mA; DP_DAC = 011 or I_{D-} < 1mA; DM_DAC = 011	1.075	1.2	1.325	V
$V_{D+D-\_2p0V\_SRC}$	D+/D- voltage source (2.0 V)	I_{D+} < 1mA; DP_DAC = 100 or I_{D-} < 1mA; DM_DAC = 100	1.875	2.0	2.125	V
$V_{D+D-\_2p7V\_SRC}$	D+/D- voltage source (2.7 V)	I_{D+} < 1mA; DP_DAC = 101 or I_{D-} < 1mA; DM_DAC = 101	2.575	2.7	2.825	V
$V_{D+D-\_3p3V\_SRC}$	D+/D- voltage source (3.3 V)	I_{D+} < 1mA; DP_DAC = 110 or I_{D-} < 1mA; DM_DAC = 110	3.1	3.3	3.5	V
$I_{D+\_10UA\_SRC}$	D+ current source (10 µA)		7	10	13	µA

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{D+D-\_100UA\_SNK}$	D+/D- current sink (100 µA)		50	90	150	µA
V_{D+D-_0P325}	D+/D- comparator threshold for Secondary Detection		250		400	mV
V_{D+_0P8}	D+ comparator threshold for Data Contact Detection		775	850	925	mV
R_{D-_19K}	D- resistor to ground (19 kΩ)	V_{D-} = 500mV	14.25		24.8	kΩ
I_{D+D-_LKG}	Leakage current into D+/D-	HiZ mode	–1		1	µA
V_{D+D-_2p8}	D+/D- comparator threshold for non-standard adapter		2.55		2.85	V
V_{D+D-_2p0}	D+/D- comparator threshold for non-standard adapter		1.85		2.15	V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 1		120		°C
		TREG = 0		60		°C
T_{SHUT}	Thermal Shutdown Rising Threshold	Temperature Increasing		150		°C
T_{SHUT_HYS}	Thermal Shutdown Falling Hysteresis	Temperature Decreasing by T_{SHUT_HYS}		30		°C
THERMISTOR COMPARATORS (CHARGE MODE)						
V_{TS_COLD}	TS pin rising voltage threshold for TH1 comparator to transition from TS_COOL to TS_COLD.	As Percentage to TS pin bias reference (–5°C with 103AT), TS_TH1 = 0	74.75	75.25	75.75	%
		As Percentage to TS pin bias reference (0°C with 103AT), TS_TH1 = 1	72.75	73.25	73.75	%
V_{TS_COLDZ}	TS pin falling voltage threshold for TH1 comparator to transition from TS_COLD to TS_COOL.	As Percentage to TS pin bias reference (–2.5°C with 103AT), TS_TH1 = 0	73.75	74.25	74.75	%
		As Percentage to TS pin bias reference (2.5°C with 103AT), TS_TH1 = 1	71.75	72.25	72.75	%
V_{TS_COOL}	TS pin rising voltage threshold for TH2 comparator to transition from TS_PRECOOL to TS_COOL.	As Percentage to TS pin bias reference (5°C with 103AT), TS_TH2 = 0	70.25	70.75	71.25	%
		As Percentage to TS pin bias reference (7.5°C with 103AT), TS_TH2 = 1	69.25	69.75	70.25	%
		As Percentage to TS pin bias reference (10°C with 103AT), TS_TH2 = 2	67.75	68.25	68.75	%
		As Percentage to TS pin bias reference (12.5°C with 103AT), TS_TH2 = 3	66.25	66.75	67.25	%
V_{TS_COOLZ}	TS pin falling voltage threshold for TH2 comparator to transition from TS_COOL to TS_PRECOOL.	As Percentage to TS pin bias reference (7.5°C with 103AT), TS_TH2 = 0	69.25	69.75	70.25	%
		As Percentage to TS pin bias reference (10°C with 103AT), TS_TH2 = 1	67.75	68.25	68.75	%
		As Percentage to TS pin bias reference (12.5°C with 103AT), TS_TH2 = 2	66.25	66.75	67.25	%
		As Percentage to TS pin bias reference (15°C with 103AT), TS_TH2 = 3	64.75	65.25	65.75	%
$V_{TS\_PRECOOL}$	TS pin rising voltage threshold for TH3 comparator to transition from TS_NORMAL to TS_PRECOOL.	As Percentage to TS pin bias reference (15°C with 103AT), TS_TH3 = 0	64.75	65.25	65.75	%
		As Percentage to TS pin bias reference (17.5°C with 103AT), TS_TH3 = 1	63.25	63.75	64.25	%
		As Percentage to TS pin bias reference (20°C with 103AT), TS_TH3 = 2	61.75	62.25	62.75	%
		As Percentage to TS pin bias reference (22.5°C with 103AT), TS_TH3 = 3	60.25	60.75	61.25	%

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TS\_PRECOOLZ}$	TS pin falling voltage threshold for TH3 comparator to transition from TS_PRECOOL to TS_NORMAL.	As Percentage to TS pin bias reference (17.5°C with 103AT), TS_TH3 =0	63.25	63.75	64.25	%
		As Percentage to TS pin bias reference (20°C with 103AT), TS_TH3 = 1	61.75	62.25	62.75	%
		As Percentage to TS pin bias reference (22.5°C with 103AT), TS_TH3 = 2	60.25	60.75	61.25	%
		As Percentage to TS pin bias reference (25°C with 103AT), TS_TH3 = 3	58.5	59.00	59.5	%
$V_{TS\_PREWARM}$	TS pin falling voltage threshold for TH4 comparator to transition from TS_NORMAL to TS_PREWARM.	As Percentage to TS pin bias reference (32.5°C with 103AT), TS_TH4 = 0	53.25	53.75	54.25	%
		As Percentage to TS pin bias reference (35°C with 103AT), TS_TH4 = 1	51.50	52.00	52.50	%
		As Percentage to TS pin bias reference (37.5°C with 103AT), TS_TH4 = 2	49.5	50	50.5	%
		As Percentage to TS pin bias reference (40°C with 103AT), TS_TH4 = 3	47.75	48.25	48.75	%
$V_{TS\_PREWARMZ}$	TS pin rising voltage threshold for TH4 comparator to transition from TS_PREWARM to TS_NORMAL.	As Percentage to TS pin bias reference (30°C with 103AT), TS_TH4 = 0	55.00	55.50	56.00	%
		As Percentage to TS pin bias reference (32.5°C with 103AT), TS_TH4 = 1	53.25	53.75	54.25	%
		As Percentage to TS pin bias reference (35°C with 103AT), TS_TH4 = 2	51.50	52.00	52.50	%
		As Percentage to TS pin bias reference (37.5°C with 103AT), TS_TH4 = 3	49.50	50.00	50.50	%
V_{TS_WARM}	TS pin falling voltage threshold for TH5 comparator to transition from TS_PREWARM to TS_WARM.	As Percentage to TS pin bias reference (42.5°C with 103AT), TS_TH5 = 0	46.00	46.50	47.00	%
		As Percentage to TS pin bias reference (45°C with 103AT), TS_TH5 = 1	44.25	44.75	45.25	%
		As Percentage to TS pin bias reference (47.5°C with 103AT), TS_TH5 = 2	42.50	43.00	43.50	%
		As Percentage to TS pin bias reference (50°C with 103AT), TS_TH5 = 3	40.75	41.25	41.75	%
V_{TS_WARMZ}	TS pin rising voltage threshold for TH5 comparator to transition from TS_WARM to TS_PREWARM.	As Percentage to TS pin bias reference (40°C with 103AT), TS_TH5 = 0	47.75	48.25	48.75	%
		As Percentage to TS pin bias reference (42.5°C with 103AT), TS_TH5 = 1	46.00	46.50	47.00	%
		As Percentage to TS pin bias reference (45°C with 103AT), TS_TH5 = 2	44.25	44.75	45.25	%
		As Percentage to TS pin bias reference (47.5°C with 103AT), TS_TH5 = 3	42.50	43.00	43.50	%
V_{TS_HOT}	TS pin falling voltage threshold for TH6 comparator to transition from TS_WARM to TS_HOT.	As Percentage to TS pin bias reference (55°C with 103AT), TS_TH6 = 0	37.25	37.75	38.25	%
		As Percentage to TS pin bias reference (60°C with 103AT), TS_TH6 = 1	34.00	34.50	35.00	%
V_{TS_HOTZ}	TS pin rising voltage threshold for TH6 comparator to transition from TS_HOT to TS_WARM.	As Percentage to TS pin bias reference (52.5°C with 103AT), TS_TH6 = 0	39.00	39.50	40.00	%
		As Percentage to TS pin bias reference (57.5°C with 103AT), TS_TH6 = 1	35.75	36.25	36.75	%
THERMISTOR COMPARATORS (OTG MODE)						

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TS\_OTG\_COLD}$	TS pin rising voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_COLD.	As Percentage to TS pin bias reference (–20°C with 103AT), TS_TH_OTG_COLD = 0	79.50	80.00	80.50	%
		As Percentage to TS pin bias reference (–10°C with 103AT), TS_TH_OTG_COLD = 1	76.50	77.00	77.50	%
$V_{TS\_OTG\_COLDZ}$	TS pin falling voltage threshold to transition from TS_OTG_COLD to TS_OTG_NORMAL.	As Percentage to TS pin bias reference (–15°C with 103AT), TS_TH_OTG_COLD = 0	78.00	78.50	79.00	%
		As Percentage to TS pin bias reference (–5°C with 103AT), TS_TH_OTG_COLD = 1	74.75	75.25	75.75	%
$V_{TS\_OTG\_HOT}$	TS pin falling voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_HOT.	As Percentage to TS pin bias reference (55°C with 103AT), TS_OTG_HOT = 00	37.25	37.75	38.25	%
		As Percentage to TS pin bias reference (60°C with 103AT), TS_OTG_HOT = 01	34.00	34.50	35.00	%
		As Percentage to TS pin bias reference (65°C with 103AT), TS_OTG_HOT = 10	30.75	31.25	31.75	%
$V_{TS\_OTG\_HOTZ}$	TS pin rising voltage threshold to transition from TS_OTG_HOT to TS_OTG_NORMAL.	As Percentage to TS pin bias reference (52.5°C with 103AT), TS_OTG_HOT = 00	39.00	39.50	40.00	%
		As Percentage to TS pin bias reference (57.5°C with 103AT), TS_OTG_HOT = 01	35.75	36.25	36.75	%
		As Percentage to TS pin bias reference (62.5°C with 103AT), TS_OTG_HOT = 10	32.50	33.00	33.50	%
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency	1.35	1.5	1.65	MHz
MOSFET TURN-ON RESISTANCE						
R_{Q1_ON}	VBUS to PMID on resistance	T_j = –40°C-85°C (typical value is under 25°C)		15	20	mΩ
R_{Q2_ON}	Buck high-side switching MOSFET turn on resistance between PMID and SW	T_j = –40°C-85°C (typical value is under 25°C)		20	27	mΩ
R_{Q3_ON}	Buck low-side switching MOSFET turn on resistance between SW and PGND	T_j = –40°C-85°C (typical value is under 25°C)		14	18	mΩ
OTG MODE CONVERTER						
V_{OTG_RANGE}	Typical OTG mode voltage regulation range		3.84		9.6	V
V_{OTG_STEP}	Typical OTG mode voltage regulation step			20		mV
V_{OTG_ACC}	OTG mode voltage regulation accuracy	IVBUS = 0A, VOTG = 9V, T_J = -20°C - 65°C	–2		2	%
V_{OTG_ACC}	OTG mode voltage regulation accuracy	IVBUS = 0A, VOTG = 5V, T_J = -20°C - 65°C	–3		3	%
I_{OTG_RANGE}	Typical OTG mode current regulation range		0.1		3.2	A
I_{OTG_STEP}	Typical OTG mode current regulation step			10		mA
I_{OTG_ACC}	OTG mode current regulation accuracy	IOTG = 1.8A, T_J = -20℃ - 65℃	–3.5		3.5	%
		IOTG = 1.5A, T_J = -20℃ - 65℃	–5		5	%
		IOTG = 1.0A, T_J = -20℃ - 65℃	–10		10	%

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OTG_UVP}	OTG mode undervoltage falling threshold at PMID			3.4		V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 20mA	4.4	4.6		V
		V_{VBUS} = 9V, I_{REGN} = 20mA	4.8	5.0	5.2	V
V_{REGNZ_OK}	REGN not good falling threshold	Converter switching		3.2		V
		Converter not switching		2.3		V
I_{REGN_LIM}	REGN LDO current limit	V_{VBUS} = 5V, VREGN = 4.3V	20			mA
PG THRESHOLD						
PG_TH	VBUS voltage falling threshold to release $\overline{PG}$ pin pulldown	PG_TH = 000b		3.7		V
		PG_TH = 001b		7.4		V
		PG_TH = 010b		8.0		V
		PG_TH = 011b		10.4		V
		PG_TH = 100b		11.0		V
		PG_TH = 101b		13.4		V
		PG_TH = 110b		14.0		V
PG_THz	VBUS voltage rising threshold to enable $\overline{PG}$ pin pulldown	PG_TH = 000b		3.9		V
		PG_TH = 001b		7.9		V
		PG_TH = 010b		8.5		V
		PG_TH = 011b		10.9		V
		PG_TH = 100b		11.5		V
		PG_TH = 101b		13.9		V
		PG_TH = 110b		14.5		V
ADC MEASUREMENT ACCURACY AND PERFORMANCE						
t_{ADC_CONV}	Conversion-time, Each Measurement	ADC_SAMPLE = 00		24		ms
		ADC_SAMPLE = 01		12		ms
		ADC_SAMPLE = 10		6		ms
		ADC_SAMPLE = 11		3		ms
ADC_RES	Effective Resolution	ADC_SAMPLE = 00	11	12		bits
		ADC_SAMPLE = 01	10	11		bits
		ADC_SAMPLE = 10	9	10		bits
		ADC_SAMPLE = 11	8	9		bits
$V_{BAT\_LOWV\_ADC}$	Minimum battery voltage to operate ADC with no adapter present, rising threshold			2.7		V
$V_{BAT\_LOWV\_ADCZ}$	Minimum battery voltage to operate ADC with no adapter present, falling threshold			2.5		V
ADC MEASUREMENT RANGE AND LSB						
IBUS_ADC	ADC Bus Current Reading (both forward and OTG)	Range	–5		5	A
		LSB		2.5		mA
VBUS_ADC	ADC VBUS Voltage Reading	Range	0		20	V
		LSB		5		mV
VPMID_ADC	ADC PMID Voltage Reading	Range	0		20	V
		LSB		5		mV
VBAT_ADC	ADC BAT Voltage Reading	Range	0		5	V
		LSB		1.25		mV

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBAT_ADC	ADC BAT Voltage Reading Accuracy	Accuracy at 4V, ADC_SAMPLE = 00	–0.5		0.5	%
CC1_ADC	CC1 Voltage Reading	Range	0		5	V
		LSB		1.25		mV
CC2_ADC	CC2 Voltage Reading	Range	0		5	V
		LSB		1.25		mV
VSYS_ADC	ADC SYS Voltage Reading	Range	0		5	V
		LSB		1.25		mV
IBAT_ADC	ADC BAT Current Reading	Range	–10		5	A
		LSB		5		mA
TS_ADC	ADC TS Voltage Reading	Range as a percent of REGN	0		99.9	%
	ADC TS Voltage Reading	LSB		0.098		%
TDIE_ADC	ADC Die Temperature Reading	Range	–40		150	°C
		LSB		0.5		°C
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SDA and SCL		0.78			V
V_{IL}	Input low threshold level, SDA and SCL				0.42	V
V_{OL_SDA}	Output low threshold level	Sink current = 5mA, 1.2V VDD			0.3	V
I_{BIAS}	High-level leakage current	Pull up rail 1.8V			1	µA
LOGIC OUTPUT PIN ($\overline{INT}$, $\overline{PG}$)						
V_{OL}	Output low threshold level	Sink current = 5mA			0.3	V
I_{OUT_BIAS}	High-level leakage current	Pull up rail 1.8V			1	µA
LOGIC INPUT PIN ($\overline{CE}$, OTG, $\overline{QON}$)						
V_{IH_CE}	Input high threshold level, /CE		0.78			V
V_{IL_CE}	Input low threshold level, /CE				0.4	V
$I_{IN\_BIAS\_CE}$	High-level leakage current, /CE	Pull up rail 1.8V			1	µA
V_{IH_QON}	Input high threshold level, /QON		1.3			V
V_{IL_QON}	Input low threshold level, /QON				0.4	V
V_{QON}	Internal /QON pull up	/QON is pulled up to VAA internally		5		V
R_{QON}	Internal /QON pull up resistance			250		kΩ

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VBUS / VBAT POWER UP						
t_{VBUS_OVP}	VBUS OVP deglitch time to set VBUS_OVP_STAT and VBUS_OVP_FLAG			200		µs
BATTERY CHARGER						
t_{TOP_OFF}	Typical top-off timer accuracy		12	15	18	min
			24	30	36	min
			36	45	54	min
t_{SAFETY_TRKCHG}	Charge safety timer accuracy in trickle charge		0.9	1	1.1	hr
t_{SAFETY_PRECHG}	Charge safety timer accuracy in pre-charge	PRECHG_TMR = 0	1.8	2	2.2	hr
		PRECHG_TMR = 1	0.45	0.5	0.55	hr

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{SAFETY}	Charge safety timer accuracy in fast charge	CHG_TMR = 0	10.8	12	13.2	hr
		CHG_TMR = 1	21.6	24	26.4	hr
BATFET CONTROL						
t_{BATFET_DLY}	Time after writing to BATFET_CTRL before BATFET turned off for ship, standby, or shutdown mode	BATFET_DLY = 1		10		s
		BATFET_DLY = 0		20		ms
t_{SM_EXIT}	Deglitch time for $\overline{QON}$ to be pulled low to exit from ship mode		480	580	680	ms
$t_{STANDBY\_EXIT}$	Deglitch time for $\overline{QON}$ to be pulled low to exit from standby mode	TSTANDBY_EXIT = 0	480	580	680	ms
		TSTANDBY_EXIT = 1	7.5	9	10.5	ms
t_{QON_RST}	Time $\overline{QON}$ is held low to initiate system power reset	TQON_RST = 0	8	9.5	11	s
		TQON_RST = 1	15	18	21	s
t_{BATFET_RST}	Duration that BATFET is disabled during system power reset			350		ms
USB Type C						
CC Timing Parameters						
$t_{CC\_ERROR\_RECOVER}$	Time a port shall remain in the ErrorRecovery state		25			ms
I2C INTERFACE						
f_{SCL}	SCL clock frequency				1.0	MHz
C_b	Capacitive load for each bus line				550	pF
DIGITAL CLOCK AND WATCHDOG						
t_{LP_WDT}	Watchdog Reset time (EN_HIZ = 1, WATCHDOG = 160s)		100	160		s
t_{WDT}	Watchdog Reset time (EN_HIZ = 0, WATCHDOG = 160s)		136	160		s

7.7 Typical Characteristics

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS} = 20µF, L = 1µH (Murata DFE322520F-1R0M=P2) (unless otherwise specified)

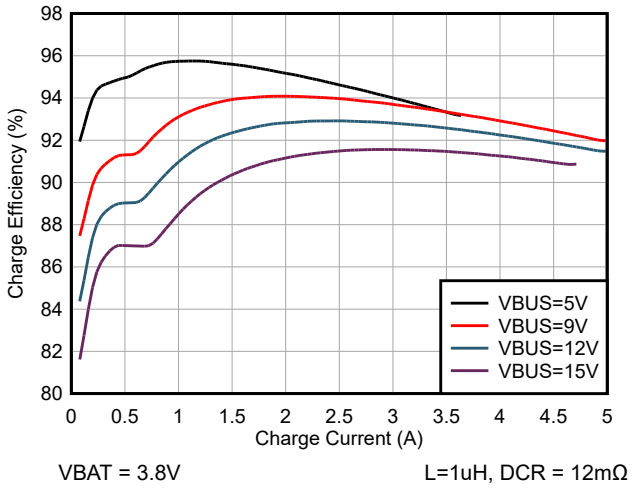


Figure 7-1. Charge Efficiency vs Charge Current

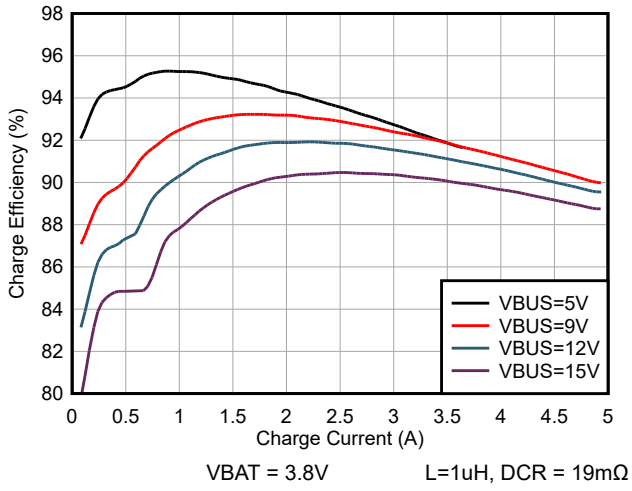


Figure 7-2. Charge Efficiency vs Charge Current

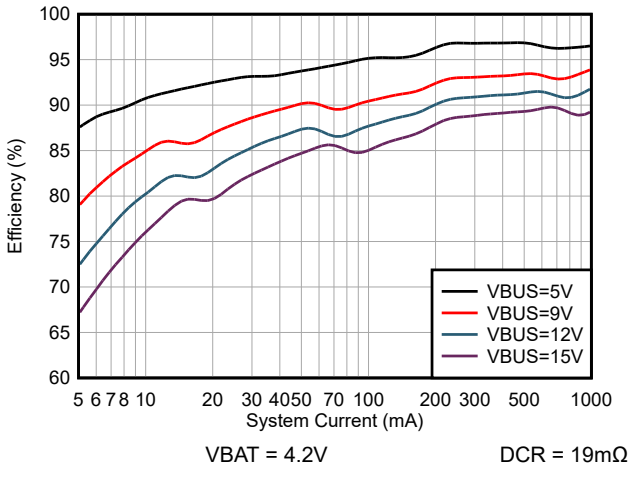


Figure 7-3. System Efficiency vs System Current

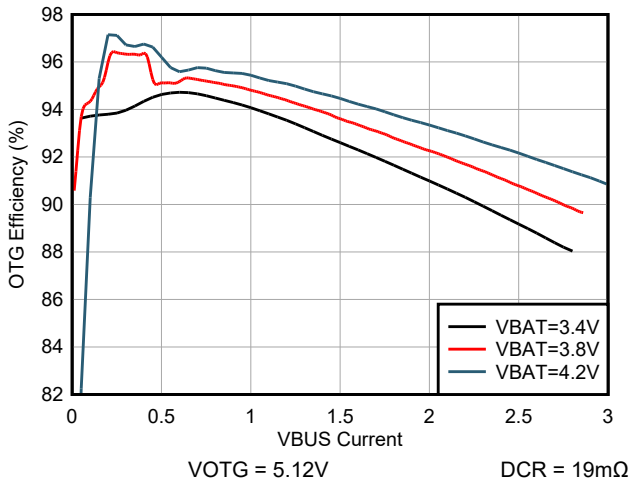


Figure 7-4. Boost Mode Efficiency vs VBUS Load Current

7.7 Typical Characteristics (continued)

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS} = 20µF, L = 1µH (Murata DFE322520F-1R0M=P2) (unless otherwise specified)

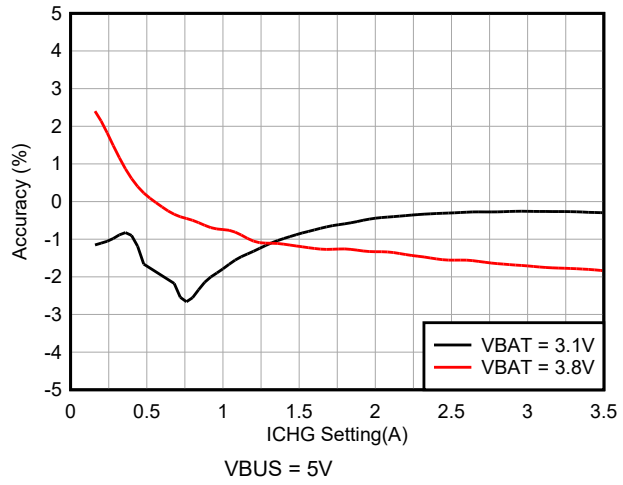


Figure 7-5. Charge Current Accuracy vs Charge Current I²C Setting

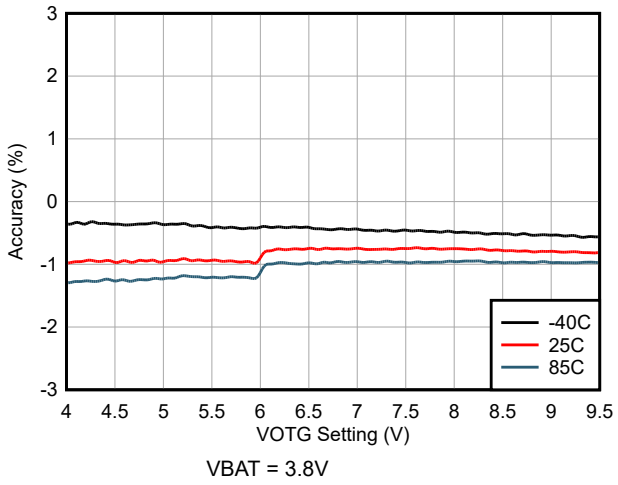


Figure 7-6. Boost Mode Voltage Accuracy vs VOTG I²C Setting

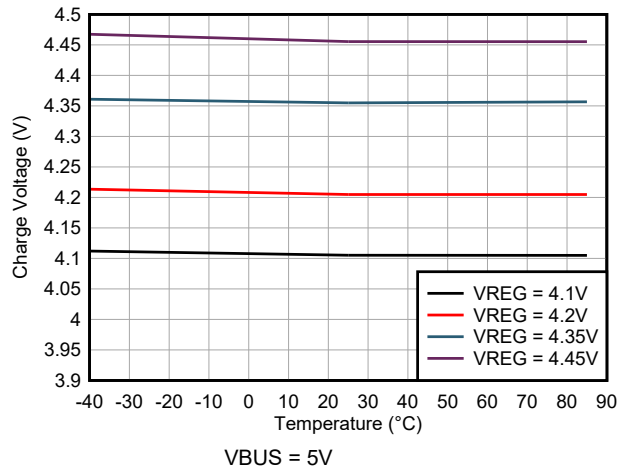


Figure 7-7. BAT Regulation Voltage vs Temperature

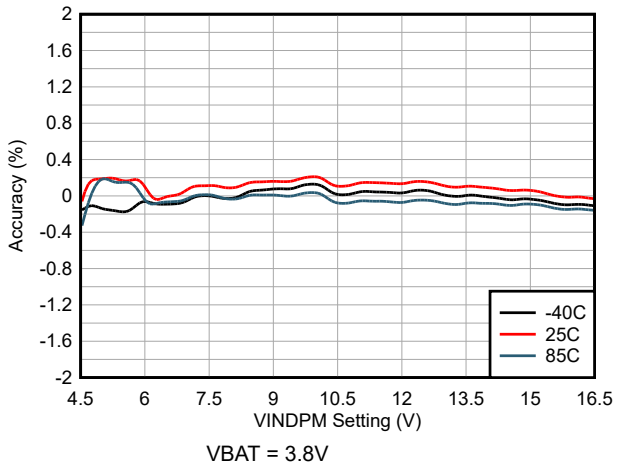


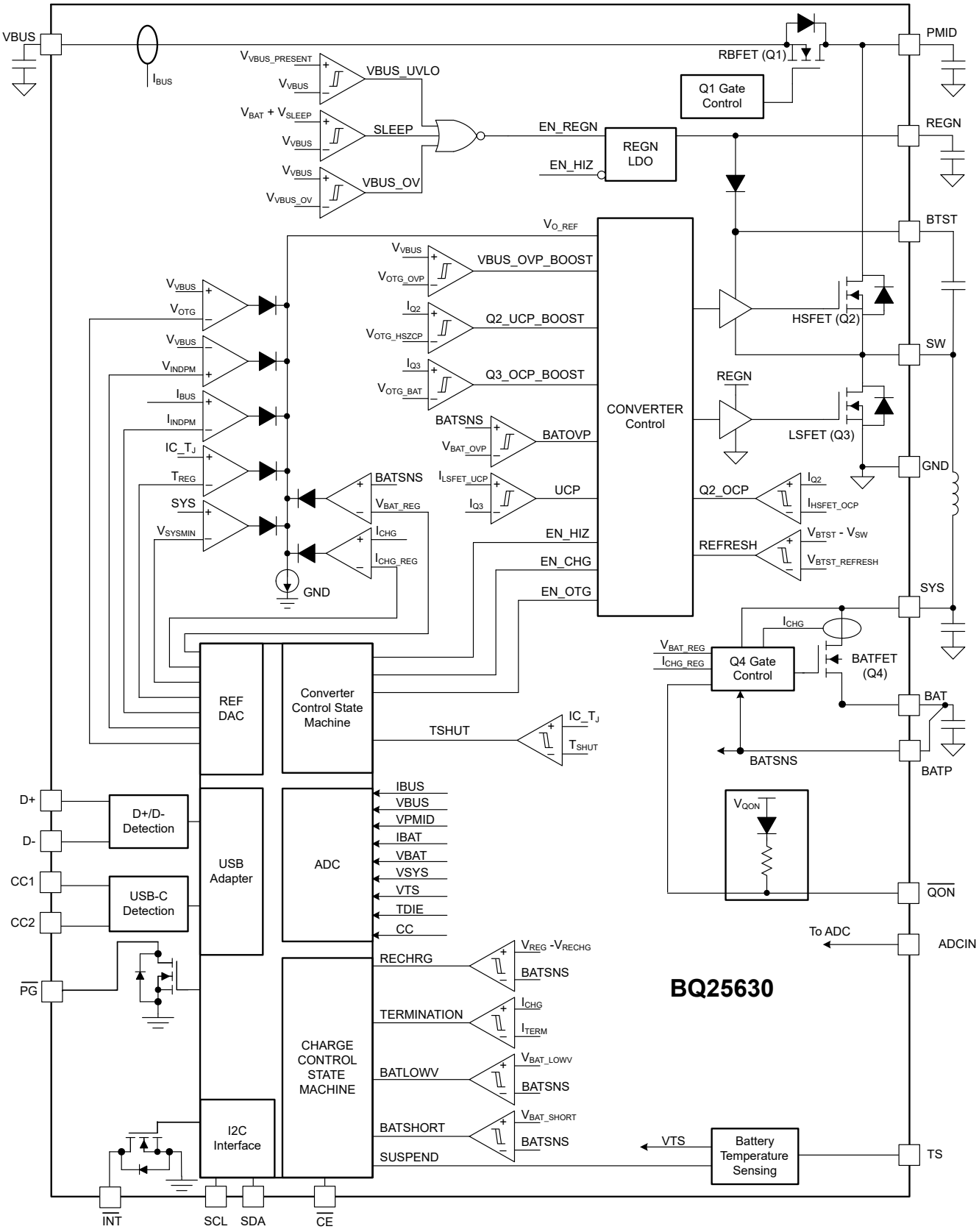
Figure 7-8. Input Voltage Limit vs VINDPM I²C Setting

8 Detailed Description

8.1 Overview

BQ25630 is a highly-integrated 5A switch mode battery charger with NVDC power path management for single cell Li-Ion and Li-polymer batteries. The device features fast charging with high input voltage supporting a wide range of portable devices. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery running time during discharging phase. The BQ25630 input voltage and input current regulation deliver maximum charging power to the battery without overloading the input source.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-On-Reset (POR)

BQ25630 powers internal bias circuits from the higher voltage of VBUS and BAT. When either voltage rises above the undervoltage lockout (UVLO) threshold, all registers are reset to the POR values and the I^2C interface is enabled for communication. A non-maskable $\overline{INT}$ pulse is generated, after which the host can access all of the registers.

8.3.2 Device Power Up from Battery

If only battery is present and the voltage is above depletion threshold (V_{BAT_UVLOZ}), BQ25630 performs a power-on reset then turns on BATFET to connect the battery to the system. The REGN stays off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

8.3.3 USB-C Detection

Type-C Specification 2.3 defines several cables, plugs, and receptacles to be used to attach ports. All cables, receptacles, and plugs that do not require VCONN power are supported. The device does not support any USB feature which requires USB Power Delivery communications over CC lines, such as e-marking or alternate mode.

USB-C added the ability to advertise as a port that sinks power (SNK), a port that sources power (SRC), or a dual role port (DRP) that can advertise both functions. The CC_MODE register selects if the device is advertising as SNK-only, SRC-only, or DRP capable.

USB-C detection is run through the CC1/CC2 lines to detect USB-C sources (Default / Medium / High), USB sinks, and legacy adapters. When DIS_CC = 0b (POR default), the detection algorithm automatically runs at all times. The orientation of the connected cable can be determined by reading the CC1_STAT and CC2_STAT registers when CC_ORIENT = 1.

After a connection is made, the USB-C detection routine can be forced to disconnect and restart by setting FORCE_CC_DET = 1b.

8.3.3.1 Legacy Adapter Detection

Legacy adapters (USB-A to USB-C) and non-USB inputs both power VBUS before presenting Rp on the CC pins. If VBUS is detected without activity on the CC pins, SNK and DRP devices detects these as “Unknown Adapters.”

To support legacy BC 1.2 adapters, IINDPM will be set based on Section 8.3.4.2.

When D+/D- detection is disabled, IINDPM will be set based on Section 8.3.4.5 if EN_ICO = 1b. If EN_ICO = 0b, IINDPM will default to 3.2A and can be overwritten by the host for situations where the host knows what input source has been connected.

8.3.3.2 USB-C Dead Battery Mode

In USB-C Dead Battery Mode (VBAT < VBAT_UVLO), the device defaults to SNK-only mode and the CC pins always present Rd regardless of the value of CC_MODE. USB-C Dead Battery Mode is enabled if the device is in shutdown or ship mode.

8.3.3.3 SNK Mode

The device defaults to SNK-only mode. The device can be reconfigured to SNK-only mode through setting CC_MODE=00b.

In SNK mode, the device constantly presents pulldown resistors (Rd) on both CC pins to detect a 5V USB-C SRC device. The device continuously monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected SRC. As a SNK, the device detects and communicates the advertised current level of the connected SRC to the system through the VBUS_STAT register. The connected

SRC can dynamically change the advertised current level after initial plug-in. When this occurs, IINDPM and VBUS_STAT is automatically updated accordingly.

If a SRC advertising default current is detected, it can be a USB-C to USB-C cable or a legacy USB-A to USB-C cable. BC 1.2 detection will be run automatically if EN_DPDM_DET = 1b in this case. If a legacy adapter is detected, IINDPM and VBUS_STAT will be set based on Section 8.3.4.2.

8.3.3.4 SRC Mode

The device can be configured to SRC-only mode through setting CC_MODE=01b. After a connection is detected, if CC_AUTO_OTG = 1b the device is automatically set to begin boosting to VBUS at 5V. EN_OTG is automatically set to 1b and VOTG Is automatically set to 5V.

In SRC mode, the device constantly presents Rp on both CC pins while looking for a connection. The RP_VALUE register can be used to specify the current advertised. The device supports advertising all three possible Type-C current options: Default (500mA / 900mA), Medium (1.5A), and High (3A). IOTG is set according to RP_VALUE and VOTG is set to 5V when a USB-C connection is made automatically.

When a connection is detected, the device supports Reverse Mode through boost converter operation to deliver power from the battery to VBUS. VBUS_STAT is set to 111b upon a successful connection.

8.3.3.5 DRP Mode - Dual Role Port

During dual role port (DRP) mode, the device advertises as both a SRC and a SNK by automatically toggling the CC lines between Rp and Rd. The device can be configured to DRP mode through setting CC_MODE=10b. EN_OTG is automatically set to 0b (Attached.SNK) or 1b (Attached.SRC) after a connection is detected. The connection result is shown in the VBUS_STAT register.

The device supports Try.SRC and Try.SNK. When two DRPs are connected together, the device can be programmed to prefer connecting as a SRC (Try.SRC), connecting as a SNK (Try.SNK), or having no preference as part of the initial handshaking through the DRP_PREF register.

To configure DRP mode:

1. Set RP_VALUE to the desired advertised current if connected as a SRC.
2. Set DRP_PREF to the desired Try behavior (defaults to no Try routine).
3. Set CC_MODE = 10b.

8.3.3.6 USB-C Debug Accessory Detection

Debug is an additional state supported by USB Type-C intended for use with Debug Accessory devices and cables. Autonomous detection of Debug Accessories is enabled when EN_DEBUG_ACC_DET = 1b.

8.3.4 Device Power Up from Input Source

When an input source is plugged in with VBAT < V_{BAT_UVLOZ}, BQ25630 performs a power-on reset then checks the input source voltage to turn on REGN LDO and all the bias circuits. The device detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. USB-C SNK and Legacy Adapter Handshake to set input current limit (IINDPM)
2. REGN LDO power up (Section 8.3.4.1)
3. Input voltage limit threshold setting (Section 8.3.4.3)
4. Converter power-up (Section 8.3.4.4)

8.3.4.1 REGN LDO Power Up

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The REGN is enabled when all the below conditions are valid:

- VBUS above V_{VBUS_UVLOZ}
- VBUS above V_{BAT} + V_{SLEEPZ}
- EN_HIZ = 0
- After 220-ms delay is completed

If any one of the above conditions is not valid, the REGN LDO and the converter power stage remain off with the converter disabled. In this state, the battery supplies power to the system.

8.3.4.2 D+/D– Detection Sets Input Current Limit

The device contains a D+/D– based input source detection to set the input current limit automatically. The D+/D- detection includes standard USB BC1.2, non-standard adapter, and adjustable high voltage adapter detections. When an input source is plugged-in and USB-C Default or no USB-C connection is detected, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable of identifying Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer of 500ms is expired, the non-standard adapter detection is applied to set the input current limit.

When DCP is detected, the device initiates adjustable high voltage adapter handshake. The handshake connects combinations of voltage sources and current sinks on D+/D- to signal input source to raise output voltage from 5V to 9V or 12V if either EN_9V or EN_12V register bits are set to 1. The adjustable high voltage adapter handshake can be disabled by clearing both EN_9V and EN_12V register bits.

Upon the completion of input source type detection, an $\overline{INT}$ pulse is asserted to the host and the following registers are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. VBUS_STAT bits are updated to indicate the detected input source type

After detection completes, the host can over-write the IINDPM register to change the input current limit if needed.

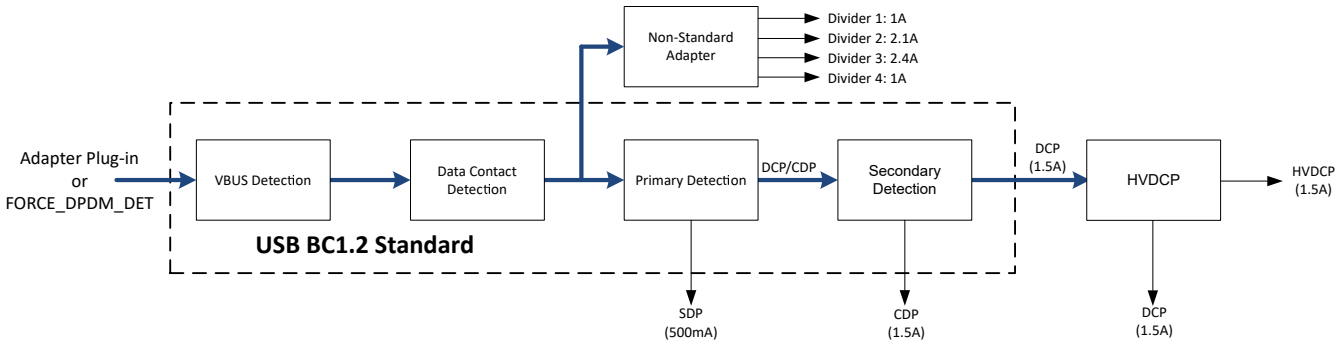


Figure 8-1. D+/D– Detection Flow

If DCP is detected (VBUS_STAT = 011), the device turns on VDP_SRC on D+ if EN_DCP_BIAS is set to 1. Setting EN_DCP_BIAS to 0 while VBUS_STAT = 011 disables the VDP_SRC, and setting EN_DCP_BIAS to 1 while VBUS_STAT = 011 enables the VDP_SRC. The EN_HIZ bit has priority over EN_DCP_BIAS.

The non-standard detection is used to distinguish vendor specific adapters based on unique dividers on the D+/D- pins. During the non-standard detection, no source or sink is applied to either D+ or D- pin. Comparators detect the voltage applied on each pin and determine the input current limit according to Table 8-1.

Table 8-1. Non-Standard Adapter Detection

Non-Standard Adapter	D+ Threshold	D– Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V_{D+D-_2p0}	V_{D-} within V_{D+D-_2p8}	1

Table 8-1. Non-Standard Adapter Detection (continued)

Non-Standard Adapter	D+ Threshold	D– Threshold	Input Current Limit (A)
Divider 2	V_{D+} within V_{D+D-_2p8}	V_{D-} within V_{D+D-_2p0}	2.1
Divider 3	V_{D+} within V_{D+D-_2p8}	V_{D-} within V_{D+D-_2p8}	2.4

Table 8-2. Input Current Limit Setting from D+/D– Detection

D+/D– Detection	Input Current Limit (IINDPM)	VBUS_STAT
USB SDP (USB500)	500mA	1h
USB CDP	1.5A	2h
USB DCP	3.2A	3h
Divider 1	1A	5h
Divider 2	2.1A	5h
Divider 3	2.4A	5h
HVDCP	1.5A	6h
Unknown 5V Adapter	3.2A	4h

8.3.4.3 Input Voltage Limit Threshold Setting (VINDPM Threshold)

BQ25630 supports a wide range of input voltage limit (3.8V – 16.8V). The POR default VINDPM is set at 4.4V. The charger also supports dynamic VINDPM tracking, which tracks the battery voltage to provide a sufficient margin between input and battery voltages for proper operation of the buck converter. This function is enabled by default, and can be disabled by clearing the VINDPM_BAT_TRACK register bit to 0b. When enabled, the actual input voltage limit is the higher of the VINDPM register and $V_{INDPM\_BAT\_TRACK}$ (VBAT + 200mV offset).

8.3.4.4 Converter Power-Up

After the input current and voltage limits are set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery. Converter startup requires the following conditions:

- VBUS > V_{BAT} + V_{SLEEPZ}
- V_{VBUS} < V_{VBUS_OVP}
- EN_HIZ = 0
- V_{SYS} < V_{SYS_OVP}
- T_J < T_{SHUT}

BQ25630 provides soft start when system rail is ramped up. Concurrently, the system short protection limits the output current to approximately 0.5A when the system rail is below V_{SYS_SHORT}.

This device uses a highly efficient 1.5MHz, fixed frequency pulse width modulated (PWM) step-down switching regulator. The internally compensated feedback loop keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

To improve light-load efficiency, the device switches to PFM control at light load condition. The effective switching frequency decreases accordingly when system load decreases. The minimum frequency can be limited to 25kHz when the Out of Audio (OOA) feature is enabled (EN_OOA=1b). The PFM_FWD_DIS and PFM_OTG_DIS bits can be used to disable the PFM operation in buck and boost respectively.

8.3.4.5 Input Current Optimizer (ICO)

The device provides innovative Input Current Optimizer (ICO) to identify maximum power point without overloading the input source. The algorithm automatically identifies maximum input current limit of power source without entering VINDPM to avoid input source overload.

This feature is enabled by default (EN_ICO=1b) and can be disabled by setting EN_ICO bit to 0b. The algorithm runs automatically when EN_ICO bit is set, and the conditions below are met. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type detected (EN_ICO = 1b is required for FORCE_ICO to work). Setting FORCE_ICO=1b or FORCE_DPDM_DET=1b or FORCE_CC_DET=1b re-runs

the algorithm and override the previous detection. To be compliant with the USB-C specification, ICO does not run automatically when a known USB-C adapter is detected.

The actual input current limit used by the Dynamic Power Management is reported in ICO_IINDPM register while Input Current Optimizer is enabled (EN_ICO = 1) or set by IINDPM register when the algorithm is disabled (EN_ICO = 0). .

8.3.4.6 Switching Frequency and Dithering Feature

Under normal operation the device switches with a fixed frequency. The charger also supports a frequency dithering function to improve EMI performance and help pass IEC-CISPR 22 specification. This function is disabled by default (EN_DITHER=00b) and can be enabled by setting EN_DITHER=01/10/11b. When dithering is enabled, the switching frequency is not fixed and varies within a range determined by the EN_DITHER setting with 01/10/11b corresponding to ±2%/4%/6% switching frequency. A larger dithering range produces a smaller EMI noise peak, but can also result in a slightly larger VBUS/VSYS capacitor voltage ripple. Select the lowest dithering range which can pass IEC-CISPR 22 specification due to this trade-off. The patented dithering pattern can improve EMI performance from switching frequency and up to 30MHz high frequency range which covers the entire conductive EMI noise range.

8.3.5 Power Path Management

BQ25630 accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

8.3.5.1 Narrow VDC Architecture

BQ25630 uses the Narrow VDC architecture (NVDC) with BATFET separating the system from the battery. The minimum system voltage is set by the VSYSMIN register setting. Even with a fully depleted battery, the system is regulated to the minimum system voltage. If charging is enabled, the BATFET operates in linear mode (LDO mode). The default minimum system voltage at POR is 3.52V.

As the battery voltage rises above the minimum system voltage, the BATFET is turned fully on and the voltage difference between the system and battery is the R_{DSON} of BATFET multiplied by the charging current. When battery charging is disabled and VBAT is above minimum system voltage setting, or charging is terminated, the system is regulated 50mV (typical) above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

8.3.5.2 Dynamic Power Management

To maximize input current without overloading the adapter, the charger features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When an input source is over-loaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters supplement mode where the BATFET turns on and the battery starts discharging to support the system from both the input source and battery.

During DPM mode, the status register bits VINDPM_STAT and/or IINDPM_STAT are set high. Figure 8-2 shows the DPM response with 9V/1.2A adapter, 3.2V battery, 2.8A charge current, and 3.4V minimum system voltage setting.

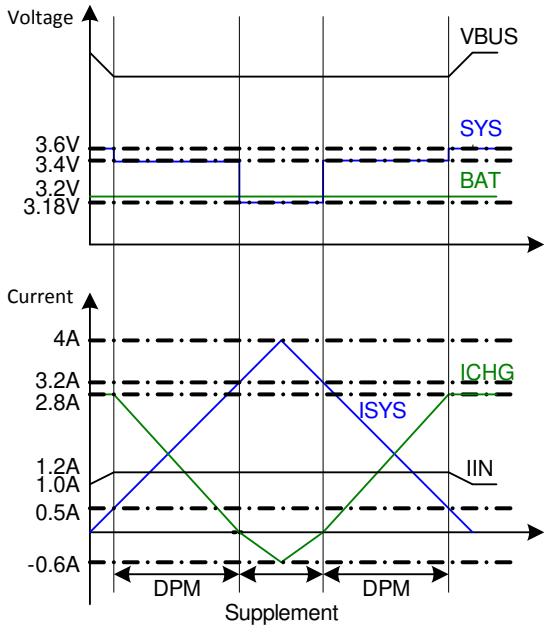


Figure 8-2. DPM Response

8.3.5.3 High Impedance (HIZ) Mode

The host can place the device into high impedance mode by writing EN_HIZ = 1b when an adapter is connected and only when the device is in forward mode. In high impedance mode, RBFET (Q1), HSFET (Q2) and LSFET (Q3) are turned off. The RBFET and HSFET block current flow to and from VBUS, putting the VBUS pin into a high impedance state. The BATFET (Q4) is turned on to connect the BAT to SYS. During high impedance mode, REGN is disabled and the digital clock is slowed to conserve power.

8.3.6 Battery Charging Management

The device charges 1cell Li-Ion battery with up to 5A charge current. The 7mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

8.3.6.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit = 1b and $\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 8-3. The host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table 8-3. Charging Parameter Default Settings

	VREG	VRECHG	ITRICKLE	IPRECHG	ICHG	ITERM	TOPOFF TIMER
BQ25630	4.2V	VREG - 100mV	80mA	200mA	2,000mA	200mA	Disabled

A new charge cycle starts when the following conditions are valid:

- Converter starts per the conditions in Section 8.3.4.4
- EN_CHG = 1b
- $\overline{CE}$ pin is low
- No thermistor fault on TS
- No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device is not in DPM or thermal regulation. When a

fully charged battery is discharged below VRECHG, the device automatically starts a new charging cycle. After charging terminates, toggling $\overline{CE}$ pin or EN_CHG bit also initiates a new charging cycle.

The status register (CHG_STAT) indicates the different charging phases as follows:

- 000b – Not Charging
- 001b – Trickle Charge ($V_{BAT} < V_{BAT\_SHORTZ}$)
- 010b – Pre-charge ($V_{BAT\_SHORTZ} < V_{BAT} < V_{BAT\_LOWV}$)
- 011b – Fast Charge (CC mode)
- 100b – Taper Charge (CV mode)
- 101b – Reserved
- 110b – Top-off Timer Active Charging
- 111b – Charge Termination Done

When the CHG_STAT transitions to any of these states, including when the charge cycle completes, an $\overline{INT}$ pulse is asserted to notify the host.

8.3.6.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage and an optional top-off charging phase. At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

If the charger device is in DPM regulation or thermal regulation during charging, the charging current can be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

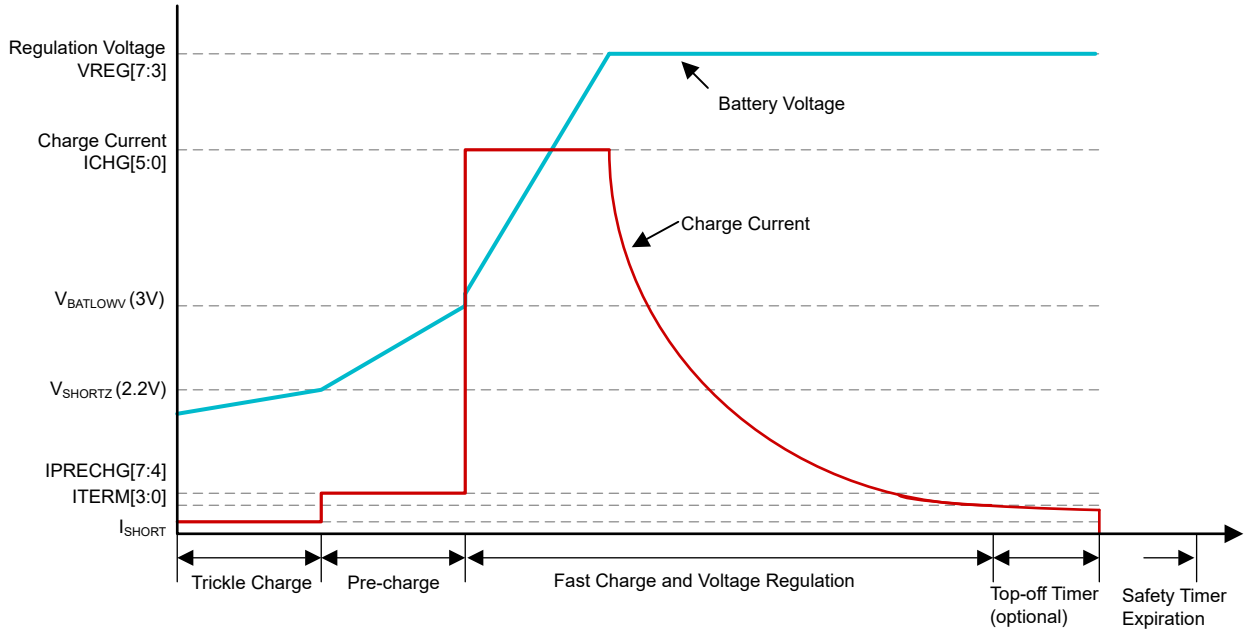


Figure 8-3. Battery Charging Profile

8.3.6.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, the converter is in constant-voltage regulation and the battery current is below ITERM. Because constant-voltage regulation is required for termination, the device does not terminate while IINDPM, VINDPM or thermal regulation loops are active. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage supplement mode.

When termination occurs, the status register CHG_STAT is set to 111b, and an $\overline{INT}$ pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be permanently disabled by writing 0b to EN_TERM bit prior to charge termination.

At low termination currents, due to the comparator offset, the actual termination current can be 10mA to 20mA higher than the termination target. An optional snubber circuit can be added from the SW pin to ground, to improve termination accuracy at low currents. Suggested values for the snubber circuit are 28Ω and 3nF.

To compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. When the top-off timer is enabled and termination occurs, the status register CHG_STAT is set to 110b. The top-off timer follows safety timer constraints, such that if the safety timers suspend, so does the top-off timer. Similarly, if the safety timers count at half-clock rate, so does the top-off timer. Refer to Section 8.3.6.5 for the list of conditions. The host can read CHG_STAT to find out the termination status.

Top-off timer gets reset by any of the following conditions:

1. Charging cycle stop and restart (toggle CE pin, toggle EN_CHG bit, charged battery falls below recharge threshold or adapter removed and replugged)
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination has no effect unless a recharge cycle is initiated. CHG_FLAG is set to 1b when entering top-off timer segment and again when the top-off timer expires.

8.3.6.4 Thermistor Qualification

The charger provides a single thermistor input (TS) for battery temperature monitor. The TS pin can be ignored by setting TS_IGNORE = 1b. When the TS pin feedback is ignored, the charger considers the TS is always good for charging and OTG modes, and TS_STAT always reports TS_NORMAL. The TS pin can be left floating if TS_IGNORE is set to 1b.

When TS_IGNORE = 0b, the charger adjusts the charging profile based on the TS pin feedback information according to the configurable profile described in Section 8.3.6.4.1. When the battery temperature crosses from one temperature range to another, TS_STAT is updated accordingly, and the charger sets the FLAG bit for the newly-entered temperature range, unless the range is TS_NORMAL, which has no FLAG. If TS_MASK is set to 0b, any change to TS_STAT, including a transition to TS_NORMAL, generates an $\overline{INT}$ pulse.

8.3.6.4.1 Advanced Temperature Profile in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges. As battery technology continues to evolve, battery manufacturers have released temperature safety specifications that extend beyond the JEITA standard. BQ25630 features a highly flexible temperature-based charging profile to meet these advanced specifications while remaining backwards compatible with the original JEITA standard.

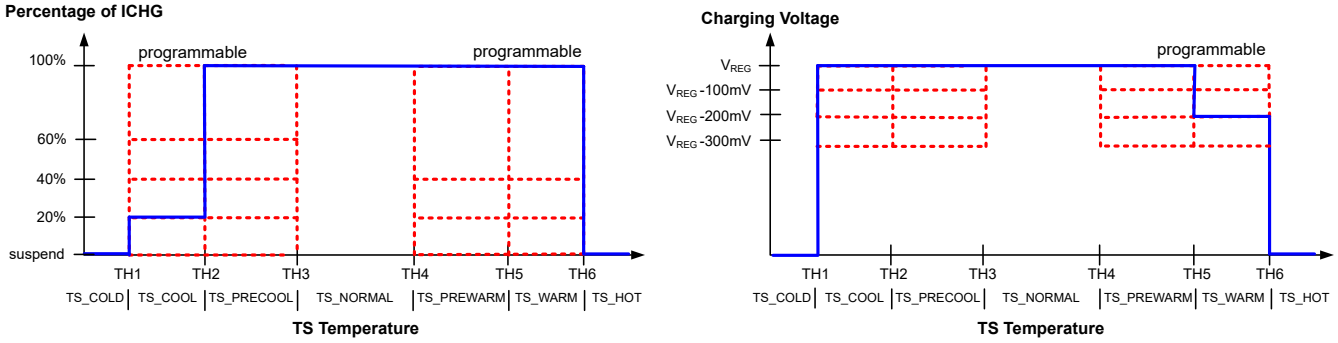


Figure 8-4. Advanced TS Charging Values

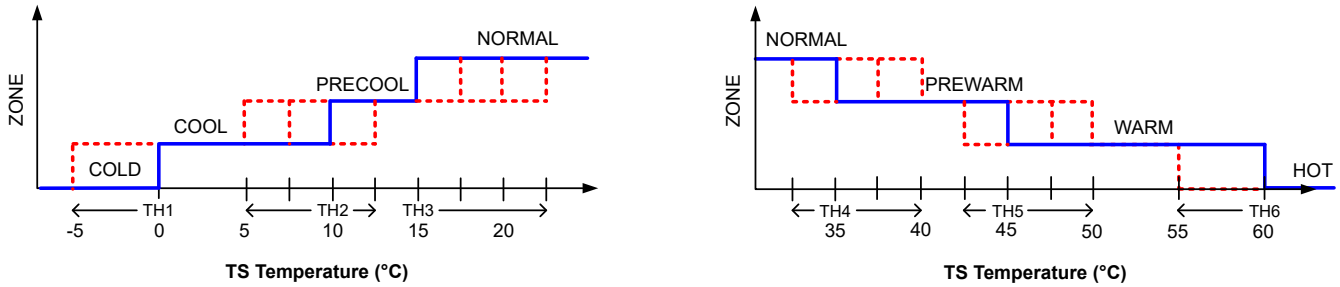


Figure 8-5. Advanced TS Charging Regions

Table 8-4. TS Threshold Settings (default values in blue)

REGION	CONTROL REGISTER	CONTROL VALUE
COLD	TS_TH1	-5ºC
		0ºC
COOL	TS_TH2	5ºC
		7.5ºC
		10ºC
		12.5ºC
PRECOOL	TS_TH3	**15ºC**
		17.5ºC
		20ºC
		22.5ºC
PREWARM	TS_TH4	32.5ºC
		35ºC
		37.5ºC
		40ºC
WARM	TS_TH5	42.5ºC
		45ºC
		47.5ºC
		50ºC
HOT	TS_TH6	55ºC
		60ºC

Charging termination and the charging safety timer are adjusted within the temperature zones to reflect changes to the charging current. When IPRECHG and ICHG are reduced to 20%, 40%, or 60% in the cool or warm temperature zones, the charging safety timer counts at half rate. If charging is suspended, the safety timer is suspended and CHG_STAT is set to 000b (not charging). Charging termination is still enabled (when EN_TERM=1b) with termination current (ITERM) unchanged when charging current is reduced in cool or warm temperature zones.

8.3.6.4.2 TS Pin Thermistor Configuration

The typical TS resistor network is illustrated below.

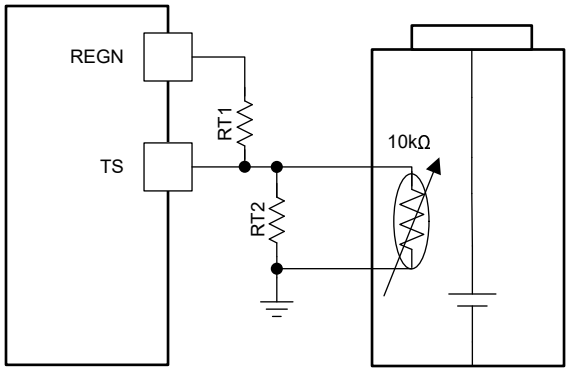


Figure 8-6. TS Resistor Network

The value of RT1 and RT2 are determined from the resistance of the recommended 103AT-2 thermistor at 0ºC and 60ºC ($RTH_{0ºC}$= 27.28kΩ and $RTH_{60ºC}$ = 3.02kΩ) and the corresponding voltage thresholds V_{TS_COLD} and V_{TS_HOT} (expressed as percentage of REGN with value between 0 and 1).

$$RT2 = \frac{RTH_{0ºC} \times RTH_{60ºC} \times \left(\frac{1}{V_{TS\_0ºC}} - \frac{1}{V_{TS\_60ºC}}\right)}{RTH_{60ºC} \times \left(\frac{1}{V_{TS\_60ºC}} - 1\right) - RTH_{0ºC} \times \left(\frac{1}{V_{TS\_0ºC}} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{TS\_0ºC}} - 1}{\frac{1}{R_{T2}} + \frac{1}{RTH_{0ºC}}} \quad (2)$$

$$RT2 = \frac{RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{1}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{1}{VT1} - 1\right)} \quad (3)$$

$$RT1 = \frac{\frac{1}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (4)$$

Assuming a 103AT-2 NTC thermistor on the battery pack, the RT1 and RT2 are calculated to be 5.23kΩ and 30.1kΩ respectively.

8.3.6.4.3 Cold/Hot Temperature Window in OTG Mode

For battery protection during boost OTG, the device monitors the battery temperature to be within the TS_TH_OTG_COLD to TS_TH_OTG_HOT thresholds. For a 103AT-2 NTC thermistor with RT1 of 5.23kΩ and RT2 of 30.1kΩ, TS_TH_OTG_COLD default is -10°C and TS_TH_OTG_HOT default is 60°C. When temperature is outside of this range, the OTG mode is suspended with REGN remaining on. In addition, VBUS_STAT bits are set to 000b, TS_STAT is set to 001b (TS_OTG_COLD) or 010b (TS_OTG_HOT), and TS_FLAG is set. In boost OTG, the converter stops switching. Once the battery temperature returns to normal temperature, the boost OTG is restarted and TS_STAT returns to 000b (TS_NORMAL).

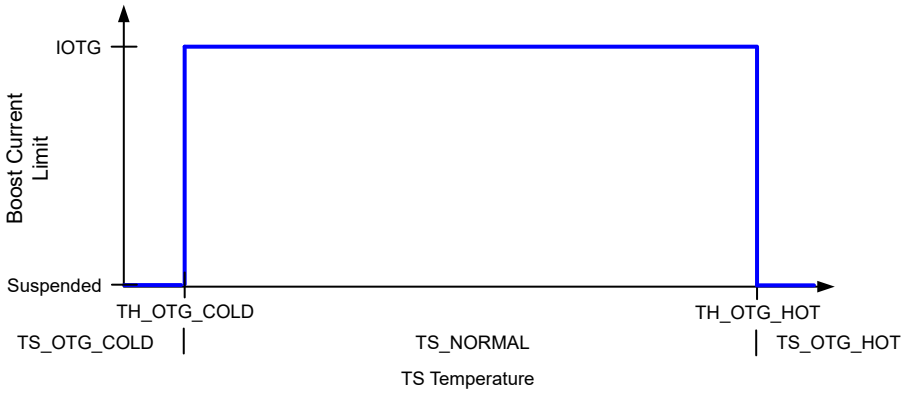


Figure 8-7. TS Pin Thermistor Sense Threshold in Boost Mode

8.3.6.4.4 JEITA Charge Rate Scaling

The TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM and TS_ISET_WARM cool and warm charge current fold backs are based on a 1C charging rate. The 1C rate is the battery capacity in mA-hours divided by 1 hour, so that a 500mA-hour battery would have a 1C charging rate of 500mA. The same battery would have a 2C charging rate of 1,000mA. To convert the charging foldback, the host must set the CHG_RATE register to the C rate for the battery. This scales the foldback accordingly.

When TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM or TS_ISET_WARM is set to either 00b (suspend) or 11b (unchanged), the CHG_RATE setting has no effect. A summary is provided in Table 8-5

Table 8-5. ICHG Fold Back

TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM or TS_ISET_WARM	CHG_RATE	FOLD-BACK CURRENT AS PERCENTAGE OF ICHG
00b	Any	0% (Suspended)
01b (20%)	00b (1C)	20%
	01b (2C)	10%
	10b (4C)	5%
	11b (6C)	3.3%
10b (40%)	00b (1C)	40%
	01b (2C)	20%
	10b (4C)	10%
	11b (6C)	6.6%
11b	Any	100%

8.3.6.5 Charging Safety Timers

BQ25630 has three built-in safety timers to prevent extended charging cycle due to abnormal battery conditions. The fast charge safety timer and pre-charge safety timers are set through I^2C CHG_TMR and PRECHG_TMR fields, respectively. The trickle charge timer is fixed as 1 hour. At the end of a safety timer expiration, charging is stopped (CHG_STAT = 000b) and the buck converter continues to operate to supply system load.

The trickle charging, pre-charging and fast charging safety timers can be disabled by setting EN_SAFETY_TMRS = 0b. EN_SAFETY_TMRS can be enabled anytime regardless of which charging stage the charger is in. Each timer starts to count as soon as the following two conditions are simultaneously true: EN_SAFETY_TMRS=1 and the corresponding charging stage is active.

When either the fast charging, trickle charging or pre-charging safety timer expires, the SAFETY_TMR_STAT and SAFETY_TMR_FLAG bits are set to 1b.

Events that cause a reduction in charging current also cause the charging safety timer to count at half-clock rate if EN_TMR2X bit is set.

During faults which suspend charging, the charge, pre-charge and trickle safety timers are also suspended, regardless of the state of the EN_TMR2X bit. Once the fault goes away, charging resumes and the safety timer resumes where the timer stopped.

The charging safety timer and the charging termination can be disabled at the same time. Under this condition, the charging keeps running until charging is disabled by the host.

8.3.6.6 Alternate Power from Input

Alternate Power from Input mode allows for an alternate power source with low current capability to provide system power and charge the battery. In API mode, the maximum input current is limited to the value set by API_ILIM and is capable of fine adjustment of an accurate current limit (10-100mA in 2.5mA steps). The EN_API bit controls entering and exiting API Mode.

For adapters with variable power capability, like solar adapters, going in and out of API mode depending on the adapter conditions can be beneficial. If a low-current adapter is detected, the LOW_PWR_ADP_STAT is set to 1b to indicate that API mode can be useful to better use the low-current adapter. Once in API mode, IINDPM_STAT can indicate that the adapter is able to reach the maximum current in API mode, and exiting API mode can be beneficial. API mode enter and exit is controlled by the host, the status bits are meant to indicate when API mode can be more beneficial than normal mode.

8.3.7 USB On-The-Go (OTG)

8.3.7.1 Boost OTG Mode

The device supports boost converter operation to deliver power from the battery to VBUS. The output voltage is set in VOTG and the maximum current is set in IOTG. VBUS_STAT is set to 111b upon a successful entry into boost OTG. The boost operation is enabled when the following conditions are met:

1. BAT above $V_{BAT\_OTG\_MIN}$
2. VBUS less than $V_{BAT}+V_{SLEEP}$
3. Boost mode operation is enabled (EN_OTG = 1)
4. $V_{TS\_OTG\_HOT} < V_{TS} < V_{TS\_OTG\_COLD}$
5. $V_{REGN} > V_{REGN\_OK}$
6. 30ms delay after EN_OTG = 1
7. Boost mode regulation voltage (VOTG) is greater than 105% of battery voltage.

Any of the following conditions causes an exit from boost OTG. Unless otherwise indicated, exit is into battery-only mode by setting EN_OTG = 0.:

- OTG mode is disabled (EN_OTG=0) .
- Entry into shutdown, ship mode, ultra-low power mode or system power reset by setting EN_OTG = 0 and then enter into shutdown, ship mode, ultra-low power mode or system power reset as selected.

8.3.8 Integrated 12-bit ADC for Monitoring

BQ25630 provides an integrated 12-bit ADC for the host to monitor various system parameters. The ADC_RATE bit allows continuous conversion or one-shot behavior.

To enable the ADC, the EN_ADC bit must be set to 1b. The ADC is disabled by default (EN_ADC = 0b) to conserve power. The ADC is allowed to operate if either VBUS > 3.7V or VBAT > $V_{BAT\_LOWV\_ADC}$ is valid. If EN_ADC is set to 1b before VBUS or VBAT reach the respective valid thresholds, then EN_ADC stays 1b. While the charger is transitioning to HIZ mode, the ADC is temporarily suspended.

In battery-only mode, if the TS_ADC channel is enabled, the ADC only operates when battery voltage is higher than 3.2V (the minimum value to turn on REGN), otherwise, the ADC operates when the battery voltage is higher than $V_{BAT\_LOWV\_ADC}$.

The ADC_DONE_STAT, ADC_DONE_FLAG bits are set when a conversion is complete in one-shot mode only. During continuous conversion mode, the ADC_DONE_STAT, ADC_DONE_FLAG bits have no meaning and remain at 0. In one-shot mode, the EN_ADC bit is set to 0 at the completion of the conversion, at the same time as the ADC_DONE_FLAG bit is set. In continuous mode, the EN_ADC bit remains at 1 until the user disables the ADC by setting EN_ADC to 0.

8.3.9 Status Outputs ($\overline{INT}$, $\overline{PG}$)

8.3.9.1 $\overline{PG}$ Pin Power Good Indicator

The $\overline{PG}$ pin goes LOW to indicate a good input source when:

- V_{VBUS} is above V_{VBUS_UVLOZ}
- V_{VBUS} is above battery (not in sleep)
- V_{VBUS} is below V_{VBUS_OVP} threshold
- V_{VBUS} is above programmable PG_TH threshold

8.3.9.2 Interrupts and Status, Flag, and Mask Bits

BQ25630 incorporates an interrupt pin ($\overline{INT}$) to inform a host microcontroller of status changes without requiring microcontroller polling. Each reported event has a status field, a flag bit and a mask bit. The status field reports the status at the time that the status is read. The flag bit is latched and, once set to 1, remains at 1 until the host reads the bit, which clears the bit to 0. The mask bit determines whether or not an interrupt pulse is generated when the corresponding bit is set.

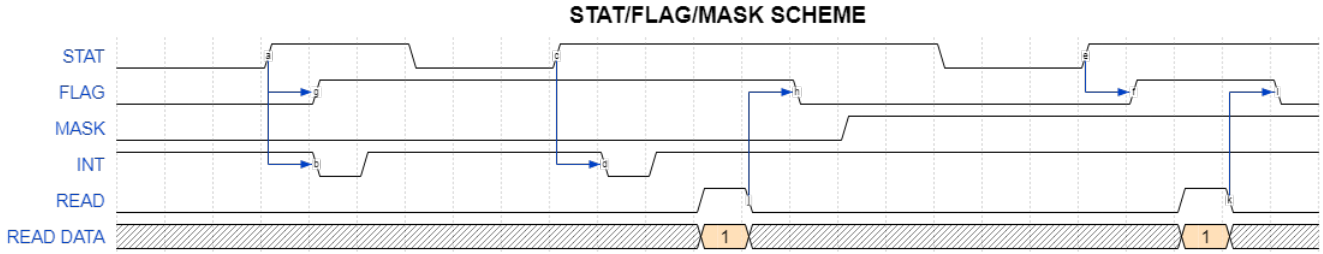


Figure 8-8. Relationship between STAT, FLAG and MASK

These transitions also generate an $\overline{INT}$ pulse if the associated mask bit is set to 0. Because the $\overline{INT}$ is generated from the status field transition and not the flag bit, an $\overline{INT}$ pulse is sent to the host even if the associated flag is already set to 1 when the status transition occurs. Details of this behavior are shown in Figure 8-8.

The default behavior is to generate a 256µs $\overline{INT}$ pulse when any flag bit is set to 1 by the change of a status bit. These pulses can be masked out on a flag-by-flag basis by setting a flag's mask bit to 1. Setting the mask bit does not affect the transition of the flag bit from 0 to 1, only the generation of the 256µs $\overline{INT}$ pulse.

8.3.9.3 Interrupt to Host ($\overline{INT}$)

In many applications, the host does not continually poll the charger status registers. Instead, the $\overline{INT}$ pin can be used to notify the host of a status change with a 256µs $\overline{INT}$ pulse. Upon receiving the interrupt pulse, the host can read the flag registers (Charger_Flag_X and FAULT_Flag_X) to determine the event that caused the interrupt, and for each flagged event, read the corresponding status registers (Charger_Status_X and FAULT_Status_X) to determine the current state. Once set to 1, the flag bits remain latched until the bits are read by the host, which clears them. The status bits, however, are updated whenever there is a change to status and always represent the current state of the system.

The $\overline{INT}$ events can be masked off to prevent $\overline{INT}$ pulses from being sent out when tinterrupts occur, with the exception of the initial power-up interrupt. Interrupt events are masked by setting the mask bit in registers (Charger_Mask_X and FAULT_Mask_X.) Events always cause the corresponding flag bit to be set to 1, regardless of whether or not the interrupt pulse has been masked.

8.3.10 BATFET Control

The device has an integrated, bi-directionally blocking BATFET that can be turned off to remove leakage current from the battery to the system. The BATFET is controlled by the BATFET_CTRL register bits, and supports shutdown mode, standby mode and ship mode. Additionally, the system power reset function is controlled by the SYS_RESET register bit.

Table 8-6. BATFET Control Modes

MODE	BATFET	I²C	ENTRY, NO ADAPTER	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =0	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =1	EXIT
Normal	On	Active	N/A			N/A
Shutdown mode	Off	Off	Writing BATFET_CTRL = 01b turns off BATFET after BATFET_DLY and enters shutdown.	Writing BATFET_CTRL = 01b with adapter present is ignored, regardless of BATFET_CTRL_WVBUS setting, and BATFET_CTRL is reset to 00b.		Adapter plug-in
Ship mode	Off	Off	Writing BATFET_CTRL = 10b turns off BATFET after BATFET_DLY and enters ship mode.	Writing BATFET_CTRL = 10b has no effect while adapter is present. When both BATFET_DLY has expired and the adapter is removed, the device turns off BATFET and enters ship mode. Writing BATFET_CTRL = 00b before adapter is removed aborts ship mode.	Writing BATFET_CTRL = 10b turns off BATFET after BATFET_DLY. When both BATFET_DLY has expired and adapter is removed, the device enters ship mode. Writing BATFET_CTRL = 00b before adapter is removed turns BATFET on and aborts ship mode.	$\overline{QON}$, adapter plug-in
Standby mode	Off	Active	Writing BATFET_CTRL = 11b turns off BATFET after BATFET_DLY and enters standby mode.	Writing BATFET_CTRL = 11b has no effect while adapter is present. When both BATFET_DLY has expired and the adapter is removed, the device turns off BATFET and enters standby mode. Writing BATFET_CTRL = 00b before adapter is removed aborts standby mode.	Writing BATFET_CTRL = 11b turns off BATFET after BATFET_DLY. When both BATFET_DLY has expired and adapter is removed, the device enters ultra-low power mode. Writing BATFET_CTRL = 00b before adapter is removed turns BATFET on and aborts standby mode.	$\overline{QON}$, I²C, adapter plug-in
System reset	On to Off to On	Active	Writing SYS_RESET = 1b initiates system reset after BATFET_DLY. If DIS_QON_RST = 0b, holding $\overline{QON}$ low for t_{QON_RST} initiates immediate reset (BATFET_DLY is not applied.)	Writing SYS_RESET = 1b is ignored and SYS_RESET resets to 0b. Holding $\overline{QON}$ low for t_{QON_RST} is ignored.	Writing SYS_RESET = 1b initiates system reset after BATFET_DLY. If DIS_QON_RST = 0b, holding $\overline{QON}$ low for t_{QON_RST} initiates immediate reset. Converter is placed in HIZ during system reset and exits HIZ when system reset completes.	N/A

8.3.10.1 Shutdown Mode

For the lowest battery leakage current, the host can shut down the device by setting the register bits BATFET_CTRL to 01b. In this mode, the BATFET is turned off to prevent the battery from powering the system,

the I^2C is disabled and the charger is totally shut down. The charger can only be woken up by plugging in an adapter. When the adapter is plugged in, the device starts back up with all register settings in the POR default.

After the host sets BATFET_CTRL to 01b, the BATFET turns off after waiting either 20ms or 10s as configured by BATFET_DLY register bit. Shutdown mode can only be entered when $V_{VBUS} < V_{VBUS\_UVLO}$, regardless of the BATFET_CTRL_WVBUS setting, which has no effect on shutdown mode entry. If the host writes BATFET_CTRL = 01b with $V_{VBUS} > V_{VBUS\_UVLOZ}$, the request is ignored and the BATFET_CTRL bits are set back to 00.

If the host writes BATFET_CTRL to 01b while boost OTG, BQ25630 first exits from boost OTG by setting EN_OTG = 0b and then enters shutdown mode.

$\overline{QON}$ has no effect during shutdown mode. The internal pull-up on the $\overline{QON}$ pin is disabled during shutdown to prevent leakage through the pin.

8.3.10.2 Ship Mode

In ship mode, the BATFET is turned off to prevent the battery from powering the system. The host can place BQ25630 into ship mode by setting BATFET_CTRL = 10b. Ship mode has slightly higher quiescent current than shutdown mode, but $\overline{QON}$ can be used to exit from ship mode. The device is taken out of ship mode by either of these methods:

- Pulling the $\overline{QON}$ pin low for t_{SM_EXIT}
- $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter plug-in)

When the charger enters ship mode, the registers are reset to the POR values.

Ship mode is only entered when the adapter is not present. Setting BATFET_CTRL = 10b while $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter present) either disables the BATFET or have no immediate effect depending on the setting of BATFET_CTRL_WVBUS.

8.3.10.3 Standby Mode

In standby mode, the BATFET is turned off to prevent the battery from powering the system. The host can place BQ25630 into standby mode by setting BATFET_CTRL = 11b. Standby mode has slightly higher quiescent current than shutdown mode and ship mode, but $\overline{QON}$ or an I^2C command can be used to exit from standby mode. The device is taken out of standby mode by either of these methods:

- Pulling the $\overline{QON}$ pin low for $t_{STANDBY\_EXIT}$
- Write BATFET_CTRL to 00b via I^2C
- $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter plug-in)

Standby mode is only entered when the adapter is not present. Setting BATFET_CTRL = 11b while $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter present) either disables the BATFET or have no immediate effect depending on the setting of BATFET_CTRL_WVBUS.

8.3.10.4 System Power Reset

The BATFET functions as a load switch between battery and system when the converter is not running. By changing the state of BATFET from on to off, systems connected to SYS can be power cycled. A system reset also resets all registers to POR state. Any of the following conditions initiate a system power reset:

- BATFET_CTRL_WVBUS = 1b and $\overline{QON}$ is pulled low for t_{QON_RST} and DIS_QON_RST = 0b
- BATFET_CTRL_WVBUS = 1b and SYS_RESET = 1b
- BATFET_CTRL_WVBUS = 0b and VBUS < V_{VBUS_UVLO} simultaneously with $\overline{QON}$ pulled low for t_{QON_RST} and DIS_QON_RST = 0b
- BATFET_CTRL_WVBUS = 0b and VBUS < V_{VBUS_UVLO} and SYS_RESET = 1b

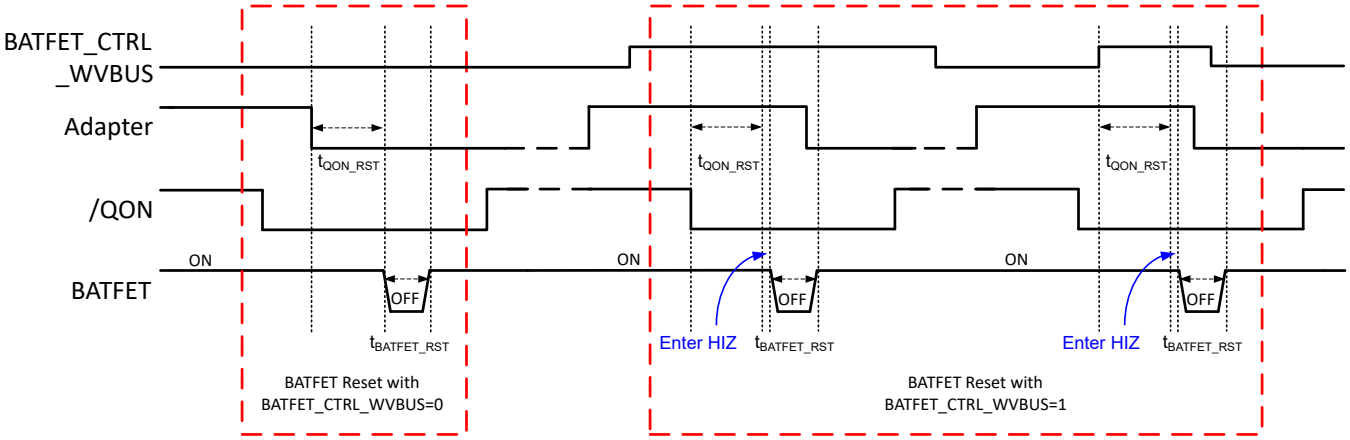


Figure 8-9. System Power Reset Timing

When BATFET_CTRL_WVBUS is set to 1, system power reset proceeds if either SYS_RESET = 1b or $\overline{QON}$ is pulled low for t_{QON_RST}, regardless of whether or not VBUS is present. There is a delay of t_{BATFET_DLY} before initiating the system power reset. If $\overline{QON}$ is pulled low, there is no delay after the t_{QON_RST} completes, regardless of BATFET_DLY setting. DIS_QON_RST bit can be set to 1b to disable system reset by $\overline{QON}$ press.

The system power reset can be initiated from the battery only condition, from OTG mode or from the forward charging mode with adapter present. If the system power is reset when the charger is in boost OTG mode, the boost OTG mode is first terminated by setting EN_OTG = 0b.

8.3.11 Protections

8.3.11.1 Voltage and Current Monitoring in Battery Only and HIZ Modes

The device monitors a reduced set of voltages and currents when operating from battery without an adapter or when operating from battery in high impedance mode. Battery Overcurrent Protection and Battery Undervoltage Lockout are monitored in this mode.

8.3.11.1.1 Battery Overcurrent Protection

BQ25630 has a two-level battery overcurrent protection. The I_{BAT_PK} threshold is set by IBAT_PK and provides a fast (100µs) protection for the battery discharging. I_{BATFET_OCP} provides a slower (50ms), fixed-threshold protection for the BATFET. If the battery discharge current becomes higher than either threshold for the deglitch time, the BAT_FAULT_STAT and BAT_FAULT_FLAG fault register bits are set to 1, and the BATFET enters hiccup mode. The BAT_FAULT_STAT returns to 0 once the BATFET is disabled for the hiccup mode. Once the BATFET is turned back on, the I_{BAT_PK} and I_{BATFET_OCP} thresholds are re-evaluated with the respective deglitch times. In boost OTG mode, if the battery discharging current is higher than either I_{BAT_PK} or I_{BATFET_OCP} for the respective deglitch times, the charger exits OTG mode by clearing the EN_OTG bit.

8.3.11.1.2 Battery Undervoltage Lockout

In battery-only mode, BQ25630 disables the BATFET if V_{BAT} falls below V_{BAT_UVLO}, separating the system from the battery. I^2C is disabled as well. Upon exit from the undervoltage lockout condition when either V_{BAT} rises above V_{BAT_UVLOZ} or V_{VBUS} rises above V_{VBUS_UVLOZ}, I^2C is re-enabled and the registers are reset to the POR values.

8.3.11.2 Voltage and Current Monitoring in Buck Mode

The device closely monitors VBUS, SYS and BAT voltages, as well as VBUS, BAT and FET currents to provide safe forward mode operation.

8.3.11.2.1 Input Overvoltage

If VBUS voltage rises above V_{VBUS_OVP}, the converter stops switching immediately to protect the internal power MOSFETs and I_{PMID_LOAD} discharge current is applied to bring down VBUS voltage. VBUS_FAULT_FLAG

is set to 1 and the VBUS_FAULT_STAT bit transitions to 1. When VBUS falls back below V_{VBUS_OVPZ}, VBUS_FAULT_STAT transitions to 0 and the converter resumes switching.

8.3.11.2.2 System Overvoltage Protection (SYSOVP)

When VSYS rises above V_{SYS_OVP} in forward converter operation, the converter stops switching immediately to limit voltage overshoot and applies I_{SYS_LOAD} to pull down the system voltage. VSYS_FAULT_FLAG is set to 1 and the VSYS_FAULT_STAT transitions to 1. Once VSYS drops below V_{SYS_OVP}, the converter resumes switching, the 30mA discharge current is removed and VSYS_FAULT_STAT transitions to 0.

8.3.11.2.3 Forward Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak overcurrent protection in the switching MOSFETs. In forward mode, if the current through Q2 exceeds the cycle-by-cycle limit, the converter immediately turns off the high-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

8.3.11.2.4 System Short

When the SYS voltage falls below V_{SYS_SHORT}, the charger immediately enters PFM operation to limit the output current to approximately 0.5A or less. SYS_FAULT_STAT and SYS_FAULT_FLAG bits are set to 1. If V_{SYS} rises above V_{SYS_SHORTZ}, the converter exits forced PFM mode, and the SYS_FAULT_STAT bit is set to 0.

8.3.11.2.5 Battery Overvoltage Protection (BATOVP)

When V_{BAT} transitions above V_{BAT_OVP}, BQ25630 immediately disables charging by disabling the BATFET and applies I_{BAT_LOAD} current source to discharge excess BAT voltage. BAT_FAULT_FLAG is set to 1 and BAT_FAULT_STAT transitions to 1. Once V_{BAT} falls below V_{BAT_OVPZ}, charging resumes and BAT_FAULT_STAT transitions back to 0.

8.3.11.2.6 Sleep Comparator

The sleep comparator is used to suspend the converter if the adapter voltage is insufficient to maintain buck converter operation while charging the battery. If V_{VBUS} falls below V_{BAT} + V_{SLEEP} the converter stops switching, the $\overline{PG}$ pin transitions high. If V_{VBUS} rises back above V_{BAT} + V_{SLEEPZ}, the converter restarts, the $\overline{PG}$ pin transitions low.

8.3.11.3 Voltage and Current Monitoring in Boost Mode

The device closely monitors VBUS, SYS and BAT voltages, as well as VBUS, BAT and FET currents to provide safe reverse mode operation.

8.3.11.3.1 Boost Mode Overvoltage Protection

During OTG operation, BQ25630 uses two comparators to sense output overvoltage at VBUS and PMID. If either VBUS or PMID voltage rises above the OVP thresholds, the converter stops switching and attempts to discharge the voltage.

If the OVP condition persists on VBUS or PMID, OTG_FAULT_FLAG is set to 1, OTG_FAULT_STAT transitions to 1 and the converter powers down into a fault condition and the device exits from OTG mode by setting EN_OTG = 0.

8.3.11.3.2 Boost Mode Duty Cycle Protection

After an initial startup blanking period, BQ25630 monitors the PMID voltage during boost OTG mode to ensure that PMID voltage remains sufficiently above VSYS to maintain the minimum duty cycle. If V_{PMID} falls below V_{BOOST_DUTY} (105% V_{SYS} typical), the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

8.3.11.3.3 Boost Mode PMID Undervoltage Protection

During boost OTG mode, BQ25630 converter monitors PMID for undervoltage. If the PMID voltage falls below V_{OTG_UVP}, the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

8.3.11.3.4 Boost Mode Battery Undervoltage

If V_{BAT} falls below V_{BAT_OTGZ} during OTG mode, the charger exits OTG mode by setting EN_OTG = 0, and BAT_FAULT_STAT and BAT_FAULT_FLAG are set to 1. Setting EN_OTG = 1 while $V_{BAT} < V_{BAT\_OTG}$ does not enter OTG and the EN_OTG bit is cleared to 0. When the battery is charged above V_{BAT_OTG}, OTG mode can be entered by setting EN_OTG = 1.

8.3.11.3.5 Boost Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak overcurrent protection in the switching MOSFETs. In OTG mode, if the current through Q3 exceeds the cycle-by-cycle current limit, the converter will immediately turn off the low-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

8.3.11.3.6 Boost Mode SYS Short

If VSYS falls below VSYS_SHORT in boost OTG mode, BQ25630 immediately stops the boost converter, enters hiccup mode, and sets SYS_FAULT_FLAG to 1.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host can attempt to restart boost OTG mode by setting EN_OTG = 1.

8.3.11.4 Thermal Regulation and Thermal Shutdown

8.3.11.4.1 Thermal Protection in Buck Mode

The device monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in buck mode. When the internal junction temperature exceeds the T_{REG} thermal regulation limit (TREG register configuration), the device lowers the charging current. During thermal regulation, the safety timer runs at half the clock rate, and the TREG_FLAG and TREG_STAT bits are set to 1. Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET and converter are re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

8.3.11.4.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT}, the boost mode is disabled by setting EN_OTG bit low and BATFET is turned off, and TSHUT_FLAG is set to 1. When IC junction temperature is below T_{SHUT} - T_{SHUT_HYS}, the BATFET is enabled automatically to allow system to restore and the host can re-enable EN_OTG bit to recover.

8.3.11.4.3 Thermal Protection in Battery-only Mode

The device monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in battery-only mode. The device has thermal shutdown to turn off the BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET is re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

8.3.11.5 Liquid Detection and Corrosion Mitigation (Patent Pending)

A USB-C connector can corrode when exposed to moisture or everyday liquids which can result in permanent decomposition of the USB connector. This device contains a liquid detection routine compliant with USB Type-C Specification 2.3.

V_{LQD} sets the threshold of the liquid detection check. A single liquid detection check can be forced by setting FORCE_LQD_DET = 1b if EN_LQD_DET = 1b. When automatic liquid detection is enabled (AUTO_LQD_EN = 1b), a liquid detection check occurs periodically until liquid is detected.

When liquid is detected, the LQD_STAT register is updated accordingly. An $\overline{INT}$ pulse is sent whenever the LQD_STAT register changes. When liquid is confirmed to be detected, VBUS is unpowered and CC1/CC2 enters Corrosion Mitigation.

The device automatically detects if the port is dry when AUTO_DRY_DET = 1b by initiating a liquid detection cycle periodically. To conserve power, the host can disable dry detection (AUTO_DRY_DET = 0b) and use FORCE_LQD_DET to check for a dry port at longer intervals.

8.4 Device Functional Modes

8.4.1 Host Mode and Default Mode

The device is a host controlled charger, but the device can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1b, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit reads as 1b upon the first read and then 0b upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

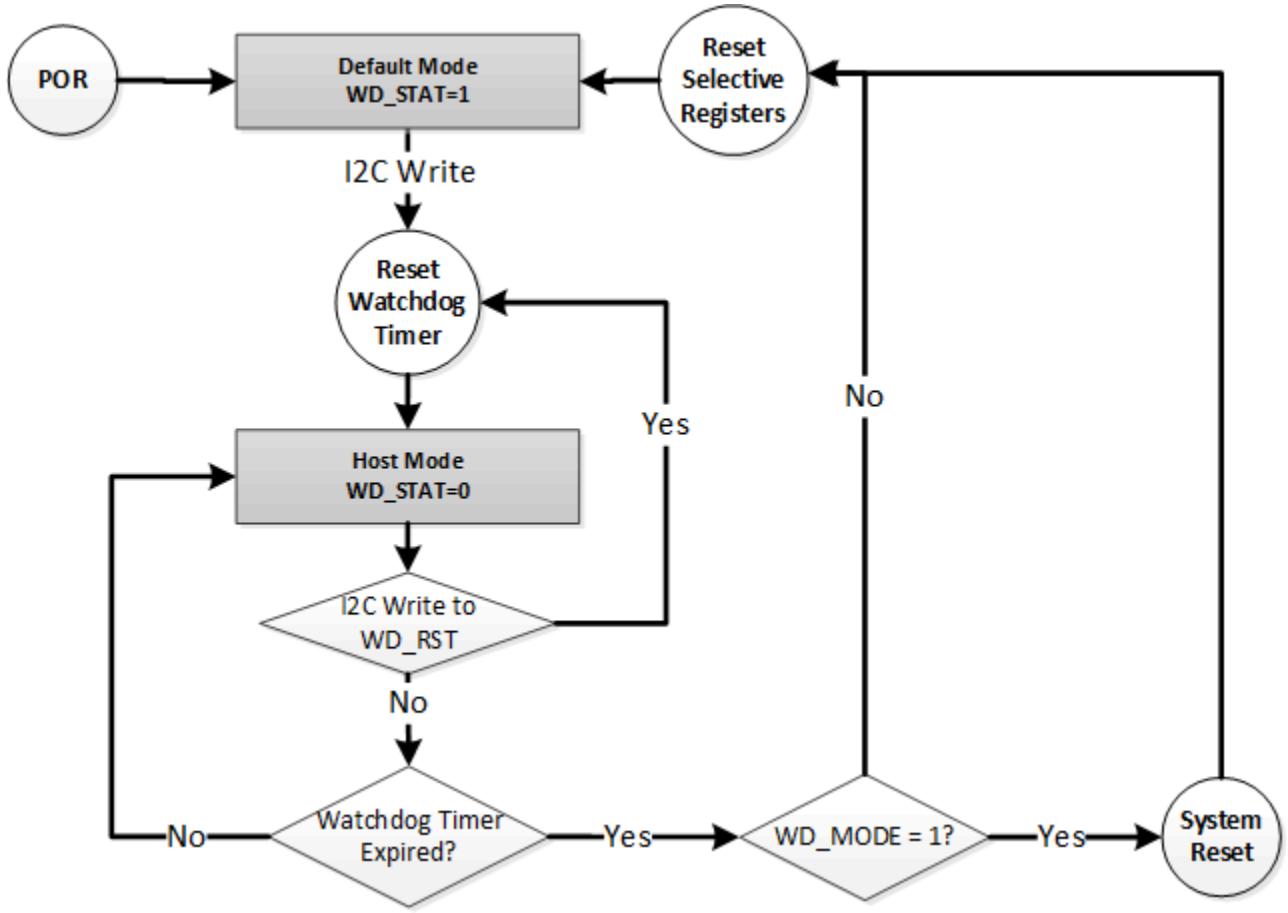
In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. If any of these timers expire, charging is stopped and the buck converter continues to operate to supply the system load.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1b to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00b.

When the watchdog expires, the device returns to default mode. The ICHG value is divided in half when the watchdog timer expires, and a number of other fields are reset to the POR default values as shown in the notes column of the register tables in Section 8.6.2. The watchdog timer is reset on any write if the watchdog timer has expired. When watchdog timer expires, WD_STAT and WD_FLAG are set to 1b, and an $\overline{INT}$ is asserted low to

alert the host (unless masked by WD_MASK). If WD_MODE bit is set to 1b and the watchdog timer expires, a system reset occurs.

Figure 8-10. Watchdog Timer Flow Chart



8.4.2 Register Bit Reset

Registers can also be reset to default values by writing the REG_RST bit to 1b. The register bits that are reset by REG_RST are noted in the Register Map section. After the register reset, the REG_RST bit reverts to 0b automatically.

8.5 Programming

8.5.1 Serial Interface

BQ25630 uses I^{2}C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^{2}C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL).

The device has 7-bit I^{2}C address 0x6B, receiving control inputs from a host device such as a micro-controller or digital signal processor through register addresses defined in the Register Map. The host device initiates all transfers and the charger responds. Register reads outside of these addresses return 0xFF. When the bus is free, both SDA and SCL lines are HIGH.

The I^{2}C interface supports standard mode (up to 100 kbits/s), fast mode (up to 400 kbits/s) and fast mode plus (up to 1 Mbits/s.) These lines are pulled up to a reference voltage via pull-up resistor. The device I^{2}C detection thresholds support a communication reference voltage between 1.2V - 5V.

8.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

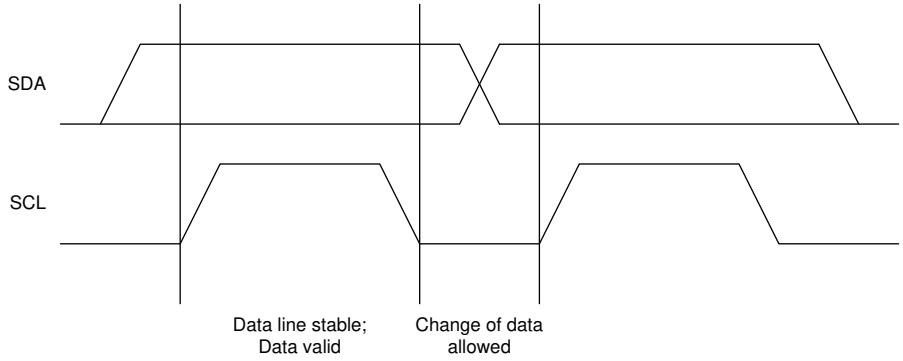


Figure 8-11. Bit Transfer on the I^{2}C Bus

8.5.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

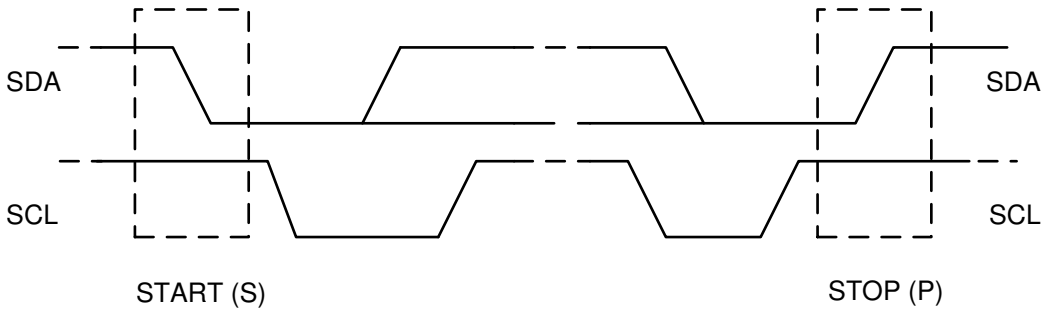


Figure 8-12. START and STOP Conditions on the I^{2}C Bus

8.5.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until the target has performed some other function, the target can hold the SCL line low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

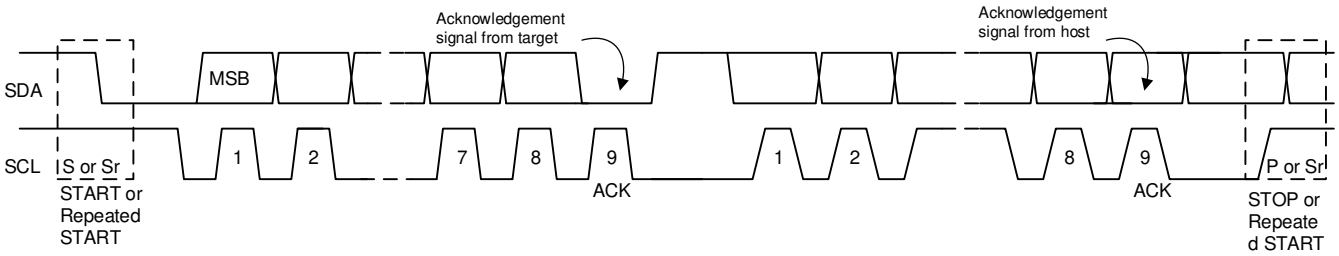


Figure 8-13. Data Transfer on the I²C Bus

8.5.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the host to signal the transmitter that the byte is successfully received and another byte can be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The transmitter releases the SDA line during the acknowledge clock pulse so the host can pull the SDA line LOW and the line remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.5.1.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8th bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as

Figure 8-14. 7-Bit Addressing (0x6B)

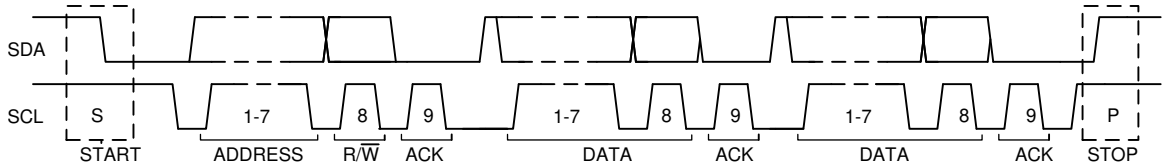


Figure 8-15. Complete Data Transfer on the I²C Bus

8.5.1.6 Single Write and Read

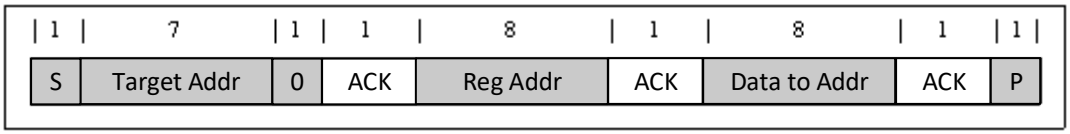


Figure 8-16. Single Write

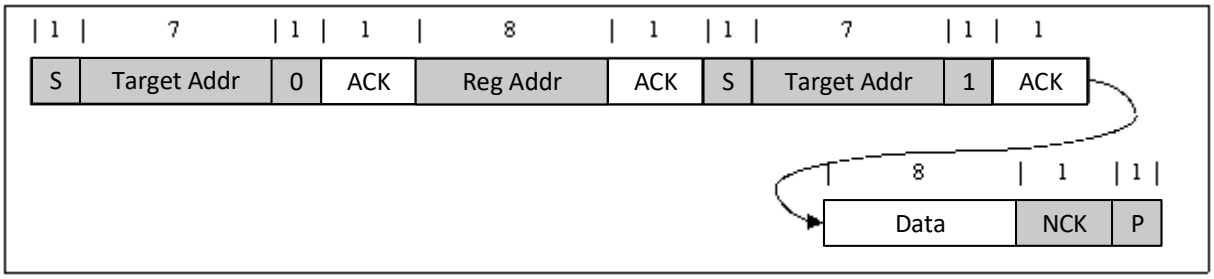


Figure 8-17. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

8.5.1.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire register map can be read in a single operation with a 39-byte read that starts at register address 0x01.

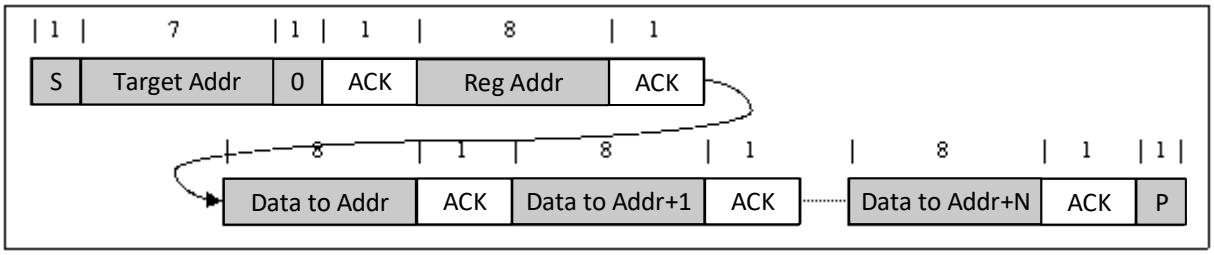


Figure 8-18. Multi-Write

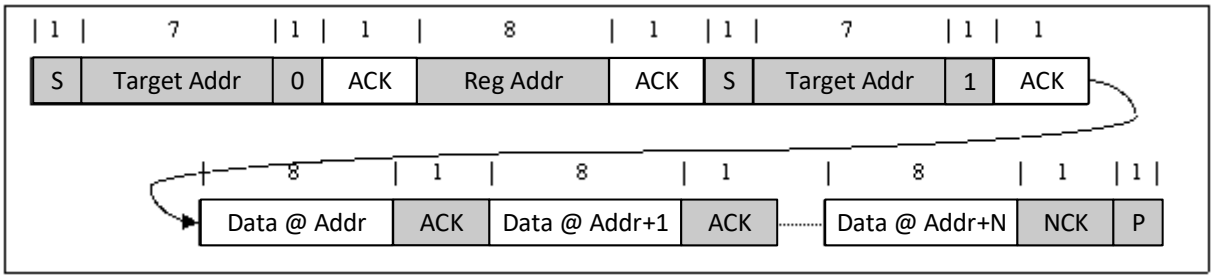


Figure 8-19. Multi-Read

8.6 Register Maps

I²C Device Address: 0x6B.

8.6.1 Register Programming

The BQ25630 has 8-bit and 16-bit registers. When writing to 16-bit registers, I²C transactions follow the little endian format, starting at the address of the least significant byte and writing both register bytes in a single 16-bit transaction.

8.6.2 BQ25630 Registers

Table 8-7 lists the memory-mapped registers for the BQ25630 registers. All register offset addresses not listed in Table 8-7 should be considered as reserved locations and the register contents should not be modified.

Table 8-7. BQ25630 Registers

Address	Acronym	Register Name	Section
2h	REG0x02_Charge_Current_Limit	Charge Current Limit	Go
4h	REG0x04_Charge_Voltage_Limit	Charge Voltage Limit	Go
6h	REG0x06_Input_Current_Limit	Input Current Limit	Go
8h	REG0x08_Input_Voltage_Limit	Input Voltage Limit	Go
Ah	REG0x0A_IOTG_regulation	IOTG regulation	Go
Ch	REG0x0C_VOTG_regulation	VOTG regulation	Go
Eh	REG0x0E_Minimal_System_Voltage	Minimal System Voltage	Go
10h	REG0x10_Precharge_Control	Precharge Control	Go
12h	REG0x12_Termination_Control	Termination Control	Go
14h	REG0x14_Charge_Timer_Control	Charge Timer Control	Go
15h	REG0x15_Charger_Control_0	Charger Control 0	Go
16h	REG0x16_Charger_Control_1	Charger Control 1	Go
17h	REG0x17_Charger_Control_2	Charger Control 2	Go
18h	REG0x18_Charger_Control_3	Charger Control 3	Go
19h	REG0x19_Charger_Control_4	Charger Control 4	Go
1Ah	REG0x1A_Charger_Control_5	Charger Control 5	Go
1Bh	REG0x1B_NTC_Control_0	NTC Control 0	Go
1Ch	REG0x1C_NTC_Control_1	NTC Control 1	Go
1Dh	REG0x1D_NTC_Control_2	NTC Control 2	Go
1Eh	REG0x1E_NTC_Control_3	NTC Control 3	Go
1Fh	REG0x1F_Charger_Status_0	Charger Status 0	Go
20h	REG0x20_Charger_Status_1	Charger Status 1	Go
21h	REG0x21_Charger_Status_2	Charger Status 2	Go
22h	REG0x22_FAULT_Status	FAULT Status	Go
23h	REG0x23_Charger_Flag_0	Charger Flag 0	Go
24h	REG0x24_Charger_Flag_1	Charger Flag 1	Go
25h	REG0x25_FAULT_Flag	FAULT Flag	Go
26h	REG0x26_Charger_Mask_0	Charger Mask 0	Go
27h	REG0x27_Charger_Mask_1	Charger Mask 1	Go
28h	REG0x28_FAULT_Mask	FAULT Mask	Go
29h	REG0x29_ICO_Current_Limit	ICO Current Limit	Go
2Bh	REG0x2B_ADC_Control	ADC Control	Go
2Ch	REG0x2C_ADC_Channel_Disable_1	ADC Channel Disable 1	Go

Table 8-7. BQ25630 Registers (continued)

Address	Acronym	Register Name	Section
2Dh	REG0x2D_ADC_Channel_Disable_2	ADC Channel Disable 2	Go
2Eh	REG0x2E_CC1_ADC	CC1 ADC	Go
30h	REG0x30_CC2_ADC	CC2 ADC	Go
32h	REG0x32_IBUS_ADC	IBUS ADC	Go
34h	REG0x34_IBAT_ADC	IBAT ADC	Go
36h	REG0x36_VBUS_ADC	VBUS ADC	Go
38h	REG0x38_VPMID_ADC	VPMID ADC	Go
3Ah	REG0x3A_VBAT_ADC	VBAT ADC	Go
3Ch	REG0x3C_VSYS_ADC	VSYS ADC	Go
3Eh	REG0x3E_TS_ADC	TS ADC	Go
40h	REG0x40_TDIE_ADC	TDIE ADC	Go
44h	REG0x44_USB_C_Control_0	USB C Control 0	Go
45h	REG0x45_USB_C_Control_1	USB C Control 1	Go
46h	REG0x46_Liquid_Control_0	Liquid Control 0	Go
47h	REG0x47_Liquid_Control_1	Liquid Control 1	Go
48h	REG0x48_USB_C_Information_0	USB C Information 0	Go
49h	REG0x49_USB_C_Information_1	USB C Information 1	Go
4Ah	REG0x4A_USB_DAC_Control_0	USB DAC Control 0	Go
4Bh	REG0x4B_USB_DAC_Control_1	USB DAC Control 1	Go
4Ch	REG0x4C_API_Control	API Control	Go
4Dh	REG0x4D_Part_Information	Part Information	Go

Complex bit access types are encoded to fit into small table cells. Table 8-8 shows the codes that are used for access types in this section.

Table 8-8. BQ25630 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.1 REG0x02_Charge_Current_Limit Register (Address = 2h) [Reset = 0640h]

REG0x02_Charge_Current_Limit is shown in Figure 8-20 and described in Table 8-9.

Return to the Summary Table.

Figure 8-20. REG0x02_Charge_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED				ICHG			
R-0h				R/W-64h			
7	6	5	4	3	2	1	0
ICHG				RESERVED			
R/W-64h				R-0h			

Figure 8-20. REG0x02_Charge_Current_Limit Register (continued)

Table 8-9. REG0x02_Charge_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:4	ICHG	R/W	64h	This 16-bit register follows the little-endian convention. Watchdog Timer expiration sets ICHG to 1/2 its previous value (rounded down) Reset by: REG_RESET WATCHDOG	Charge Current Regulation Limit: NOTE: When Q4_FULLON=1, this register has a minimum value of 320mA POR: 2000mA (64h) Range: 80mA-5040mA (4h-FCh) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0h		Reserved

8.6.2.2 REG0x04_Charge_Voltage_Limit Register (Address = 4h) [Reset = 0D20h]

REG0x04_Charge_Voltage_Limit is shown in Figure 8-21 and described in Table 8-10.

Return to the Summary Table.

Figure 8-21. REG0x04_Charge_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED				VREG			
R-0h				R/W-1A4h			
7	6	5	4	3	2	1	0
VREG					RESERVED		
R/W-1A4h					R-0h		

Table 8-10. REG0x04_Charge_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:3	VREG	R/W	1A4h	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Battery Voltage Regulation Limit: POR: 4200mV (1A4h) Range: 3500mV-4800mV (15Eh-1E0h) Clamped Low Clamped High Bit Step: 10mV
2:0	RESERVED	R	0h		Reserved

8.6.2.3 REG0x06_Input_Current_Limit Register (Address = 6h) [Reset = 0A00h]

REG0x06_Input_Current_Limit is shown in Figure 8-22 and described in Table 8-11.

Return to the Summary Table.

Figure 8-22. REG0x06_Input_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED				IINDPM			
R-0h				R/W-140h			
7	6	5	4	3	2	1	0
IINDPM					RESERVED		
R/W-140h					R-0h		

Table 8-11. REG0x06_Input_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:3	IINDPM	R/W	140h	This 16-bit register follows the little-endian convention Reset by: REG_RESET Adapter Unplug	Input Current Regulation Limit: Based on Detection results: USB SDP/USB C Default/Unknown Adapter = 500mA USB CDP/USB C Medium = 1.5A USB C High = 3A USB DCP = 3.2A Non-Standard Adapter = 1A/2A/2.1A/2.4A POR: 3200mA (140h) Range: 100mA-3200mA (Ah-140h) Clamped Low Clamped High Bit Step: 10mA
2:0	RESERVED	R	0h		Reserved

8.6.2.4 REG0x08_Input_Voltage_Limit Register (Address = 8h) [Reset = 0DC0h]

REG0x08_Input_Voltage_Limit is shown in Figure 8-23 and described in Table 8-12.

Return to the Summary Table.

Figure 8-23. REG0x08_Input_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED				VINDPM			
R-0h				R/W-6Eh			
7	6	5	4	3	2	1	0
VINDPM				RESERVED			
R/W-6Eh				R-0h			

Table 8-12. REG0x08_Input_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:14	RESERVED	R	0h		Reserved
13:5	VINDPM	R/W	6Eh	This 16-bit register follows the little-endian convention	Absolute Input Voltage Regulation Limit: POR: 4400mV (6Eh) Range: 3800mV-16800mV (5Fh-1A4h) Clamped Low Clamped High Bit Step: 40mV
4:0	RESERVED	R	0h		Reserved

8.6.2.5 REG0x0A_IOTG_regulation Register (Address = Ah) [Reset = 04B0h]

REG0x0A_IOTG_regulation is shown in Figure 8-24 and described in Table 8-13.

Return to the Summary Table.

Figure 8-24. REG0x0A_IOTG_regulation Register

15	14	13	12	11	10	9	8
RESERVED				IOTG			
R-0h				R/W-96h			
7	6	5	4	3	2	1	0
IOTG				RESERVED			
R/W-96h				R-0h			

Table 8-13. REG0x0A_IOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:3	IOTG	R/W	96h	This 16-bit register follows the little-endian convention Reset by: REG_RESET WATCHDOG	OTG mode current regulation limit: POR: 1500mA (96h) Range: 100mA-3200mA (Ah-140h) Clamped Low Clamped High Bit Step: 10mA
2:0	RESERVED	R	0h		Reserved

8.6.2.6 REG0x0C_VOTG_regulation Register (Address = Ch) [Reset = 0FF0h]

REG0x0C_VOTG_regulation is shown in Figure 8-25 and described in Table 8-14.

Return to the Summary Table.

Figure 8-25. REG0x0C_VOTG_regulation Register

15	14	13	12	11	10	9	8
RESERVED			VOTG				
R-0h			R/W-FFh				
7	6	5	4	3	2	1	0
VOTG				RESERVED			
R/W-FFh				R-0h			

Table 8-14. REG0x0C_VOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:13	RESERVED	R	0h		Reserved
12:4	VOTG	R/W	FFh	This 16-bit register follows the little-endian convention Reset by: REG_RESET	OTG mode regulation voltage: POR: 5100mV (FFh) Range: 3840mV-9600mV (C0h-1E0h) Clamped Low Clamped High Bit Step: 20mV
3:0	RESERVED	R	0h		Reserved

8.6.2.7 REG0x0E_Minimal_System_Voltage Register (Address = Eh) [Reset = 0B00h]

REG0x0E_Minimal_System_Voltage is shown in Figure 8-26 and described in Table 8-15.

Return to the Summary Table.

Figure 8-26. REG0x0E_Minimal_System_Voltage Register

15	14	13	12	11	10	9	8
RESERVED				VSYSMIN			
R-0h				R/W-2Ch			
7	6	5	4	3	2	1	0
VSYSMIN		RESERVED					
R/W-2Ch		R-0h					

Table 8-15. REG0x0E_Minimal_System_Voltage Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved

Table 8-15. REG0x0E_Minimal_System_Voltage Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
11:6	VSYSMIN	R/W	2Ch	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Minimal System Voltage: POR: 3520mV (2Ch) Range: 2560mV-4000mV (20h-32h) Clamped Low Clamped High Bit Step: 80mV
5:0	RESERVED	R	0h		Reserved

8.6.2.8 REG0x10_Precharge_Control Register (Address = 10h) [Reset = 00A0h]

REG0x10_Precharge_Control is shown in Figure 8-27 and described in Table 8-16.

Return to the Summary Table.

Figure 8-27. REG0x10_Precharge_Control Register

15	14	13	12	11	10	9	8
RESERVED						IPRECHG	
R-0h						R/W-Ah	
7	6	5	4	3	2	1	0
IPRECHG				RESERVED			
R/W-Ah				R-0h			

Table 8-16. REG0x10_Precharge_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:10	RESERVED	R	0h		Reserved
9:4	IPRECHG	R/W	Ah	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Pre-charge current regulation limit: NOTE: When Q4_FULLON=1, this register has a minimum value of 320mA POR: 200mA (Ah) Range: 40mA-1000mA (2h-32h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0h		Reserved

8.6.2.9 REG0x12_Termination_Control Register (Address = 12h) [Reset = 00A0h]

REG0x12_Termination_Control is shown in Figure 8-28 and described in Table 8-17.

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Figure 8-28. REG0x12_Termination_Control Register

15	14	13	12	11	10	9	8
RESERVED						ITERM	
R-0h						R/W-14h	
7	6	5	4	3	2	1	0
ITERM					RESERVED		
R/W-14h					R-0h		

Table 8-17. REG0x12_Termination_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:10	RESERVED	R	0h		Reserved

Table 8-17. REG0x12_Termination_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
9:3	ITERM	R/W	14h	Reset by: REG_RESET	Termination Current Threshold: NOTE: When Q4_FULLON=1, this register has a minimum value of 240mA POR: 200mA (14h) Range: 30mA-1000mA (3h-64h) Clamped Low Clamped High Bit Step: 10mA
2:0	RESERVED	R	0h		Reserved

8.6.2.10 REG0x14_Charge_Timer_Control Register (Address = 14h) [Reset = 9Ch]

REG0x14_Charge_Timer_Control is shown in Figure 8-29 and described in Table 8-18.

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Figure 8-29. REG0x14_Charge_Timer_Control Register

7	6	5	4	3	2	1	0
RESERVED	SYS_RESET	RESERVED	PFM_TERM_DIS	EN_TMR2X	EN_SAFETY_TMRS	PRECHG_TMR	CHG_TMR
R-1h	R/W-0h	R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

Table 8-18. REG0x14_Charge_Timer_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	1h		Reserved
6	SYS_RESET	R/W	0h	Reset by: REG_RESET WATCHDOG	Reset system by opening BATFET. The bit is reset to 0 after reset is complete. Also resets all registers to POR value. 0b = Disable 1b = System Reset
5	RESERVED	R	0h		Reserved
4	PFM_TERM_DIS	R/W	1h		Disables PFM when charging is near termination 0b = Enable 1b = Disable (Default)
3	EN_TMR2X	R/W	1h	Reset by: REG_RESET	2X charging timer control 0b = Trickle charge, pre-charge and fast charge timer not slowed by 2X during input DPM or thermal regulation. 1b = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default)
2	EN_SAFETY_TMRS	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable fast charge, pre-charge and trickle charge timers 0b = Disable 1b = Enable (default)
1	PRECHG_TMR	R/W	0h	Reset by: REG_RESET	Pre-charge safety timer setting 0b = 2 hrs (default) 1b = 0.5 hrs
0	CHG_TMR	R/W	0h	Reset by: REG_RESET	Fast charge safety timer setting 0b = 12 hrs (default) 1b = 24 hrs

8.6.2.11 REG0x15_Charger_Control_0 Register (Address = 15h) [Reset = 26h]

REG0x15_Charger_Control_0 is shown in Figure 8-30 and described in Table 8-19.

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Figure 8-30. REG0x15_Charger_Control_0 Register

7	6	5	4	3	2	1	0
Q1_FULLON	Q4_FULLON	ITRICKLE	TOPOFF_TMR		EN_TERM	VINDPM_BAT_TRACK	VRECHG
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h

Table 8-19. REG0x15_Charger_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	Q1_FULLON	R/W	0h		Forces RBFET (Q1) into low resistance state (15 mOhm), regardless of IINDPM setting. 0b = RBFET RDSON determined by IINDPM setting 1b = RBFET RDSON is always 15 mOhm
6	Q4_FULLON	R/W	0h		Forces BATFET (Q4) into low resistance state (7 mOhm), regardless of ICHG setting. 0b = BATFET RDSON determined by charge current 1b = BATFET RDSON is always 7 mOhm
5	ITRICKLE	R/W	1h	When Q4_FULLON, this setting is forced to 80mA Reset by: REG_RESET	Trickle charging current setting: 0b = 20mA 1b = 80mA
4:3	TOPOFF_TMR	R/W	0h	Reset by: REG_RESET	Top-off timer control: 00b = Disabled (default) 01b = 15 mins 10b = 30 mins 11b = 45 mins
2	EN_TERM	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable termination 0b = Disable 1b = Enable (default)
1	VINDPM_BAT_TRACK	R/W	1h	Reset by: REG_RESET	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of the VINDPM register value and VBAT + VINDPM_BAT_TRACK. 0b = Disable function (VINDPM set by register) 1b = VBAT + 200mV (default)
0	VRECHG	R/W	0h	Reset by: REG_RESET	Battery Recharge Threshold Offset (Below VREG) 0b = 100mV (default) 1b = 200mV

8.6.2.12 REG0x16_Charger_Control_1 Register (Address = 16h) [Reset = A1h]

REG0x16_Charger_Control_1 is shown in Figure 8-31 and described in Table 8-20.

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Figure 8-31. REG0x16_Charger_Control_1 Register

7	6	5	4	3	2	1	0
EN_AUTO_IBAT_DSCHG	FORCE_IBAT_DSCHG	EN_CHG	EN_HIZ	FORCE_PMID_DSCHG	WD_RST	WATCHDOG	
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	

Table 8-20. REG0x16_Charger_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_AUTO_IBAT_DSCHG	R/W	1h	Reset by: REG_RESET	Enable the auto battery discharging during the battery OVP fault 0b = The charger will NOT apply a discharging current on BAT during battery OVP triggered 1b = The charger will apply a discharging current on BAT during battery OVP triggered (default)
6	FORCE_IBAT_DSCHG	R/W	0h	Reset by: REG_RESET WATCHDOG	Enable BAT pull down current source 0b = Disable 1b = Enable
5	EN_CHG	R/W	1h	Reset by: REG_RESET WATCHDOG	Charger enable configuration 0b = Charge Disable 1b = Charge Enable (default)
4	EN_HIZ	R/W	0h	Reset by: REG_RESET WATCHDOG Adapter Plug In Adapter Unplug	Enable HIZ mode. This bit will be reset to 0, when the adapter is plugged in at VBUS. 0b = Disable (default) 1b = Enable
3	FORCE_PMID_DSCHG	R/W	0h	Reset by: REG_RESET WATCHDOG	Enable PMID pull down current source 0b = Disable 1b = Enable
2	WD_RST	R/W	0h	Reset by: REG_RESET	I2C watchdog timer reset 0b = Normal (default) 1b = Reset (this bit goes back to 0 after timer reset)
1:0	WATCHDOG	R/W	1h	Reset by: REG_RESET	Watchdog timer setting 00b = Disable 01b = 40s (default) 10b = 80s 11b = 160s

8.6.2.13 REG0x17_Charger_Control_2 Register (Address = 17h) [Reset = 4Fh]

REG0x17_Charger_Control_2 is shown in Figure 8-32 and described in Table 8-21.

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Figure 8-32. REG0x17_Charger_Control_2 Register

7	6	5	4	3	2	1	0
REG_RST	TREG	EN_DITHER		RESERVED			VBUS_OVP
R/W-0h	R/W-1h	R/W-0h		R-7h			R/W-1h

Table 8-21. REG0x17_Charger_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	REG_RST	R/W	0h		Reset registers to default values and reset timer Value resets to 0 after reset completes. 0b = Not reset (default) 1b = Reset
6	TREG	R/W	1h	Reset by: REG_RESET	Thermal regulation thresholds. 0b = 60°C 1b = 120°C (Default)

Table 8-21. REG0x17_Charger_Control_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
5:4	EN_DITHER	R/W	0h	Reset by: REG_RESET	Frequency Dither configuration: 00b = Disable (Default) 01b = 1X 10b = 2X 11b = 3X
3:1	RESERVED	R	7h		Reserved
0	VBUS_OVP	R/W	1h	Reset by: REG_RESET	Set VBUS overvoltage protection threshold 0b = 6.5V 1b = 18.5V (Default)

8.6.2.14 REG0x18_Charger_Control_3 Register (Address = 18h) [Reset = 04h]

REG0x18_Charger_Control_3 is shown in Figure 8-33 and described in Table 8-22.

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Figure 8-33. REG0x18_Charger_Control_3 Register

7	6	5	4	3	2	1	0
RESERVED	EN_OTG	PFM_OTG_DIS	PFM_FWD_DIS	BATFET_CTRL_WVBUS	BATFET_DLY	BATFET_CTRL	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	

Table 8-22. REG0x18_Charger_Control_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R/W	0h		Reserved
6	EN_OTG	R/W	0h	Reset by: REG_RESET WATCHDOG	OTG mode control 0b = OTG Disable (default) 1b = OTG Enable
5	PFM_OTG_DIS	R/W	0h	Reset by: REG_RESET	Disable PFM in OTG boost mode 0b = Enable (Default) 1b = Disable
4	PFM_FWD_DIS	R/W	0h	Reset by: REG_RESET	Disable PFM in forward buck mode 0b = Enable (Default) 1b = Disable
3	BATFET_CTRL_WVBUS	R/W	0h		Start system power reset with or without adapter present. 0b = Start system power reset after adapter is removed from VBUS. (default) 1b = Start system power reset whether or not adapter is present on VBUS.
2	BATFET_DLY	R/W	1h	Reset by: REG_RESET	Delay time added to the taking action in bits [1:0] of the BATFET_CTRL 0b = Add 20ms delay 1b = Add 10s delay (Default)
1:0	BATFET_CTRL	R/W	0h	Reset by: REG_RESET	BATFET control The control logic of the BATFET to force the device enter different modes. 00b = Idle 01b = Shutdown Mode 10b = Ship Mode 11b = Standby Mode

8.6.2.15 REG0x19_Charger_Control_4 Register (Address = 19h) [Reset = 81h]

REG0x19_Charger_Control_4 is shown in Figure 8-34 and described in Table 8-23.

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Figure 8-34. REG0x19_Charger_Control_4 Register

7	6	5	4	3	2	1	0
IBAT_PK		VBAT_UVLO	VBAT_OTG_MIN		EN_OOA	FORCE_ICO	EN_ICO
R/W-2h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

Table 8-23. REG0x19_Charger_Control_4 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	IBAT_PK	R/W	2h	Reset by: REG_RESET	Battery discharging over current protection threshold setting 00b = 3A 01b = 6A 10b = 9A (Default) 11b = RESERVED
5	VBAT_UVLO	R/W	0h	Reset by: REG_RESET	Select the VBAT UVLO falling thresholds 0b = 2.2V (default) 1b = 1.8V
4:3	VBAT_OTG_MIN	R/W	0h	Reset by: REG_RESET	Select the minimal battery voltage to start the OTG mode 00b = 3.2V rising / 3.0V falling (default) 01b = 3.0V rising / 2.8V falling 10b = 2.8V rising / 2.6V falling 11b = 2.6V rising / 2.4V falling
2	EN_OOA	R/W	0h		Out-of-Audio Enable 0b = No limit of PFM burst frequency 1b = Set minimum PFM burst frequency to above 25kHz to avoid audible noise
1	FORCE_ICO	R/W	0h	Reset by: REG_RESET WATCHDOG	Force Start Input Current Optimizer (ICO): Note: This bit can only be set and always returns to 0 after ICO starts. This bit is only valid when EN_ICO = 1 0b = Do not force ICO 1b = Force ICO start
0	EN_ICO	R/W	1h	Reset by: REG_RESET	Input Current Optimization (ICO) Algorithm Control: 0b = Disable ICO 1b = Enable ICO (Default)

8.6.2.16 REG0x1A_Charger_Control_5 Register (Address = 1Ah) [Reset = 00h]

REG0x1A_Charger_Control_5 is shown in Figure 8-35 and described in Table 8-24.

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Figure 8-35. REG0x1A_Charger_Control_5 Register

7	6	5	4	3	2	1	0
PG_TH			TQON_RST	TSTANDBY_EXIT	FORCE_ISYS_DSCHG	BATLOWV	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 8-24. REG0x1A_Charger_Control_5 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:5	PG_TH	R/W	0h	Reset by: REG_RESET Adapter Unplug	Programmable PG indicator falling threshold: 000b = 3.7V (Default) 001b = 7.4V 010b = 8V 011b = 10.4V 100b = 11V 101b = 13.4V 110b = 14V 111b = Reserved
4	TQON_RST	R/W	0h		System Reset (tQON_RST) control: 0b = 10s (Default) 1b = 18s
3	TSTANDBY_EXIT	R/W	0h		Standby Mode exit control: 0b = 580ms (Default) 1b = 10ms
2	FORCE_ISYS_DSCHG	R/W	0h	Reset by: REG_RESET WATCHDOG	Enable SYS pull down current source 0b = Disable (Default) 1b = Enable
1:0	BATLOWV	R/W	0h		Battery precharge to fast-charge threshold: 00b = 3.0V (Default) 01b = 2.8V 10b = 2.7V 11b = 2.2V

8.6.2.17 REG0x1B_NTC_Control_0 Register (Address = 1Bh) [Reset = 0Fh]

REG0x1B_NTC_Control_0 is shown in Figure 8-36 and described in Table 8-25.

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Figure 8-36. REG0x1B_NTC_Control_0 Register

7	6	5	4	3	2	1	0
TS_IGNORE	CHG_RATE		TS_TH_OTG_HOT		TS_TH_OTG_COLD	TS_TH1	TS_TH6
R/W-0h	R/W-0h		R/W-1h		R/W-1h	R/W-1h	R/W-1h

Table 8-25. REG0x1B_NTC_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	TS_IGNORE	R/W	0h	Reset by: REG_RESET WATCHDOG	Ignore the TS feedback, the charger will consider the TS is always good to allow charging and OTG modes, TS_STAT always reports TS_NORMAL 0b = Not ignored (Default) 1b = Ignore
6:5	CHG_RATE	R/W	0h	Reset by: REG_RESET	The charge rate used when device is in fast-charge. Once device enters JEITA region where charge current is reduced, the resulting current is = (ICHG * foldback ratio)/CHG_RATE: 00b = 1C (Default) 01b = 2C 10b = 4C 11b = 6C

Table 8-25. REG0x1B_NTC_Control_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
4:3	TS_TH_OTG_HOT	R/W	1h	Reset by: REG_RESET	OTG Mode TS_HOT falling voltage threshold (as a percentage of REGN) to transition from normal operation into suspended OTG mode. 00b = 55°C 01b = 60°C (Default) 10b = 65°C 11b = Disable
2	TS_TH_OTG_COLD	R/W	1h	Reset by: REG_RESET	OTG Mode TS_COLD rising voltage threshold (as a percentage of REGN) to transition from normal operation into suspended OTG mode. 0b = -10°C 1b = -20°C (Default)
1	TS_TH1	R/W	1h	Reset by: REG_RESET	TS TH1 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kW and RT2=30.31kW 0b = -5°C 1b = 0°C (Default)
0	TS_TH6	R/W	1h	Reset by: REG_RESET	TS TH6 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kW and RT2=30.31kW 0b = 55°C 1b = 60°C (Default)

8.6.2.18 REG0x1C_NTC_Control_1 Register (Address = 1Ch) [Reset = 85h]

REG0x1C_NTC_Control_1 is shown in Figure 8-37 and described in Table 8-26.

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Figure 8-37. REG0x1C_NTC_Control_1 Register

7	6	5	4	3	2	1	0
TS_TH2		TS_TH3		TS_TH4		TS_TH5	
R/W-2h		R/W-0h		R/W-1h		R/W-1h	

Table 8-26. REG0x1C_NTC_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_TH2	R/W	2h	Reset by: REG_RESET	TS TH2 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kW and RT2=30.31kW 00b = 5°C 01b = 7.5°C 10b = 10°C (Default) 11b = 12.5°C
5:4	TS_TH3	R/W	0h	Reset by: REG_RESET	TS TH3 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kW and RT2=30.31kW 00b = 15°C (Default) 01b = 17.5°C 10b = 20°C 11b = 22.5°C

Table 8-26. REG0x1C_NTC_Control_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
3:2	TS_TH4	R/W	1h	Reset by: REG_RESET	TS TH4 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kW and RT2=30.31kW 00b = 32.5°C 01b = 35°C (Default) 10b = 37.5°C 11b = 40°C
1:0	TS_TH5	R/W	1h	Reset by: REG_RESET	TS TH5 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kW and RT2=30.31kW 00b = 42.5°C 01b = 45°C (Default) 10b = 47.5°C 11b = 50°C

8.6.2.19 REG0x1D_NTC_Control_2 Register (Address = 1Dh) [Reset = 7Fh]

REG0x1D_NTC_Control_2 is shown in Figure 8-38 and described in Table 8-27.

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Figure 8-38. REG0x1D_NTC_Control_2 Register

7	6	5	4	3	2	1	0
TS_VSET_WARM		TS_ISET_WARM		TS_VSET_PREWARM		TS_ISET_PREWARM	
R/W-1h		R/W-3h		R/W-3h		R/W-3h	

Table 8-27. REG0x1D_NTC_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_VSET_WARM	R/W	1h	Reset by: REG_RESET	TS_WARM (TH5 - TH6) Voltage Setting 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV (Default) 10b = Set VREG to VREG-100mV 11b = VREG unchanged
5:4	TS_ISET_WARM	R/W	3h	Reset by: REG_RESET	TS_WARM (TH5 - TH6) Current Setting 00b = Charge Suspend 01b = Set ICHG to TS_ISET_SEL (20% or 60%) 10b = Set ICHG to 40% 11b = ICHG unchanged (Default)
3:2	TS_VSET_PREWARM	R/W	3h	Reset by: REG_RESET	TS_PREWARM (TH4 - TH5) Voltage Setting 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV 10b = Set VREG to VREG-100mV 11b = VREG unchanged (Default)
1:0	TS_ISET_PREWARM	R/W	3h	Reset by: REG_RESET	TS_PREWARM (TH4 - TH5) Current Setting 00b = Charge Suspend 01b = Set ICHG to TS_ISET_SEL (20% or 60%) 10b = Set ICHG to 40% 11b = ICHG unchanged (Default)

8.6.2.20 REG0x1E_NTC_Control_3 Register (Address = 1Eh) [Reset = DFh]

REG0x1E_NTC_Control_3 is shown in Figure 8-39 and described in Table 8-28.

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Figure 8-39. REG0x1E_NTC_Control_3 Register

7	6	5	4	3	2	1	0
TS_VSET_COOL		TS_ISET_COOL		TS_VSET_PRECOOL		TS_ISET_PRECOOL	
R/W-3h		R/W-1h		R/W-3h		R/W-3h	

Table 8-28. REG0x1E_NTC_Control_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_VSET_COOL	R/W	3h	Reset by: REG_RESET	TS_COOL (TH1 - TH2) Voltage Setting 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV 10b = Set VREG to VREG-100mV 11b = VREG unchanged (Default)
5:4	TS_ISET_COOL	R/W	1h	Reset by: REG_RESET	TS_COOL (TH1 - TH2) Current Setting 00b = Charge Suspend 01b = Set ICHG to TS_ISET_SEL (20% or 60%) (Default) 10b = Set ICHG to 40% 11b = ICHG unchanged
3:2	TS_VSET_PRECOOL	R/W	3h	Reset by: REG_RESET	TS_PRECOOL (TH2 - TH3) Voltage Setting: 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV 10b = Set VREG to VREG-100mV 11b = VREG unchanged (Default)
1:0	TS_ISET_PRECOOL	R/W	3h	Reset by: REG_RESET	TS_PRECOOL (TH2 - TH3) Current Setting: 00b = Charge Suspend 01b = Set ICHG to TS_ISET_SEL (20% or 60%) 10b = Set ICHG to 40% 11b = ICHG unchanged (Default)

8.6.2.21 REG0x1F_Charger_Status_0 Register (Address = 1Fh) [Reset = 00h]

REG0x1F_Charger_Status_0 is shown in Figure 8-40 and described in Table 8-29.

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Figure 8-40. REG0x1F_Charger_Status_0 Register

7	6	5	4	3	2	1	0
PG_STAT	ADC_DONE_STAT	TREG_STAT	VSYS_STAT	IINDPM_STAT	VINDPM_STAT	SAFETY_TMR_STAT	WD_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-29. REG0x1F_Charger_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG_STAT	R	0h	Power Good Indicator Status: 0b = VBUS below PG_TH 1b = VBUS above PG_TH
6	ADC_DONE_STAT	R	0h	ADC Conversion Status (in one-shot mode only) Note: Always reads 0 in continuous mode 0b = Conversion not complete 1b = Conversion complete
5	TREG_STAT	R	0h	IC Thermal regulation status 0b = Normal 1b = Device in thermal regulation
4	VSYS_STAT	R	0h	VSYS Regulation Status (forward mode) 0b = Not in VSYSMIN regulation (BAT>VSYSMIN) 1b = In VSYSMIN regulation (BAT<VSYSMIN)

Table 8-29. REG0x1F_Charger_Status_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	IINDPM_STAT	R	0h	IINDPM status (forward mode) or IOTG status (OTG mode) 0b = Normal 1b = In IINDPM regulation or IOTG regulation
2	VINDPM_STAT	R	0h	VINDPM status (forward mode) or VOTG status (OTG mode, backup mode) 0b = Normal 1b = In VINDPM regulation or VOTG regualtion
1	SAFETY_TMR_STAT	R	0h	Fast charge, trickle charge and pre-charge timer status 0b = Normal 1b = Safety timer expired
0	WD_STAT	R	0h	I2C watch dog timer status 0b = Normal 1b = WD timer expired

8.6.2.22 REG0x20_Charger_Status_1 Register (Address = 20h) [Reset = 00h]

REG0x20_Charger_Status_1 is shown in Figure 8-41 and described in Table 8-30.

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Figure 8-41. REG0x20_Charger_Status_1 Register

7	6	5	4	3	2	1	0
ICO_STAT		CHG_STAT			LOW_PWR_ADP_STAT	RESERVED	VBAT_OTG_STAT
R-0h		R-0h			R-0h	R-0h	R-0h

Table 8-30. REG0x20_Charger_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	ICO_STAT	R	0h	Input Current Optimizer (ICO) Status: 00b = ICO Disabled 01b = ICO Optimization in Progress 10b = Maximum input current detected 11b = ICO Routine Suspended
5:3	CHG_STAT	R	0h	Charge Status: 000b = Not Charging 001b = Trickle Charge 010b = Pre-charge 011b = Fast Charge (CC) 100b = Taper Charge (CV) 101b = Reserved 110b = Top-off Timer Active Charging 111b = Charge Termination Done
2	LOW_PWR_ADP_STAT	R	0h	Low Power Adapter Status. Adapter current capability may be too low to charge battery. Consider entering API mode when this status is set. 0b = Adapter Power is Normal 1b = Adapter Power is Low
1	RESERVED	R	0h	Reserved
0	VBAT_OTG_STAT	R	0h	VBAT OTG Status 0b = Normal 1b = VBAT below VBAT_OTG_MIN

8.6.2.23 REG0x21_Charger_Status_2 Register (Address = 21h) [Reset = 00h]

REG0x21_Charger_Status_2 is shown in Figure 8-42 and described in Table 8-31.

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Figure 8-42. REG0x21_Charger_Status_2 Register

7	6	5	4	3	2	1	0
VBUS_STAT				RESERVED			
R-0h				R-0h			

Table 8-31. REG0x21_Charger_Status_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	VBUS_STAT	R	0h	VBUS status: 0000b = Not powered from VBUS 0001b = USB SDP (500mA) 0010b = USB CDP (1.5A) 0011b = USB DCP (1.5A) 0100b = Unknown adaptor (3.2A or result of ICO) 0101b = Non-Standard Adapter (1A/2A/2.1A/2.4A) 0110b = HVDCP (1.5A) 0111b = In Boost OTG (Host Enabled) 1000b = USB-C Default (500mA) 1001b = USB-C Medium (1.5A) 1010b = USB-C High (3.0A) 1011b = SRC Mode (EN_OTG=0) 1100b = SRC Mode (EN_OTG=1) 1101b = In API Mode
3:0	RESERVED	R	0h	Reserved

8.6.2.24 REG0x22_FAULT_Status Register (Address = 22h) [Reset = 00h]

REG0x22_FAULT_Status is shown in Figure 8-43 and described in Table 8-32.

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Figure 8-43. REG0x22_FAULT_Status Register

7	6	5	4	3	2	1	0
VBUS_FAULT_STAT	BAT_FAULT_STAT	VSYS_FAULT_STAT	OTG_FAULT_STAT	TSHUT_STAT	TS_STAT		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		

Table 8-32. REG0x22_FAULT_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_STAT	R	0h	VBUS overvoltage status 0b = Normal 1b = Device in over voltage protection
6	BAT_FAULT_STAT	R	0h	Battery fault status 0b = Normal 1b = Dead, under-voltage, or over-voltage battery detected
5	VSYS_FAULT_STAT	R	0h	VSYS under voltage and over voltage status 0b = Normal 1b = SYS in SYS short circuit or over voltage
4	OTG_FAULT_STAT	R	0h	OTG under voltage and over voltage status. 0b = Normal 1b = Fault Detected
3	TSHUT_STAT	R	0h	IC temperature shutdown status 0b = Normal 1b = Device in thermal shutdown protection

Table 8-32. REG0x22_FAULT_Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	TS_STAT	R	0h	The TS temperature zone. 000b = TS_NORMAL 001b = TS_COLD or TS_OTG_COLD 010b = TS_HOT or TS_OTG_HOT 011b = TS_COOL 100b = TS_WARM 101b = TS_PRECOOL 110b = TS_PREWARM 111b = RESERVED

8.6.2.25 REG0x23_Charger_Flag_0 Register (Address = 23h) [Reset = 00h]

REG0x23_Charger_Flag_0 is shown in Figure 8-44 and described in Table 8-33.

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Figure 8-44. REG0x23_Charger_Flag_0 Register

7	6	5	4	3	2	1	0
PG_FLAG	ADC_DONE_FLAG	TREG_FLAG	VSYS_FLAG	IINDPM_FLAG	VINDPM_FLAG	SAFETY_TMR_FLAG	WD_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-33. REG0x23_Charger_Flag_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG_FLAG	R	0h	Power Good indicator flag: Access: R (ClearOnRead) 0b = Normal 1b = PG status changed
6	ADC_DONE_FLAG	R	0h	ADC conversion flag (only in one-shot mode) Access: R (ClearOnRead) 0b = Conversion not completed 1b = Conversion completed
5	TREG_FLAG	R	0h	IC Thermal regulation flag Access: R (ClearOnRead) 0b = Normal 1b = TREG signal rising threshold detected
4	VSYS_FLAG	R	0h	VSYS min regulation flag Access: R (ClearOnRead) 0b = Normal 1b = Entered or exited VSYS min regulation
3	IINDPM_FLAG	R	0h	IINDPM or IOTG flag Access: R (ClearOnRead) 0b = Normal 1b = IINDPM signal rising edge detected
2	VINDPM_FLAG	R	0h	VINDPM or VOTG flag Access: R (ClearOnRead) 0b = Normal 1b = VINDPM regulation signal rising edge detected
1	SAFETY_TMR_FLAG	R	0h	Fast charge, trickle charge and pre-charge timer flag Access: R (ClearOnRead) 0b = Normal 1b = Fast charging timer expired rising edge detected

Table 8-33. REG0x23_Charger_Flag_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WD_FLAG	R	0h	I2C watchdog timer flag Access: R (ClearOnRead) 0b = Normal 1b = WD timer signal rising edge detected

8.6.2.26 REG0x24_Charger_Flag_1 Register (Address = 24h) [Reset = 00h]

REG0x24_Charger_Flag_1 is shown in Figure 8-45 and described in Table 8-34.

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Figure 8-45. REG0x24_Charger_Flag_1 Register

7	6	5	4	3	2	1	0
VBUS_FLAG	ICO_FLAG	LOW_PWR_ADP_FLAG	CC_ORIENT_FLAG	CHG_FLAG	CC2_FLAG	CC1_FLAG	VBAT_OTG_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-34. REG0x24_Charger_Flag_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FLAG	R	0h	VBUS status flag Access: R (ClearOnRead) 0b = Normal 1b = VBUS status changed
6	ICO_FLAG	R	0h	Input Current Optimizer (ICO) flag Access: R (ClearOnRead) 0b = Normal 1b = ICO_STAT[1:0] changed (transition to any state)
5	LOW_PWR_ADP_FLAG	R	0h	Low Power Adapter Flag: 0b = Normal 1b = Low power adapter status detected
4	CC_ORIENT_FLAG	R	0h	CC Orientation Flag Access: R (ClearOnRead) 0b = Normal 1b = CC orientation detected
3	CHG_FLAG	R	0h	Charge status flag Access: R (ClearOnRead) 0b = Normal 1b = Charge status changed
2	CC2_FLAG	R	0h	CC2 status flag Access: R (ClearOnRead) 0b = Normal 1b = CC2 status changed
1	CC1_FLAG	R	0h	CC1 status flag Access: R (ClearOnRead) 0b = Normal 1b = CC1 status changed
0	VBAT_OTG_FLAG	R	0h	VBAT below VBAT_OTG_MIN flag Access: R (ClearOnRead) 0b = Normal 1b = VBAT dropped below VBAT_OTG_MIN

8.6.2.27 REG0x25_FAULT_Flag Register (Address = 25h) [Reset = 00h]

REG0x25_FAULT_Flag is shown in Figure 8-46 and described in Table 8-35.

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Figure 8-46. REG0x25_FAULT_Flag Register

7	6	5	4	3	2	1	0
VBUS_FAULT_FLAG	BAT_FAULT_FLAG	VSYS_FAULT_FLAG	OTG_FAULT_FLAG	TSHUT_FLAG	CC_FAULT_FLAG	LQD_FLAG	TS_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-35. REG0x25_FAULT_Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_FLAG	R	0h	VBUS over-voltage flag Access: R (ClearOnRead) 0b = Normal 1b = Entered VBUS OVP
6	BAT_FAULT_FLAG	R	0h	VBAT over-voltage flag Access: R (ClearOnRead) 0b = Normal 1b = Entered VBAT OVP
5	VSYS_FAULT_FLAG	R	0h	VSYS over voltage and SYS short flag Access: R (ClearOnRead) 0b = Normal 1b = Stopped switching due to system over-voltage or SYS short fault
4	OTG_FAULT_FLAG	R	0h	OTG under voltage and over voltage flag Access: R (ClearOnRead) 0b = Normal 1b = Stopped OTG due to VBUS under voltage or over voltage fault
3	TSHUT_FLAG	R	0h	IC thermal shutdown flag Access: R (ClearOnRead) 0b = Normal 1b = TS shutdown signal rising threshold detected
2	CC_FAULT_FLAG	R	0h	USB-C CC1/CC2 short to VBUS fault flag Access: R (ClearOnRead) 0b = Normal 1b = CC1 or CC2 shorted to VBUS
1	LQD_FLAG	R	0h	Liquid detection flag Access: R (ClearOnRead) 0b = Normal 1b = Liquid detected
0	TS_FLAG	R	0h	TS status flag Access: R (ClearOnRead) 0b = Normal 1b = A change to TS status was detected

8.6.2.28 REG0x26_Charger_Mask_0 Register (Address = 26h) [Reset = 00h]

REG0x26_Charger_Mask_0 is shown in Figure 8-47 and described in Table 8-36.

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Figure 8-47. REG0x26_Charger_Mask_0 Register

7	6	5	4	3	2	1	0
PG_MASK	ADC_DONE_MASK	TREG_MASK	VSYS_MASK	IINDPM_MASK	VINDPM_MASK	SAFETY_TMR_MASK	WD_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Figure 8-47. REG0x26_Charger_Mask_0 Register (continued)

Table 8-36. REG0x26_Charger_Mask_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_MASK	R/W	0h	Reset by: REG_RESET	Power Good indicator INT mask 0b = PG status change does produce INT pulse 1b = PG status change does not produce INT pulse
6	ADC_DONE_MASK	R/W	0h	Reset by: REG_RESET	ADC conversion INT mask (only in one-shot mode) 0b = ADC conversion done does produce INT pulse 1b = ADC conversion done does not produce INT pulse
5	TREG_MASK	R/W	0h	Reset by: REG_RESET	IC thermal regulation INT mask 0b = Entering TREG does produce INT 1b = Entering TREG does not produce INT
4	VSYS_MASK	R/W	0h	Reset by: REG_RESET	VSYS min regulation INT mask 0b = Enter or exit VSYSMIN regulation does produce INT pulse 1b = Enter or exit VSYSMIN regulation does not produce INT pulse
3	IINDPM_MASK	R/W	0h	Reset by: REG_RESET	IINDPM or IOTG INT mask 0b = Enter IINDPM or IOTG does produce INT pulse 1b = Enter IINDPM or IOTG does not produce INT pulse
2	VINDPM_MASK	R/W	0h	Reset by: REG_RESET	VINDPM or VOTG INT mask 0b = Enter VINDPM does produce INT pulse 1b = Enter VINDPM does not produce INT pulse
1	SAFETY_TMR_MASK	R/W	0h	Reset by: REG_RESET	Fast charge, trickle charge and pre-charge timer INT mask 0b = Fast charge, trickle charge or pre-charge timer expiration does produce INT 1b = Fast charge, trickle charge or pre-charge timer expiration does not produce INT
0	WD_MASK	R/W	0h	Reset by: REG_RESET	I2C watch dog timer INT mask 0b = I2C watch dog timer expired does produce INT pulse 1b = I2C watch dog timer expired does not produce INT pulse

8.6.2.29 REG0x27_Charger_Mask_1 Register (Address = 27h) [Reset = 20h]

REG0x27_Charger_Mask_1 is shown in Figure 8-48 and described in Table 8-37.

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Figure 8-48. REG0x27_Charger_Mask_1 Register

7	6	5	4	3	2	1	0
VBUS_MASK	ICO_MASK	LOW_PWR_ADP_MASK	CC_ORIENT_MASK	CHG_MASK	CC2_MASK	CC1_MASK	VBAT_OTG_MASK
R/W-0h	R/W-0h	R-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-37. REG0x27_Charger_Mask_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VBUS_MASK	R/W	0h	Reset by: REG_RESET	VBUS status INT mask 0b = VBUS status change does produce INT 1b = VBUS status change does not produce INT

Table 8-37. REG0x27_Charger_Mask_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
6	ICO_MASK	R/W	0h	Reset by: REG_RESET	Input Current Optimizer (ICO) INT mask 0b = ICO_STAT change does produce INT 1b = ICO_STAT change does not produce INT
5	LOW_PWR_ADP_MASK	R	1h	Reset by: REG_RESET	Low Power Adapter mask 0b = Low Power Adapter status does produce INT 1b = Low Power Adapter status does not produce INT
4	CC_ORIENT_MASK	R/W	0h	Reset by: REG_RESET	CC Orientation Mask 0b = CC Orientation status change does produce INT 1b = CC Orientation status change does not produce INT
3	CHG_MASK	R/W	0h	Reset by: REG_RESET	Charge status INT mask 0b = Charging status change does produce INT 1b = Charging status change does not produce INT
2	CC2_MASK	R/W	0h	Reset by: REG_RESET	CC2 status mask 0b = CC2 status change does produce INT 1b = CC2 status change does not produce INT
1	CC1_MASK	R/W	0h	Reset by: REG_RESET	CC1 status mask 0b = CC1 status change does produce INT 1b = CC1 status change does not produce INT
0	VBAT_OTG_MASK	R/W	0h	Reset by: REG_RESET	VBAT below VBAT_OTG_MIN mask 0b = VBAT below VBAT_OTG_MIN does produce INT 1b = VBAT below VBAT_OTG_MIN does not produce INT

8.6.2.30 REG0x28_FAULT_Mask Register (Address = 28h) [Reset = 00h]

REG0x28_FAULT_Mask is shown in Figure 8-49 and described in Table 8-38.

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Figure 8-49. REG0x28_FAULT_Mask Register

7	6	5	4	3	2	1	0
VBUS_FAULT_MASK	BAT_FAULT_MASK	VSYS_FAULT_MASK	OTG_FAULT_MASK	TSHUT_MASK	CC_FAULT_MASK	LQD_MASK	TS_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-38. REG0x28_FAULT_Mask Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VBUS_FAULT_MASK	R/W	0h	Reset by: REG_RESET	VBUS over-voltage INT mask 0b = Entering VBUS OVP does produce INT 1b = Entering VBUS OVP does not produce INT
6	BAT_FAULT_MASK	R/W	0h	Reset by: REG_RESET	IBAT/VBAT over-current/over-voltage INT mask 0b = Entering IBAT OCP or VBAT OVP does produce INT 1b = Entering IBAT OCP or VBAT OVP does not produce INT
5	VSYS_FAULT_MASK	R/W	0h	Reset by: REG_RESET	VSYS over voltage and SYS short INT mask 0b = System over-voltage or SYS short fault does produce INT 1b = Neither system over voltage nor SYS short fault produces INT

Table 8-38. REG0x28_FAULT_Mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
4	OTG_FAULT_MASK	R/W	0h	Reset by: REG_RESET	OTG under voltage and over voltage INT mask 0b = OTG VBUS under voltage or over voltage fault does produce INT 1b = Neither OTG VBUS under voltage nor over voltage fault produces INT
3	TSHUT_MASK	R/W	0h	Reset by: REG_RESET	IC thermal shutdown INT mask 0b = TSHUT does produce INT 1b = TSHUT does not produce INT
2	CC_FAULT_MASK	R/W	0h	Reset by: REG_RESET	USB-C CC1/CC2 short to VBUS fault mask 0b = CC_FAULT_STAT change does produce INT 1b = CC_FAULT_STAT change does not produce INT
1	LQD_MASK	R/W	0h	Reset by: REG_RESET	Liquid detection mask 0b = LQD_STAT change does produce INT 1b = LQD_STAT change does not produce INT
0	TS_MASK	R/W	0h	Reset by: REG_RESET	Temperature charging profile INT mask 0b = A change to TS temperature zone does produce INT 1b = A change to the TS temperature zone does not produce INT

8.6.2.31 REG0x29_ICO_Current_Limit Register (Address = 29h) [Reset = 0000h]

REG0x29_ICO_Current_Limit is shown in Figure 8-50 and described in Table 8-39.

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Figure 8-50. REG0x29_ICO_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED				ICO_IINDPM			
R-0h				R-0h			
7	6	5	4	3	2	1	0
ICO_IINDPM						RESERVED	
R-0h						R-0h	

Table 8-39. REG0x29_ICO_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:3	ICO_IINDPM	R	0h	This 16-bit register follows the little-endian convention Reset by: Adapter Unplug	Optimized Input Current Limit when ICO is enabled: POR: 0mA (0h) Range: 100mA-3200mA (Ah-140h) Clamped Low Clamped High Bit Step: 10mA
2:0	RESERVED	R	0h		Reserved

8.6.2.32 REG0x2B_ADC_Control Register (Address = 2Bh) [Reset = 30h]

REG0x2B_ADC_Control is shown in Figure 8-51 and described in Table 8-40.

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Figure 8-51. REG0x2B_ADC_Control Register

7	6	5	4	3	2	1	0

Figure 8-51. REG0x2B_ADC_Control Register (continued)

EN_ADC	ADC_RATE	ADC_SAMPLE	ADC_AVG	ADC_AVG_INIT	RESERVED
R/W-0h	R/W-0h	R/W-3h	R/W-0h	R/W-0h	R-0h

Table 8-40. REG0x2B_ADC_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_ADC	R/W	0h	Reset by: REG_RESET WATCHDOG	ADC Control 0b = Disable (default) 1b = Enable
6	ADC_RATE	R/W	0h	Reset by: REG_RESET	ADC conversion rate control 0b = Continuous conversion (default) 1b = One shot conversion
5:4	ADC_SAMPLE	R/W	3h	Reset by: REG_RESET	ADC sample speed 00b = 11 bit effective resolution 01b = 10 bit effective resolution 10b = 9 bit effective resolution 11b = 8 bit effective resolution (default)
3	ADC_AVG	R/W	0h	Reset by: REG_RESET	ADC average control 0b = Single value (default) 1b = Running average
2	ADC_AVG_INIT	R/W	0h	Reset by: REG_RESET	ADC average initial value control 0b = Start average using the existing register value 1b = Start average using a new ADC conversion
1:0	RESERVED	R	0h		Reserved

8.6.2.33 REG0x2C_ADC_Channel_Disable_1 Register (Address = 2Ch) [Reset = 00h]

REG0x2C_ADC_Channel_Disable_1 is shown in Figure 8-52 and described in Table 8-41.

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Figure 8-52. REG0x2C_ADC_Channel_Disable_1 Register

7	6	5	4	3	2	1	0
DIS_IBUS_ADC	DIS_IBAT_ADC	DIS_VBUS_ADC	DIS_VBAT_ADC	DIS_VSYS_ADC	DIS_TS_ADC	DIS_TDIE_ADC	DIS_VPMID_ADC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-41. REG0x2C_ADC_Channel_Disable_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	DIS_IBUS_ADC	R/W	0h	Reset by: REG_RESET	IBUS ADC channel disable 0b = Enable 1b = Disable
6	DIS_IBAT_ADC	R/W	0h	Reset by: REG_RESET	IBAT ADC control 0b = Enable 1b = Disable
5	DIS_VBUS_ADC	R/W	0h	Reset by: REG_RESET	VBUS ADC control 0b = Enable 1b = Disable
4	DIS_VBAT_ADC	R/W	0h	Reset by: REG_RESET	VBAT ADC control 0b = Enable 1b = Disable
3	DIS_VSYS_ADC	R/W	0h	Reset by: REG_RESET	VSYS ADC control 0b = Enable 1b = Disable

Table 8-41. REG0x2C_ADC_Channel_Disable_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
2	DIS_TS_ADC	R/W	0h	Reset by: REG_RESET Adapter Plug In	TS ADC control 0b = Enable 1b = Disable
1	DIS_TDIE_ADC	R/W	0h	Reset by: REG_RESET	TDIE ADC control 0b = Enable 1b = Disable
0	DIS_VPMID_ADC	R/W	0h	Reset by: REG_RESET	VPMID ADC control 0b = Enable 1b = Disable

8.6.2.34 REG0x2D_ADC_Channel_Disable_2 Register (Address = 2Dh) [Reset = 20h]

REG0x2D_ADC_Channel_Disable_2 is shown in Figure 8-53 and described in Table 8-42.

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Figure 8-53. REG0x2D_ADC_Channel_Disable_2 Register

7	6	5	4	3	2	1	0
DIS_CC1_ADC	DIS_CC2_ADC	RESERVED	RESERVED			DIS_QON_RST	RESERVED
R/W-0h	R/W-0h	R-1h	R-0h			R/W-0h	R-0h

Table 8-42. REG0x2D_ADC_Channel_Disable_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	DIS_CC1_ADC	R/W	0h	Reset by: REG_RESET	CC1 ADC control 0b = Enable 1b = Disable
6	DIS_CC2_ADC	R/W	0h	Reset by: REG_RESET	CC2 ADC control 0b = Enable 1b = Disable
5	RESERVED	R	1h		Reserved
4:2	RESERVED	R	0h		Reserved
1	DIS_QON_RST	R/W	0h	Reset by: REG_RESET	QON system reset control 0b = QON pulled low for t_QON_RST initiates system reset 1b = QON pulled low for t_QON_RST does not initiatee system reset
0	RESERVED	R	0h	Reset by: REG_RESET	

8.6.2.35 REG0x2E_CC1_ADC Register (Address = 2Eh) [Reset = 0000h]

REG0x2E_CC1_ADC is shown in Figure 8-54 and described in Table 8-43.

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Figure 8-54. REG0x2E_CC1_ADC Register

15	14	13	12	11	10	9	8
RESERVED			CC1_ADC				
R-0h			R-0h				
7	6	5	4	3	2	1	0
CC1_ADC							RESERVED
R-0h							R-0h

Figure 8-54. REG0x2E_CC1_ADC Register (continued)

Table 8-43. REG0x2E_CC1_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0h	Reserved
12:1	CC1_ADC	R	0h	CC1 ADC reading POR: 0mV(0h) Range: 0mV - 5000mV (0h-FA0h) Clamped High Bit Step: 1.25mV
0	RESERVED	R	0h	Reserved

8.6.2.36 REG0x30_CC2_ADC Register (Address = 30h) [Reset = 0000h]

REG0x30_CC2_ADC is shown in Figure 8-55 and described in Table 8-44.

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Figure 8-55. REG0x30_CC2_ADC Register

15	14	13	12	11	10	9	8
RESERVED			CC2_ADC				
R-0h			R-0h				
7	6	5	4	3	2	1	0
CC2_ADC							RESERVED
R-0h							R-0h

Table 8-44. REG0x30_CC2_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0h	Reserved
12:1	CC2_ADC	R	0h	CC2 ADC reading POR: 0mV(0h) Range: 0mV - 5000mV (0h-FA0h) Clamped High Bit Step: 1.25mV
0	RESERVED	R	0h	Reserved

8.6.2.37 REG0x32_IBUS_ADC Register (Address = 32h) [Reset = 0000h]

REG0x32_IBUS_ADC is shown in Figure 8-56 and described in Table 8-45.

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Figure 8-56. REG0x32_IBUS_ADC Register

15	14	13	12	11	10	9	8
IBUS_ADC							
R-0h							
7	6	5	4	3	2	1	0
IBUS_ADC							RESERVED
R-0h							R-0h

Table 8-45. REG0x32_IBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	IBUS_ADC	R	0h	IBUS ADC reading Reported in 2s Complement. When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value. POR: 0mA(0h) Format: 2s Complement Range: -5000mA - 5000mA (7830h-7D0h) Clamped Low Clamped High Bit Step: 2.5mA
0	RESERVED	R	0h	Reserved

8.6.2.38 REG0x34_IBAT_ADC Register (Address = 34h) [Reset = 0000h]

REG0x34_IBAT_ADC is shown in Figure 8-57 and described in Table 8-46.

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Figure 8-57. REG0x34_IBAT_ADC Register

15	14	13	12	11	10	9	8
IBAT_ADC							
R-0h							
7	6	5	4	3	2	1	0
IBAT_ADC					RESERVED		
R-0h					R-0h		

Table 8-46. REG0x34_IBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	IBAT_ADC	R	0h	IBAT ADC reading Reported in 2s Complement. The IBAT ADC reports positive value for the battery charging current, and negative value for the battery discharging current. If polarity of battery current changes from charging to discharging or vice-versa during the ADC measurement, the conversion is aborted and the register reports code 0x8000 (which is code 0x2000 for IBAT_ADC field) When Q4_FULLON bit changes, ADC is reset to all 0's and start a new conversion POR: 0mA (0h) Format: 2s Complement Range: -10000mA-5025mA (1830h-3EDh) Clamped Low Clamped High Bit Step: 5mA
2:0	RESERVED	R	0h	Reserved

8.6.2.39 REG0x36_VBUS_ADC Register (Address = 36h) [Reset = 0000h]

REG0x36_VBUS_ADC is shown in Figure 8-58 and described in Table 8-47.

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Figure 8-58. REG0x36_VBUS_ADC Register

15	14	13	12	11	10	9	8
RESERVED	VBUS_ADC						

Figure 8-58. REG0x36_VBUS_ADC Register (continued)

R-0h							R-0h
7	6	5	4	3	2	1	0
VBUS_ADC						RESERVED	
R-0h						R-0h	

Table 8-47. REG0x36_VBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14:2	VBUS_ADC	R	0h	VBUS ADC reading POR: 0mV (0h) Range: 0mV-20000mV (0h-FA0h) Clamped High Bit Step: 5mV
1:0	RESERVED	R	0h	Reserved

8.6.2.40 REG0x38_VPMID_ADC Register (Address = 38h) [Reset = 0000h]

REG0x38_VPMID_ADC is shown in Figure 8-59 and described in Table 8-48.

Return to the Summary Table.

Figure 8-59. REG0x38_VPMID_ADC Register

15	14	13	12	11	10	9	8
RESERVED	VPMID_ADC						
R-0h	R-0h						
7	6	5	4	3	2	1	0
VPMID_ADC						RESERVED	
R-0h						R-0h	

Table 8-48. REG0x38_VPMID_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14:2	VPMID_ADC	R	0h	VPMID ADC reading POR: 0mV (0h) Range: 0mV-20000mV (0h-FA0h) Clamped High Bit Step: 5mV
1:0	RESERVED	R	0h	Reserved

8.6.2.41 REG0x3A_VBAT_ADC Register (Address = 3Ah) [Reset = 0000h]

REG0x3A_VBAT_ADC is shown in Figure 8-60 and described in Table 8-49.

Return to the Summary Table.

Figure 8-60. REG0x3A_VBAT_ADC Register

15	14	13	12	11	10	9	8
RESERVED			VBAT_ADC				
R-0h			R-0h				
7	6	5	4	3	2	1	0
VBAT_ADC							RESERVED
R-0h							R-0h

Table 8-49. REG0x3A_VBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0h	Reserved
12:1	VBAT_ADC	R	0h	VBAT ADC reading POR: 0mV(0h) Range: 0mV - 5000mV (0h-FA0h) Clamped High Bit Step: 1.25mV
0	RESERVED	R	0h	Reserved

8.6.2.42 REG0x3C_VSYS_ADC Register (Address = 3Ch) [Reset = 0000h]

REG0x3C_VSYS_ADC is shown in Figure 8-61 and described in Table 8-50.

Return to the Summary Table.

Figure 8-61. REG0x3C_VSYS_ADC Register

15	14	13	12	11	10	9	8
RESERVED			VSYS_ADC				
R-0h			R-0h				
7	6	5	4	3	2	1	0
VSYS_ADC						RESERVED	
R-0h						R-0h	

Table 8-50. REG0x3C_VSYS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0h	Reserved
12:1	VSYS_ADC	R	0h	VSYS ADC reading POR: 0mV(0h) Range: 0mV - 5000mV (0h-FA0h) Clamped High Bit Step: 1.25mV
0	RESERVED	R	0h	Reserved

8.6.2.43 REG0x3E_TS_ADC Register (Address = 3Eh) [Reset = 0000h]

REG0x3E_TS_ADC is shown in Figure 8-62 and described in Table 8-51.

Return to the Summary Table.

Figure 8-62. REG0x3E_TS_ADC Register

15	14	13	12	11	10	9	8
RESERVED				TS_ADC			
R-0h				R-0h			
7	6	5	4	3	2	1	0
TS_ADC							
R-0h							

Table 8-51. REG0x3E_TS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved

Table 8-51. REG0x3E_TS_ADC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	TS_ADC	R	0h	TS ADC reading POR: 0%(0h) Range: 0% - 99.90234375% (0h-3FFh) Clamped High Bit Step: 0.09765625%

8.6.2.44 REG0x40_TDIE_ADC Register (Address = 40h) [Reset = 0000h]

REG0x40_TDIE_ADC is shown in Figure 8-63 and described in Table 8-52.

Return to the Summary Table.

Figure 8-63. REG0x40_TDIE_ADC Register

15	14	13	12	11	10	9	8
TDIE_ADC							
R-0h							
7	6	5	4	3	2	1	0
TDIE_ADC							
R-0h							

Table 8-52. REG0x40_TDIE_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TDIE_ADC	R	0h	TDIE ADC reading Reported in 2's Complement. POR: 0°C(0h) Format: 2s Complement Range: -40°C - 150°C (FFB0h-12Ch) Clamped Low Clamped High Bit Step: 0.5°C

8.6.2.45 REG0x44_USB_C_Control_0 Register (Address = 44h) [Reset = 08h]

REG0x44_USB_C_Control_0 is shown in Figure 8-64 and described in Table 8-53.

Return to the Summary Table.

Figure 8-64. REG0x44_USB_C_Control_0 Register

7	6	5	4	3	2	1	0
CC_MODE		RP_VALUE		DRP_PREF		RESERVED	
R/W-0h		R/W-0h		R/W-2h		R-0h	

Table 8-53. REG0x44_USB_C_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	CC_MODE	R/W	0h	Reset by: REG_RESET WATCHDOG	USB-C Role Control. Selects the advertsing mode of the USB-C CC pins. 00b = SNK only mode - unnattached.SNK (default) 01b = SRC only mode - unnattached.SRC 10b = DRP mode - starts from unnattached.SNK 11b = RESERVED

Table 8-53. REG0x44_USB_C_Control_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
5:4	RP_VALUE	R/W	0h	Reset by: REG_RESET	Rp Value. Sets the maximum current advertised as a USB-C SRC. 00b = Rp default current (500mA/900mA) (default) 01b = Rp medium current (1.5A) 10b = Rp high current (3A) 11b = RESERVED
3:2	DRP_PREF	R/W	2h	Reset by: REG_RESET	Selects the advertsing role prefered in DRP mode. 00b = Try.SNK 01b = Try.SRC 10b = DRP prefers no role (default) 11b = RESERVED
1:0	RESERVED	R	0h		Reserved

8.6.2.46 REG0x45_USB_C_Control_1 Register (Address = 45h) [Reset = 16h]

REG0x45_USB_C_Control_1 is shown in Figure 8-65 and described in Table 8-54.

Return to the Summary Table.

Figure 8-65. REG0x45_USB_C_Control_1 Register

7	6	5	4	3	2	1	0
DIS_CC	FORCE_CC_DET	EN_DEBUG_ACC_DET	EN_DPDM_DET	FORCE_DPDM_DET	EN_DCP_BIAS	CC_AUTO_OTG	CC_OVP
R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-0h

Table 8-54. REG0x45_USB_C_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	DIS_CC	R/W	0h	Reset by: REG_RESET WATCHDOG	Disables USB-C detection 0b = Enabled (Default) 1b = Disabled
6	FORCE_CC_DET	R/W	0h	Automatically clears after CC Handshaking completes. Reset by: REG_RESET WATCHDOG	Restarts USB-C detection 0b = Cleared 1b = USB-C detection restarted
5	EN_DEBUG_ACC_DET	R/W	0h	Reset by: REG_RESET	Enable debug accessory detection 0b = Disabled (Default) 1b = Enabled
4	EN_DPDM_DET	R/W	1h	Reset by: REG_RESET WATCHDOG	Automatic D+/D- Detection Enable 0b = Disable DPDM detection when VBUS is plugged-in 1b = Enable DPDM detection when VBUS is plugged-in (default)
3	FORCE_DPDM_DET	R/W	0h	Reset by: REG_RESET WATCHDOG	Force D+/D- detection 0b = Do not force DPDM detection (default) 1b = Force DPDM algorithm, when DPDM detection is done, this bit will be reset to 0
2	EN_DCP_BIAS	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable 600mV bias on D+ pin when DCP is detected (VBUS_STAT = 0011b) 0b = Disable 1b = Enable (Default)

Table 8-54. REG0x45_USB_C_Control_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
1	CC_AUTO_OTG	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable Automatic OTG upon entering Attached.SRC. 0b = Disable: Host must manually set EN_OTG. Sets VBUS_STAT = 1100b upon entering Attached.SRC. 1b = Enable: Automatically set EN_OTG = 1b and VBUS_STAT = 1100b upon entering Attached.SRC. (Default)
0	CC_OVP	R/W	0h		CC OVP Threshold 0b = 3.6V (Default) 1b = 6V

8.6.2.47 REG0x46_Liquid_Control_0 Register (Address = 46h) [Reset = 20h]

REG0x46_Liquid_Control_0 is shown in Figure 8-66 and described in Table 8-55.

Return to the Summary Table.

Figure 8-66. REG0x46_Liquid_Control_0 Register

7	6	5	4	3	2	1	0
EN_LQD_DET	AUTO_LQD_DET	AUTO_DRY_DET	LQD_WAIT	FORCE_LQD_DET	LQD_HICCUP		LQD_PIN_SEL
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

Table 8-55. REG0x46_Liquid_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_LQD_DET	R/W	0h	Reset by: REG_RESET WATCHDOG	Enable Liquid Detection Feature and Corrosion Mitigation 0b = Disabled (Default) 1b = Enabled
6	AUTO_LQD_DET	R/W	0h	Reset by: REG_RESET WATCHDOG	Enable automatic liquid detection 0b = Disabled (Default) 1b = Enabled
5	AUTO_DRY_DET	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable dry detection 0b = Disabled 1b = Enabled (Default)
4	LQD_WAIT	R/W	0h	Reset by: REG_RESET	Determine wait interval between liquid check cycle. 0b = 500ms (Default) 1b = 10s
3	FORCE_LQD_DET	R/W	0h	Automatically clears after liquid check completes.	Force liquid detection check 0b = Cleared 1b = Liquid detection forced
2:1	LQD_HICCUP	R/W	0h	Reset by: REG_RESET	Hiccup count for liquid detection 00b = 1 01b = 2 10b = 4 11b = RESERVED
0	LQD_PIN_SEL	R/W	0h	Reset by: REG_RESET	Determine pins used for liquid detection. 0b = CC1/CC2 (Default) 1b = D+/D-

8.6.2.48 REG0x47_Liquid_Control_1 Register (Address = 47h) [Reset = 9Ch]

REG0x47_Liquid_Control_1 is shown in Figure 8-67 and described in Table 8-56.

Return to the Summary Table.

Figure 8-67. REG0x47_Liquid_Control_1 Register

7	6	5	4	3	2	1	0
TLQD		ILQD		VLQD			
R/W-2h		R/W-1h		R/W-Ch			

Table 8-56. REG0x47_Liquid_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TLQD	R/W	2h	Reset by: REG_RESET	Liquid detection test duration 00b = 1 - Longest 01b = 2 10b = 3 (Default) 11b = 4 - Shortest
5:4	ILQD	R/W	1h	Reset by: REG_RESET	Liquid detection test strength 00b = 1 - Weakest 01b = 2 (Default) 10b = 3 11b = 4 - Strongest
3:0	VLQD	R/W	Ch	Reset by: REG_RESET	Liquid detection threshold VLQD_TH 0000b = 0.4V 0001b = 0.5V 0010b = 0.6V 0011b = 0.7V 0100b = 0.8V 0101b = 0.9V 0110b = 1.0V 0111b = 1.1V 1000b = 1.2V 1001b = 1.3V 1010b = 1.4V 1011b = 1.5V 1100b = 1.6V (Default) 1101b = 1.7V 1110b = 1.8V 1111b = 1.9V

8.6.2.49 REG0x48_USB_C_Information_0 Register (Address = 48h) [Reset = 00h]

REG0x48_USB_C_Information_0 is shown in Figure 8-68 and described in Table 8-57.

Return to the Summary Table.

Figure 8-68. REG0x48_USB_C_Information_0 Register

7	6	5	4	3	2	1	0
CC_FAULT_STAT	LQD_STAT	DEBUG_ACC_STAT	CC_ORIENT_STAT	RESERVED			
R-0h	R-0h	R-0h	R-0h	R-0h			

Table 8-57. REG0x48_USB_C_Information_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CC_FAULT_STAT	R	0h	USB-C CC1/CC2 short to VBUS fault status 0b = Normal 1b = CC1 or CC2 shorted to VBUS
6	LQD_STAT	R	0h	Liquid detection status 0b = No liquid detected (Dry) 1b = Liquid detected

Table 8-57. REG0x48_USB_C_Information_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DEBUG_ACC_STAT	R	0h	Debug Accessory status 0b = No Debug Accessory detected (default) 1b = Debug Accessory detected
4	CC_ORIENT_STAT	R	0h	USB-C Connector Orientation 0b = Unoriented 1b = Oriented
3:0	RESERVED	R	0h	Reserved

8.6.2.50 REG0x49_USB_C_Information_1 Register (Address = 49h) [Reset = 00h]

REG0x49_USB_C_Information_1 is shown in Figure 8-69 and described in Table 8-58.

Return to the Summary Table.

Figure 8-69. REG0x49_USB_C_Information_1 Register

7	6	5	4	3	2	1	0
RESERVED			CC2_STAT			CC1_STAT	
R-0h			R-0h			R-0h	

Table 8-58. REG0x49_USB_C_Information_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0h		Reserved
5:3	CC2_STAT	R	0h	Reset by: REG_RESET	CC2 Status 000b = CC2 sees 'HiZ 001b = CC2 sees Rd (5.1kOhm) 010b = CC2 seesRp Default (80uA) 011b = CC2 sees Rp Medium (180uA) 100b = CC2 sees Rp High (330uA) 101b = CC2 sees Ra/GND (1.0kOhm) 110b = CC2 sees OPEN 111b = CC2 in Corrosion Mitigation
2:0	CC1_STAT	R	0h	Reset by: REG_RESET	CC1 Status 000b = CC1 sees 'HiZ 001b = CC1 sees Rd (5.1kOhm) 010b = CC1 sees Rp Default (80uA) 011b = CC1 sees Rp Medium (180uA) 100b = CC1 sees Rp High (330uA) 101b = CC1 sees Ra/GND (1.0kOhm) 110b = CC1 sees OPEN 111b = CC1 in Corrosion Mitigation

8.6.2.51 REG0x4A_USB_DAC_Control_0 Register (Address = 4Ah) [Reset = 00h]

REG0x4A_USB_DAC_Control_0 is shown in Figure 8-70 and described in Table 8-59.

Return to the Summary Table.

Figure 8-70. REG0x4A_USB_DAC_Control_0 Register

7	6	5	4	3	2	1	0
DP_DAC				DM_DAC		EN_9V	EN_12V
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Table 8-59. REG0x4A_USB_DAC_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:5	DP_DAC	R/W	0h	Reset by: REG_RESET Adapter Plug In	D+ Pin Output Driver 000b = HiZ mode 001b = 0V (V_0MV_SRC) 010b = 0.6V (V_600MV_SRC) 011b = 1.2V (V_1p2V_SRC) 100b = 2.0V (V_2p0V_SRC) 101b = 2.7V (V_2p7V_SRC) 110b = 3.3V (V_3p3V_SRC) 111b = Reserved
4:2	DM_DAC	R/W	0h	Reset by: REG_RESET Adapter Plug In	D- Pin Output Driver 000b = HiZ mode 001b = 0V (V_0MV_SRC) 010b = 0.6V (V_600MV_SRC) 011b = 1.2V (V_1p2V_SRC) 100b = 2.0V (V_2p0V_SRC) 101b = 2.7V (V_2p7V_SRC) 110b = 3.3V (V_3p3V_SRC) 111b = Reserved
1	EN_9V	R/W	0h	Reset by: REG_RESET WATCHDOG	Enable HVDCP detection when DCP is detected via automatic or forced D+/D- detection 0b = Disable (Default) 1b = Enable
0	EN_12V	R/W	0h	Reset by: REG_RESET WATCHDOG	Enable HVDCP detection when DCP is detected via automatic or forced D+/D- detection 0b = Disable (Default) 1b = Enable

8.6.2.52 REG0x4B_USB_DAC_Control_1 Register (Address = 4Bh) [Reset = XXh]

REG0x4B_USB_DAC_Control_1 is shown in Figure 8-71 and described in Table 8-60.

Return to the Summary Table.

Figure 8-71. REG0x4B_USB_DAC_Control_1 Register

7	6	5	4	3	2	1	0
CC2_DAC			CC1_DAC			TS_ISET_SEL	RESERVED
R/W-X			R/W-X			R/W-0h	R-0h

Table 8-60. REG0x4B_USB_DAC_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:5	CC2_DAC	R/W	X	Reset by: REG_RESET	CC2 Pin Output Driver 000b = HiZ mode 001b = Rd (5.1kOhm) 010b = Rp Default (80uA) 011b = Rp Medium (180uA) 100b = Rp High (330uA) 101b = Ra/GND (1.0kOhm)
4:2	CC1_DAC	R/W	X	Reset by: REG_RESET	CC1 Pin Output Driver 000b = HiZ mode 001b = Rd (5.1kOhm) 010b = Rp Default (80uA) 011b = Rp Medium (180uA) 100b = Rp High (330uA) 101b = Ra/GND (1.0kOhm)

Table 8-60. REG0x4B_USB_DAC_Control_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
1	TS_ISET_SEL	R/W	0h	Reset by: REG_RESET	TS_ISET Foldback Value 0b = 20% (Default) 1b = 0.6
0	RESERVED	R	0h		Reserved

8.6.2.53 REG0x4C_API_Control Register (Address = 4Ch) [Reset = 07h]

REG0x4C_API_Control is shown in Figure 8-72 and described in Table 8-61.

Return to the Summary Table.

Figure 8-72. REG0x4C_API_Control Register

7	6	5	4	3	2	1	0
EN_API	WD_MODE	API_ILIM					
R/W-0h	R/W-0h	R/W-7h					

Table 8-61. REG0x4C_API_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_API	R/W	0h	Reset by: REG_RESET WATCHDOG	Enable Alternate Power from Input Mode 0b = Disabled (Default) 1b = Enabled
6	WD_MODE	R/W	0h	Reset by: REG_RESET	Enable System Reset when Watchdog Timer expires. 0b = No System Reset on Watchdog Timer Expiration (Default) 1b = System Reset on Watchdog Timer Expiration
5:0	API_ILIM	R/W	7h	Reset by: REG_RESET	Current limit in API Mode POR: 17.5mA(7h) Range: 10mA - 100mA (4h-28h) Clamped Low Clamped High Bit Step: 2.5mA

8.6.2.54 REG0x4D_Part_Information Register (Address = 4Dh) [Reset = 01h]

REG0x4D_Part_Information is shown in Figure 8-73 and described in Table 8-62.

Return to the Summary Table.

Figure 8-73. REG0x4D_Part_Information Register

7	6	5	4	3	2	1	0
TEST_REV		PN				DEV_REV	
R-0h		R-0h				R-1h	

Table 8-62. REG0x4D_Part_Information Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TEST_REV	R	0h	Test Revision
5:2	PN	R	0h	Device Part number BQ25630: 0h
1:0	DEV_REV	R	1h	Device Revision

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the device configured as an I²C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphone and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application

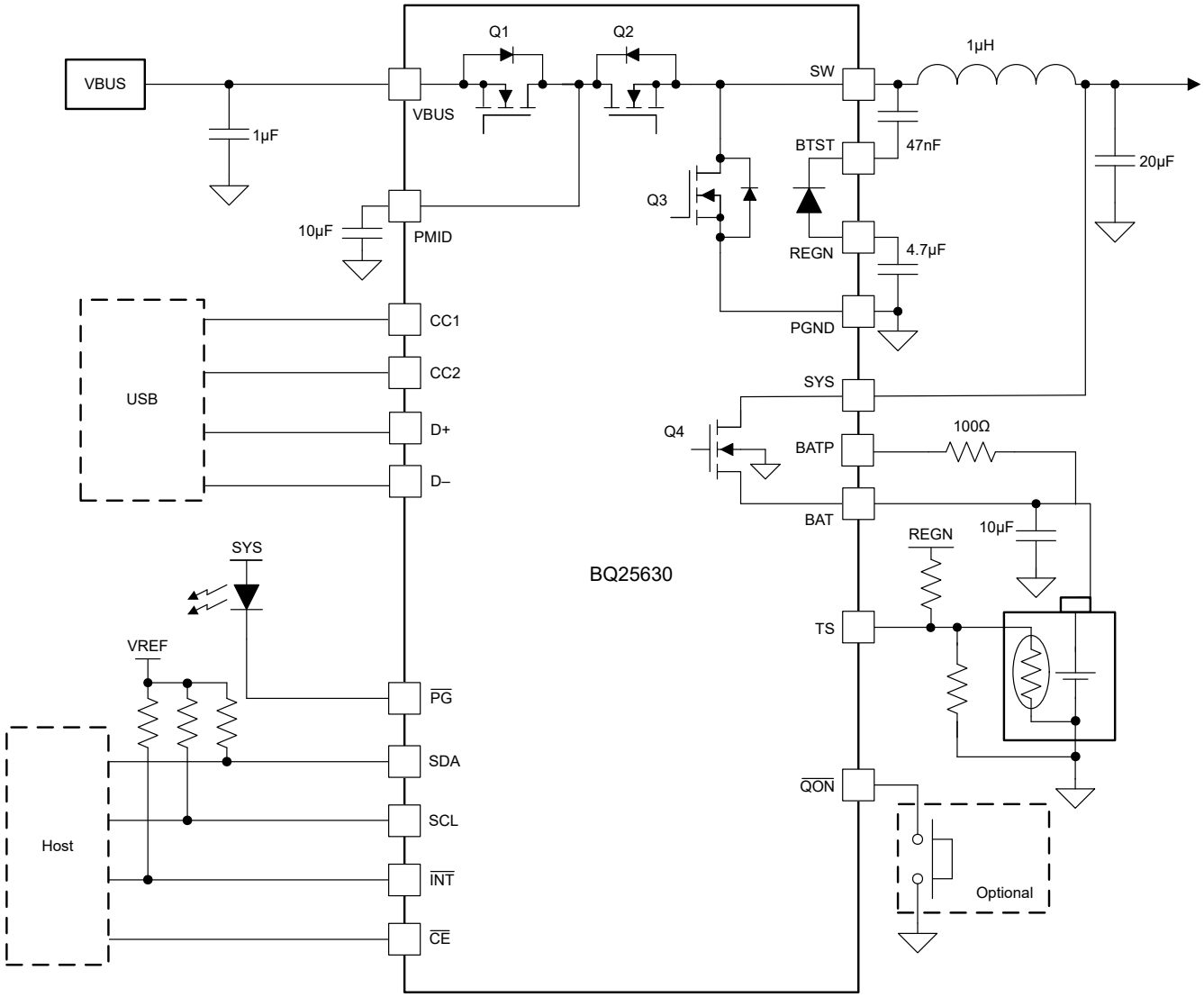


Figure 9-1. BQ25630 Typical Application

9.2.1 Design Requirements

Table 9-1. Design Requirements

PARAMETER	VALUE
VBUS range	3.9 - 18.0V
Input current limit (REG0x06-0x07)	3200mA
Fast charge current (REG0x02-0x03)	5040mA
Minimum system voltage (REG0x0E-0x0F)	2520-4000mV
Battery regulation voltage (REG0x04-0x05)	4200mV

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The 1.5MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \tag{5}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \tag{6}$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Typically inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.2 Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{Cin} occurs where the duty cycle is closest to 50% and can be estimated using Equation 7.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{7}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and must be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25V or higher capacitor is preferred for 15V input voltage.

9.2.2.3 Output Capacitor

Verify that the output capacitance has enough ripple current rating to absorb the output switching ripple current. Equation 8 shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{8}$$

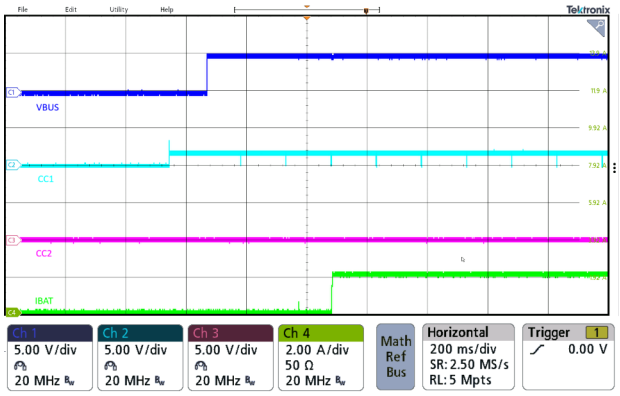
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{9}$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensation optimized for ≥ 10µF ceramic output capacitor. The preferred ceramic capacitor is 10V rating, X7R or X5R.

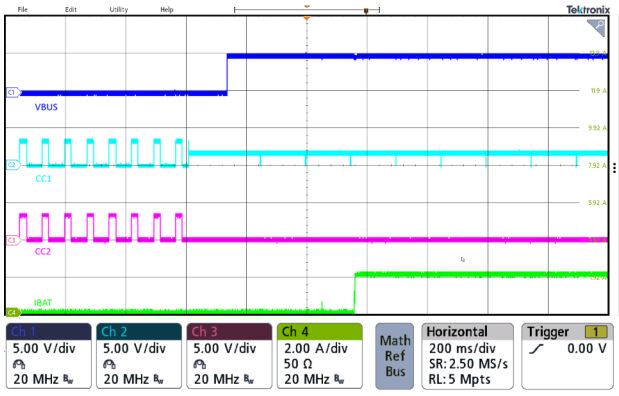
9.2.3 Application Curves



V_{VBUS} = 5V
SNK-Only Mode

V_{BAT} = 3.8V
I_{CHG} = 2A

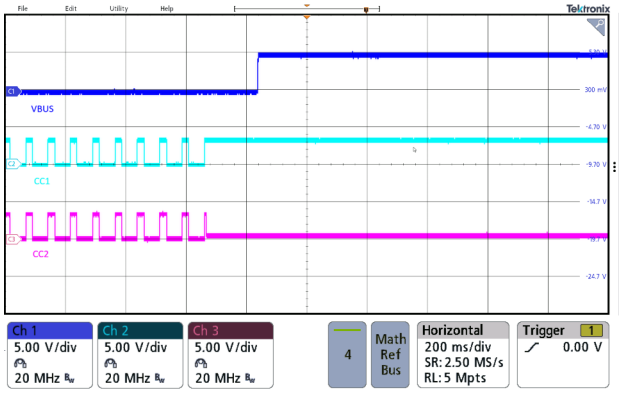
Figure 9-2. USB-C Adapter Plug-In, SNK Mode



V_{VBUS} = 5V
DRP Mode

V_{BAT} = 3.8V
I_{CHG} = 2A

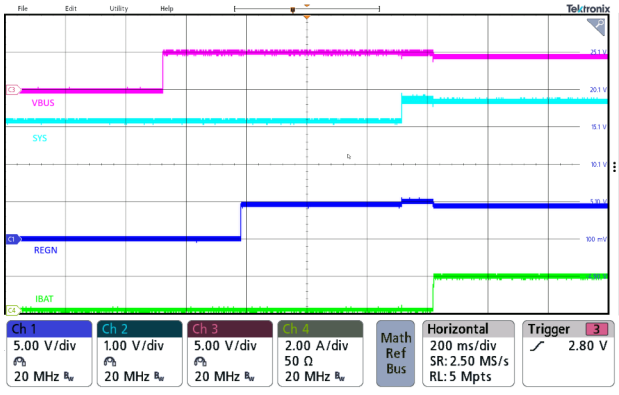
Figure 9-3. USB-C Adapter Plug-In, DRP Mode



V_{VBUS} = 5V
DRP Mode

V_{BAT} = 3.8V
V_{OTG} = 5.1V

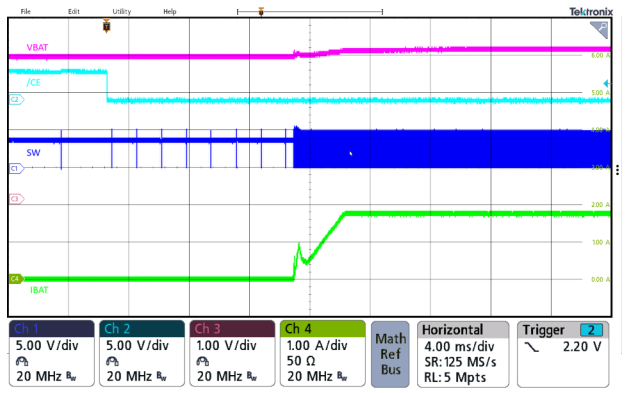
Figure 9-4. USB-C SNK Plugged in, DRP Mode



V_{VBUS} = 5V
V_{SYSMIN} = 3.52V

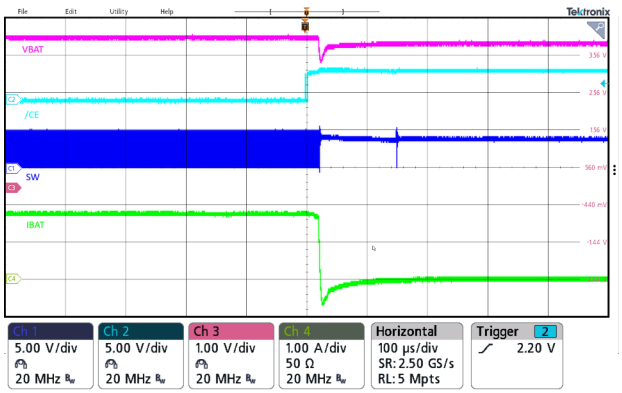
V_{BAT} = 3.2V
I_{CHG} = 2A

Figure 9-5. Power-Up Sequence



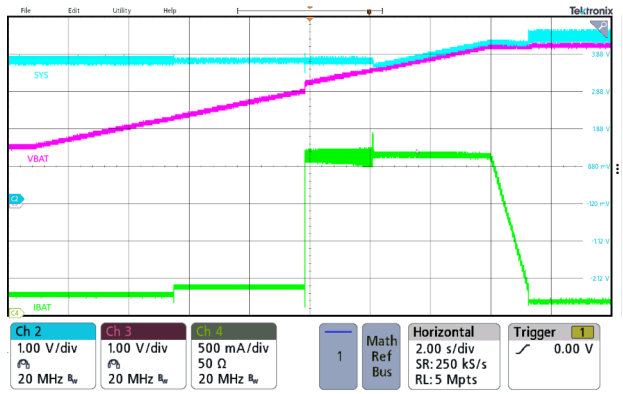
V_{VBUS} = 5V
I_{CHG} = 2A
V_{BAT} = 3.8V

Figure 9-6. Charge Enable via $\overline{CE}$ Pin



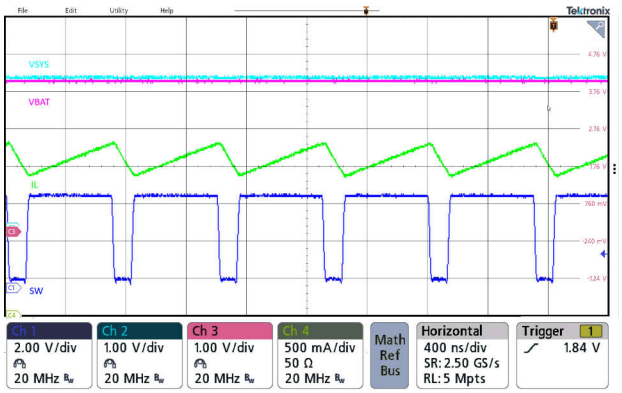
V_{VBUS} = 5V
I_{CHG} = 2A
V_{BAT} = 3.8V

Figure 9-7. Charge Disable via $\overline{CE}$ Pin



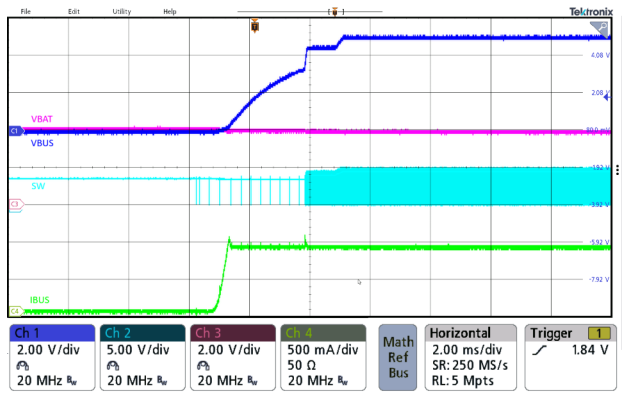
V_{VBUS} = 5V
I_{CHG} = 2A
V_{REG} = 4.2V
V_{SYSMIN} = 3.52V

Figure 9-8. Charge Profile



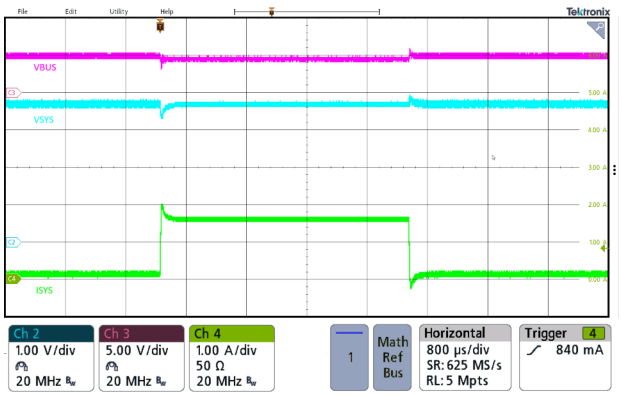
V_{VBUS} = 5V
I_{CHG} = 2A
V_{BAT} = 3.8V

Figure 9-9. Charging Switching Waveform



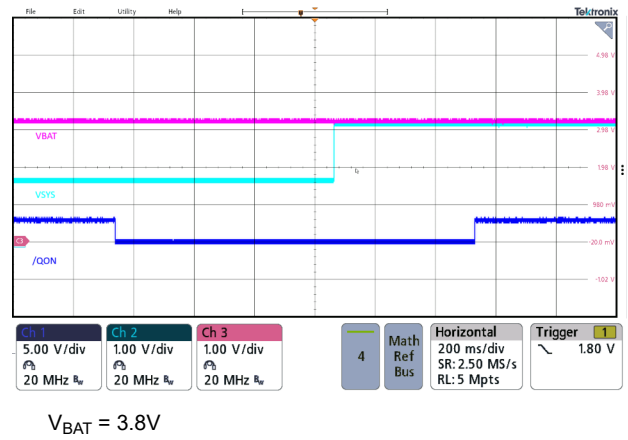
V_{OTG} = 5V
I_{BUS} = 1A
V_{BAT} = 4.0V

Figure 9-10. OTG Enable



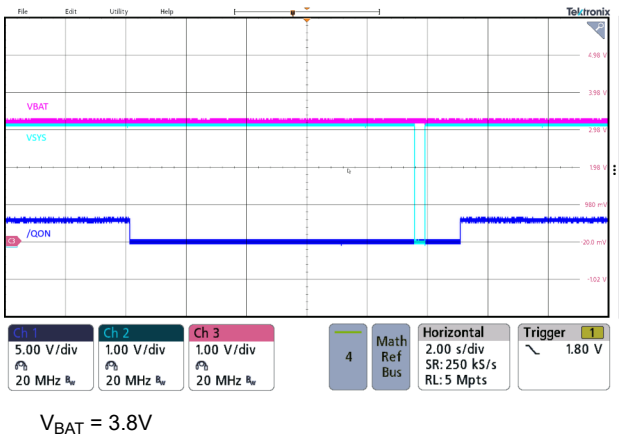
V_{VBUS} = 5V
V_{SYSMIN}= 3.52V
V_{BAT} = 3.2V
I_{SYS} 0A - 2A - 0A

Figure 9-11. SYS Transient



V_{BAT} = 3.8V

Figure 9-12. Wake-Up from Ship Mode with $\overline{QON}$



V_{BAT} = 3.8V

Figure 9-13. System Reset with $\overline{QON}$

9.3 Power Supply Recommendations

To provide an output voltage on SYS, the device requires a power supply between 3.9V and 18V input with at least 100mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage > V_{BAT_UVLO} connected to BAT.

9.4 Layout

9.4.1 Layout Guidelines

The switching node rise and fall times must be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 9-14) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
5. Verify that the number and sizes of vias allow enough copper for a given current path.

9.4.2 Layout Example

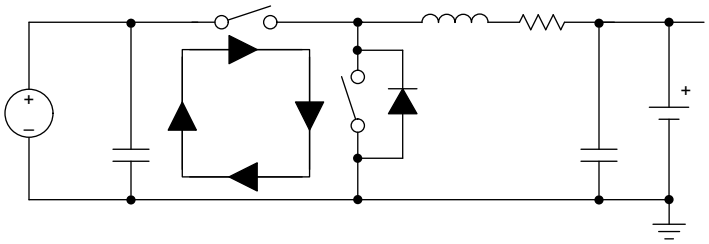


Figure 9-14. High Frequency Current Path

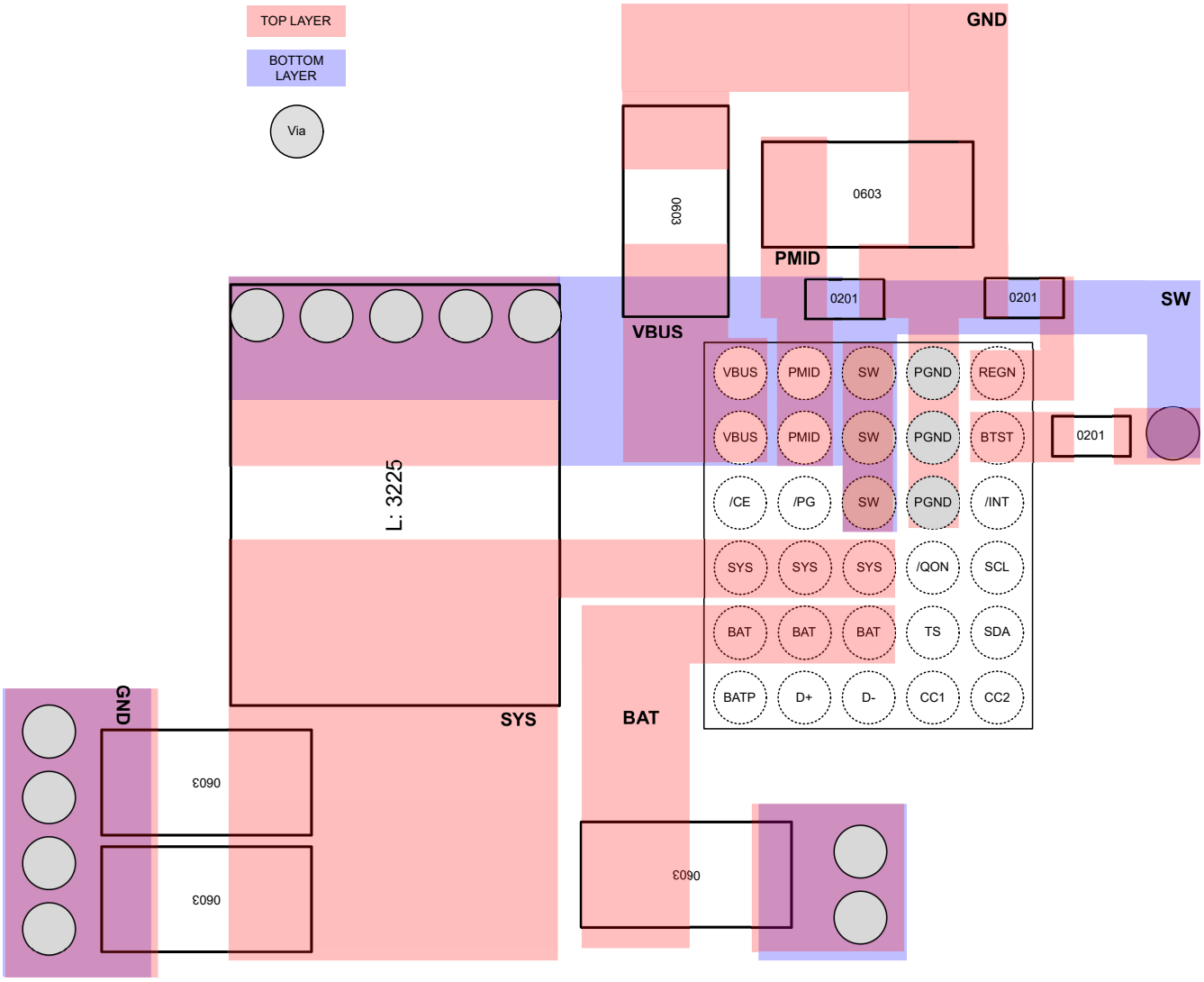


Figure 9-15. Layout

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- *BQ25601 and BQ25601D (PWR877) Evaluation Module User's Guide*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2025) to Revision A (December 2025)	Page
• Changed the device status from Advanced to Production data	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
BQ25630YBGR	PREVIEW	DSBGA	YBG	30	3000		SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25630

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

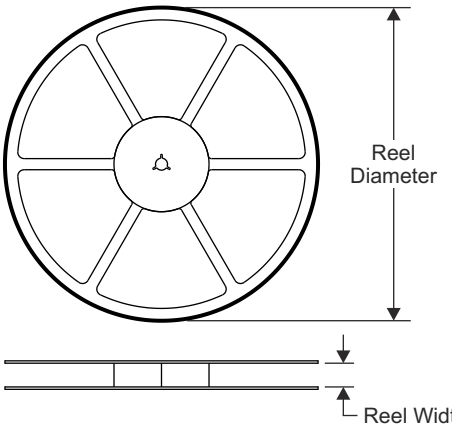
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

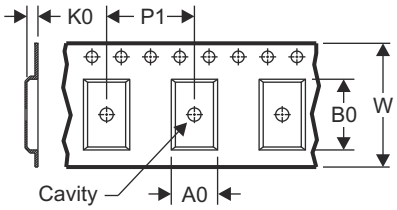
(6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

12.1.2 Tape and Reel Information

REEL DIMENSIONS

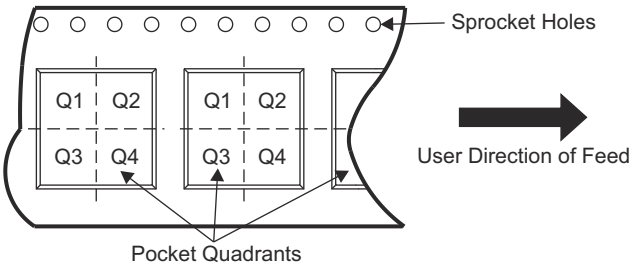


TAPE DIMENSIONS



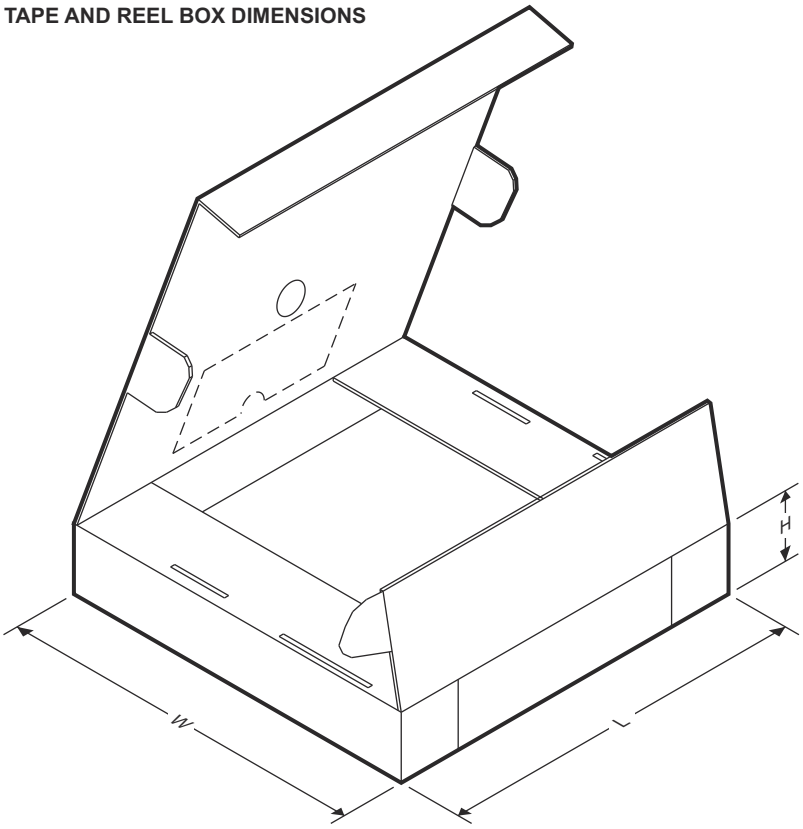
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25630YBGR	DSBGA	YBG	30	3000	330.0	12.4	2.30	2.68	0.65	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25630YBGR	DSBGA	YBG	30	3000	360.0	360.0	36.0

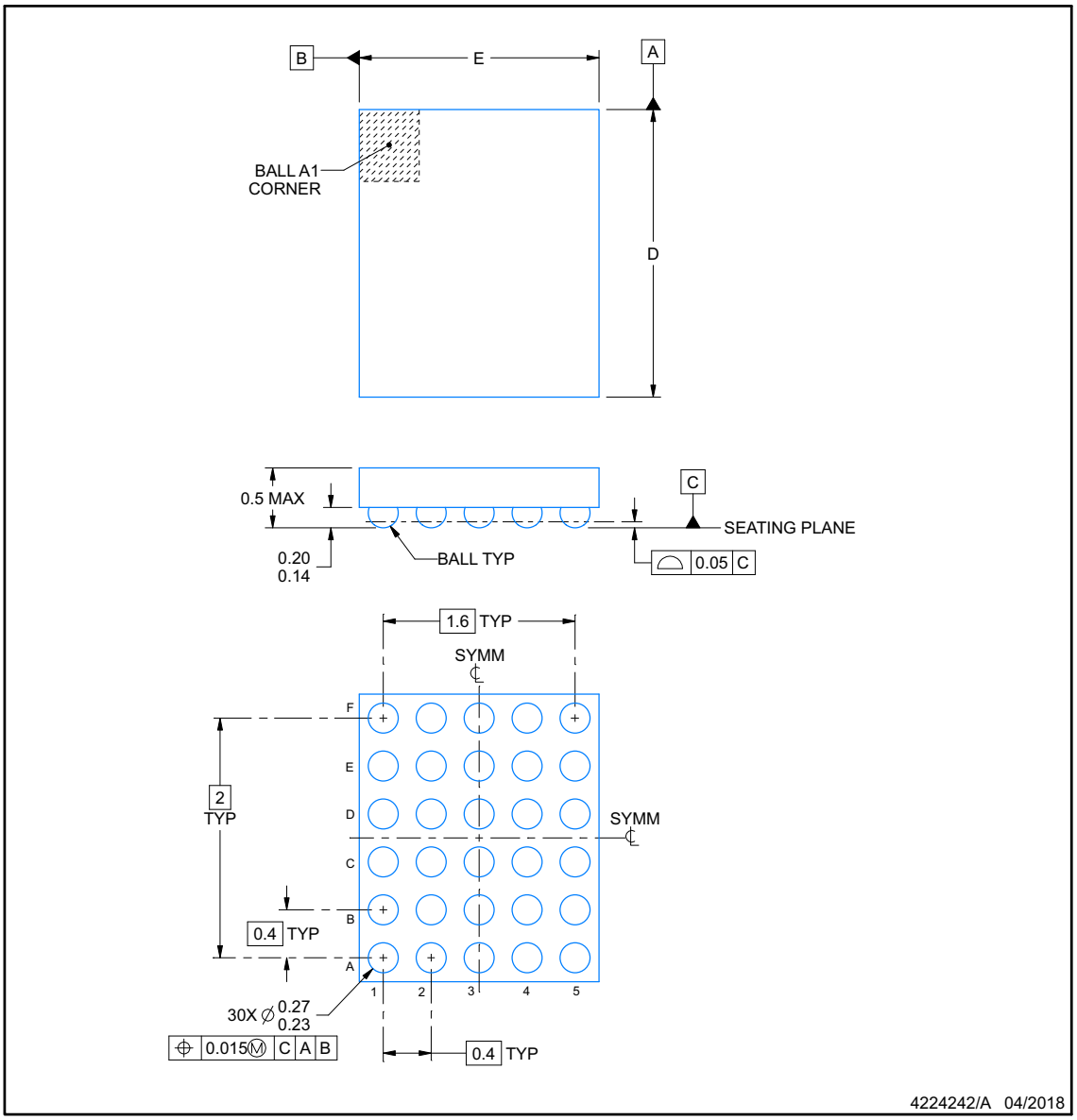
12.2 Mechanical Data

YBG0030

PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

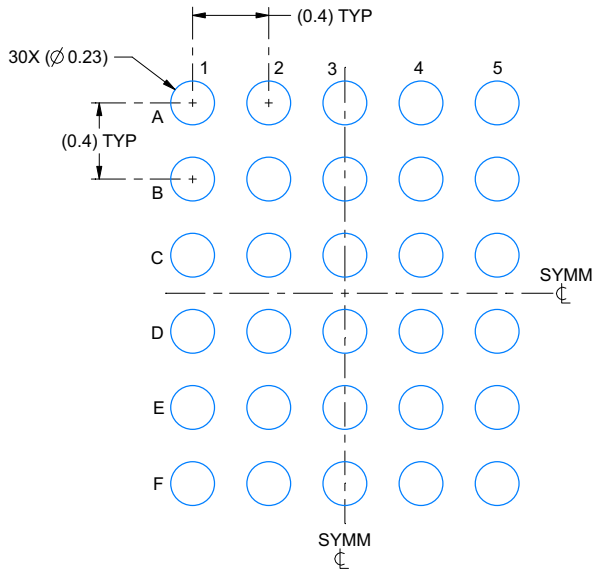
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

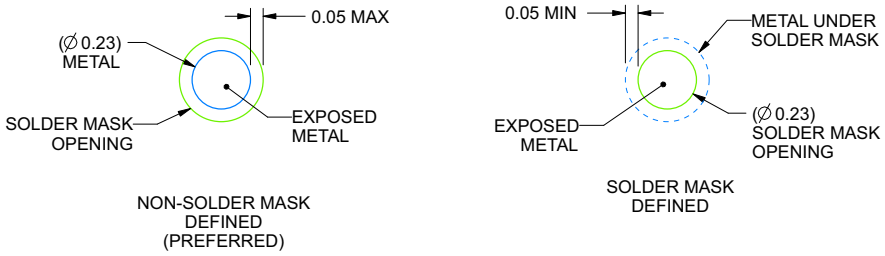
YBG0030

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

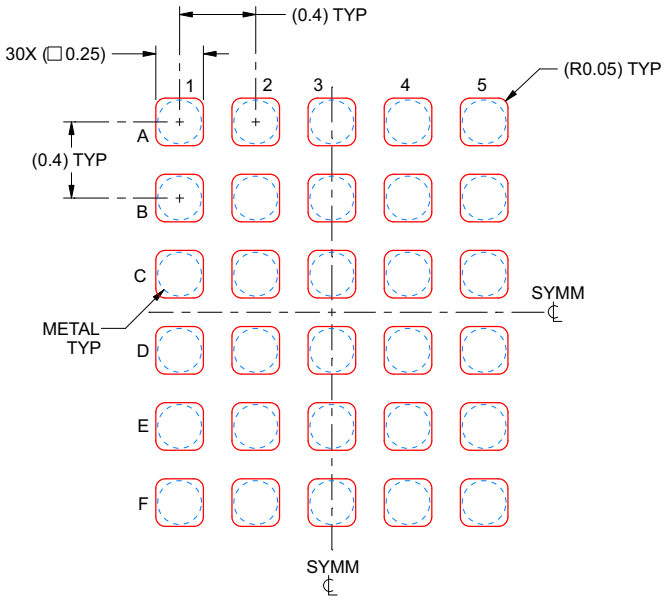
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBG0030

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

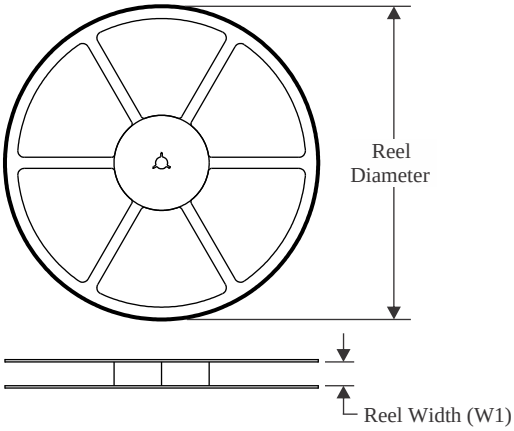
4224242/A 04/2018

NOTES: (continued)

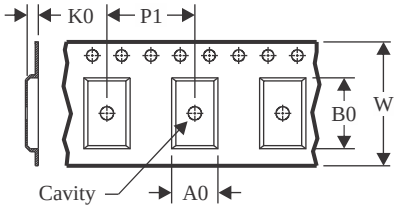
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

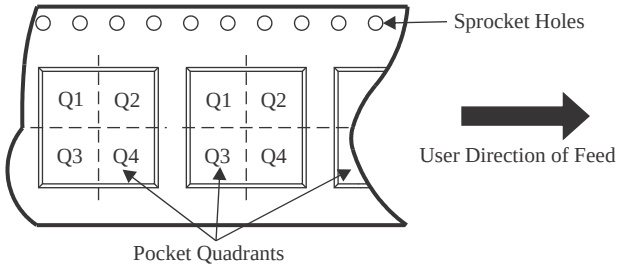


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

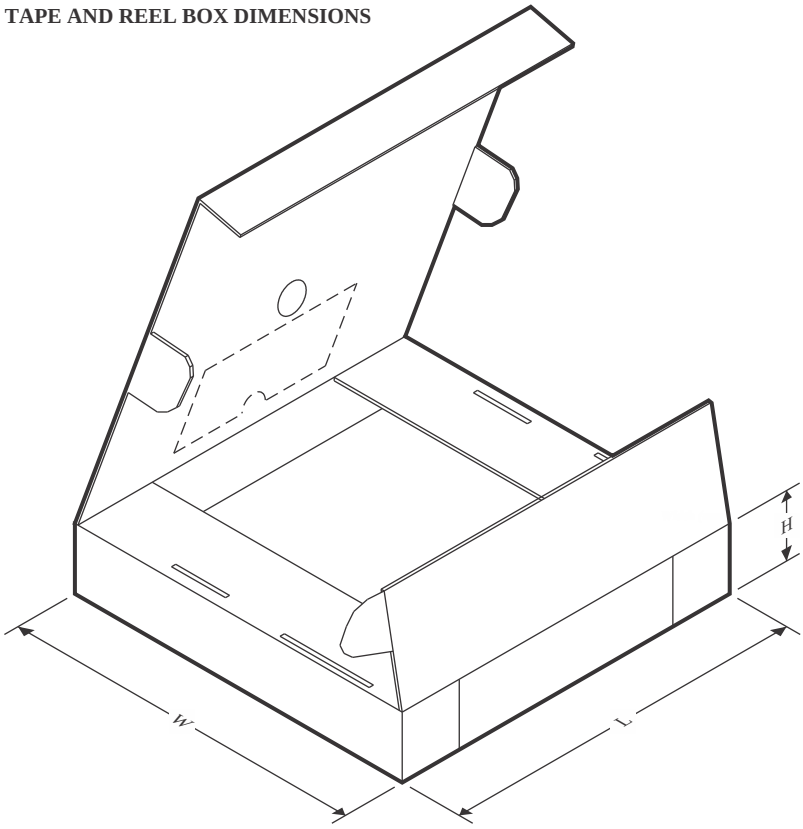
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25630YBGR	DSBGA	YBG	30	3000	180.0	8.4	2.6	2.62	0.75	4.0	8.0	Q1

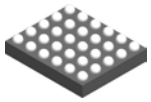
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25630YBGR	DSBGA	YBG	30	3000	182.0	182.0	20.0

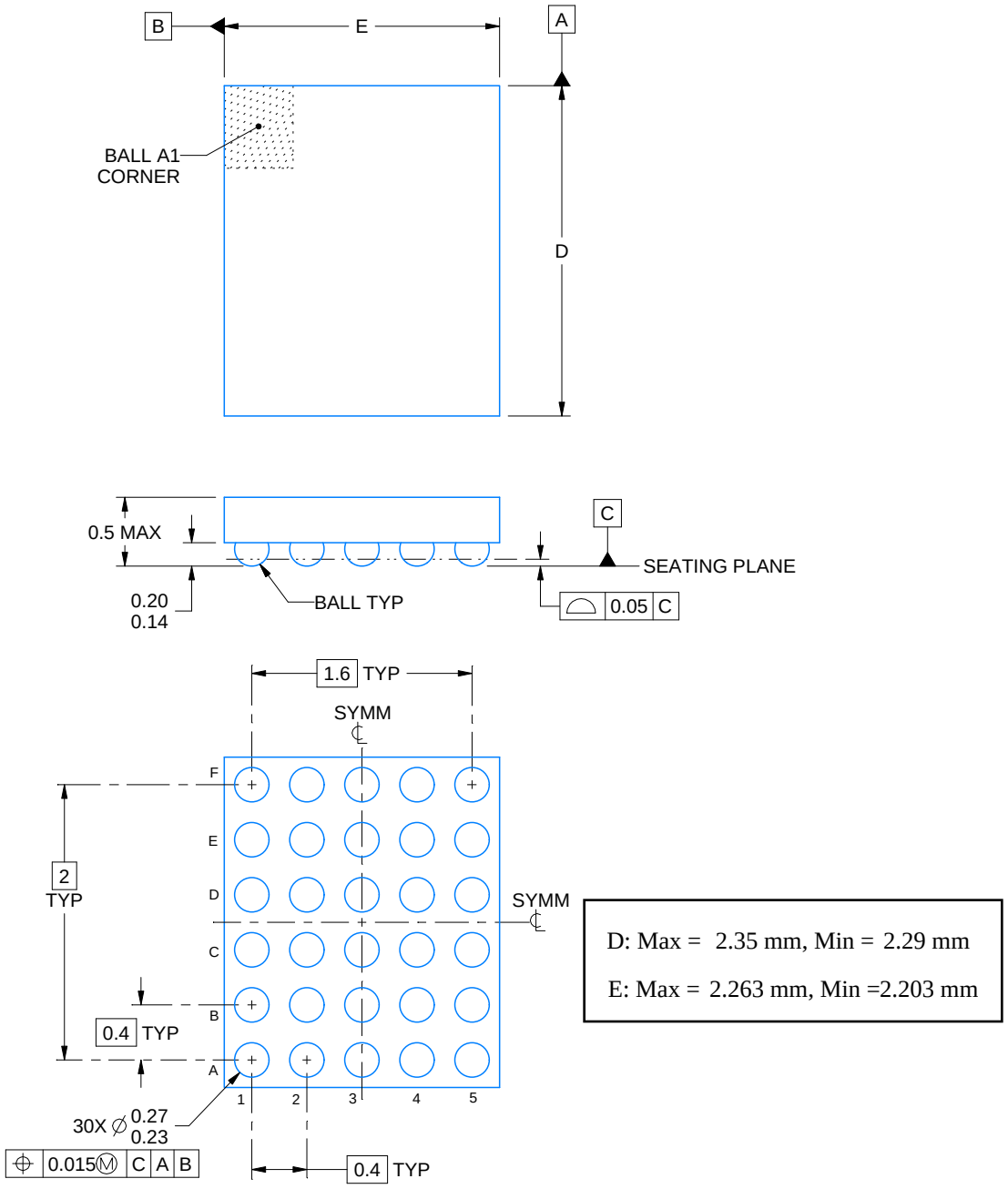
YBG0030



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

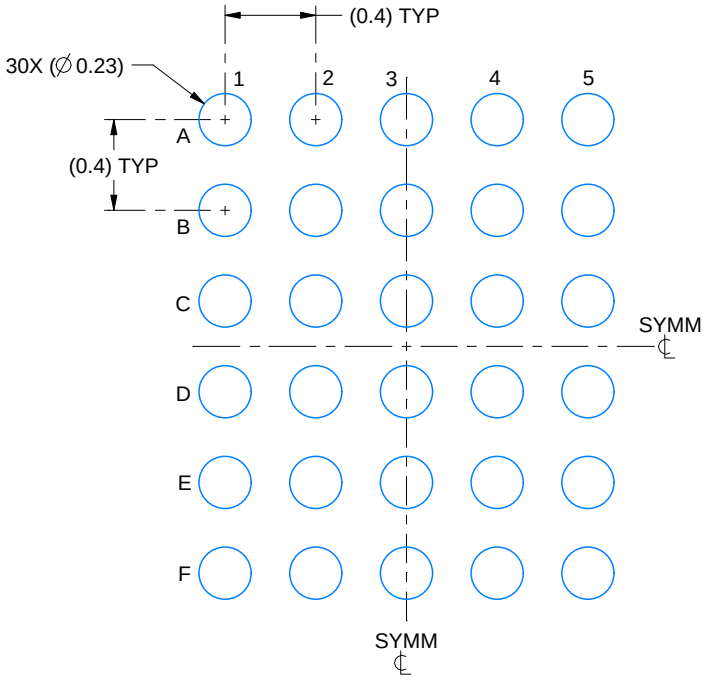
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

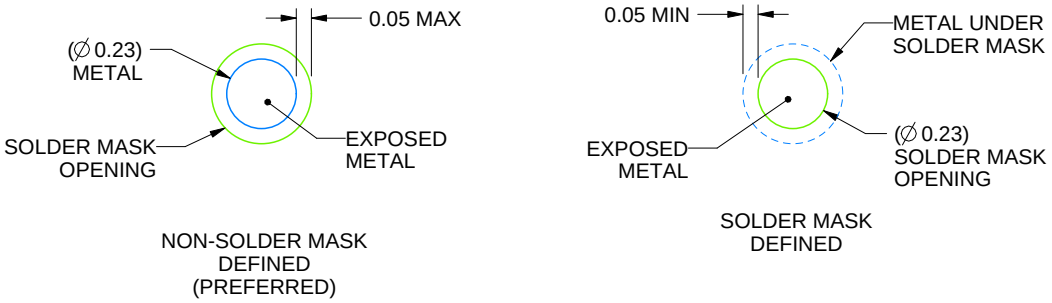
YBG0030

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

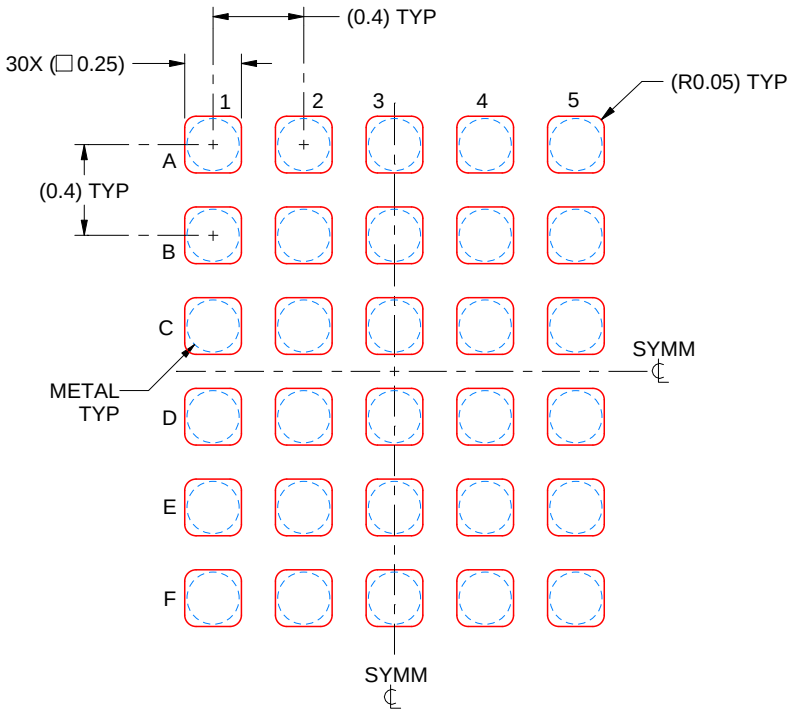


SOLDER MASK DETAILS
NOT TO SCALE

4224242/A 04/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224242/A 04/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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Last updated 10/2025