TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS096

CD40105B Types

CMOS FIFO Register

4 Bits X 16 Words

High-Voltage Types (20-Volt Rating)

■ CD40105B is a low-power first-in-first-out (FIFO) "elastic" storage register that can store 16 4-bit words. It is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems.

Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

Loading Data – Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

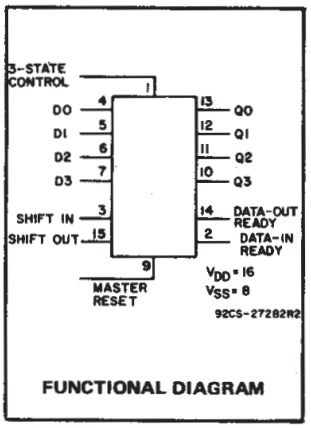
Unloading Data – As soon as the first word has rippled to the output, DATA-OUT READY (DOR) goes high, and data can be removed by a falling edge on the SO input. This falling edge causes the DOR signal to go low while the word on the output is dumped and the next word moves to the output. As long as valid data are available in the FIFO, the DOR signal will go high again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain low, and any further commands will be ignored until a "1" marker ripples down to the last control register, when DOR goes high. Unloading of data is inhibited while the 3-state control input is high. The 3-state control signal should not be shifted from high to low (data outputs turned on) while the SHIFT-OUT is at logic 0. This level change would cause the first word to be shifted out (unloaded) immediately and the data to be lost.

Cascading – The CD40105B can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than 4 bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions (see Figs. 3 and 15).

3-State Outputs – In order to facilitate data busing, 3-state outputs are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output.

Master Reset – A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded. The shift-in must be low during Master Reset.

The CD40105B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).



FUNCTIONAL DIAGRAM

Features:

- **Independent asynchronous inputs and outputs**
- **3-state outputs** ■ **Expandable in either direction**
- **Status indicators on input and output** ■ **Reset capability**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Bit rate smoothing**
- **CPU/terminal buffering**
- **Data communications**
- **Peripheral buffering**
- **Line printer input buffers**
- **Auto dialers**
- **CRT buffer memories**
- **Radar data acquisition**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW
OPERATING-TEMPERATURE RANGE (T_A) .....-55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .....-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

RECOMMENDED OPERATING CONDITIONS at 25°C, Except as Noted

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package – Temperature Range)	–	3	18	V
Shift-In or Shift-Out Rate	5	–	1.5	MHz
	10	–	3	
	15	–	4	
Shift-In Pulse Width (Pin 3)	5	200	–	ns
	10	80	–	
	15	60	–	
Shift-Out Pulse Width (Pin 15)	5	180	–	ns
	10	75	–	
	15	55	–	
Shift-In or Shift-Out Rise Time	5	–	15	μs
	10	–	15	
	15	–	15	
Shift-In Fall Time	5	–	15	μs
	10	–	15	
	15	–	15	
Shift-Out Fall Time	5	–	15	μs
	10	–	5	
	15	–	5	
Data Hold Time	5	350	–	ns
	10	150	–	
	15	120	–	
Master Reset Pulse Width	5	220	–	ns
	10	90	–	
	15	60	–	

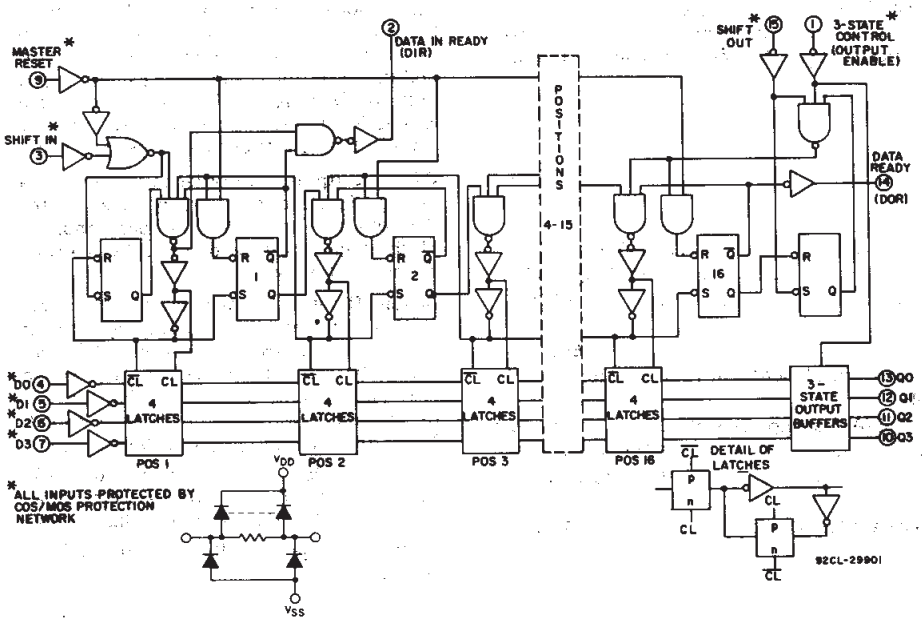


Fig. 1 – Logic diagram for the CD40105B.

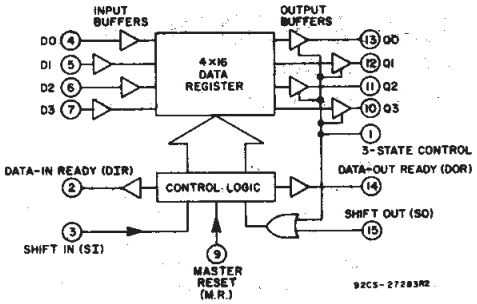
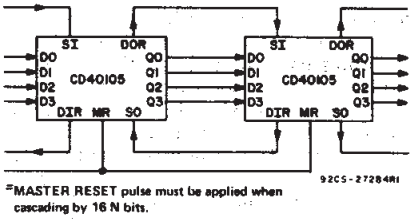


Fig. 2 – CD40105B functional block diagram.



*MASTER RESET pulse must be applied when cascading by 16 N bits.

Fig. 3 – Expansion, 4-bits wide-by-16 N-bits long.

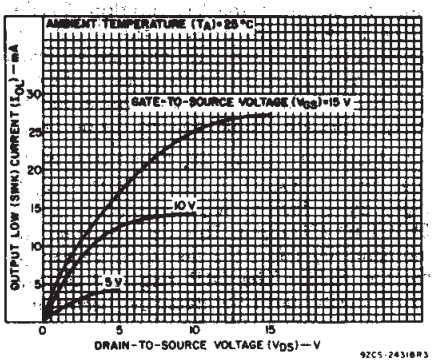


Fig. 4 – Typical output low (sink) current characteristics.

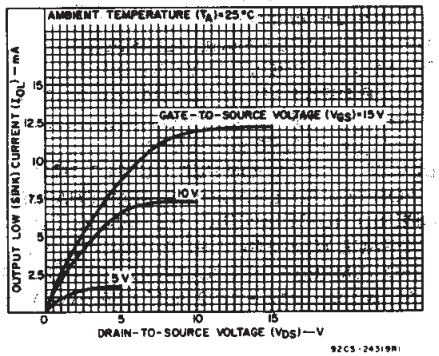


Fig. 5 – Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

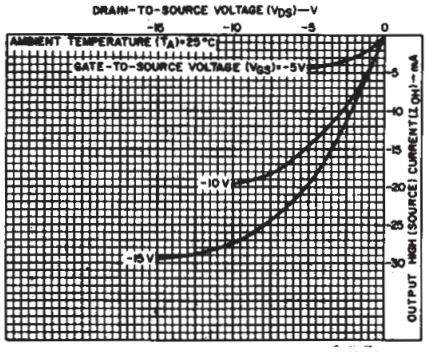


Fig. 6 – Typical output high (source) current characteristics.

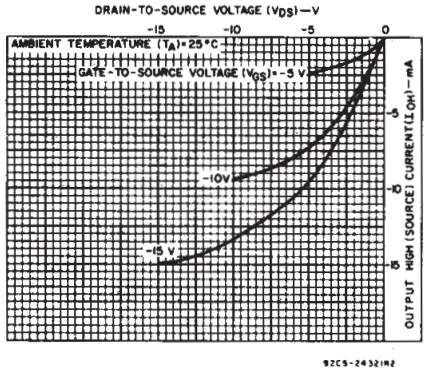


Fig. 7 – Minimum output high (source) current characteristics.

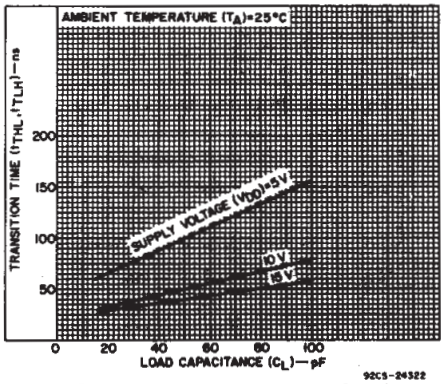


Fig. 8 – Typical transition time as a function of load capacitance.

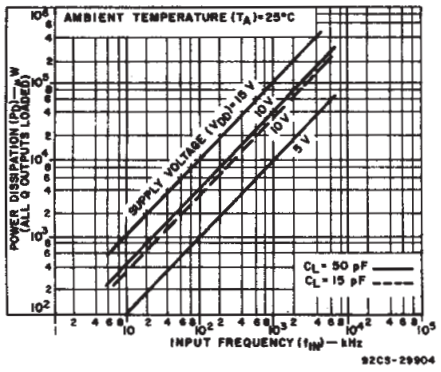


Fig. 9 – Typical dynamic power dissipation as a function of frequency.

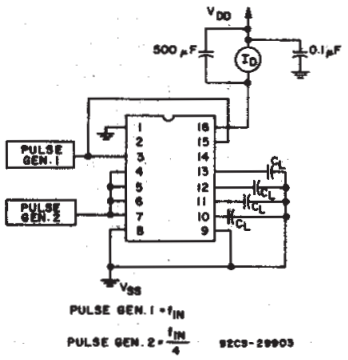


Fig. 10 – Dynamic power dissipation test circuit.

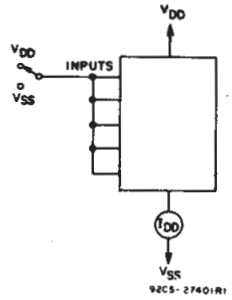


Fig. 11 – Quiescent-device-current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		V_{DD} (V)	Min.	Typ.	Max.	
Propagation Delay Time: Shift-Out or Reset to Data-Out Ready, t_{PHL}		5	–	185	370	ns
		10	–	90	180	
		15	–	65	130	
Shift-In to Data-In Ready, t_{PHL}		5	–	160	320	ns
		10	–	65	130	
		15	–	45	90	
Shift-Out to Q_n Out, t_{PHL}, t_{PLH}		5	–	210	420	ns
		10	–	100	205	
		15	–	70	150	
3-State Control to Data Out Note 1 t_{PZH}, t_{PZL}		5	–	140	280	ns
		10	–	60	120	
		15	–	40	80	
t_{PHZ}, t_{PLZ}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Ripple-Through Delay Input to Output, t_{PLH}		5	–	2	4	μs
		10	–	1	2	
		15	–	0.7	1.4	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Shift-In or Shift-Out Rate, f_l		5	1.5	3	–	MHz
		10	3	6	–	
		15	4	8	–	
Minimum Shift-In Pulse Width, (Pin 3) t_W		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Minimum Shift-Out Pulse Width, (Pin 15) t_{WL}		5	–	90	180	ns
		10	–	35	75	
		15	–	25	55	
Maximum Shift-In or Shift-Out Rise Time, t_r		5	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Maximum Shift-In Fall Time, t_f		5	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Maximum Shift-Out Fall Time, t_f		5	–	–	15	μs
		10	–	–	5	
		15	–	–	5	
Minimum Data Setup Time, t_{SU}		5	–	–	0	ns
		10	–	–	0	
		15	–	–	0	
Minimum Data Hold Time, t_H		5	–	175	350	ns
		10	–	75	150	
		15	–	60	120	
Data-In Ready Pulse Width, t_{WL} (Pin 2)		5	–	260	520	ns
		10	–	100	200	
		15	–	70	140	
Data-Out Ready Pulse Width, t_{WL} (Pin 14)		5	–	220	440	ns
		10	–	90	180	
		15	–	65	130	
Minimum Master Reset Pulse Width, t_{WH}		5	–	100	200	ns
		10	–	45	90	
		15	–	30	60	
Input Capacitance C_{IN}	(Any Input)	–	–	5	7.5	pF

Note 1: The Output Enable Line (Pin 1) should be low for limits specified.

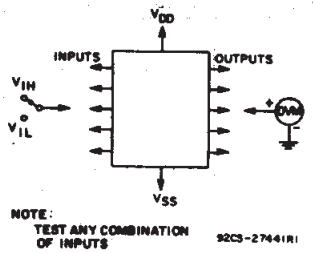


Fig. 12 – Input-voltage test circuit.

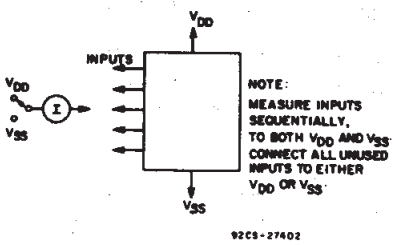
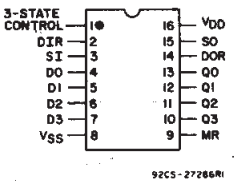
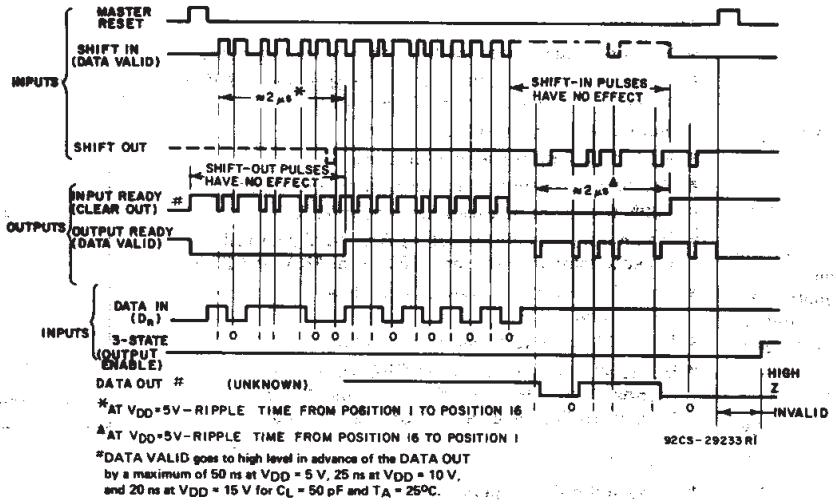


Fig. 13 – Input current test circuit.



TERMINAL ASSIGNMENT



#DATA VALID goes to high level in advance of the DATA OUT by a maximum of 50 ns at V_{DD} = 5 V, 25 ns at V_{DD} = 10 V, and 20 ns at V_{DD} = 15 V for C_L = 50 pF and T_A = 25°C.

Fig. 14 — Timing diagram for the CD40105B.

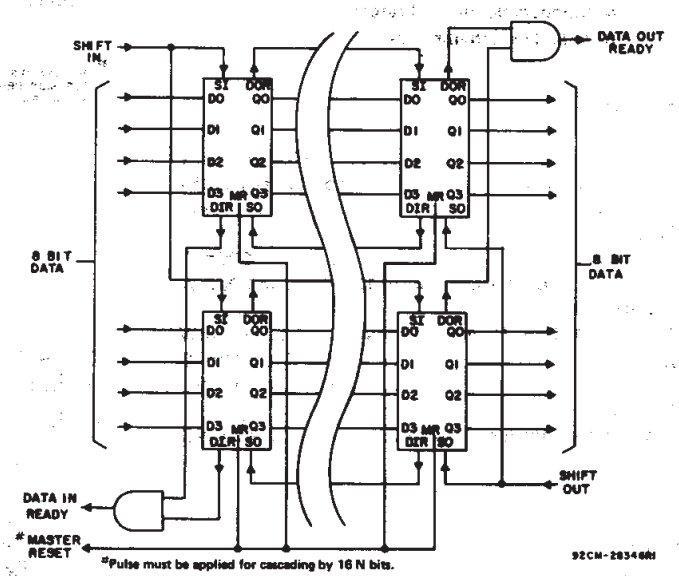
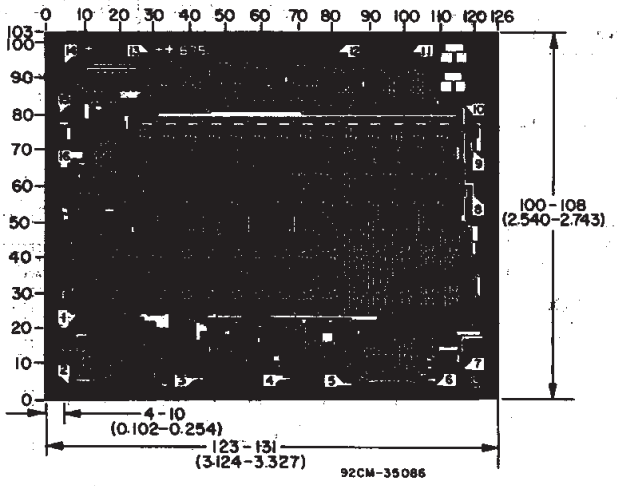


Fig. 15 — Expansion, 8-bits-wide-by-16 N-bits long using CD40105.



Dimension and pad layout for CD40105B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD40105BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40105BE
CD40105BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40105BE
CD40105BF	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40105BF
CD40105BF.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40105BF
CD40105BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40105BF3A
CD40105BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40105BF3A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

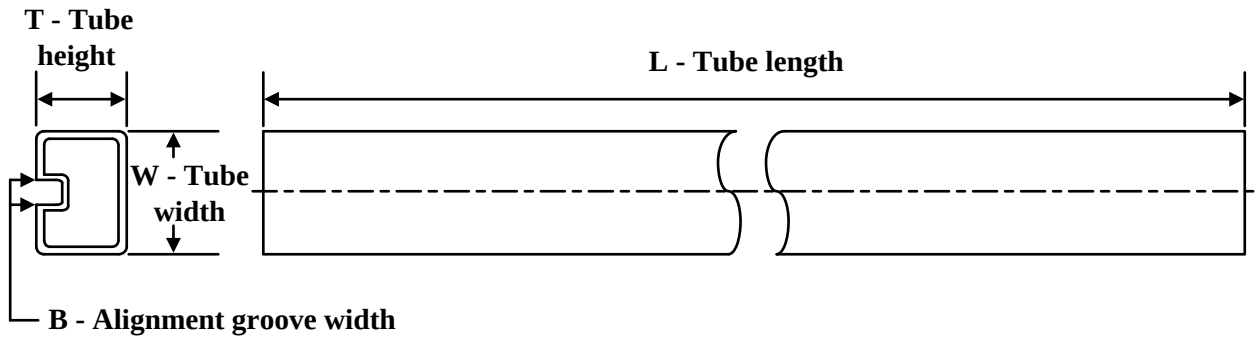
OTHER QUALIFIED VERSIONS OF CD40105B, CD40105B-MIL :

- Catalog : CD40105B
- Military : CD40105B-MIL

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



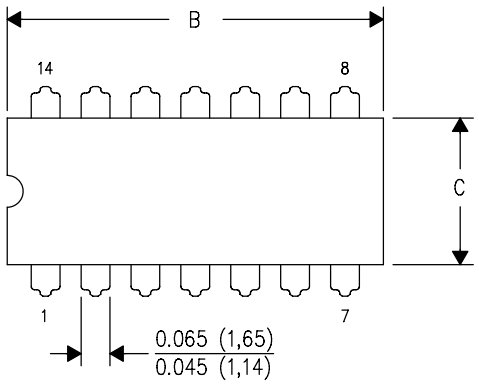
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD40105BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40105BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40105BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD40105BE.A	N	PDIP	16	25	506	13.97	11230	4.32

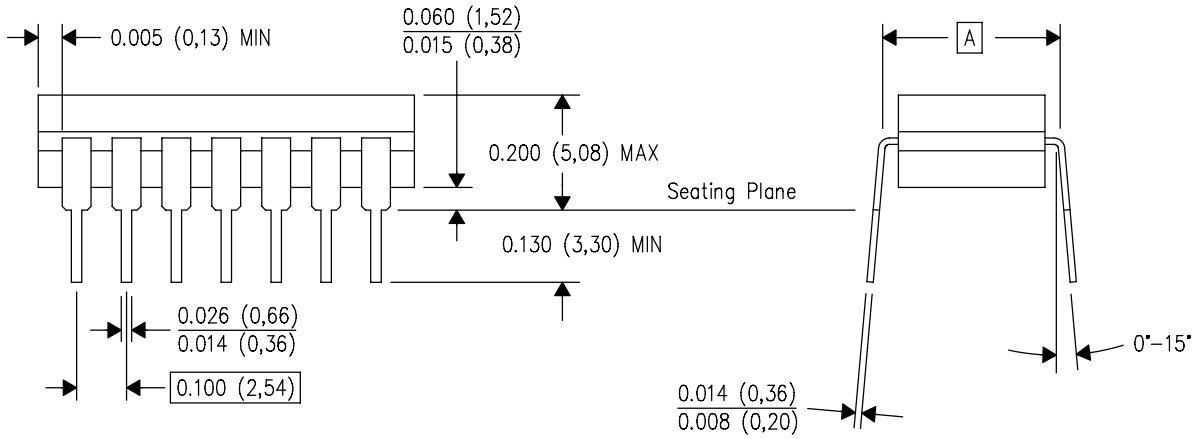
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



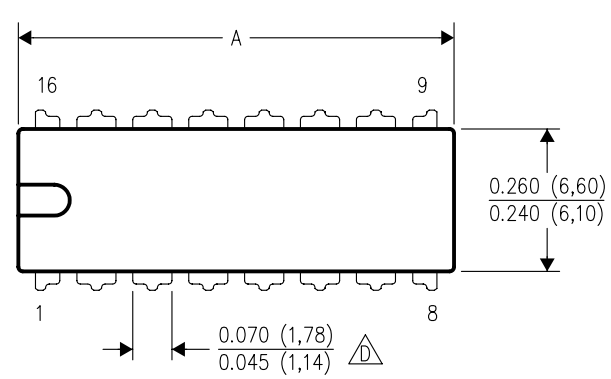
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

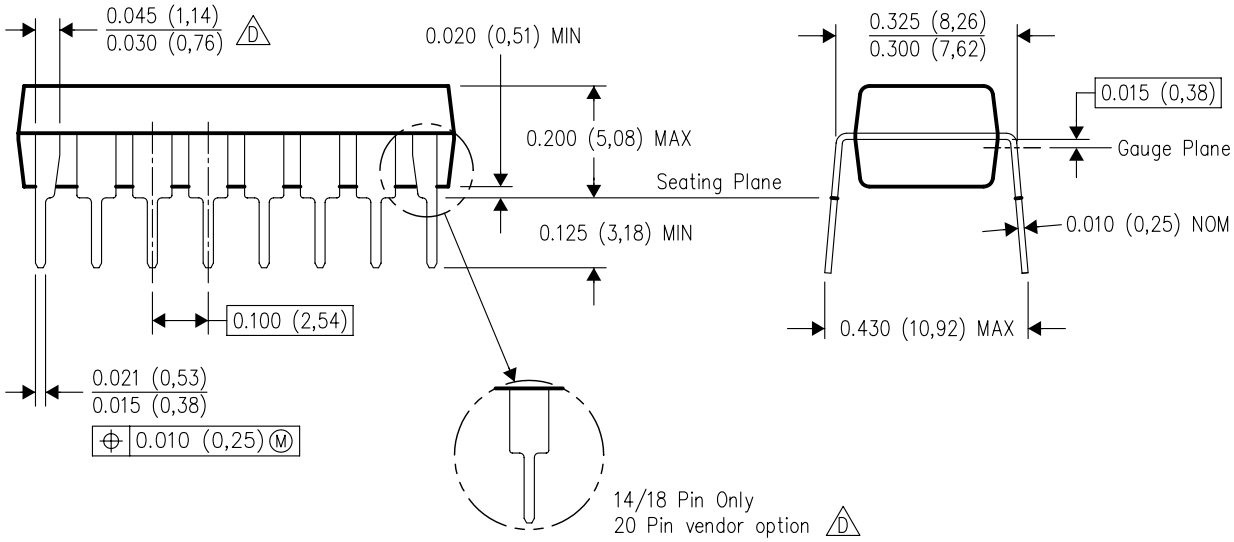
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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