

CMOS Ripple-Carry Binary Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4020B - 14 Stage

CD4024B - 7 Stage

CD4040B - 12 Stage

■ CD4020B, CD4024B, and CD4040B are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

The CD4020B and CD4040B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4040B type also is supplied in 16-lead small-outline packages (M and M96 suffixes).

The CD4024B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (PD):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55 $^\circ\text{C}$ to +125 $^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

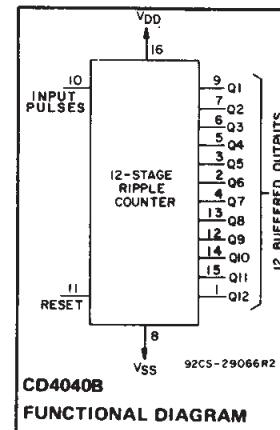
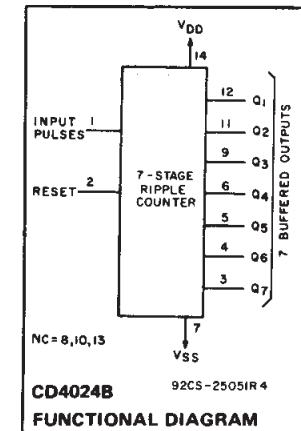
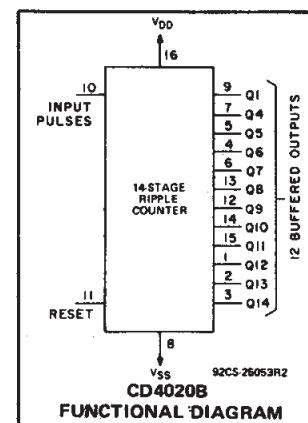
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max +265 $^\circ\text{C}$

Features:

- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- Fully static operation
- Common reset
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25 $^\circ\text{C}$
- Noise margin (over full package-temperature range): 1 V at $V_{DD} = 5\text{V}$
2 V at $V_{DD} = 10\text{V}$
2.5 V at $V_{DD} = 15\text{V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

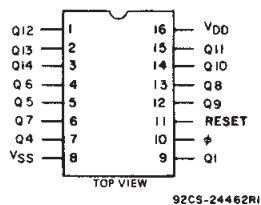
Applications:

- Control counters
- Frequency dividers
- Timers
- Time-delay circuits

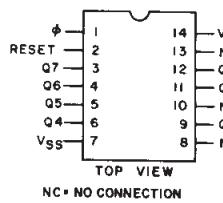


TERMINAL ASSIGNMENTS

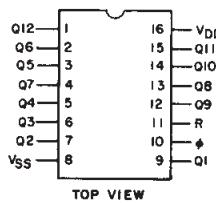
CD4020B



CD4024B



CD4040B



CD4020B, CD4024B, CD4040B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at $T_A = 25^\circ\text{C}$)		3	18	V
Input-Pulse Frequency, f_ϕ	5	—	3.5	MHz
	10	—	8	
	15	—	12	
Input-Pulse Width, t_W	5	140	—	
	10	60	—	ns
	15	40	—	
Input-Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$	5	Unlimited		μs
	10			
	15			
Reset Pulse Width, t_W	5	200	—	ns
	10	80	—	
	15	60	—	
Reset Removal Time, t_{REM}	5	350	—	ns
	10	150	—	
	15	100	—	

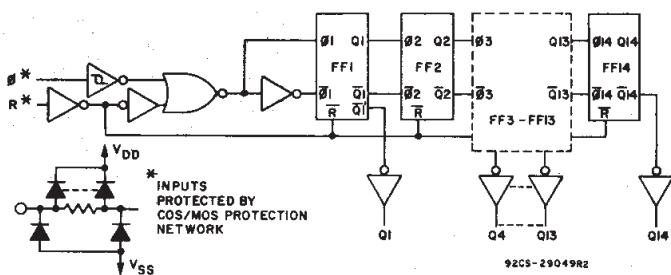


Fig. 1 – Logic diagram for CD4020B.

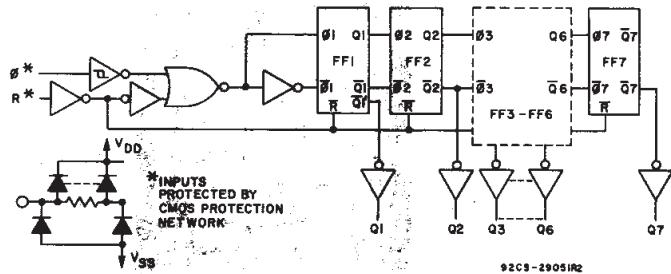


Fig. 2 – Logic diagram for CD4024B.

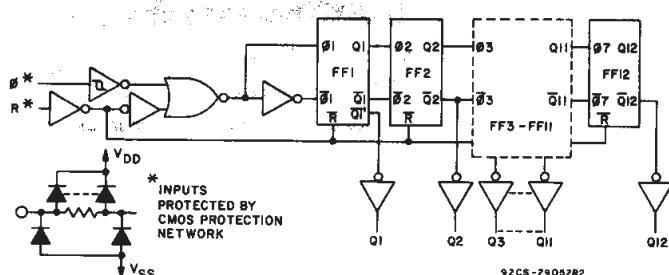
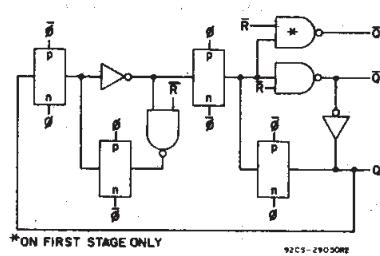


Fig. 3 – Logic diagram for CD4040B.



*ON FIRST STAGE ONLY

Fig. 4 – Detail of typical flip-flop stage.

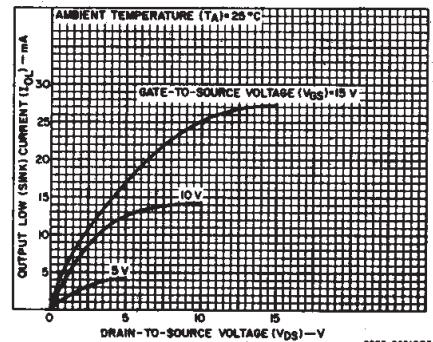


Fig. 5 – Typical output low (sink) current characteristics.

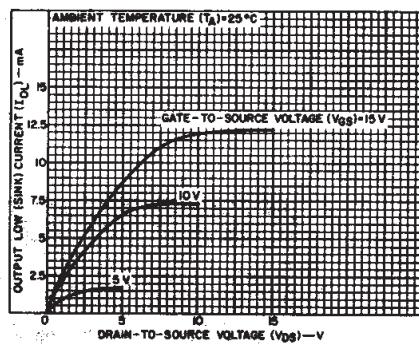


Fig. 6 – Minimum output low (sink) current characteristics.

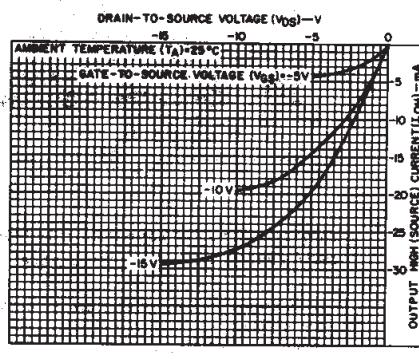


Fig. 7 – Typical output high (source) current characteristics.

CD4020B, CD4024B, CD4040B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS		LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0,04	5	μA
	—	0,10	10	10	10	300	300	—	0,04	10	
	—	0,15	15	20	20	600	600	—	0,04	20	
	—	0,20	20	100	100	3000	3000	—	0,08	100	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—	
Output Voltage: Low-Level, VOL Max.	—	0,5	5	0,05				—	0	0,05	V
	—	0,10	10	0,05				—	0	0,05	
	—	0,15	15	0,05				—	0	0,05	
Output Voltage: High-Level, VOH Min.	—	0,5	5	4,95				4,95	5	—	V
	—	0,10	10	9,95				9,95	10	—	
	—	0,15	15	14,95				14,95	15	—	
Input Low Voltage, V _{IL} Max.	0,5, 4,5	—	5	1,5				—	—	1,5	V
	1,9	—	10	3				—	—	3	
	1,5, 13,5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0,5, 4,5	—	5	3,5				3,5	—	—	V
	1,9	—	10	7				7	—	—	
	1,5, 13,5	—	15	11				11	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0,1	±0,1	±1	±1	—	±10 ⁻⁵	±0,1	μA

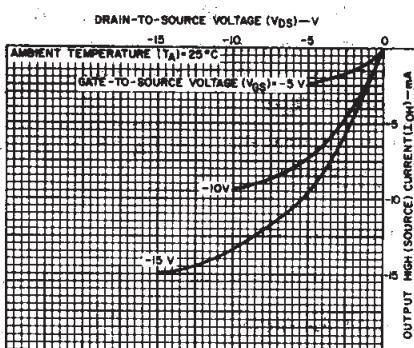


Fig. 8 - Minimum output high (source) current characteristics

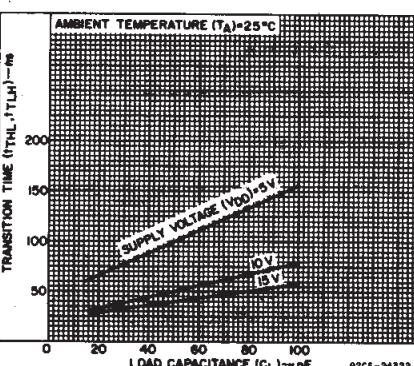
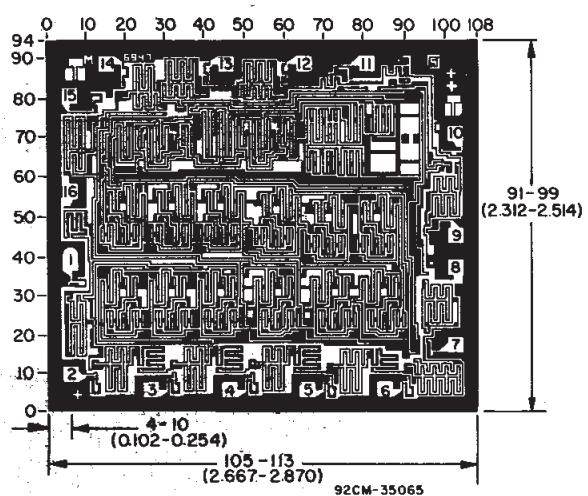
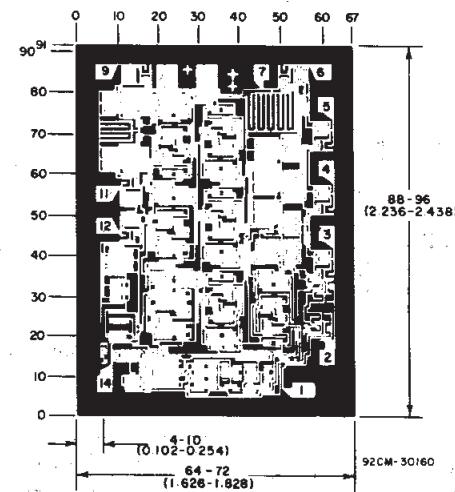


Fig. 9 – Typical transition time as a function of load capacitance.



Dimensions and Pad Layout for CD40208H. Dimensions and pad layout for CD4040BH are identical.



Dimensions and Pad Layout for CD4024BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CD4020B, CD4024B, CD4040B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20 \text{ ns}$,
 $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS			UNITS	
			Min.	Typ.	Max.		
Input-Pulse Operation							
Propagation Delay Time, ϕ to Q_1 Out; t_{PHL}, t_{PLH}		5	—	180	360	ns	
		10	—	80	160		
		15	—	65	130		
Q_n to Q_{n+1} ; t_{PHL}, t_{PLH}		5	—	100	330	ns	
		10	—	40	80		
		15	—	30	60		
Transition Time, t_{THL}, t_{TLH}		5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Minimum Input-Pulse Width, t_W		5	—	70	140	ns	
		10	—	30	60		
		15	—	20	40		
Input-Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$		5	Unlimited			μs	
		10	Unlimited				
		15	Unlimited				
Maximum Input-Pulse Frequency, f_ϕ		5	3.5	7	—	MHz	
		10	8	16	—		
		15	12	24	—		
Input Capacitance, C_I	Any Input	—	5	7.5	pF		
Reset Operation							
Propagation Delay Time, t_{PHL}		5	—	140	280	ns	
		10	—	60	120		
		15	—	50	100		
Minimum Reset Pulse Width, t_W		5	—	100	200	ns	
		10	—	40	80		
		15	—	30	60		
Reset Removal Time, t_{REM}		5	—	175	350	ns	
		10	—	75	150		
		15	—	50	100		

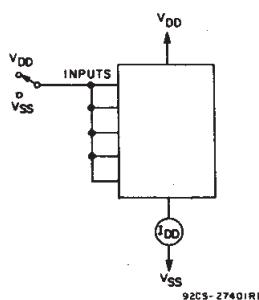


Fig. 13 – Quiescent device
current test circuit.

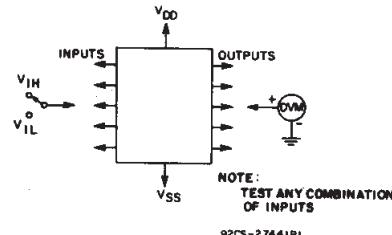


Fig. 14 – Input voltage test circuits.

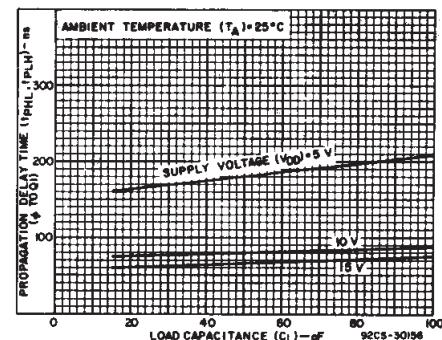


Fig. 10 – Typical propagation delay time as a function of load capacitance (ϕ to Q_1).

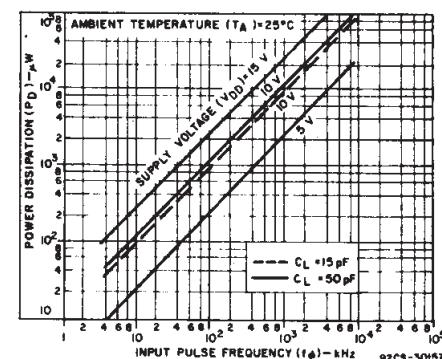


Fig. 11 – Typical dynamic power dissipation as a function of input pulse frequency for CD4020B.

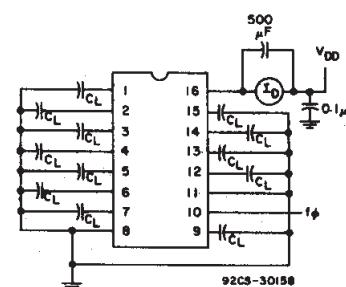


Fig. 12 – Dynamic power dissipation test circuit for CD4020B.

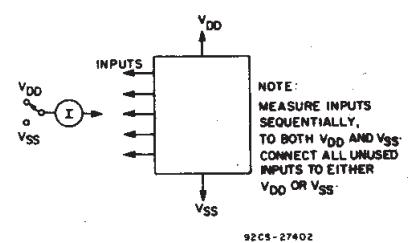


Fig. 15 – Input current test circuit.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4020BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4020BE
CD4020BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4020BE
CD4020BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4020BE
CD4020BF	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4020BF
CD4020BF.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4020BF
CD4020BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4020BF3A
CD4020BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4020BF3A
CD4020BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4020B
CD4020BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4020B
CD4020BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM020B
CD4020BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM020B
CD4020BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM020B
CD4024BE	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4024BE
CD4024BE.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4024BE
CD4024BEE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4024BE
CD4024BF	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4024BF
CD4024BF.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4024BF
CD4024BF3A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4024BF3A
CD4024BF3A.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4024BF3A
CD4024BM	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	CD4024BM
CD4024BM96	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4024BM
CD4024BM96.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4024BM
CD4024BMT	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	CD4024BM
CD4024BNSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4024B
CD4024BNSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4024B
CD4024BPW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-55 to 125	CM024B
CD4024BPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	CM024B
CD4024BPWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM024B
CD4040BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4040BE

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4040BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4040BE
CD4040BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4040BE
CD4040BF	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4040BF
CD4040BF.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4040BF
CD4040BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4040BF3A
CD4040BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4040BF3A
CD4040BM	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4040BM
CD4040BM.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4040BM
CD4040BM96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4040BM
CD4040BM96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4040BM
CD4040BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4040B
CD4040BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4040B
CD4040BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM040B
CD4040BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM040B
CD4040BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM040B
CD4040BPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM040B
JM38510/05653BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05653BEA
JM38510/05653BEA.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05653BEA
JM38510/05655BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05655BCA
JM38510/05655BCA.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05655BCA
M38510/05653BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05653BEA
M38510/05655BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05655BCA

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

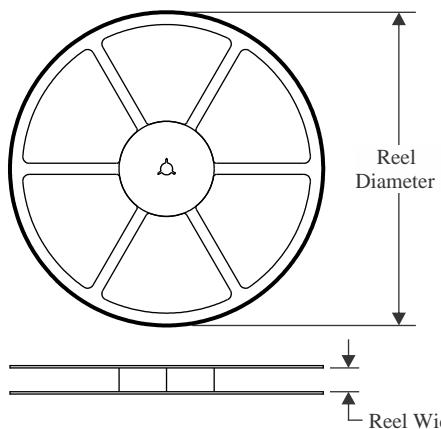
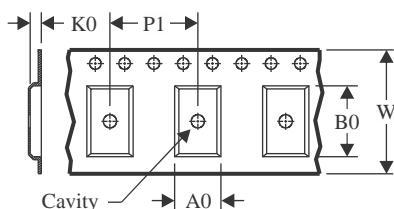
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4020B, CD4020B-MIL, CD4024B, CD4024B-MIL, CD4040B, CD4040B-MIL :

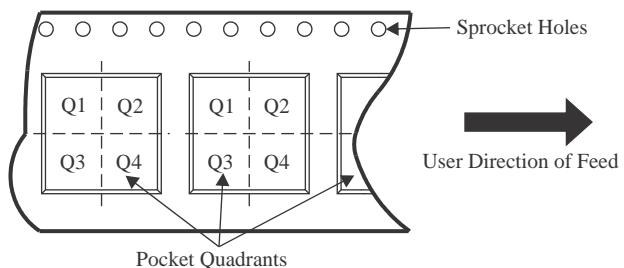
- Catalog : [CD4020B](#), [CD4024B](#), [CD4040B](#)
- Military : [CD4020B-MIL](#), [CD4024B-MIL](#), [CD4040B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


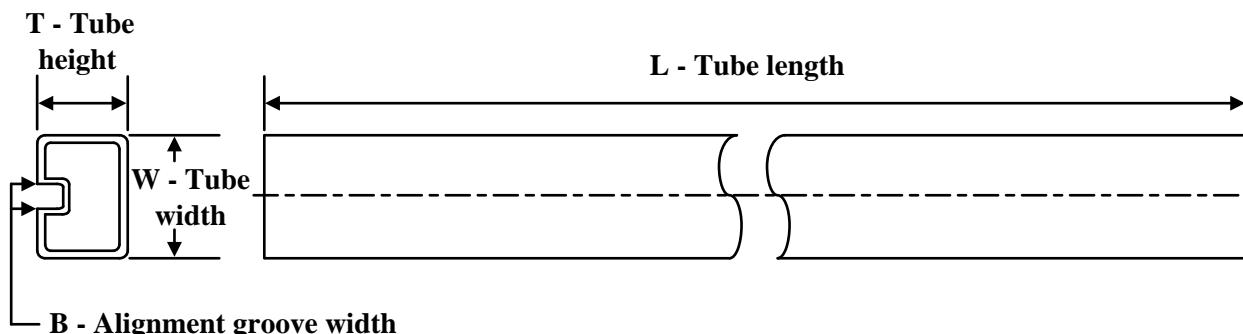
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4020BNSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD4020BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4024BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4024BNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4024BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4040BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4040BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4040BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4020BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4020BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD4024BM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4024BNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4024BPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
CD4040BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4040BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4040BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

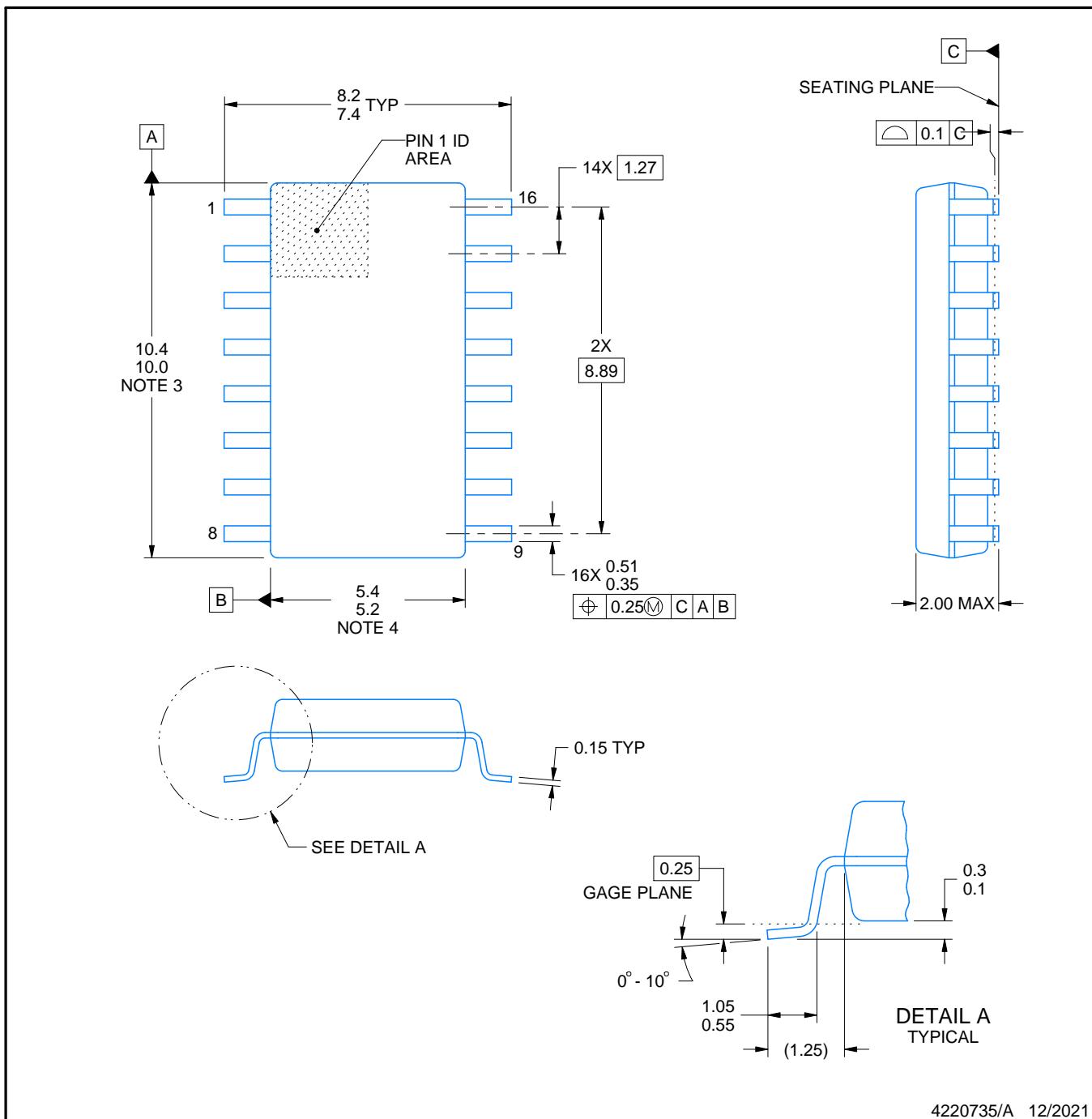
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4020BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4020BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4020BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4020BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4020BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4020BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4024BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4024BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4024BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4040BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4040BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4040BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4040BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4040BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4040BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4040BM	D	SOIC	16	40	507	8	3940	4.32
CD4040BM.A	D	SOIC	16	40	507	8	3940	4.32



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



NOTES:

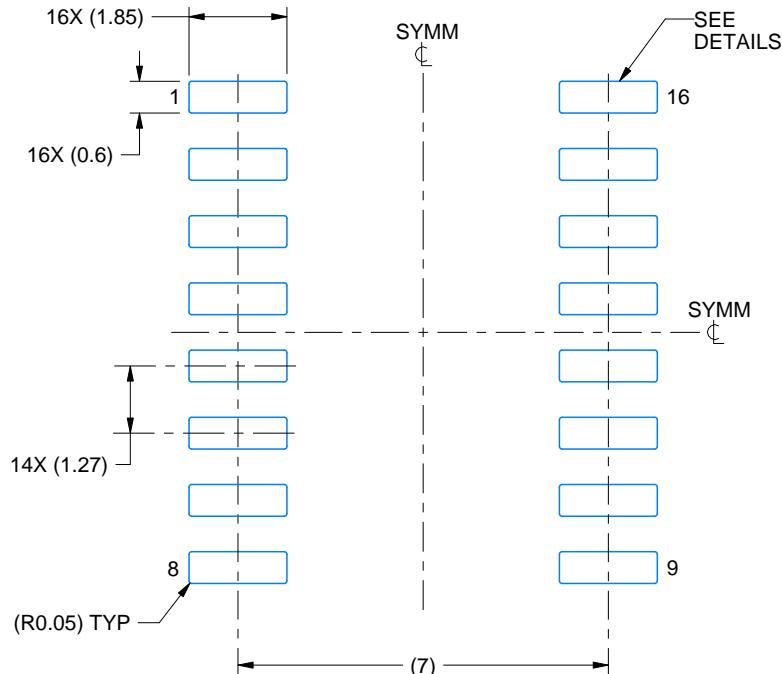
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

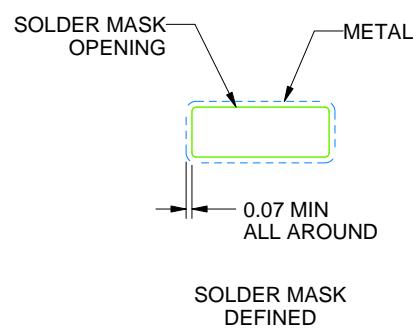
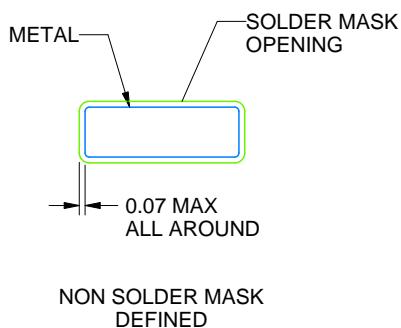
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

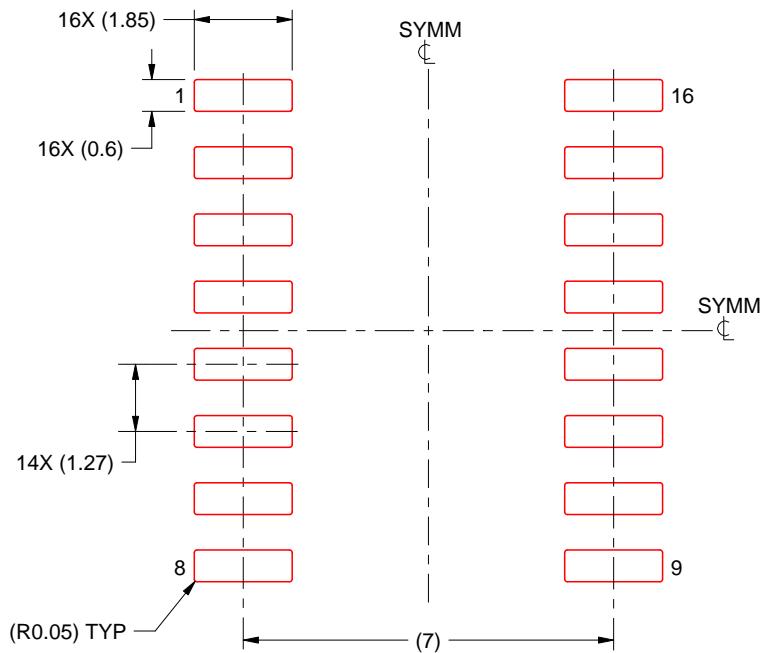
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

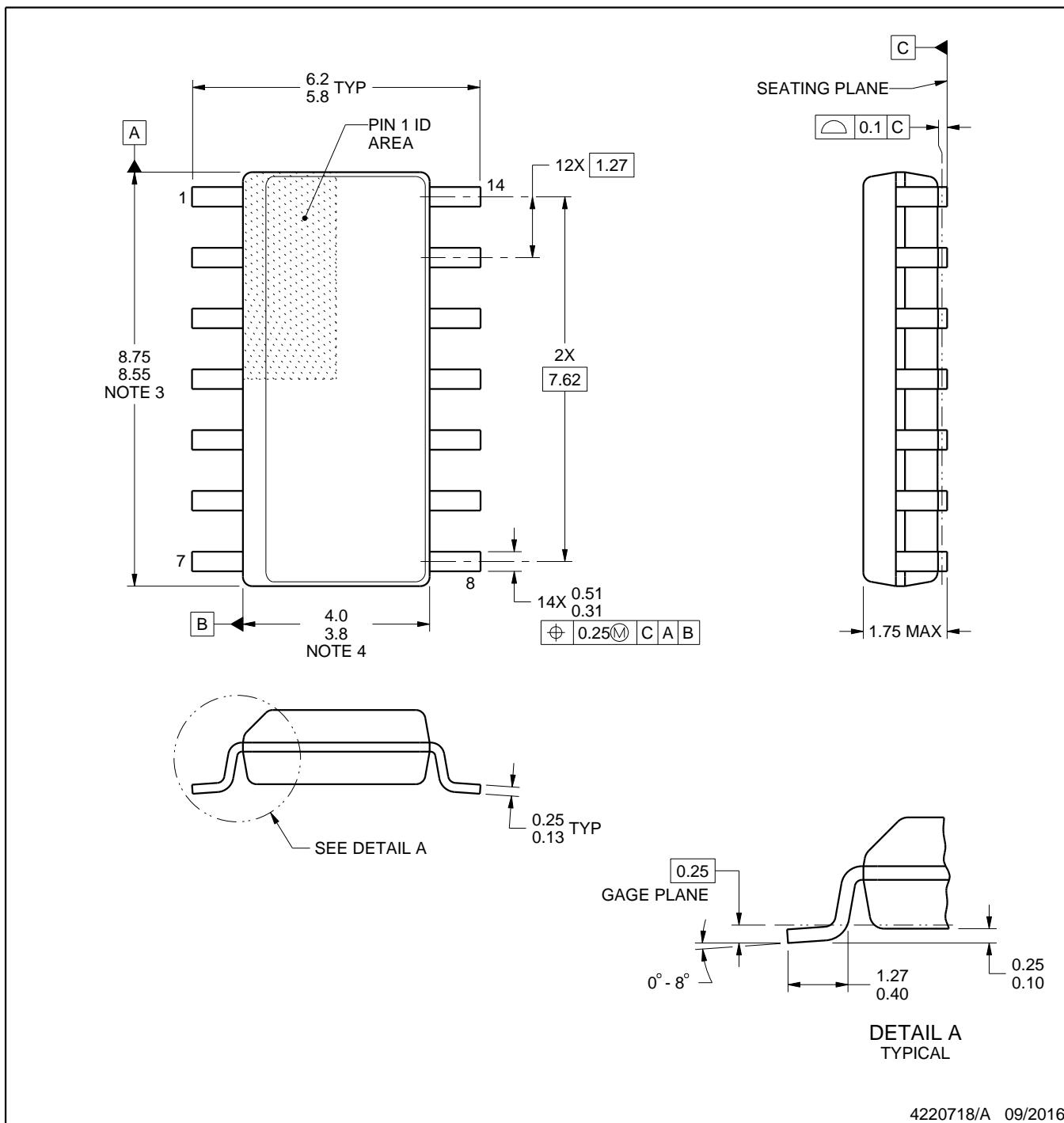
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

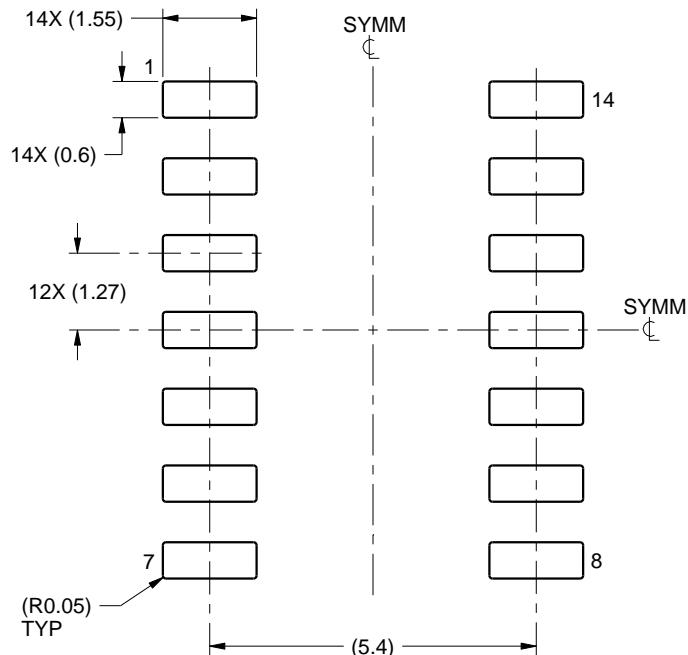
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

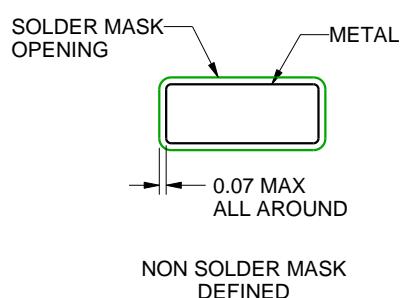
D0014A

SOIC - 1.75 mm max height

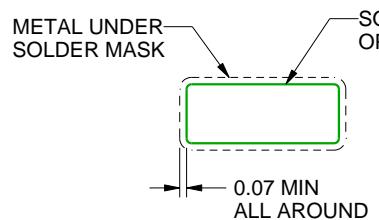
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

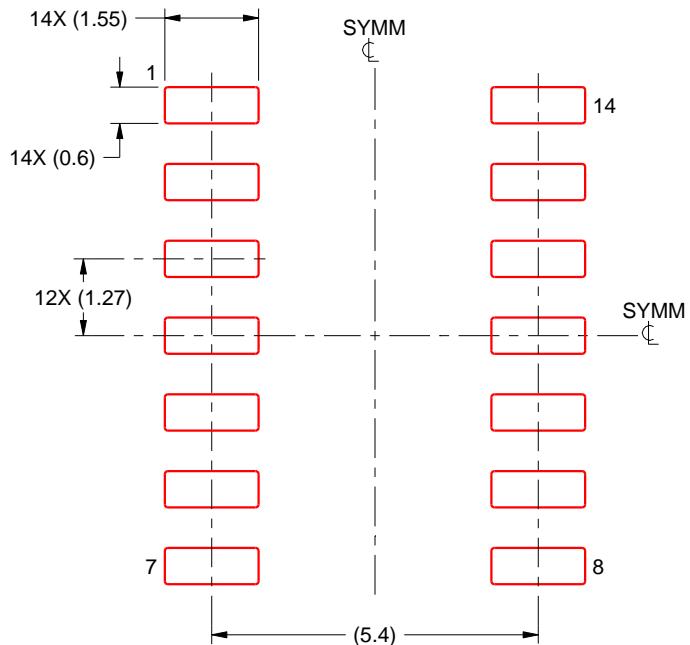
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

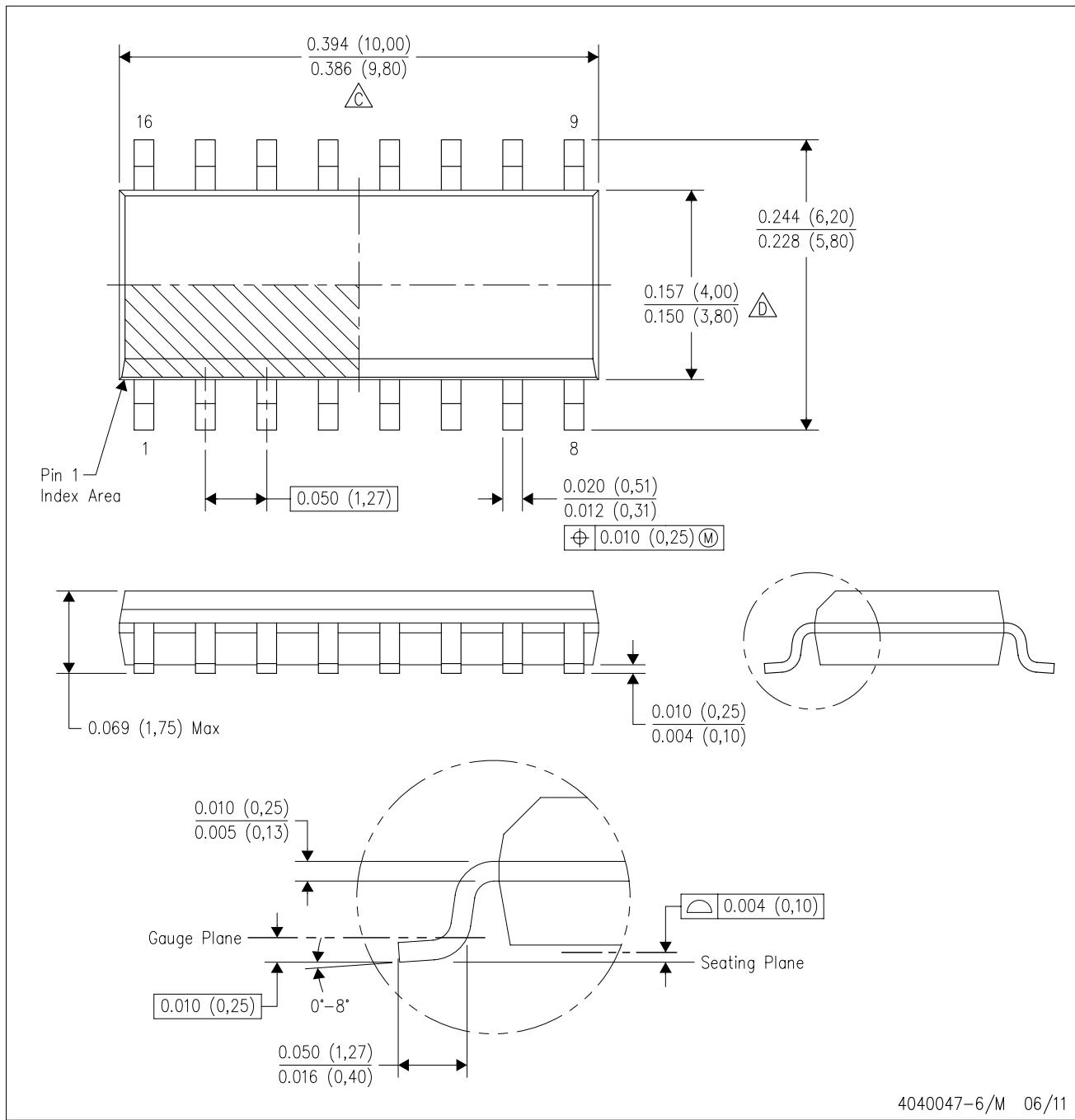
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

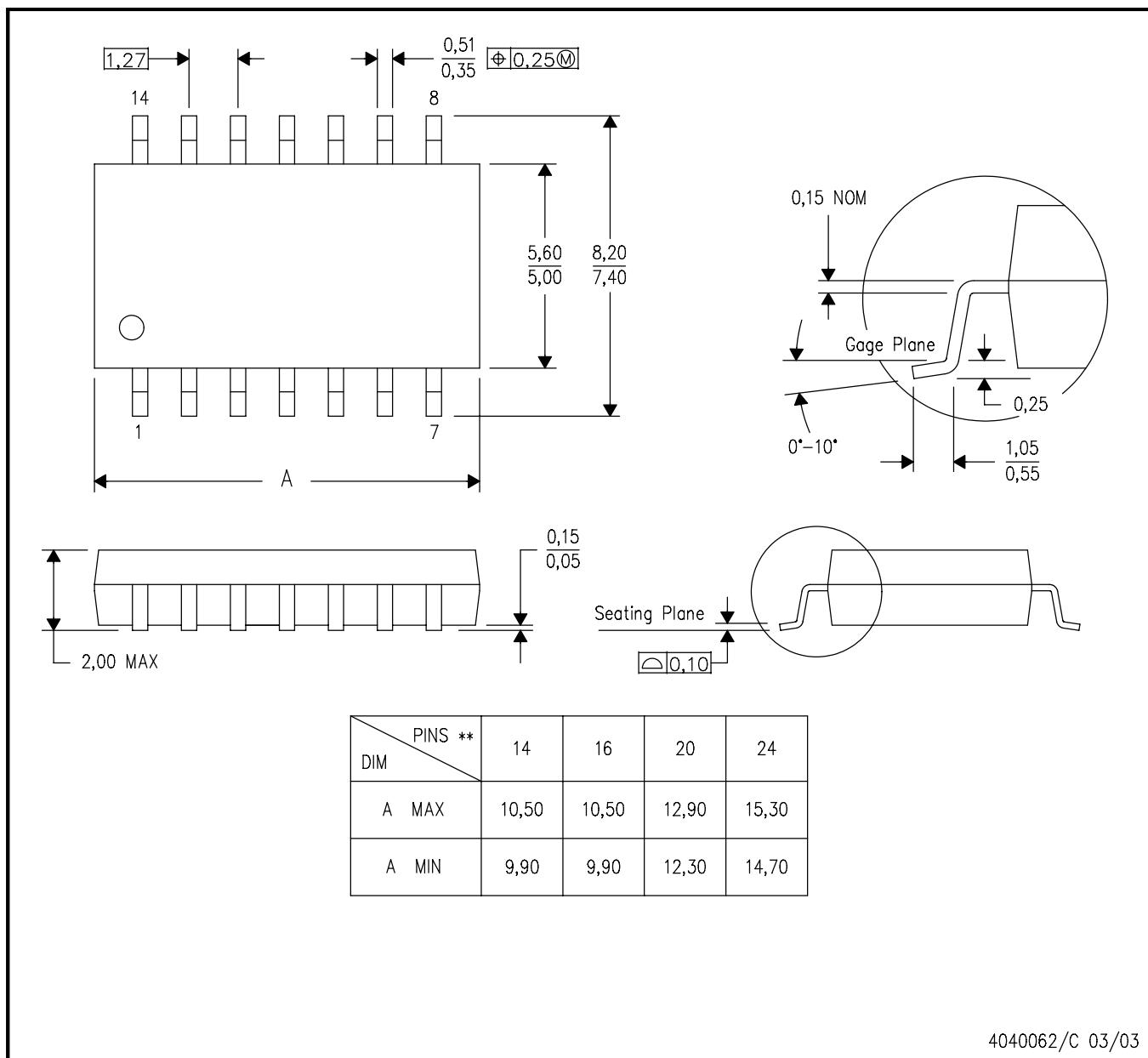
E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



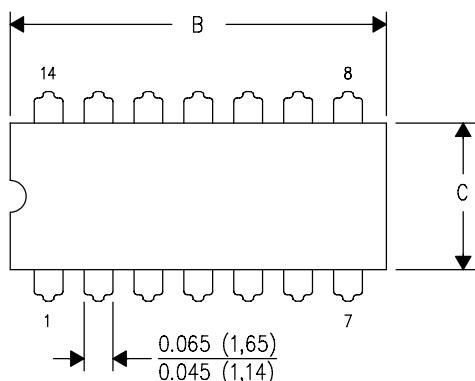
NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

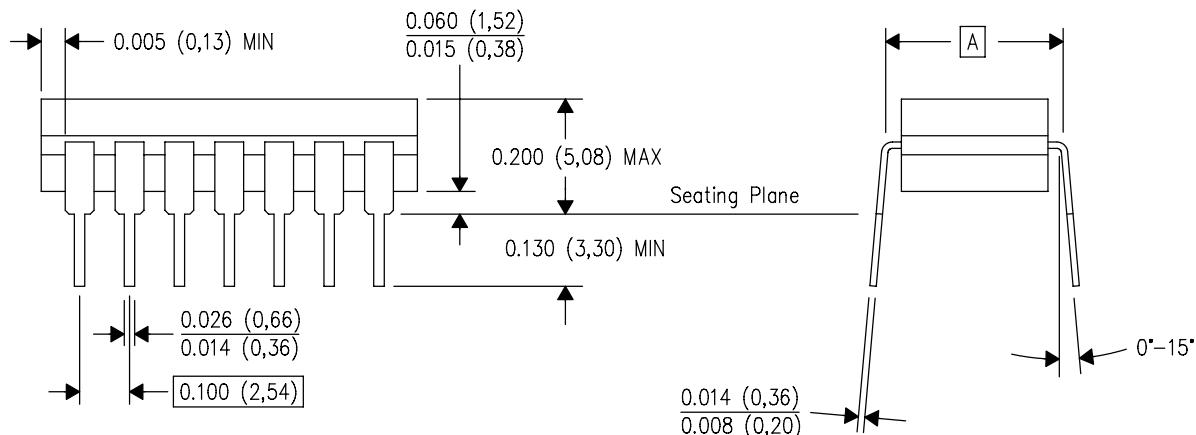
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

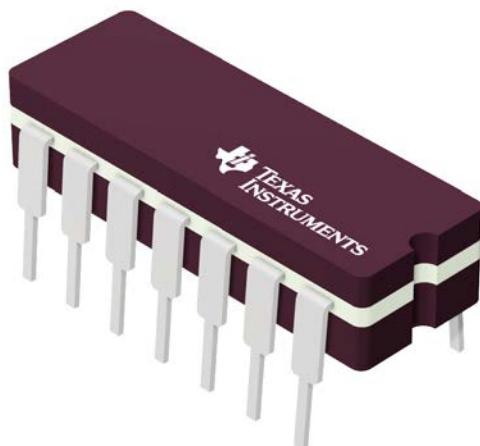
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

J 14

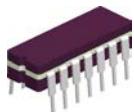
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

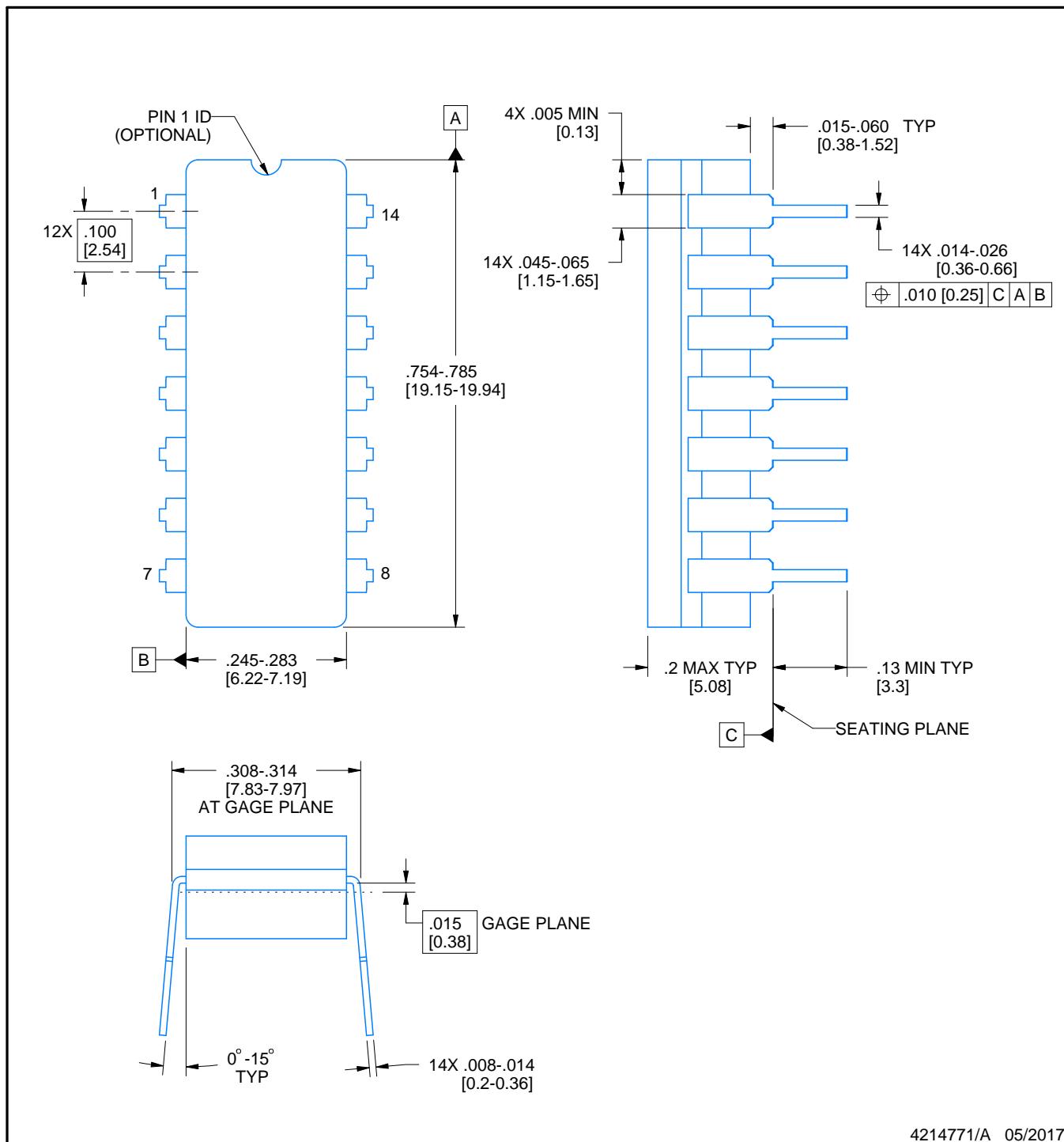


PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

J0014A



4214771/A 05/2017

NOTES:

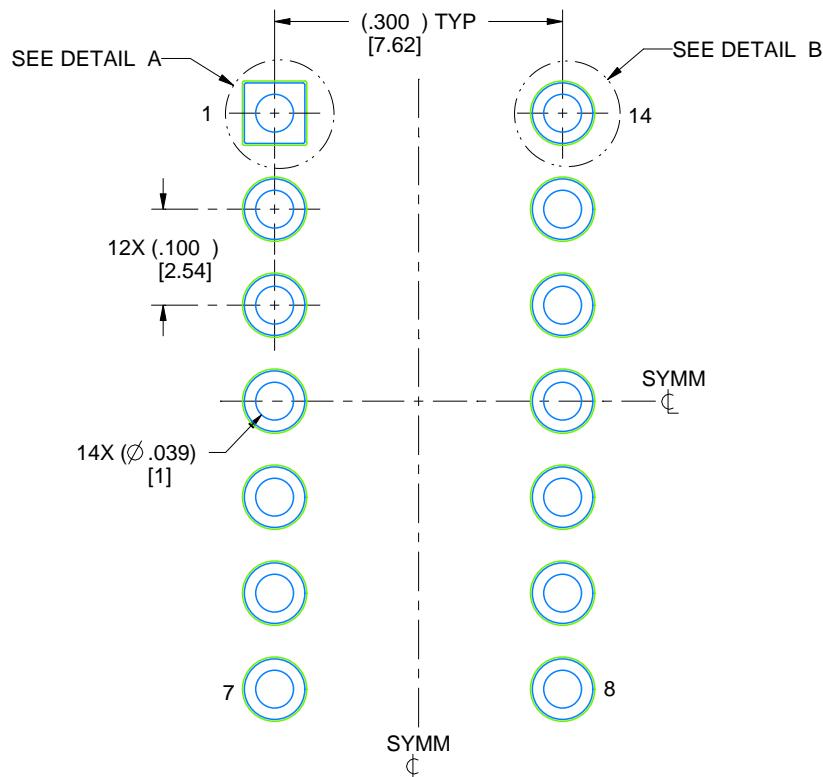
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

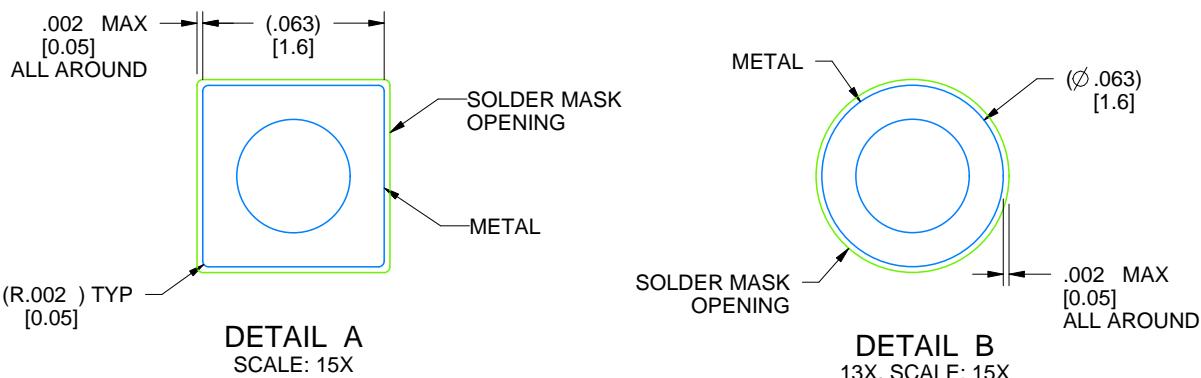
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

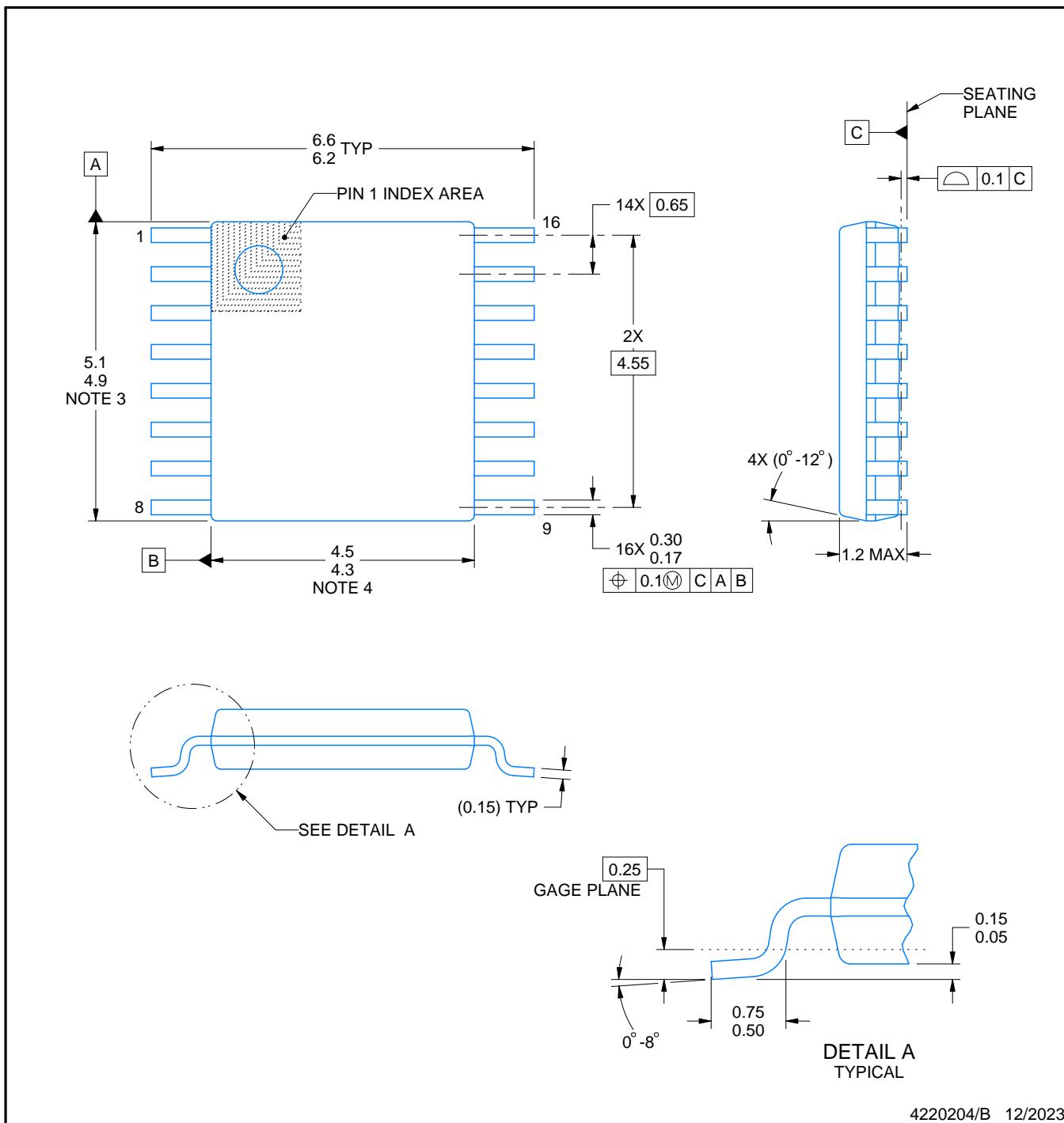
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

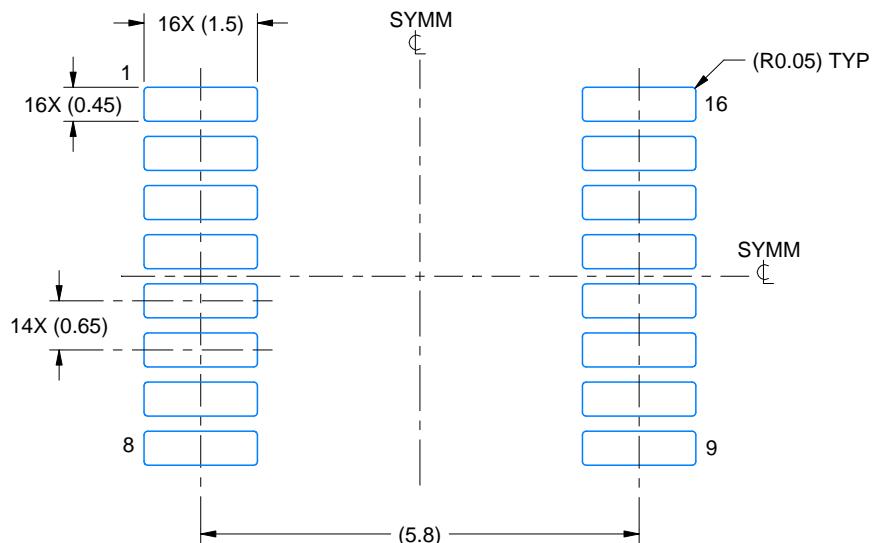
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

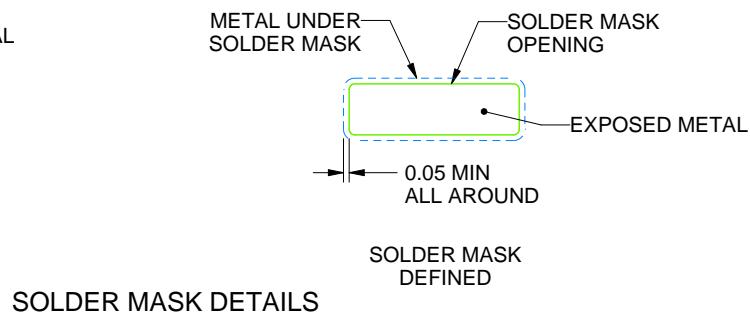
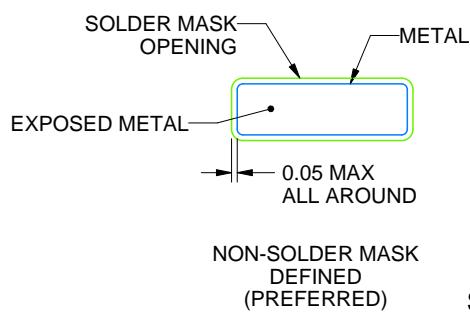
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

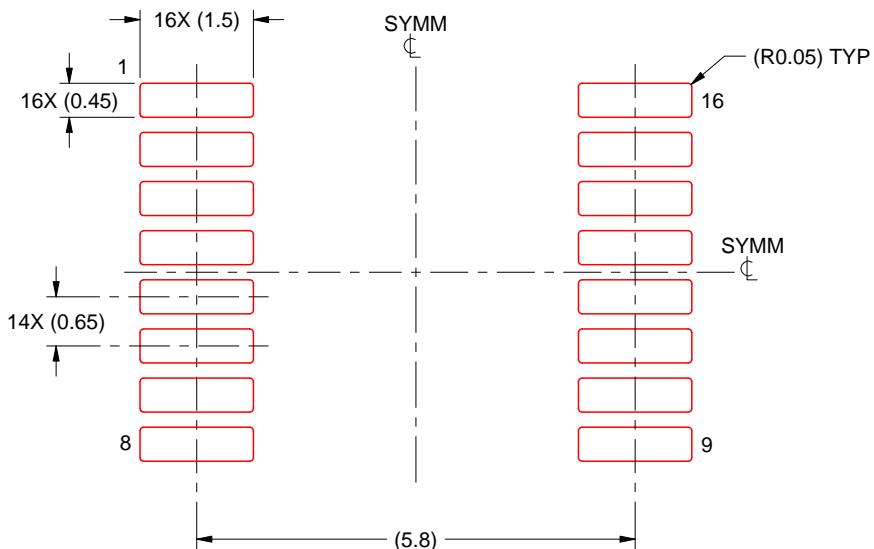
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

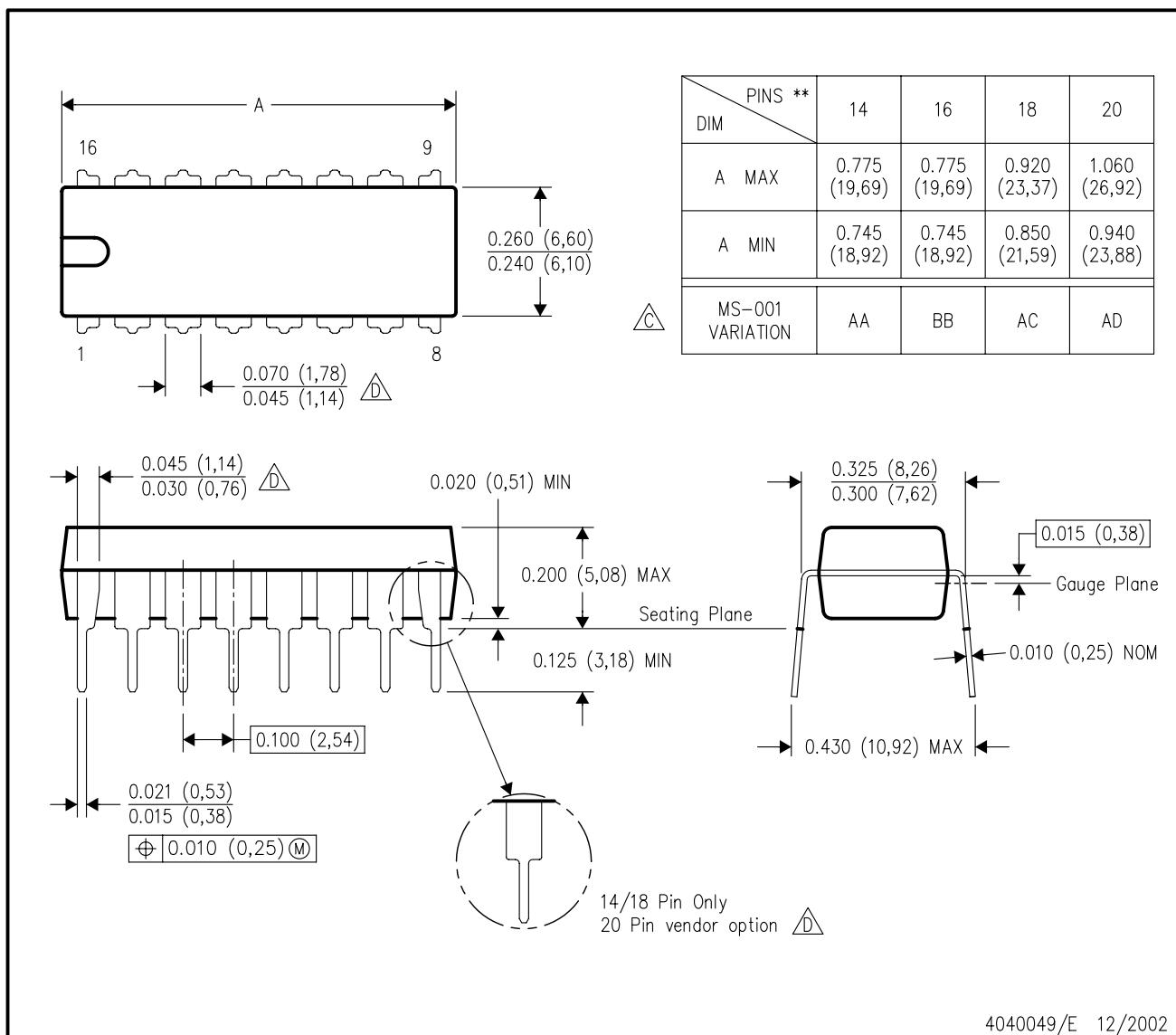
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



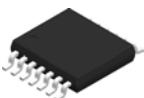
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

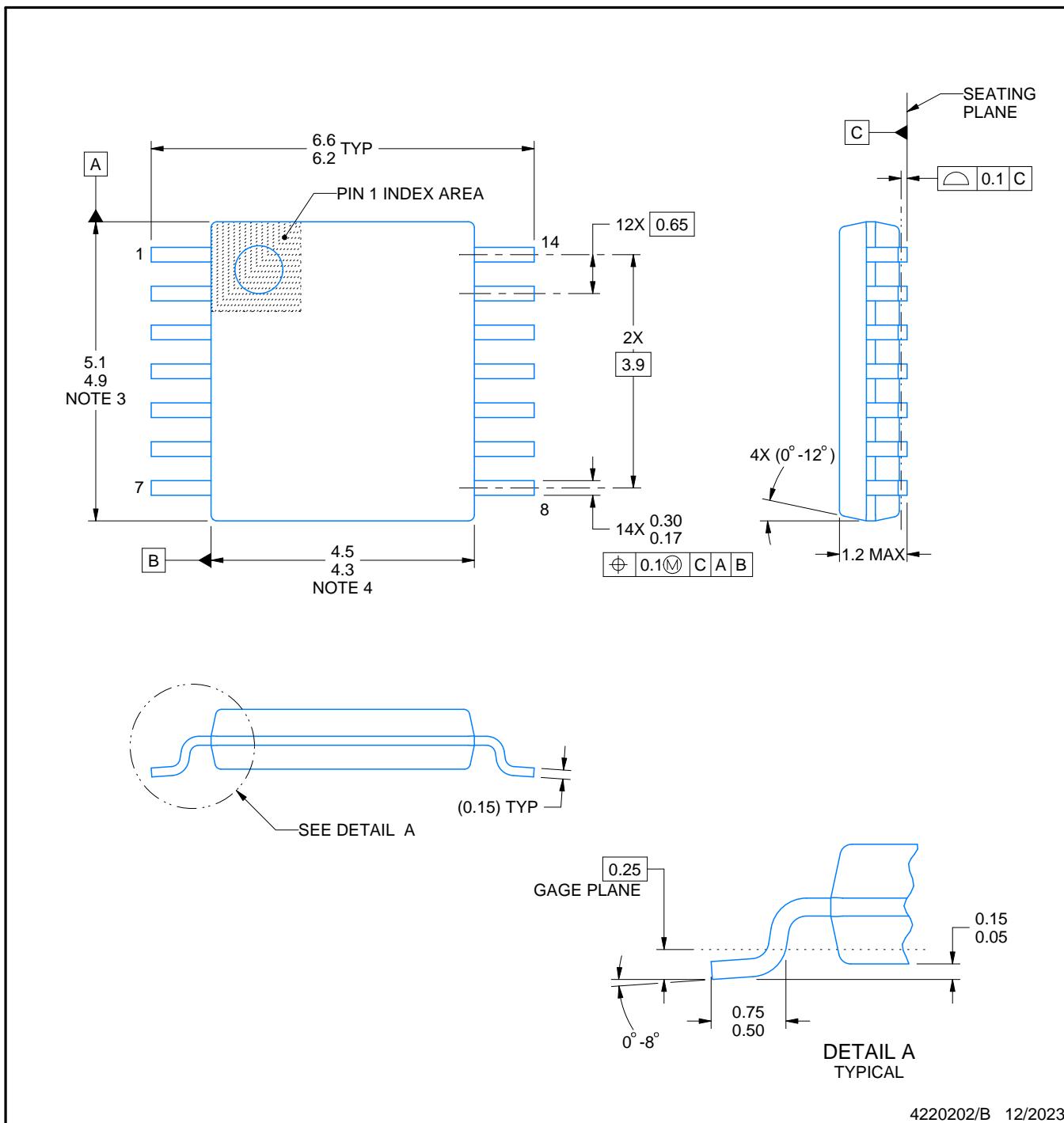
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

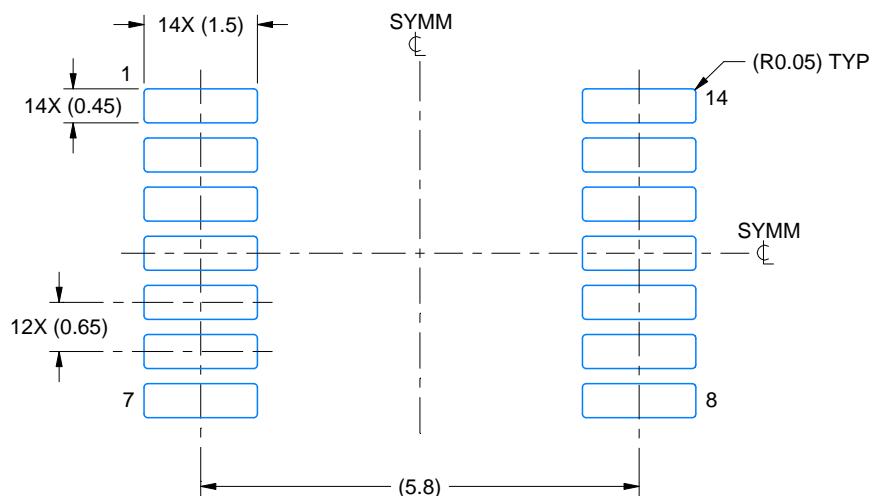
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

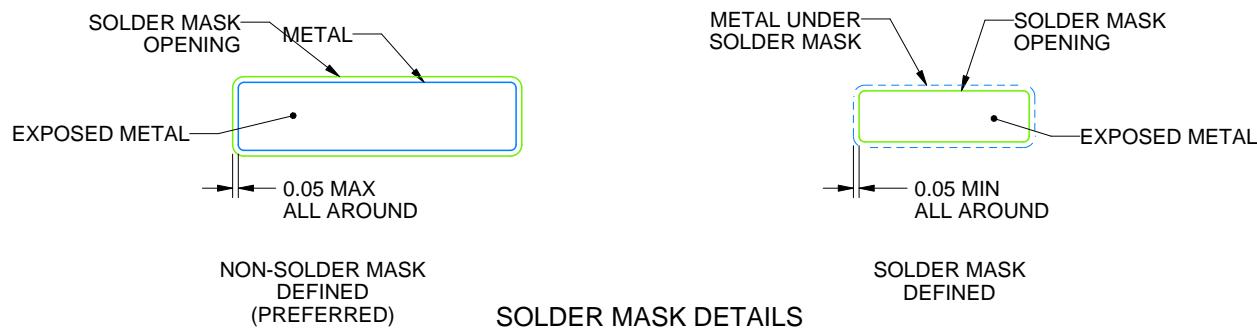
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

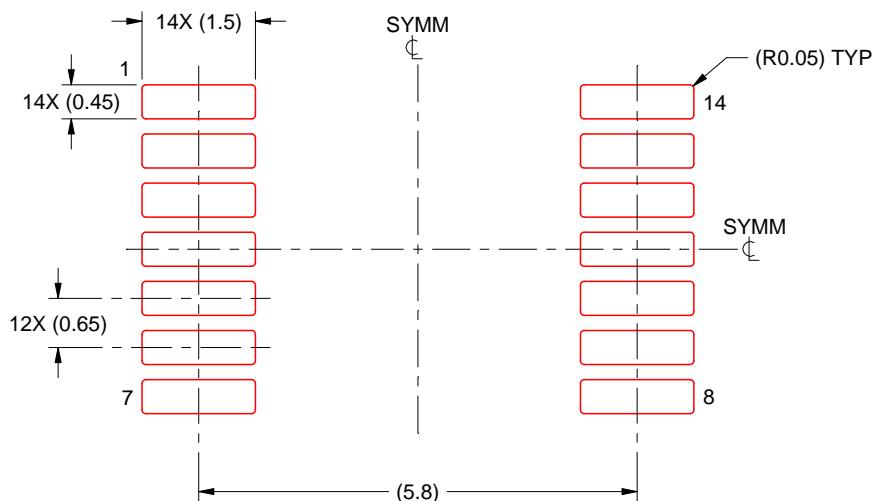
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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