

CMOS 8-Input NOR/OR Gate

High-Voltage Types (20-Volt Rating)

■ CD4078B NOR/OR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR and OR functions and supplements the existing family of CMOS gates.

The CD4078B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Voltages referenced to V_{SS} Terminal) $-0.5V$ to $+20V$

INPUT VOLTAGE RANGE, ALL INPUTS $-0.5V$ to $V_{DD} + 0.5V$

DC INPUT CURRENT, ANY ONE INPUT $\pm 10mA$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ C$ to $+100^\circ C$ $500mW$

For $T_A = +100^\circ C$ to $+125^\circ C$ Derate Linearity at $12mW/^\circ C$ to $200mW$

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) $100mW$

OPERATING-TEMPERATURE RANGE (T_A) $-55^\circ C$ to $+125^\circ C$

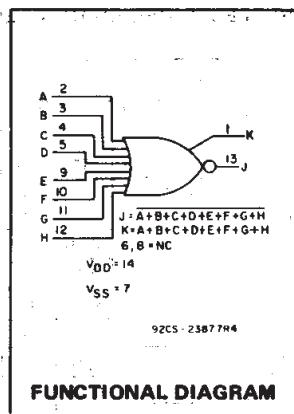
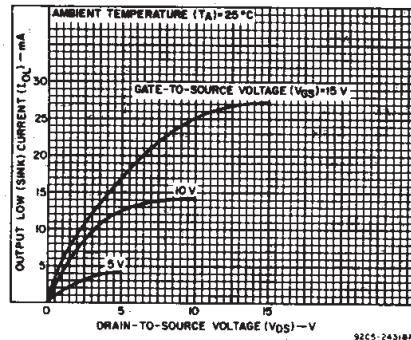
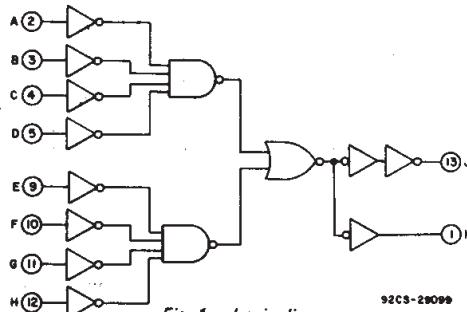
STORAGE TEMPERATURE RANGE (T_{STG}) $-65^\circ C$ to $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max $+265^\circ C$

Features:

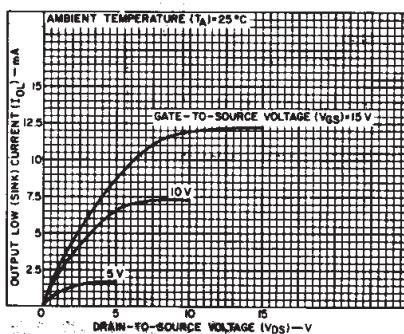
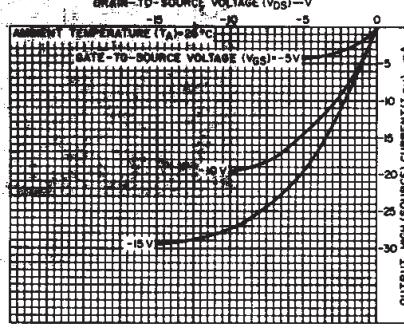
- Medium-Speed Operation:
 $t_{PHL}, t_{PLH} = 75\text{-ns (typ.)}$ at $V_{DD} = 10\text{ V}$
- Buffered inputs and output
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of $1\text{ }\mu\text{A}$ at 18 V over full package-temperature range:
 100 nA at 18 V and $25^\circ C$
- Noise margin (over full package-temperature range): 1 V at $V_{DD} = 5\text{ V}$
 2 V at $V_{DD} = 10\text{ V}$ 2.5 V at $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"


FUNCTIONAL DIAGRAM

Fig. 2 – Typical output low (sink) current characteristics.

Fig. 1 – Logic diagram.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For T_A Full Package Temperature Range)	3	18	V


Fig. 3 – Minimum output low (sink) current characteristics.

Fig. 4 – Typical output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ C$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200k\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	150	300	ns
		10	75	150	
		15	55	110	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF	

CD4078B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25				Min.	Typ.	Max.		
				-55	-40	+85	+125					
Quiescent Device Current, I _{DD} Max.	-	0,5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA	
	-	0,10	10	0.5	0.5	15	15	-	0.01	0.5		
	-	0,15	15	1	1	30	30	-	0.01	1		
	-	0,20	20	5	5	150	150	-	0.02	5		
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1		mA	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6			
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8			
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1		mA	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2			
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6			
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8			
Output Voltage: Low Level, VOL Max.	-	0,5	5	0.05				-	0	0.05	V	
	-	0,10	10	0.05				-	0	0.05		
	-	0,15	15	0.05				-	0	0.05		
Output Voltage: High-Level, VOH Min.	-	0,5	5	4.95				4.95	5		V	
	-	0,10	10	9.95				9.95	10			
	-	0,15	15	14.95				14.95	15			
Input Low Voltage, V _{IL} Max.	0,5,4,5	-	5	1.5				-	-	1.5	V	
	1,9	-	10	3				-	-	3		
	1,5,13,5	-	15	4				-	-	4		
Input High Voltage, V _{IH} Min.	0,5,4,5	-	5	3.5				3.5	-	-	V	
	1,9	-	10	7				7	-	-		
	1,5,13,5	-	15	11				11	-	-		
Input Current I _{IN} Max.				0,18	18	±0,1	±0,1	±1	±1	±10 ⁻⁵	±0,1	μA

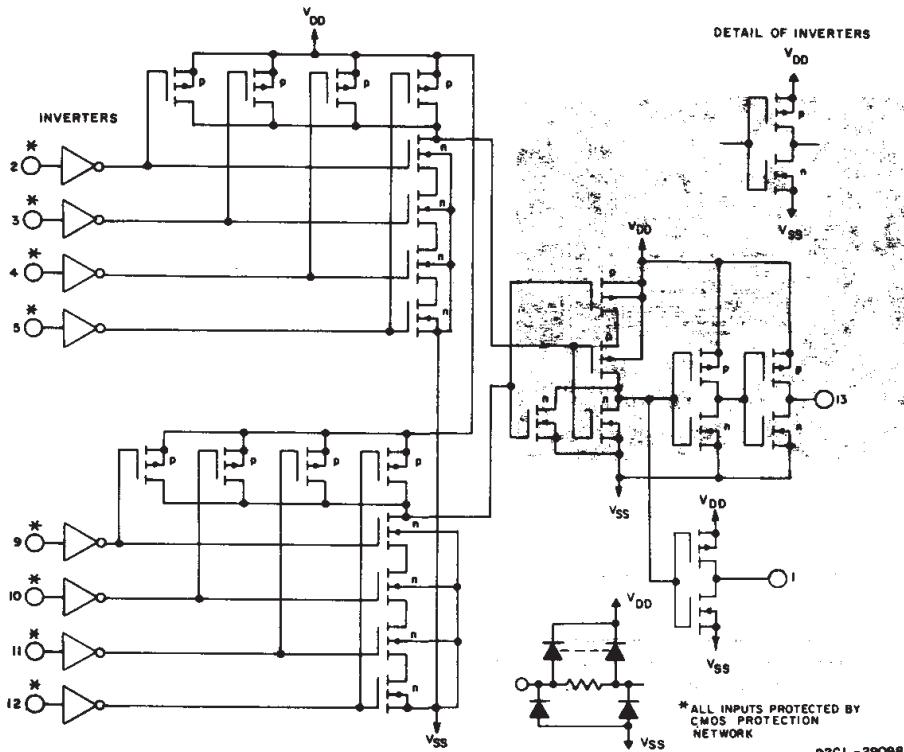


Fig. 8 — Schematic diagram.

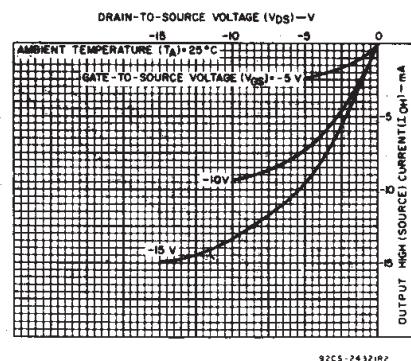


Fig. 5 — Minimum output high (source) current characteristics.

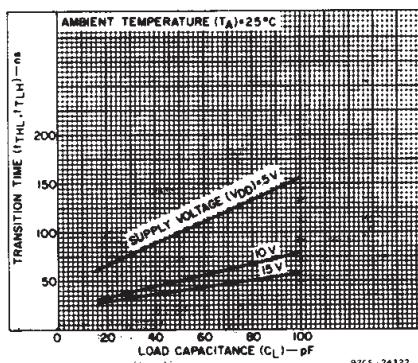


Fig. 6 — Typical transition time as a function of load capacitance.

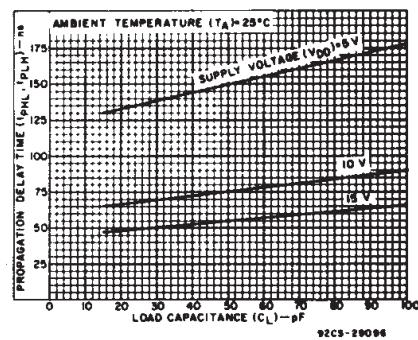


Fig. 7 — Typical propagation delay time as a function of load capacitance.

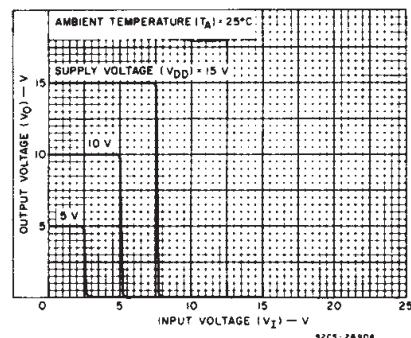


Fig. 9 — Typical voltage transfer characteristics (NOR output).

CD4078B Types

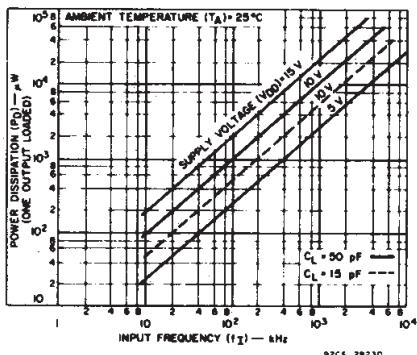


Fig. 10 – Typical dynamic power dissipation as a function of frequency.

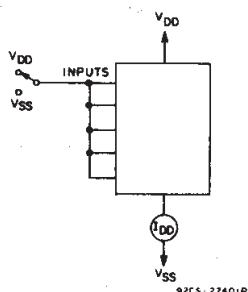


Fig. 11 – Quiescent-device-current test circuit.

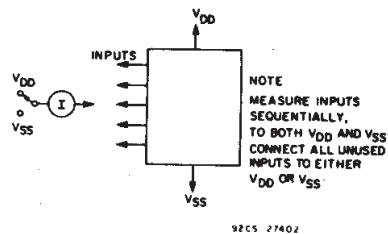


Fig. 12 – Input current test circuit.

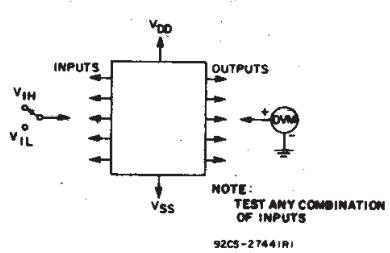


Fig. 13 – Input-voltage test circuit.

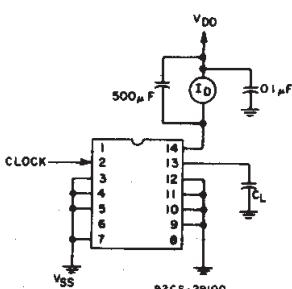
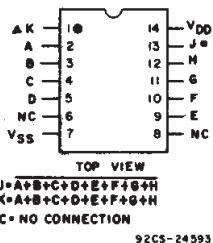
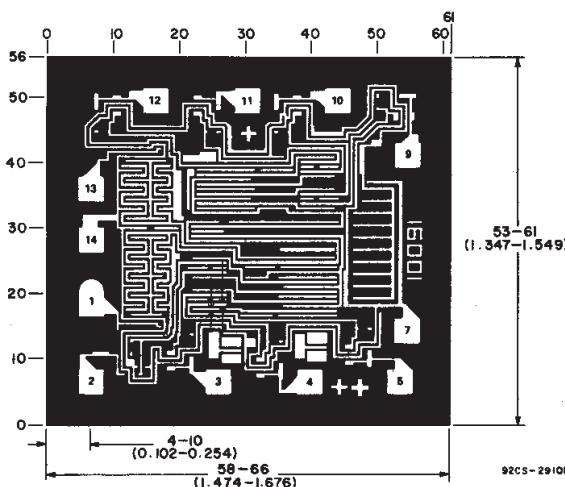


Fig. 14 – Dynamic power dissipation test circuit.



92CS-24593R2

TERMINAL ASSIGNMENT



Dimensions and pad layout for CD4078BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
7704402CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7704402CA CD4078BF3A
CD4078BE	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4078BE
CD4078BE.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4078BE
CD4078BF	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4078BF
CD4078BF.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4078BF
CD4078BF3A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7704402CA CD4078BF3A
CD4078BF3A.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7704402CA CD4078BF3A
CD4078BM	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	CD4078BM
CD4078BM96	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4078BM
CD4078BM96.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4078BM
CD4078BMT	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	CD4078BM
CD4078BNSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4078B
CD4078BNSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4078B
CD4078BPW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-55 to 125	CM078B
CD4078BPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM078B
CD4078BPWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM078B
CD4078BPWRE4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM078B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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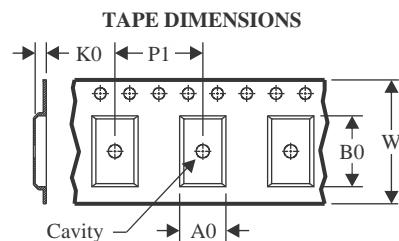
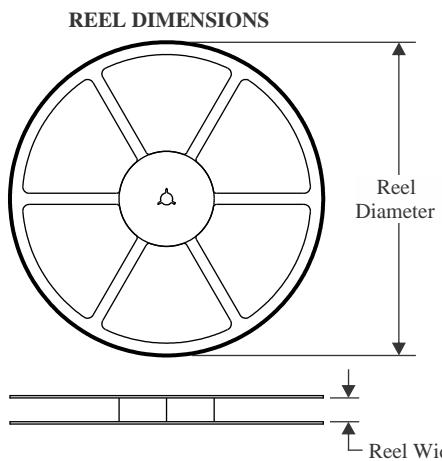
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4078B, CD4078B-MIL :

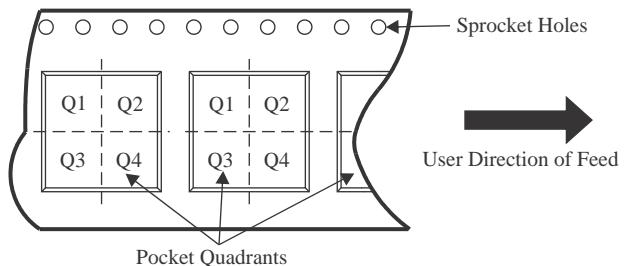
- Catalog : [CD4078B](#)
- Military : [CD4078B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

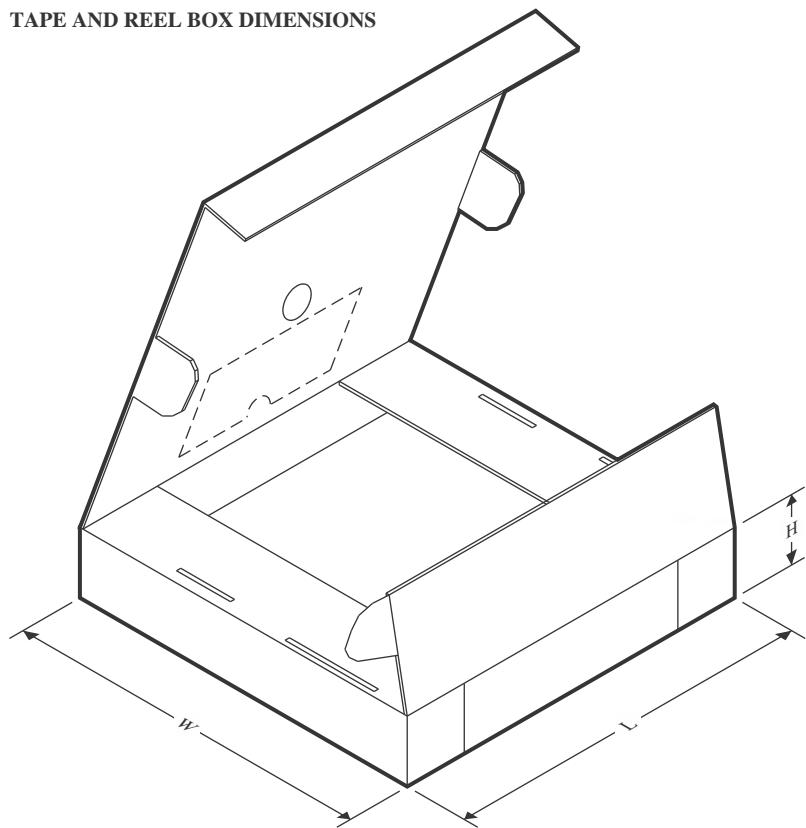
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


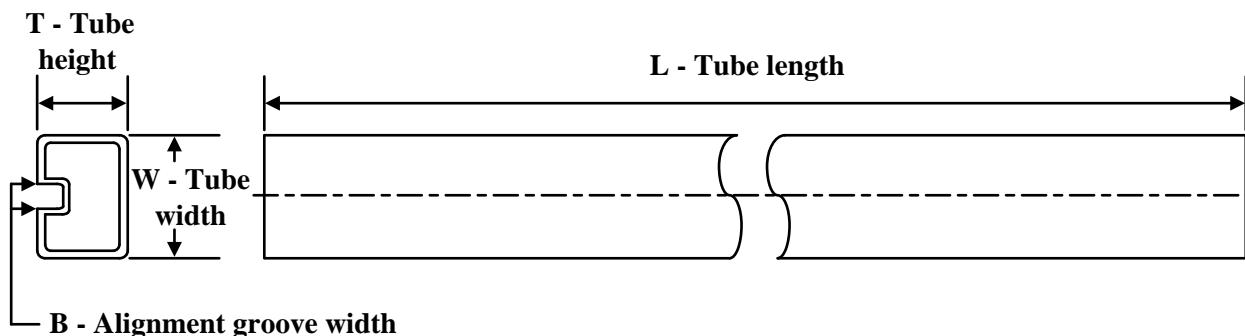
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4078BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4078BNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4078BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4078BM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4078BNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4078BPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

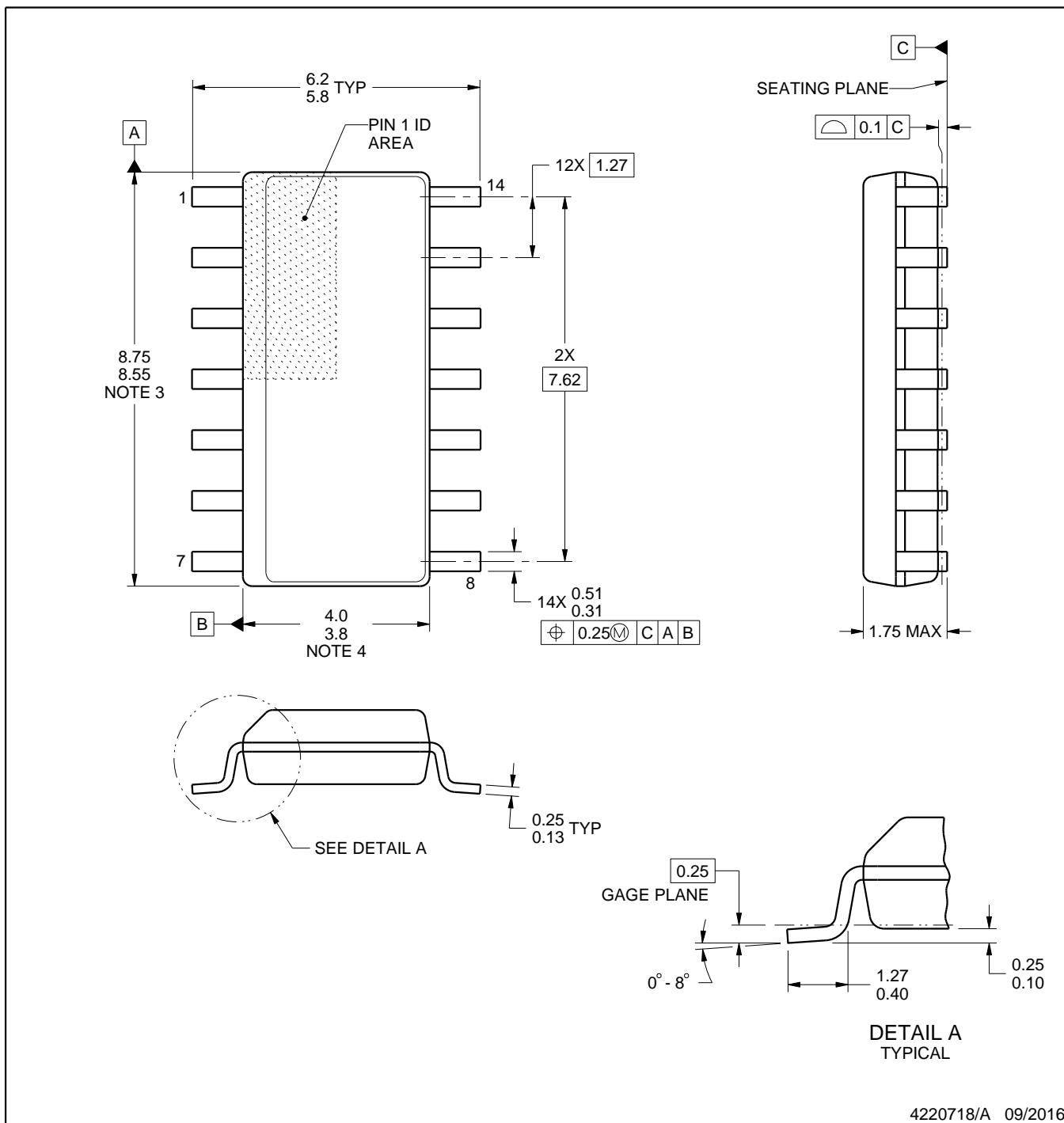
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
CD4078BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4078BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4078BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4078BE.A	N	PDIP	14	25	506	13.97	11230	4.32

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

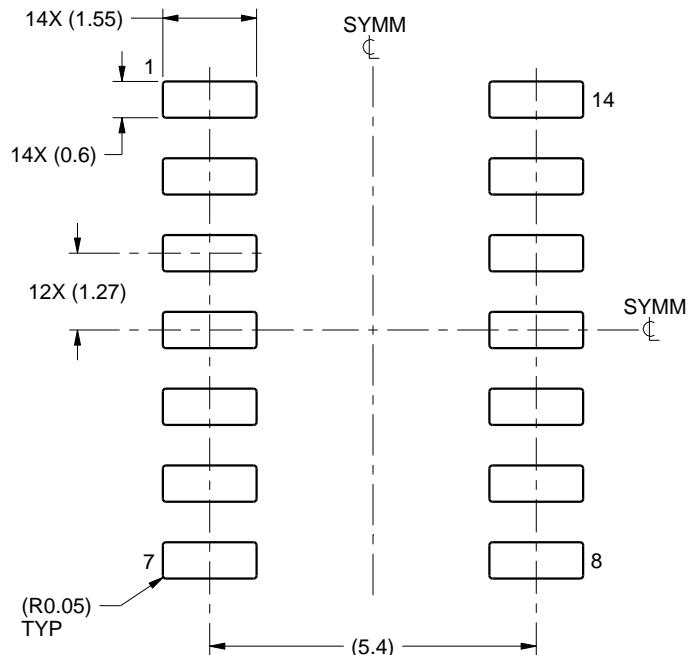
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

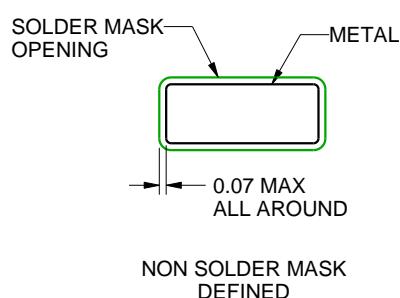
D0014A

SOIC - 1.75 mm max height

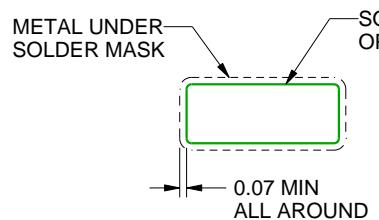
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

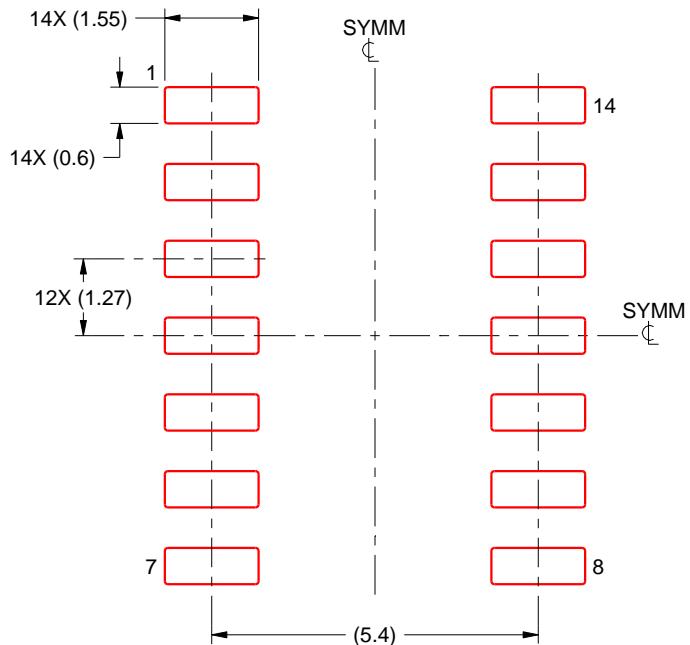
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

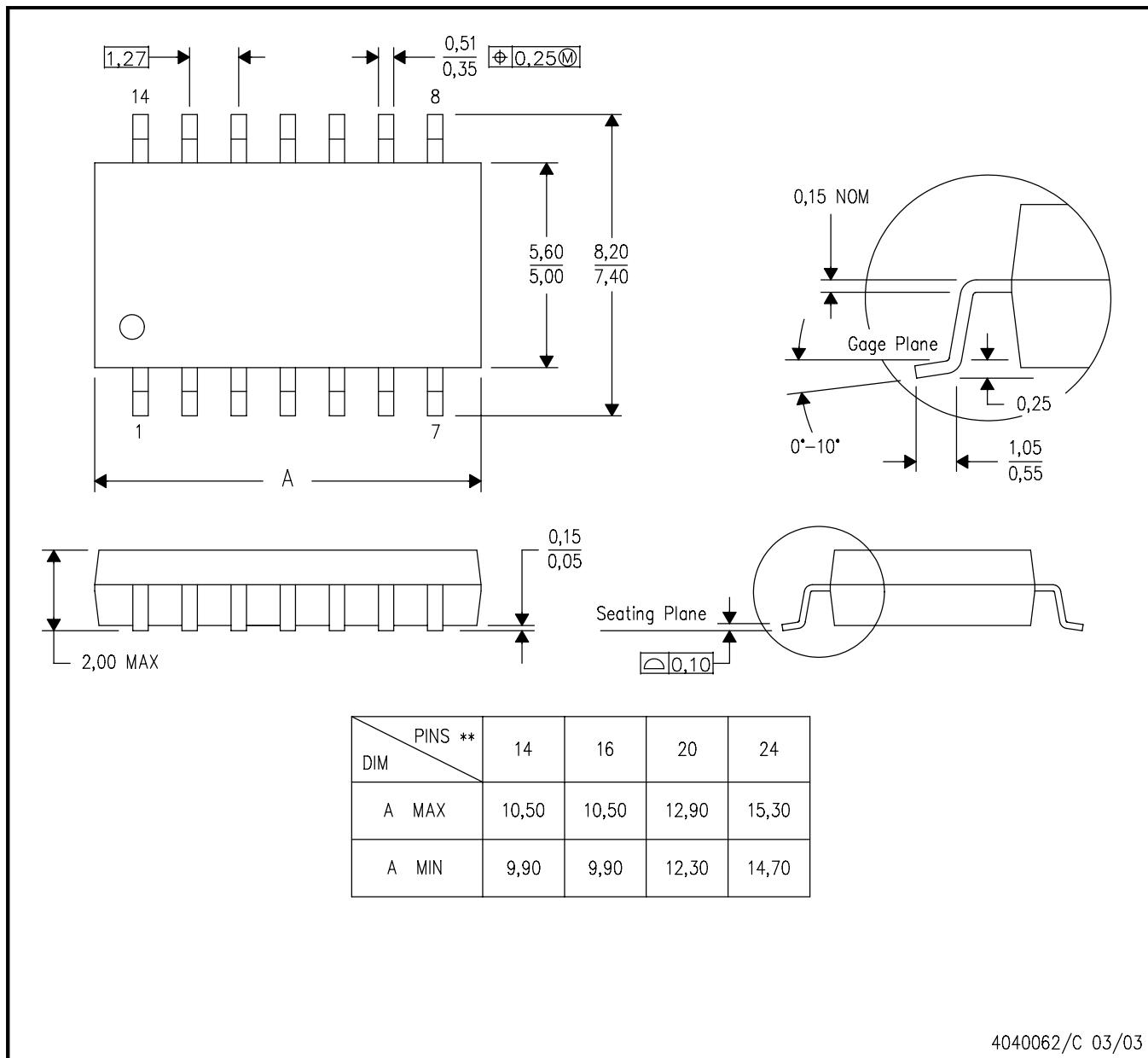
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

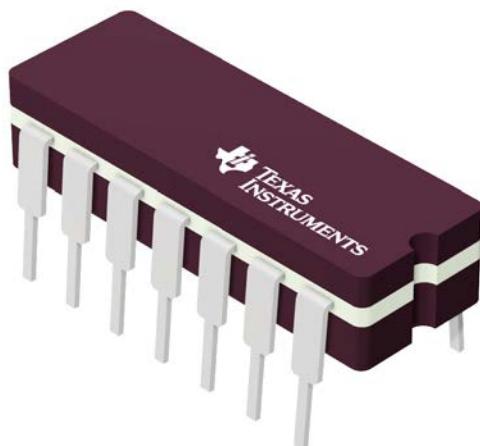
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

J 14

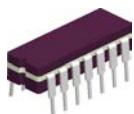
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

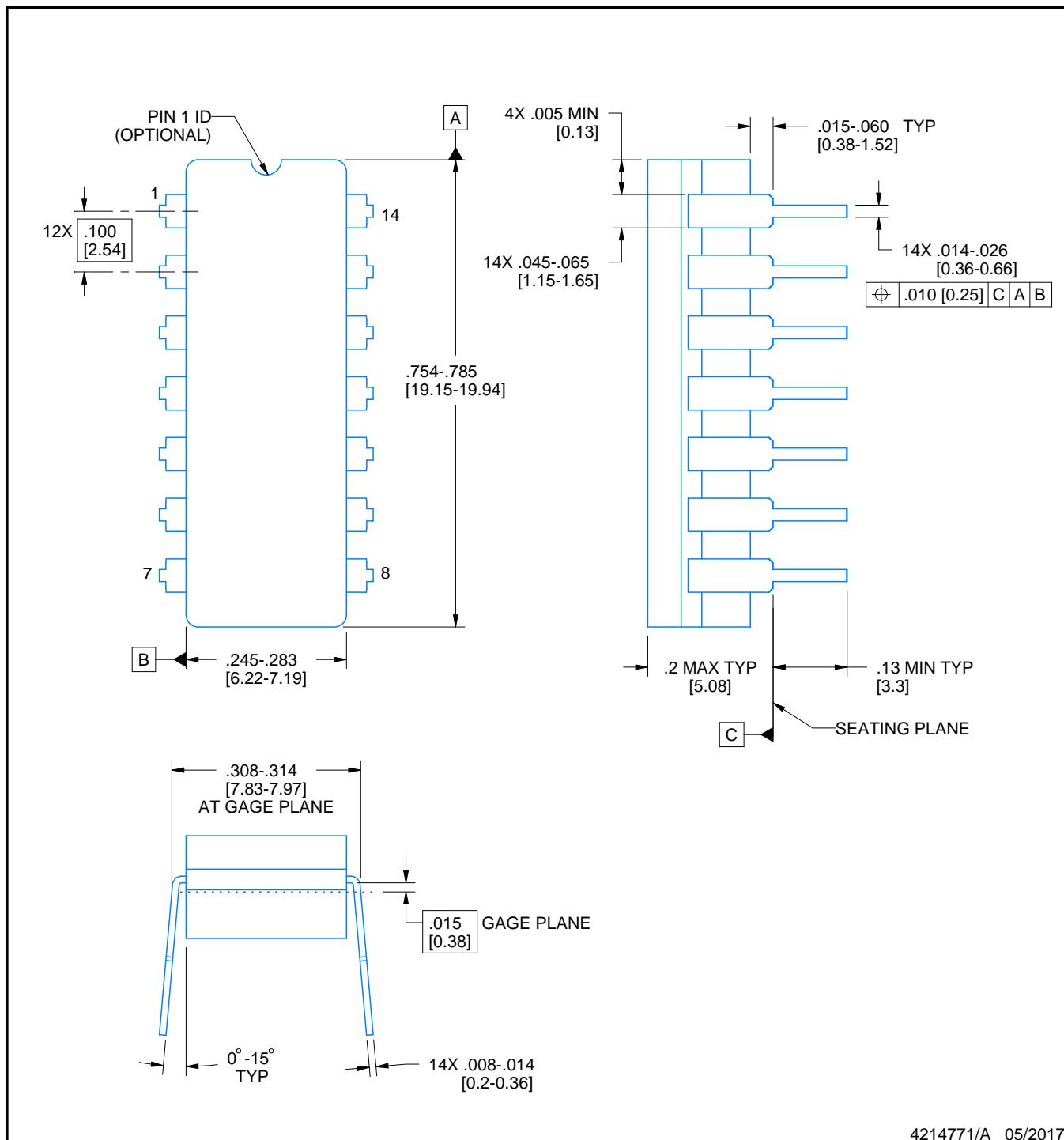


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

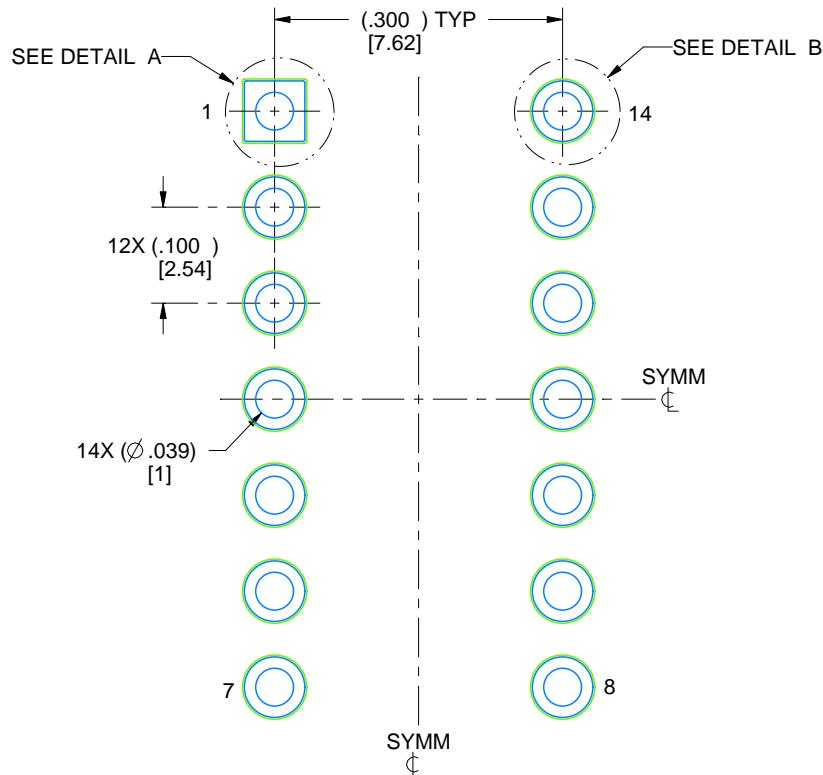
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

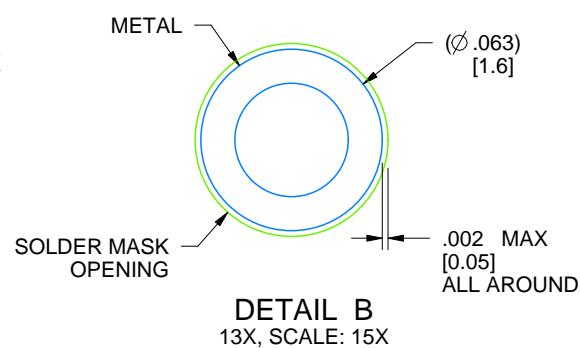
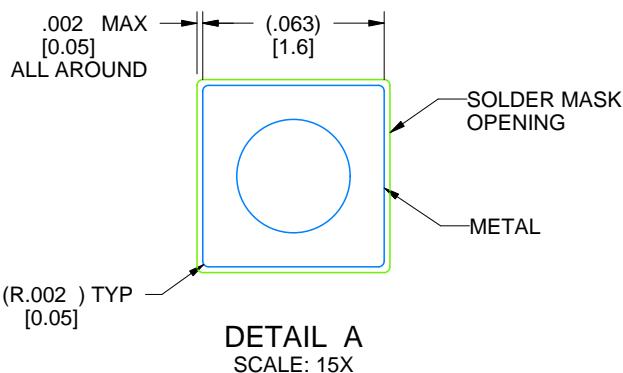
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

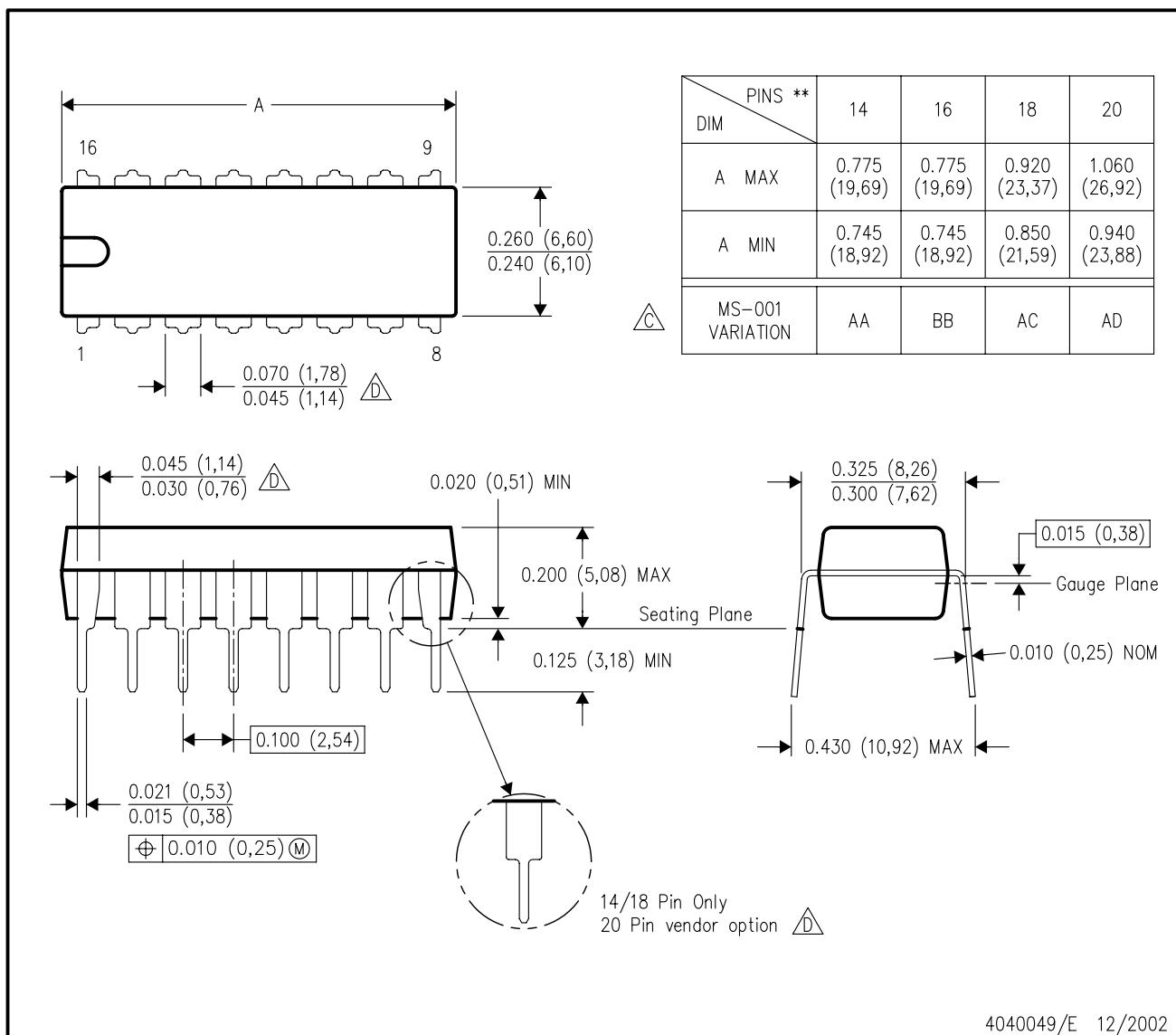


4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



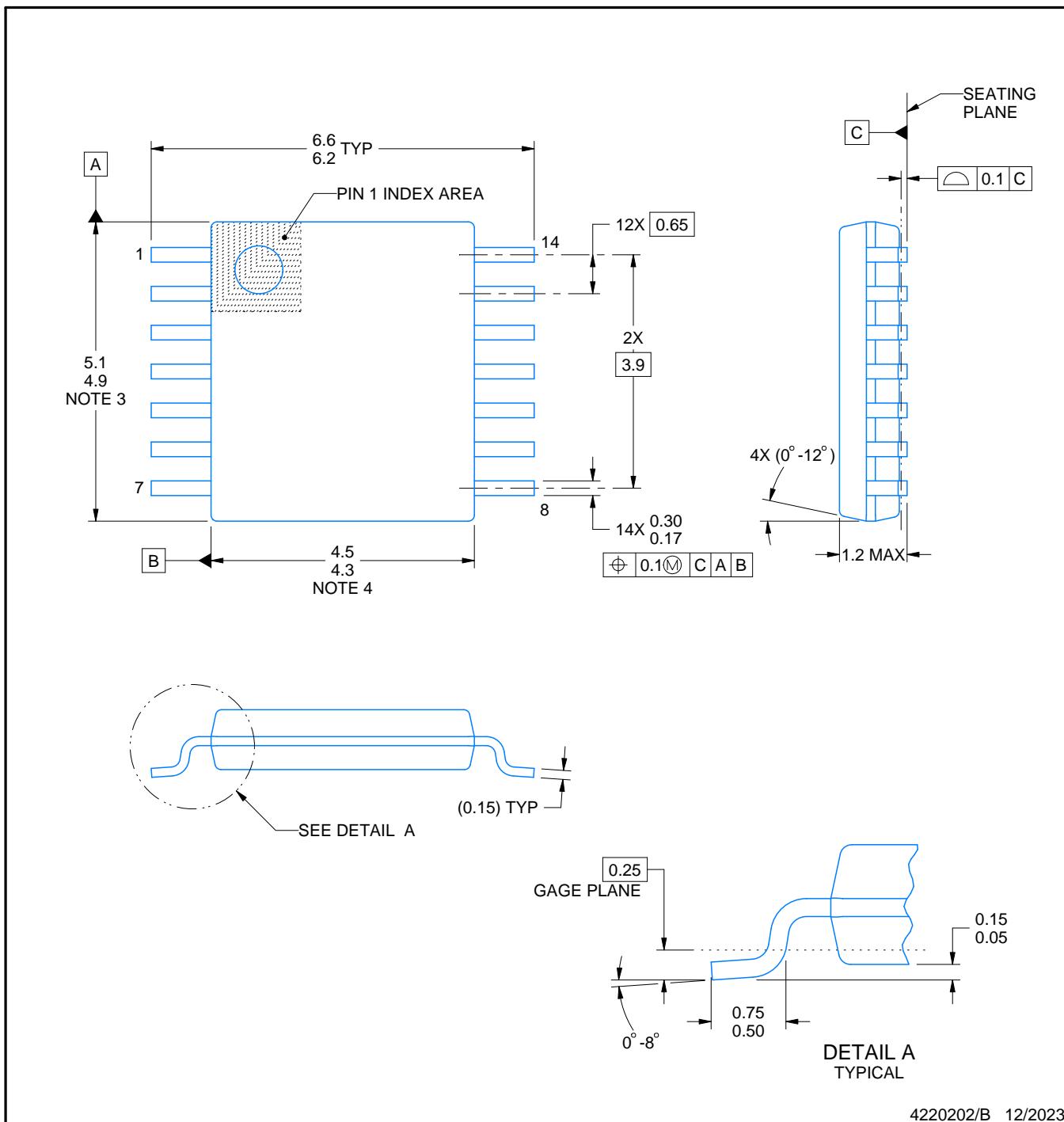
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

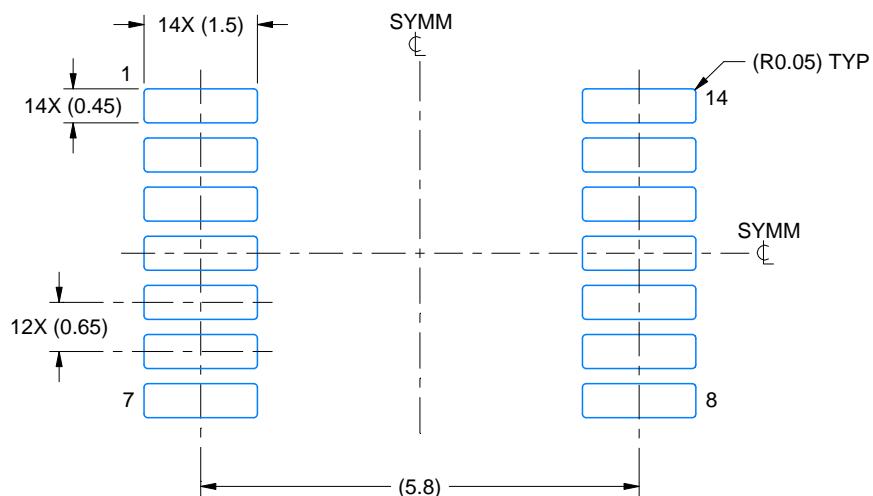
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

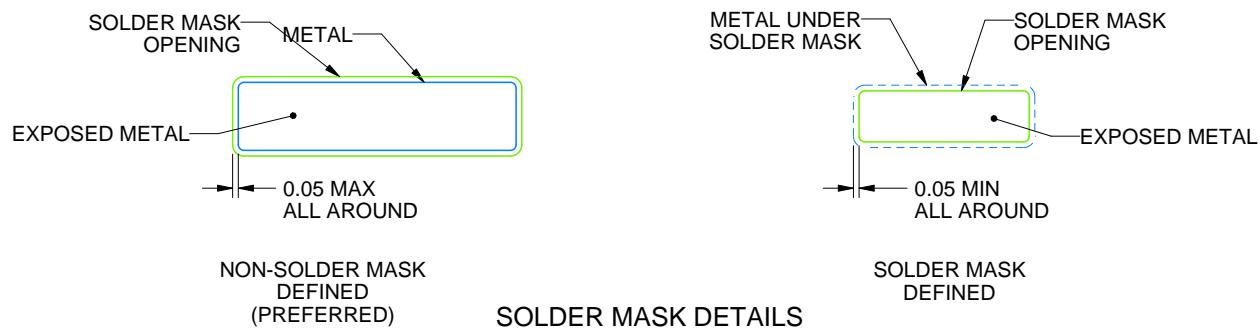
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

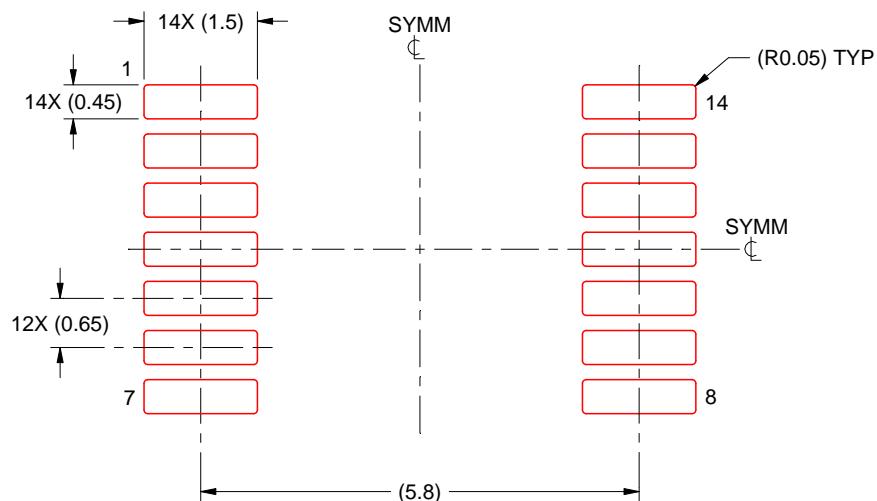
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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