

CDx4ACT05 Hex Inverters With Open-Drain Outputs

1 Features

- Inputs are TTL-voltage compatible
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit design
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

2 Description

The 'ACT05 devices contain six independent inverters.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ | BODY SIZE ⁽³⁾ |
|----------------|------------------------|-----------------------------|--------------------------|
| CD54ACT05 | J (CDIP, 14) | 19.55mm x 7.9mm | 19.55 mm x 6.7mm |
| | BQA (WQFN, 14) | 3mm x 2.5mm | 3mm x 2.5mm |
| | D (SOIC, 14) | 8.65mm x 6mm | 8.65mm x 3.9mm |
| | N (PDIP, 14) | 19.3mm x 9.4mm | 19.3mm x 6.35mm |
| PW (TSSOP, 14) | 5mm x 6.4mm | 5mm x 4.4mm | |

(1) For more information, see [Section 10](#).

(2) The package size (length x width) is a nominal value and includes pins, where applicable.

(3) The body size (length x width) is a nominal value and does not include pins.

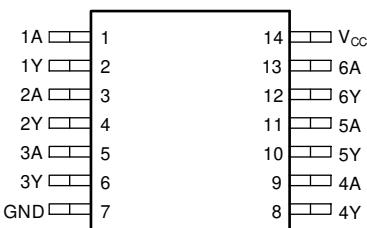


An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

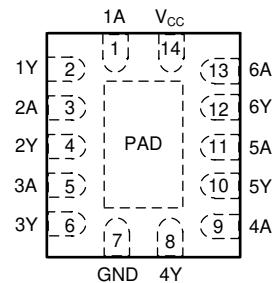
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3 Pin Configuration and Functions



**Figure 3-1. CD54ACT05 J Package, 14-Pin CDIP;
CD74ACT05 D, N, or PW Package; 14-Pin SOIC,
PDIP, or TSSOP (Top View)**



**Figure 3-2. CD74ACT05 BQA Package, 14-Pin
WQFN**

Table 3-1. Pin Functions

| NAME | PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------|-----------|-----------|--------------------|--|
| | CD74ACT05 | CD54ACT05 | | |
| BQA, D, N, PW | J | | | |
| 1A | 1 | 1 | I | 1A Input |
| 1Y | 2 | 2 | O | 1Y Output |
| 2A | 3 | 3 | I | 2A Input |
| 2Y | 4 | 4 | O | 2Y Output |
| 3A | 5 | 5 | I | 3A Input |
| 3Y | 6 | 6 | O | 3Y Output |
| GND | 7 | 7 | — | Ground Pin |
| 4Y | 8 | 8 | O | 4Y Output |
| 4A | 9 | 9 | I | 4A Input |
| 5Y | 10 | 10 | I | 5Y Output |
| 5A | 11 | 11 | I | 5A Input |
| 6Y | 12 | 12 | O | 6Y Output |
| 6A | 13 | 13 | I | 6A Input |
| V _{CC} | 14 | 14 | — | Power Pin |
| NC | — | — | — | No Connection |
| Thermal pad | | | — | Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance. |

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|-------------------------------------|--|------|-----|------|
| V _{CC} | Supply voltage range | | -0.5 | 6 | V |
| I _{IK} | Input clamp current ⁽²⁾ | V _I < 0 or V _I > V _{CC} | | ±20 | mA |
| I _{OK} | Output clamp current ⁽²⁾ | V _O < 0 | | -50 | mA |
| I _O | Continuous current | | | ±50 | mA |
| T _{stg} | Storage temperature range | | -65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | T _A = 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNIT |
|-----------------|------------------------------------|-----------------------|-----------------|---------------|-----------------|----------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | | 0.8 | V |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| V _O | Output voltage | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V |
| I _{OL} | Low-level output current | | 24 | | 24 | | 24 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | | 10 | | 10 | ns/V |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | CD74ACT05 | | | | UNIT | |
|-------------------------------|--|-------------|-------------|---------------|-------|------|
| | BQA (WQFN) | D (SOIC) | N (PDIP) | PW (TSSOP) | | |
| | 14 PINS | | | | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 85.4 | 89.9 | 80 | 132.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNIT |
|------------------|---|--|-----------------------|-----|---------------|------|----------------|------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 50 mA | 4.5 V | | 0.1 | 0.1 | 0.1 | 0.1 | V |
| | | I _{OL} = 24 mA | 4.5 V | | 0.36 | 0.44 | 0.5 | 0.5 | |
| | | I _{OL} = 50 mA ⁽¹⁾ | 5.5 V | | | | 1.65 | 1.65 | |
| | | I _{OL} = 75 mA ⁽¹⁾ | 5.5 V | | | 1.65 | | | |
| I _I | V _I = V _{CC} or GND | | 5.5 V | | ±0.1 | ±1 | ±1 | ±1 | µA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | | 5.5 V | | 4 | 40 | 80 | 80 | µA |
| ΔI _{CC} | V _I = V _{CC} – 2.1 V | | 4.5 V to 5.5 V | | 2.4 | 2.8 | 3 | 3 | mA |
| C _i | | | | | 10 | 10 | 10 | 10 | pF |

**Table 4-1. ACT INPUT
LOAD TABLE⁽¹⁾**

| Input | Unit Load |
|-------|-----------|
| A | 0.18 |

(1) Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

4.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

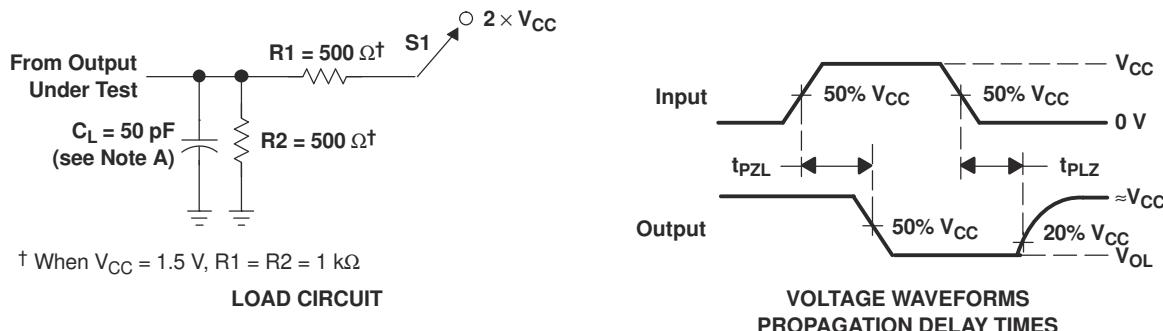
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C TO 85°C | | -55°C TO 125°C | | UNIT |
|------------------|-----------------|----------------|---------------|-----|----------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{PZL} | A or B | Y | 2.4 | 8.5 | 2.3 | 9.3 | ns |
| t _{PLZ} | | | 2.8 | 9.8 | 2.7 | 10.8 | |

4.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

| PARAMETER | TYP | UNIT |
|---|-----|------|
| C _{pd} Power dissipation capacitance | 105 | pF |

5 Parameter Measurement Information



NOTES:

- C_L includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.

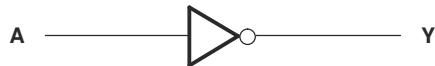
Figure 5-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

These devices perform the Boolean function $Y = \bar{A}$. The open-drain outputs require pullup resistors to perform correctly, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

6.2 Functional Block Diagram



6.3 Device Functional Modes

**Function Table
(Each Inverter)**

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | Z |

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 4.3](#).

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Layout Example](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

7.2.2 Layout Example

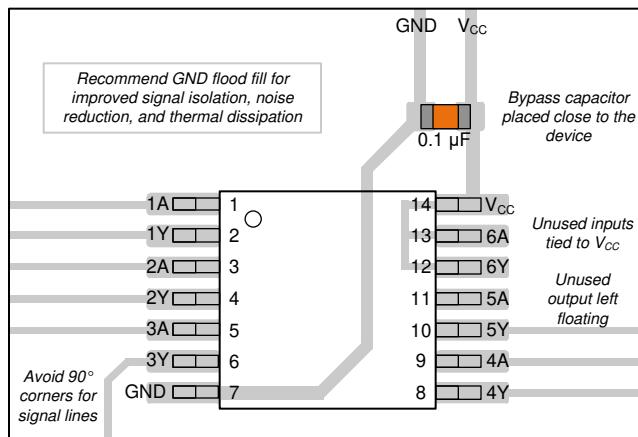


Figure 7-1. Example Layout for the CD74ACT05

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CD54ACT05 | Click here |
| CD74ACT05 | Click here |

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (August 2024) to Revision E (November 2024) | Page |
|---|-------------------|
| • Added BQA and PW packages to <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, and <i>Thermal Information</i> table..... | 1 |

| Changes from Revision C (January 2007) to Revision D (August 2024) | Page |
|--|-------------------|
| • Added <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1 |
| • Updated R _{0JA} values: D = 86 to 89.9, all values in °C/W..... | 4 |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------------|
| 5962-9068601QCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9068601QC A CD54ACT05F3A |
| CD54ACT05F3A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9068601QC A CD54ACT05F3A |
| CD54ACT05F3A.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9068601QC A CD54ACT05F3A |
| CD74ACT05BQAR | Active | Production | WQFN (BQA) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AD05 |
| CD74ACT05BQAR.A | Active | Production | WQFN (BQA) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AD05 |
| CD74ACT05E | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74ACT05E |
| CD74ACT05E.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74ACT05E |
| CD74ACT05EE4 | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74ACT05E |
| CD74ACT05M | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -55 to 125 | ACT05M |
| CD74ACT05M96 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT05M |
| CD74ACT05M96.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT05M |
| CD74ACT05M96G4 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT05M |
| CD74ACT05M96G4.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT05M |
| CD74ACT05PWR | Active | Production | TSSOP (PW) 14 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -55 to 125 | AD05 |
| CD74ACT05PWR.A | Active | Production | TSSOP (PW) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AD05 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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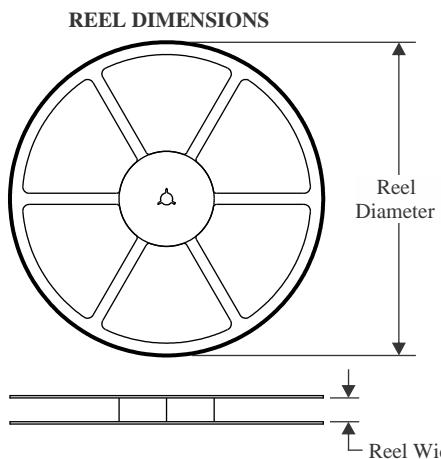
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54ACT05, CD74ACT05 :

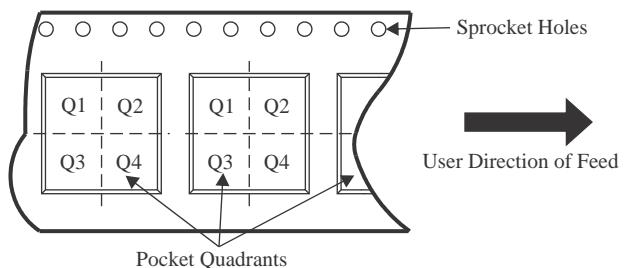
- Catalog : [CD74ACT05](#)
- Military : [CD54ACT05](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74ACT05BQAR | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| CD74ACT05M96 | SOIC | D | 14 | 2500 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |
| CD74ACT05PWR | TSSOP | PW | 14 | 3000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74ACT05PWR | TSSOP | PW | 14 | 3000 | 330.0 | 12.4 | 6.85 | 5.45 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74ACT05BQAR | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| CD74ACT05M96 | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| CD74ACT05PWR | TSSOP | PW | 14 | 3000 | 353.0 | 353.0 | 32.0 |
| CD74ACT05PWR | TSSOP | PW | 14 | 3000 | 366.0 | 364.0 | 50.0 |

TUBE


*All dimensions are nominal

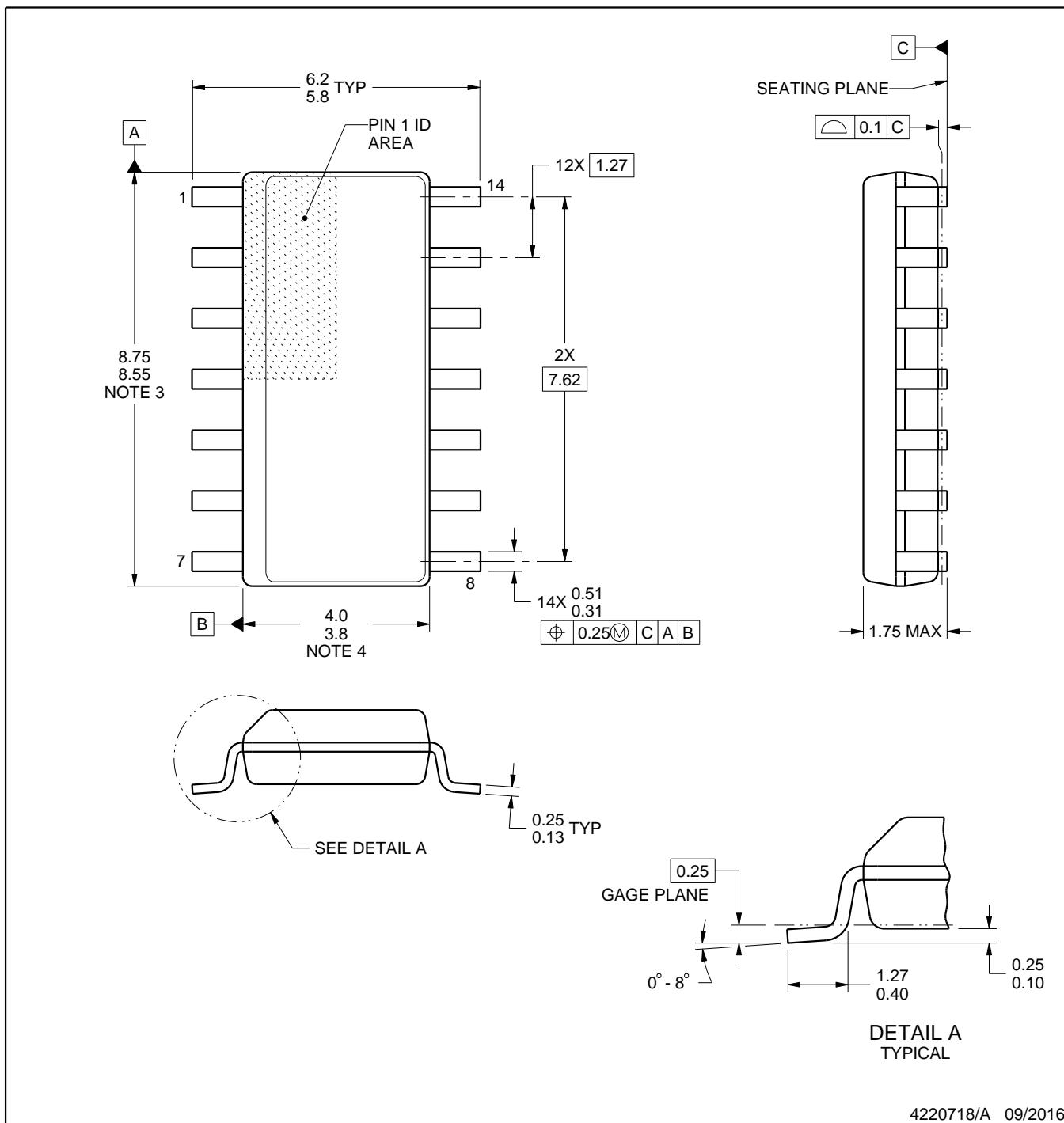
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μ m) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------------|--------|
| CD74ACT05E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT05E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT05E.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT05E.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT05EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT05EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

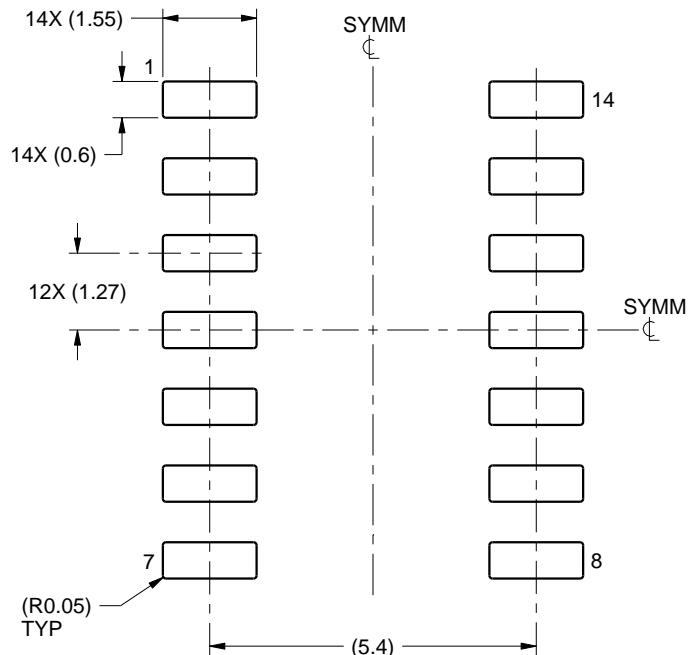
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

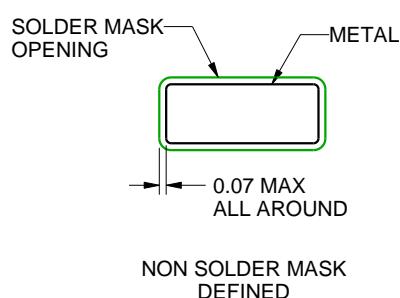
D0014A

SOIC - 1.75 mm max height

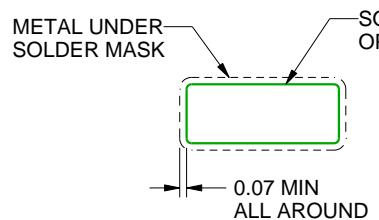
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

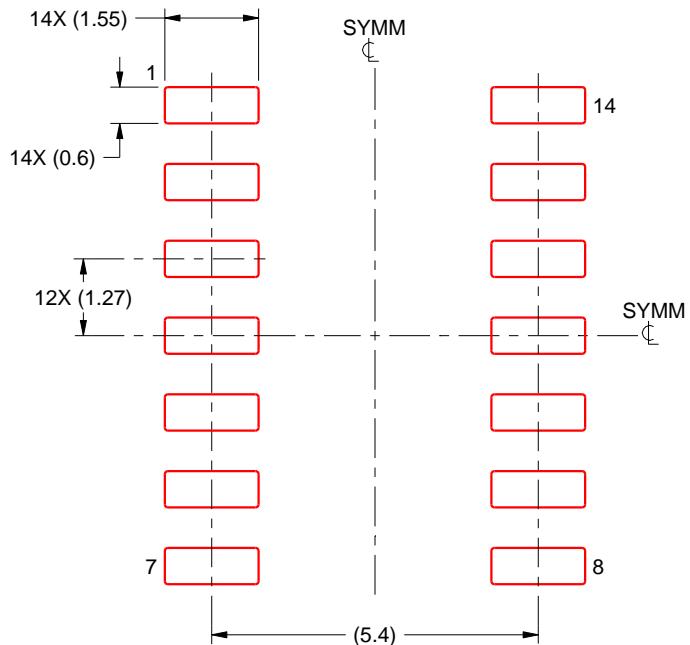
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

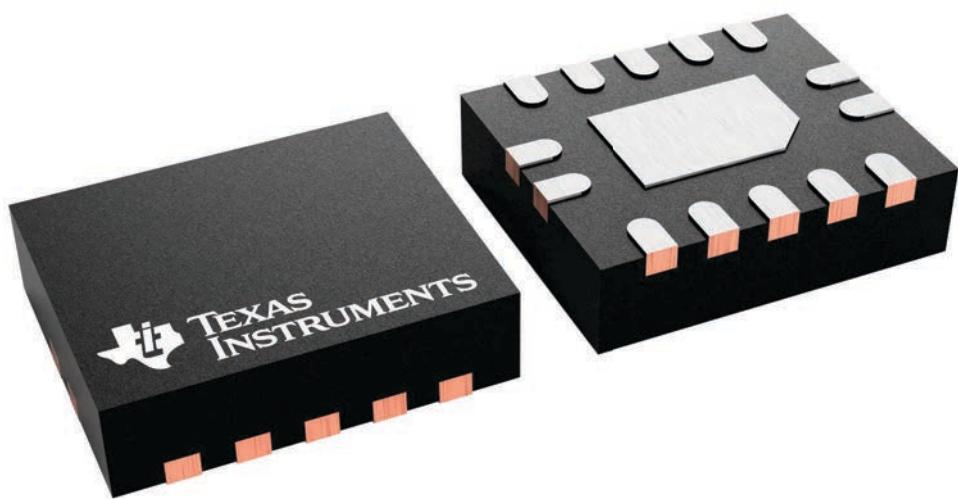
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



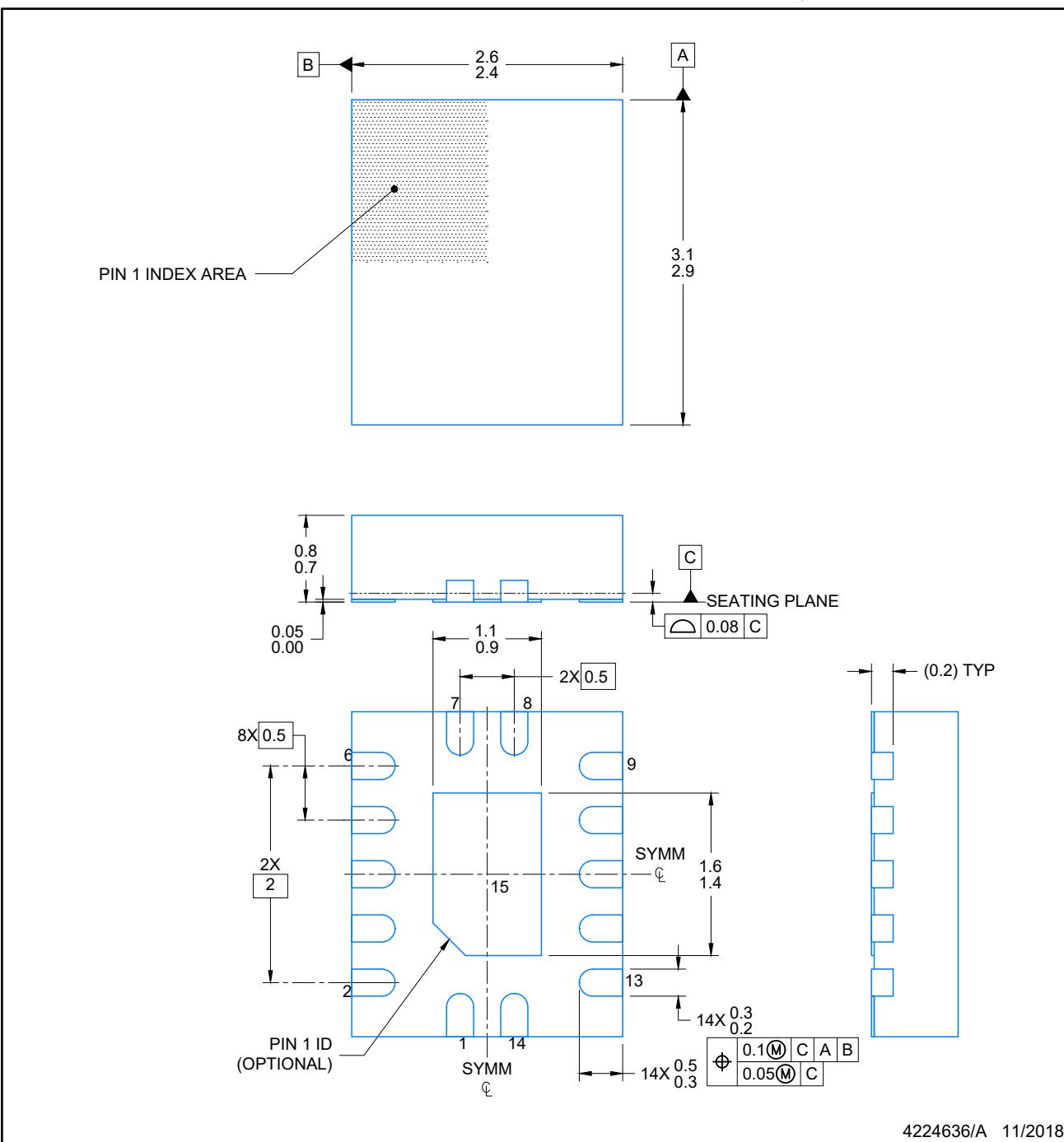
4227145/A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



4224636/A 11/2018

NOTES:

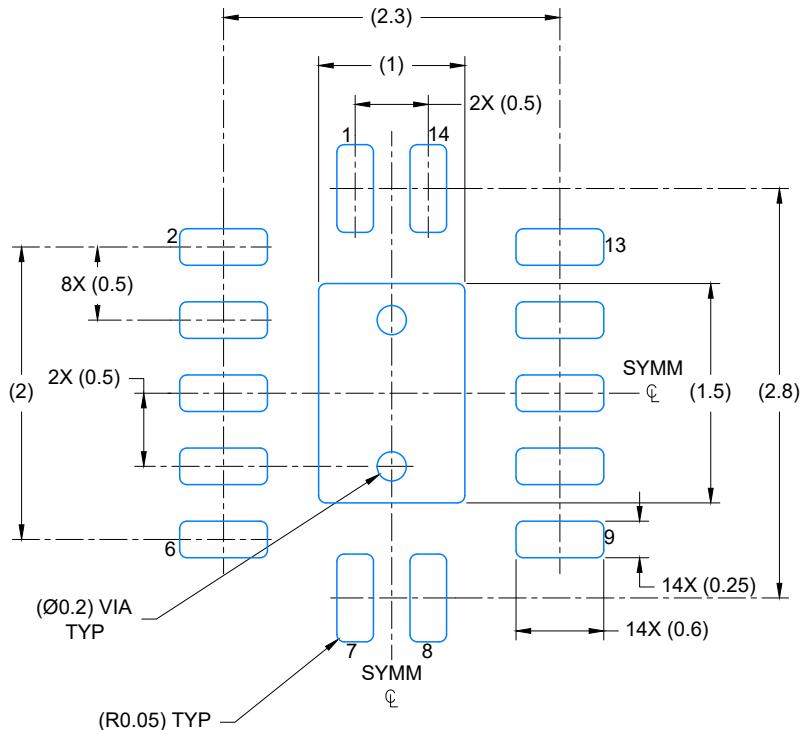
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

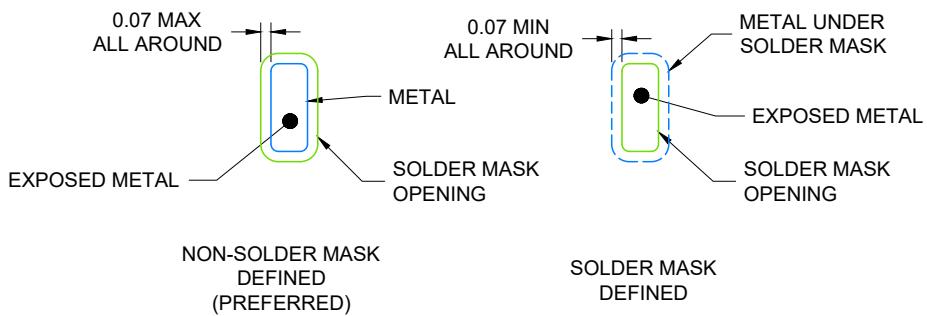
BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

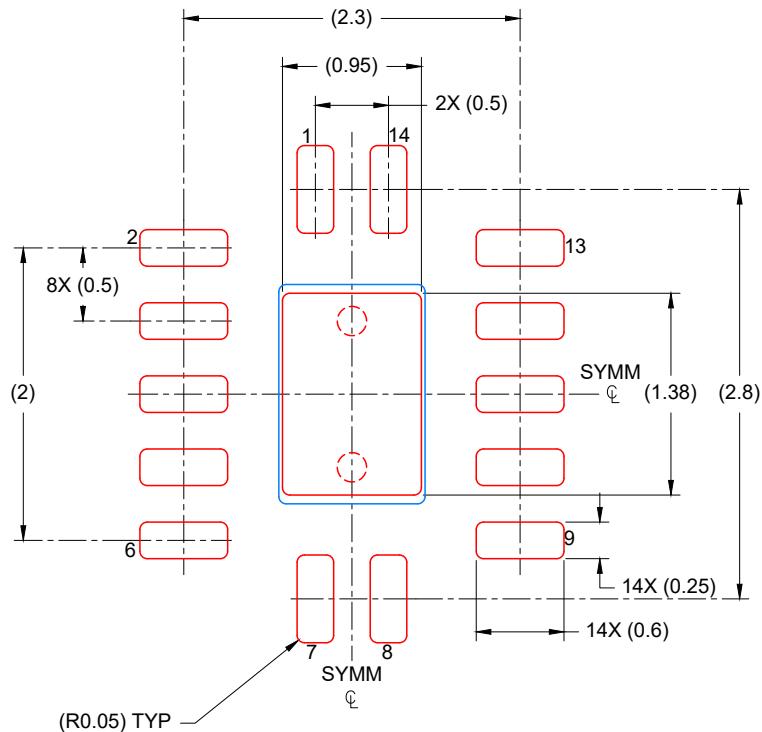
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

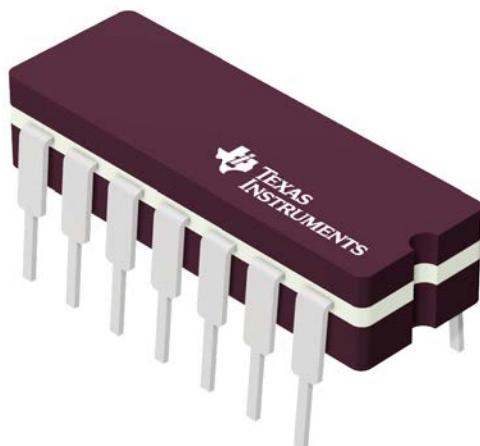
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

J 14

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

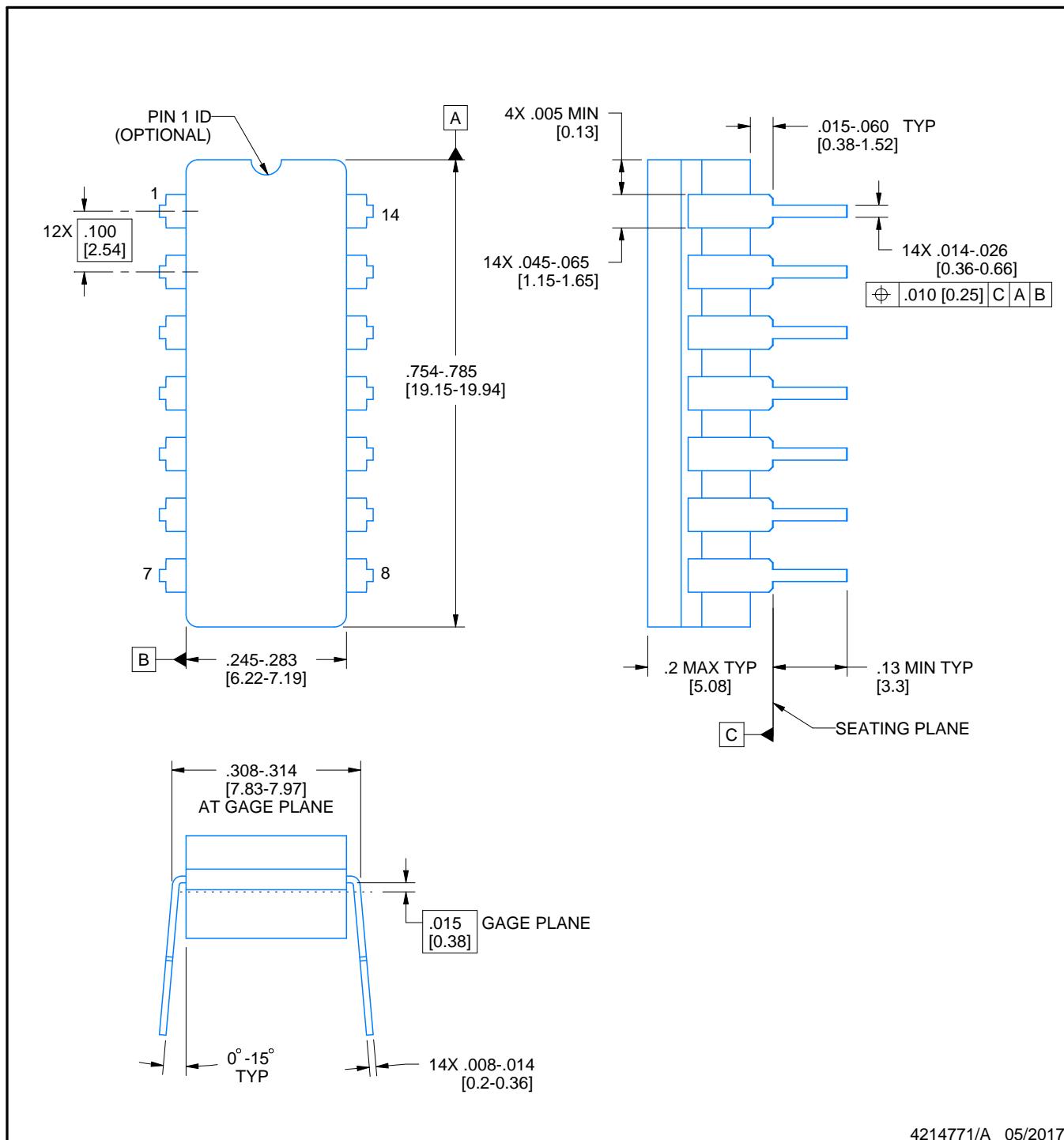


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

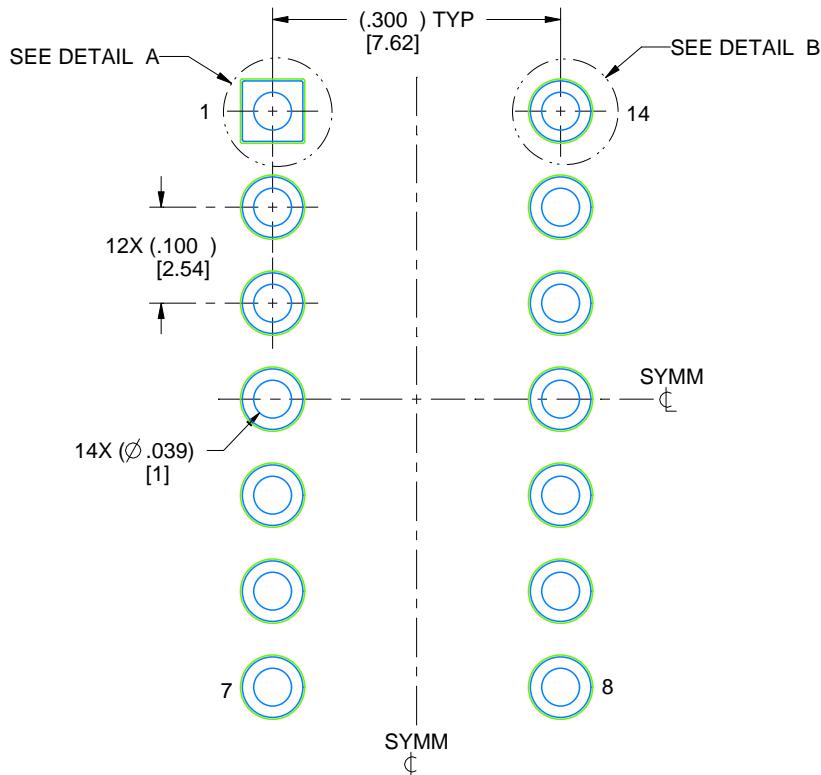
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

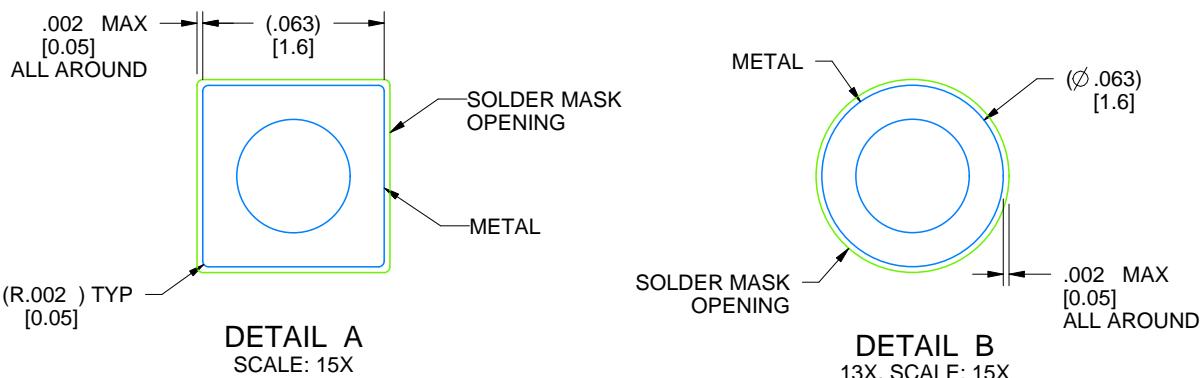
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

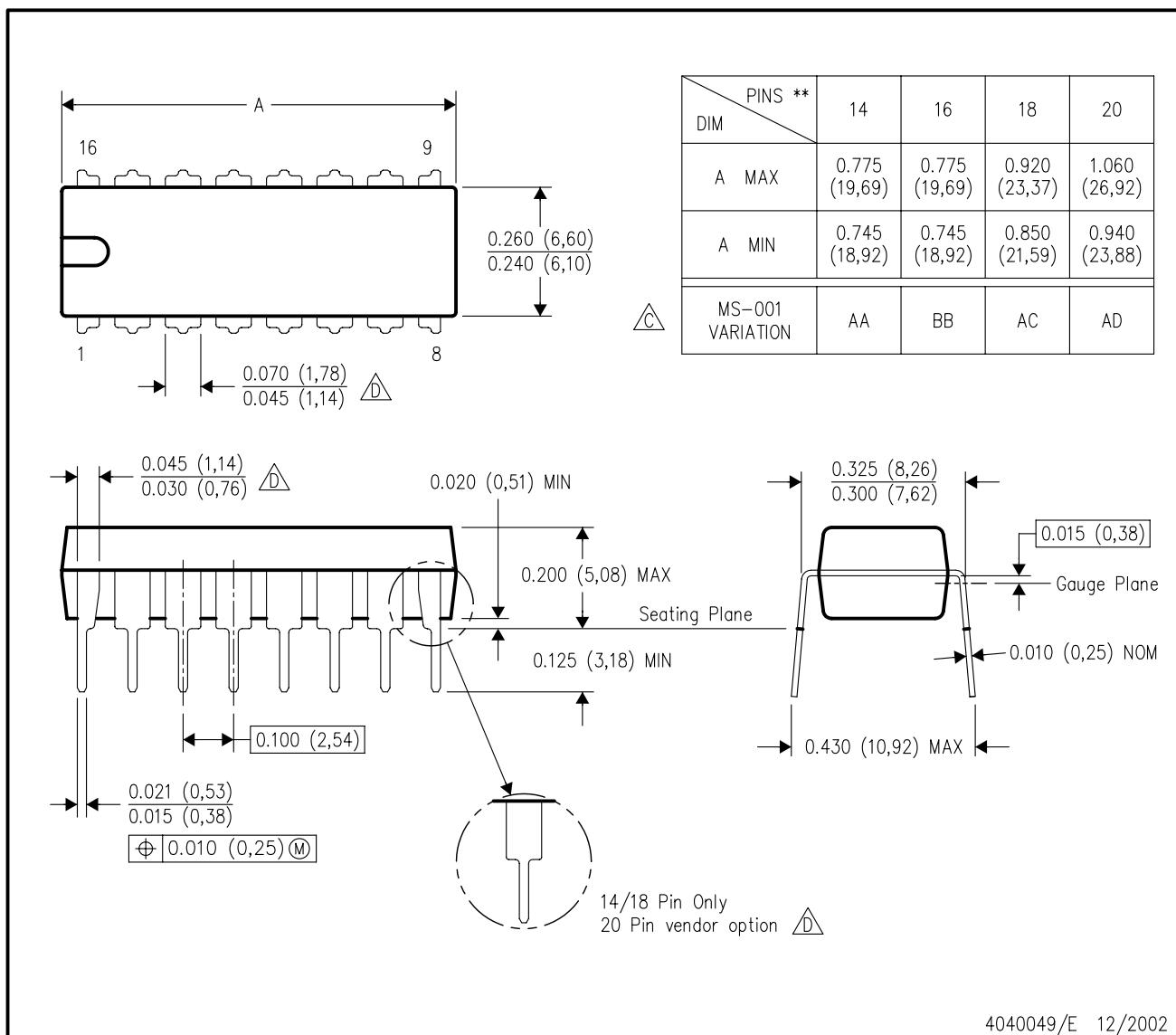


4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



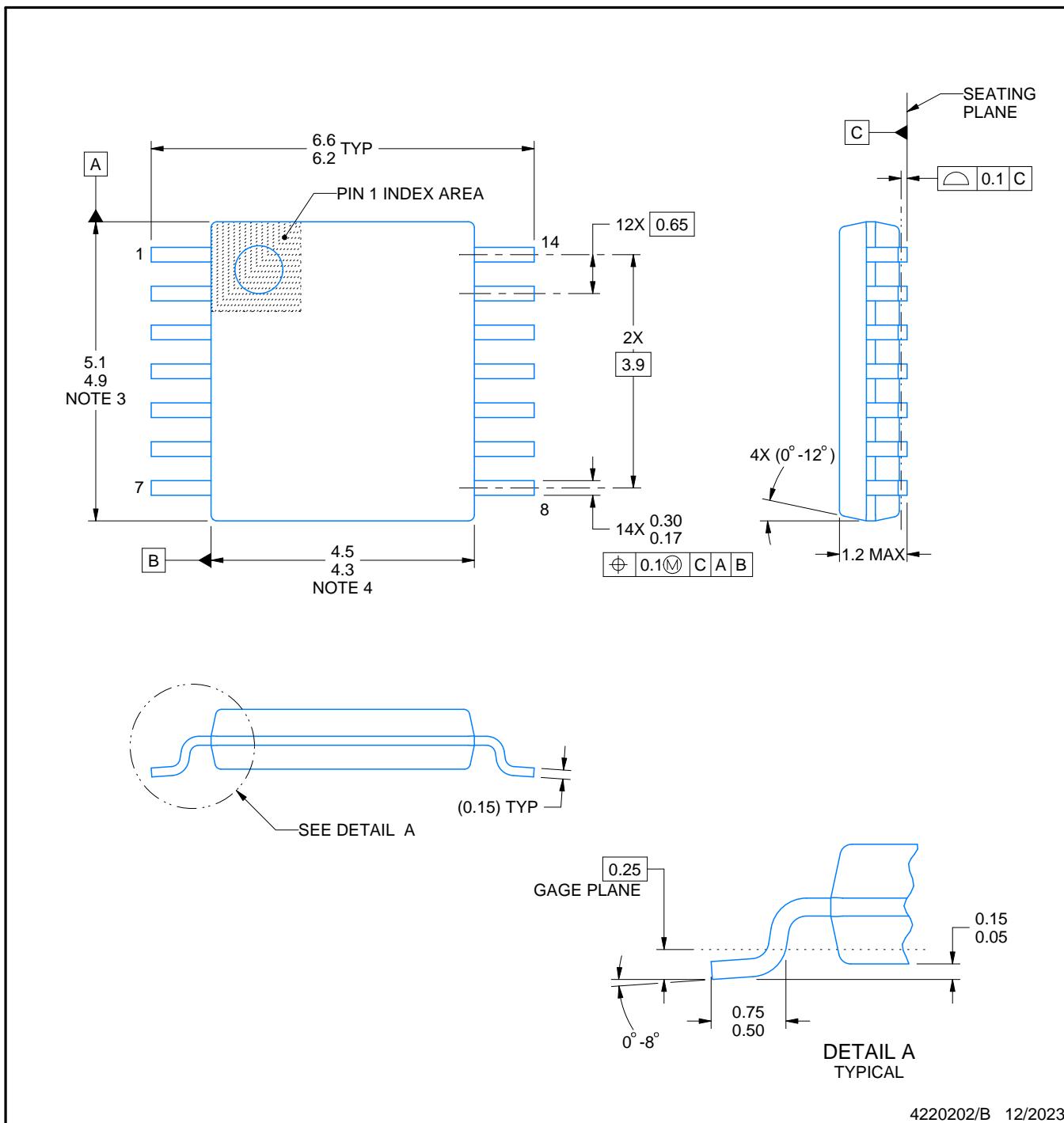
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

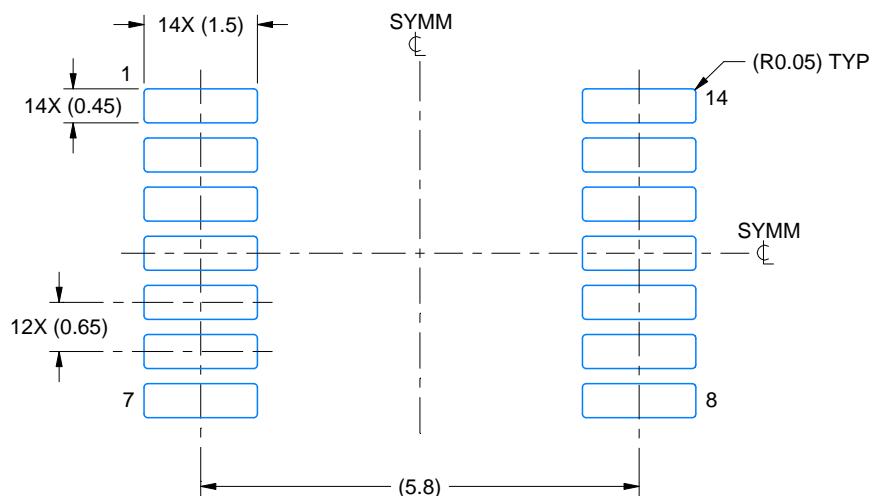
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

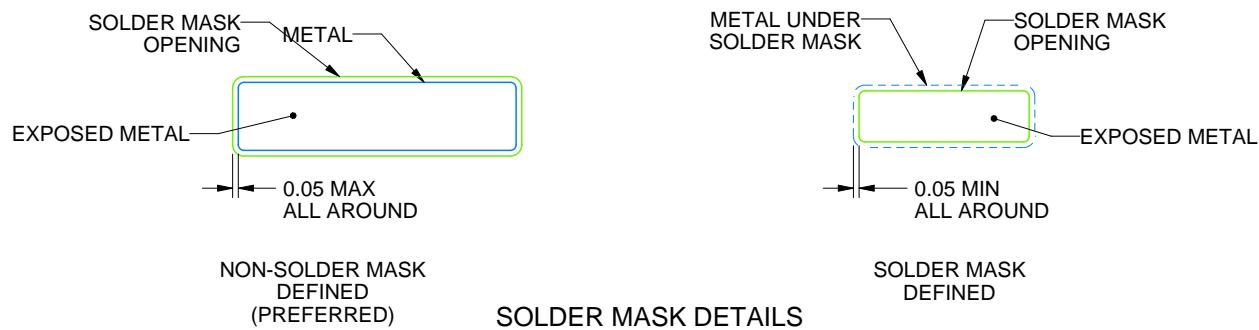
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

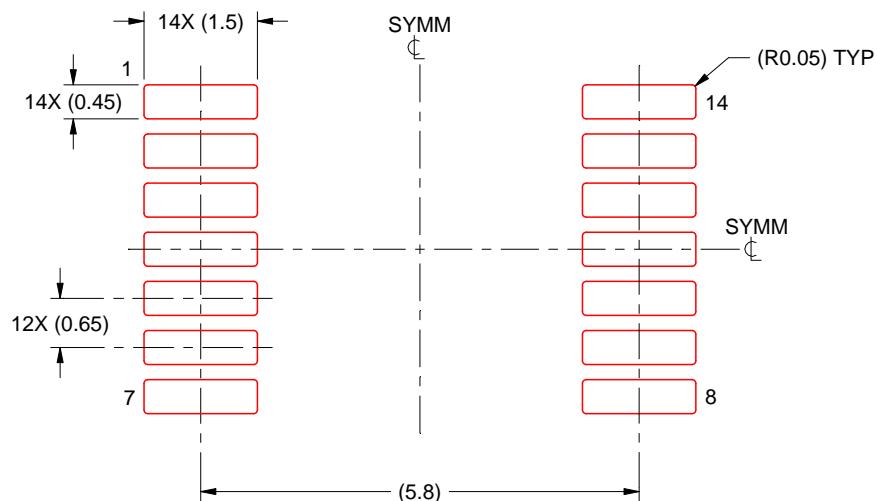
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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