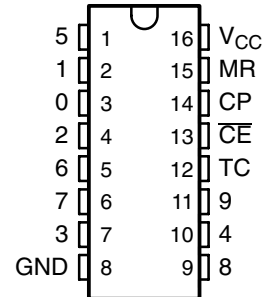


CD74HC4017-Q1 HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER WITH 10 DECODED OUTPUTS

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- Qualified for Automotive Applications
- Fully Static Operation
- Buffered Inputs
- Common Reset
- Positive Edge Clocking
- Typical $f_{MAX} = 60$ MHz at $V_{CC} = 5$ V, $C_L = 15$ pF, $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
 - Standard Outputs . . . 10 LSTTL Loads
 - Bus Driver Outputs . . . 15 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- V_{CC} Voltage = 2 V to 6 V
- High Noise Immunity N_{IL} or $N_{IH} = 30\%$ of V_{CC} , $V_{CC} = 5$ V

M OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD74HC4017 is a high-speed silicon-gate CMOS 5-stage Johnson counter with ten decoded outputs. Each of the decoded outputs normally is low and sequentially goes high on the low-to-high transition clock period of the ten-clock-period cycle. The carry (TC) output transitions low to high after output 9 goes from high to low, and can be used in conjunction with the clock enable ($\overline{CE}$) input to cascade several stages. $\overline{CE}$ disables counting when in the high state. A master reset (MR) input also is provided that, when taken high, sets all the decoded outputs, except output 0, to low.

The device can drive up to ten low-power Schottky equivalent loads.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC4017QM96Q1	HC4017Q
	TSSOP – PW	Tape and reel	CD74HC4017QPWRQ1	HC4017Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

FUNCTION TABLE

INPUTS			OUTPUT STATE†
CP	$\overline{CE}$	MR	
L	X	L	No change
X	H	L	No change
X	X	H	0 = H, 1–9 = L
↑	L	L	Increments counter
↓	X	L	No change
X	↑	L	No change
H	↓	L	Increments counter

NOTE: H = high voltage level, L = low voltage level,
X = don't care, ↑ = transition from low to high
level, ↓ = transition from high to low level

† If $n < 5$, TC = H, otherwise TC = L



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TEXAS
INSTRUMENTS

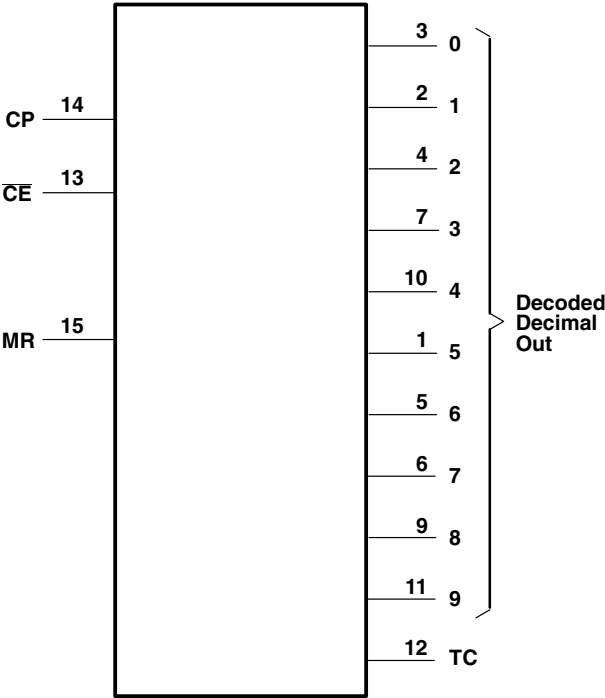
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CD74HC4017-Q1
HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER
WITH 10 DECODED OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
Output clamp current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±20 mA
Source or sink current per output pin, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): M package	73°C/W
PW package	108°C/W
Maximum junction temperature, T_J	150°C
Lead temperature (during soldering):	
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max	300°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			2	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$		1.5		V
		$V_{CC} = 4.5\text{ V}$		3.15		
		$V_{CC} = 6\text{ V}$		4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$			0.5	V
		$V_{CC} = 4.5\text{ V}$			1.35	
		$V_{CC} = 6\text{ V}$			1.8	
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
t_i	Input transition (rise and fall) time	$V_{CC} = 2\text{ V}$		0	1000	ns
		$V_{CC} = 4.5\text{ V}$		0	500	
		$V_{CC} = 6\text{ V}$		0	400	
T_A	Operating free-air temperature			-40	125	°C

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
					MIN	MAX			
V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	CMOS loads	-0.02	2 V	1.9		1.9		V
			-0.02	4.5 V	4.4		4.4		
			-0.02	6 V	5.9		5.9		
		TTL loads	-4	4.5 V	3.98		3.7		
			-5.2	6 V	5.48		5.2		
V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	CMOS loads	0.02	2 V		0.1		0.1	V
			0.02	4.5 V		0.1		0.1	
			0.02	6 V		0.1		0.1	
		TTL loads	4	4.5 V		0.26		0.4	
			5.2	6 V		0.26		0.4	
I_I	$V_I = V_{CC} \text{ or } \text{GND}$			6 V		± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC} \text{ or } \text{GND}$		0	6 V		8		160	μA
C_{IN}	$C_L = 50\text{ pF}$					10		10	pF



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WITH 10 DECODED OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			V _{CC}	T _A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
f _{max}	Maximum clock frequency		2 V	6		4		MHz
			4.5 V	30		20		
			6 V	35		23		
t _w	Pulse duration	CP	2 V	80		120		ns
			4.5 V	16		24		
			6 V	14		20		
		MR	2 V	80		120		
			4.5 V	16		24		
			6 V	14		20		
t _{su}	Setup time	CE to CP	2 V	75		110		ns
			4.5 V	15		22		
			6 V	13		19		
		MR inactive	2 V	5		5		
			4.5 V	5		5		
			6 V	5		5		
t _h	Hold time, CE to CP		2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		

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HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER WITH 10 DECODED OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t _{pd}	CP	Decade out	C _L = 50 pF	2 V			230		345	ns
				4.5 V			46		69	
				6 V			39		59	
			C _L = 15 pF	5 V		19				
		TC	C _L = 50 pF	2 V			230		345	
				4.5 V			46		69	
				6 V			39		59	
			C _L = 15 pF	5 V		19				
	CE	Decade out	C _L = 50 pF	2 V			250		375	
				4.5 V			50		75	
				6 V			43		64	
			C _L = 15 pF	5 V		21				
		TC	C _L = 50 pF	2 V			250		375	
				4.5 V			50		75	
				6 V			43		64	
			C _L = 15 pF	5 V		21				
	MR	Decade out	C _L = 50 pF	2 V			230		345	
				4.5 V			46		69	
				6 V			39		59	
			C _L = 15 pF	5 V		19				
		TC	C _L = 50 pF	2 V			230		345	
				4.5 V			46		69	
				6 V			39		59	
			C _L = 15 pF	5 V		19				
t _t		TC, Decade out	C _L = 50 pF	2 V			75		110	ns
				4.5 V			15		22	
				6 V			13		19	
f _{max}	CP		C _L = 15 pF	5 V		60				MHz

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns, C_L = 15 pF

PARAMETER		TYP	UNIT
C _{pd}	Power dissipation capacitance (see Note 4)	39	pF

NOTE 4: C_{pd} is used to determine the dynamic power consumption per package.

$$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage

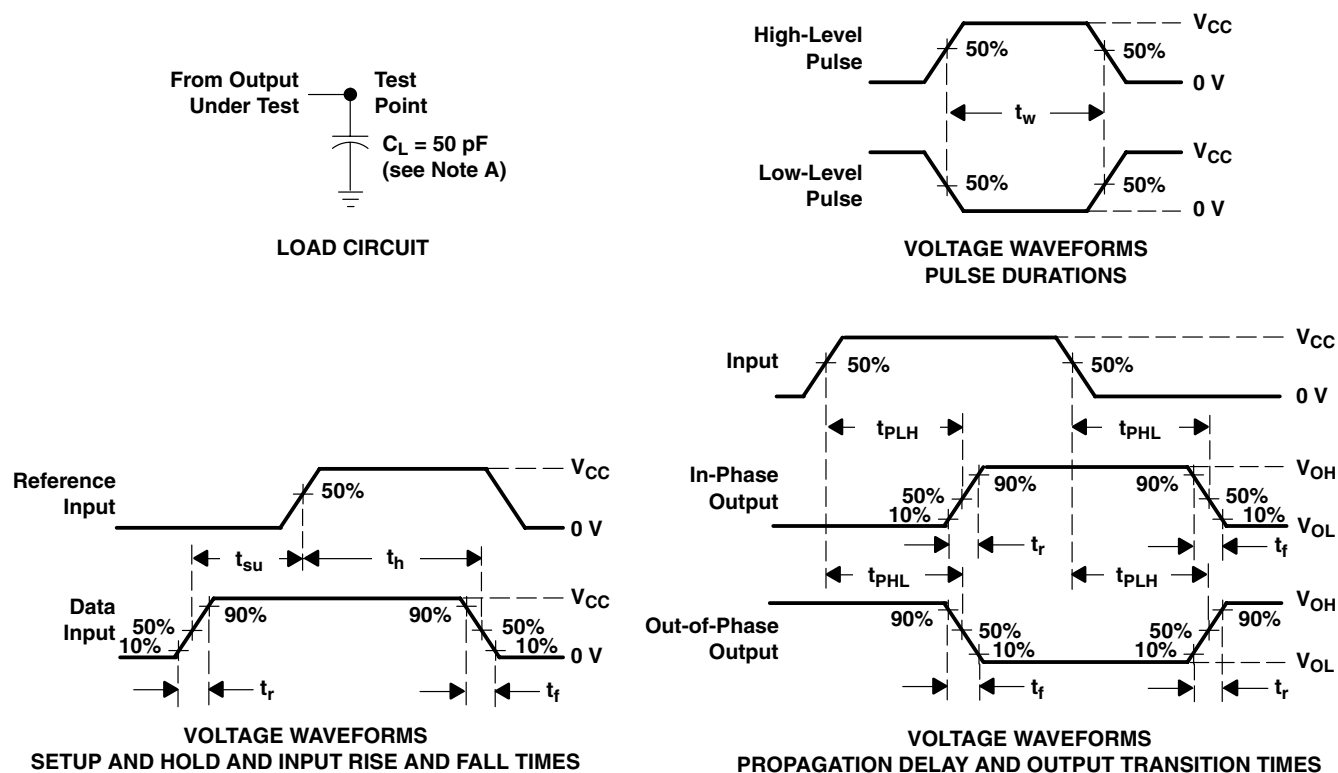
CD74HC4017-Q1

HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4017QPWRG4Q1	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4017Q
CD74HC4017QPWRG4Q1.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4017Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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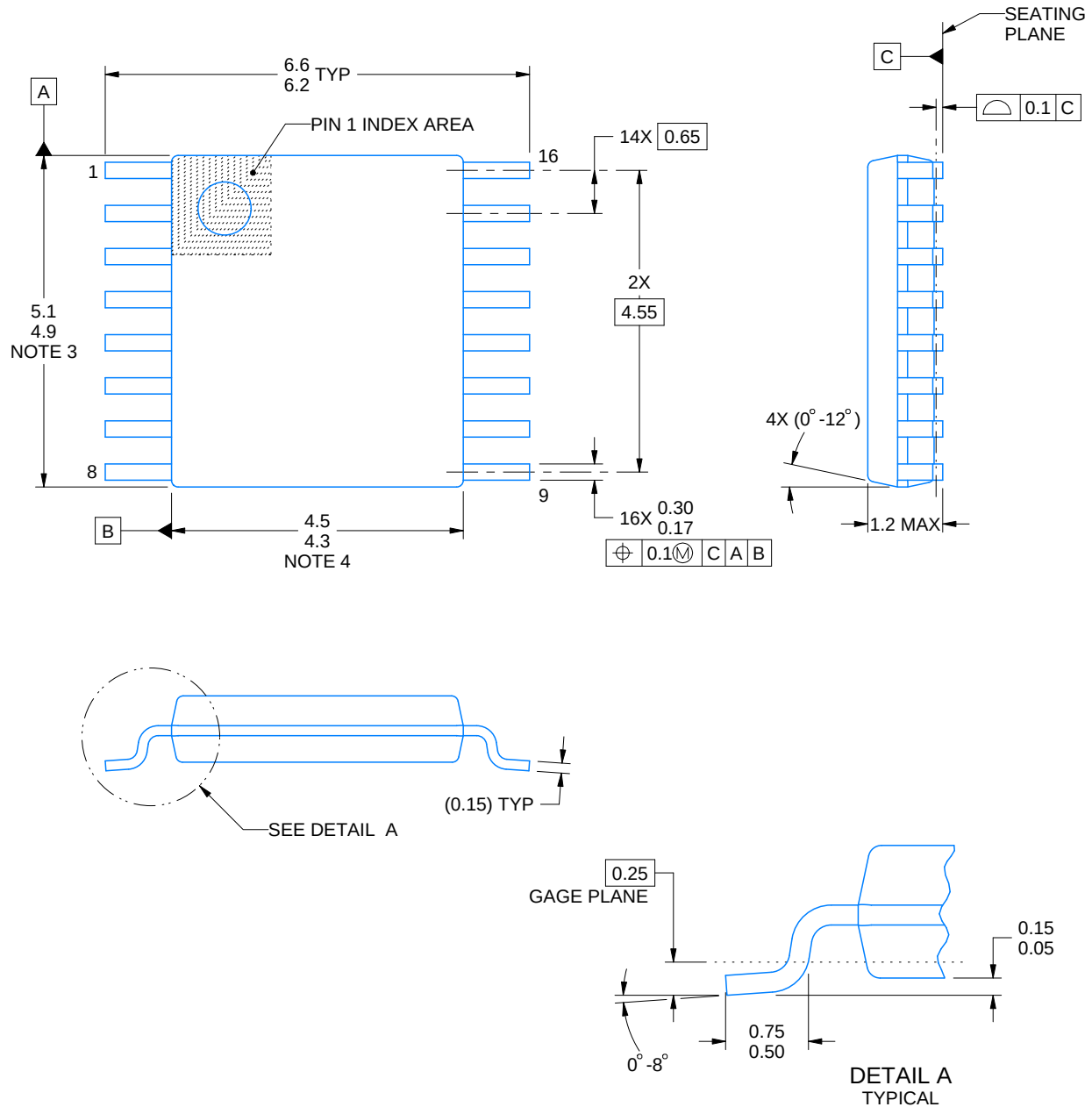
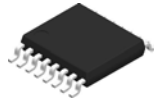
OTHER QUALIFIED VERSIONS OF CD74HC4017-Q1 :

- Catalog : [CD74HC4017](#)

- Enhanced Product : [CD74HC4017-EP](#)
- Military : [CD54HC4017](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications



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NOTES:

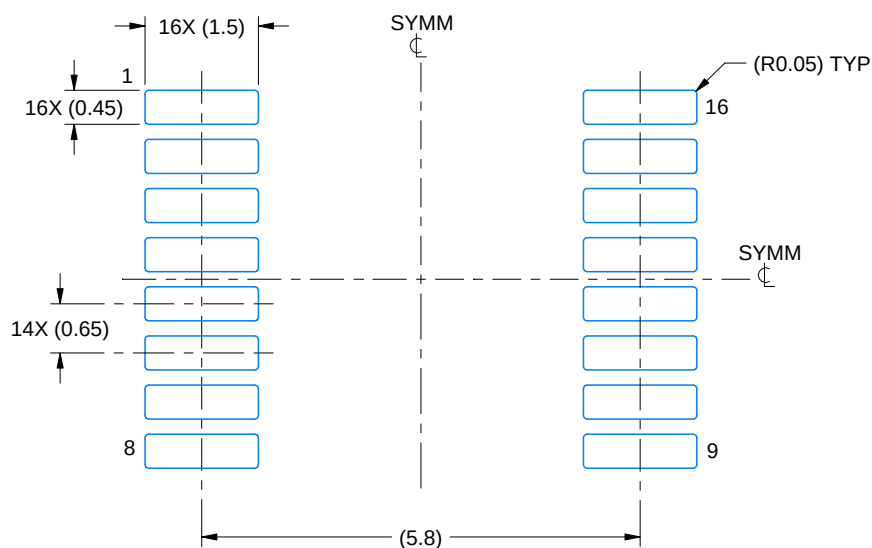
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

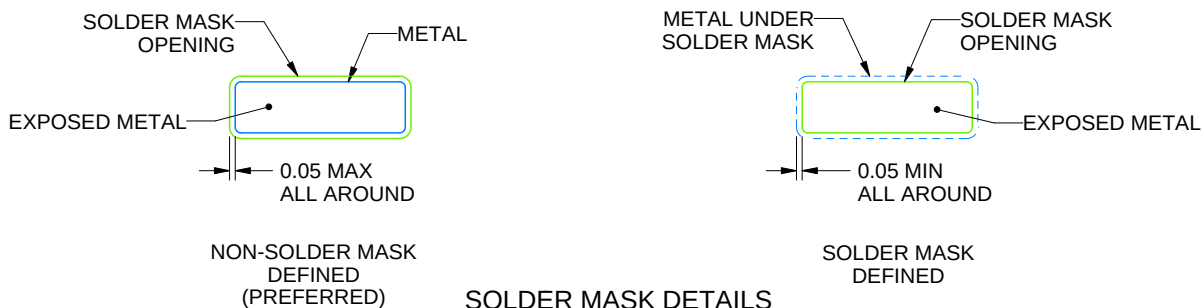
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

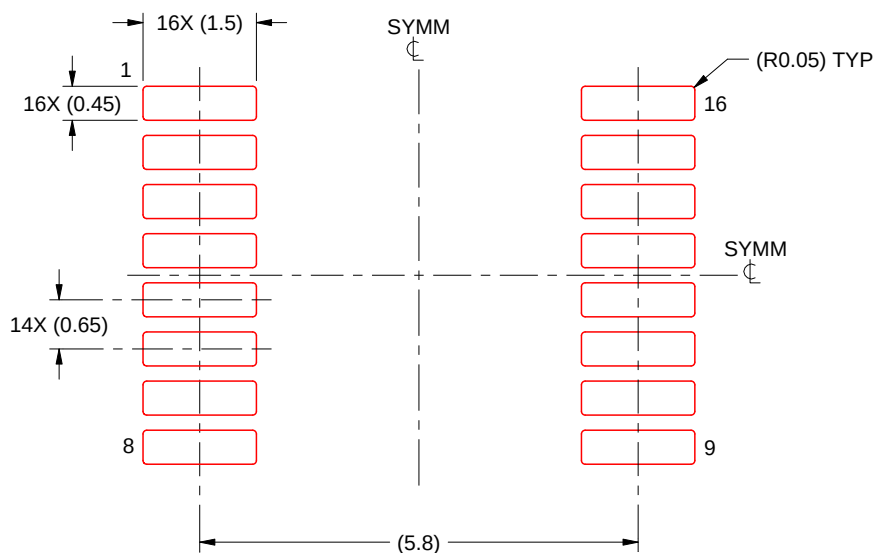
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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