CDx4HC640 CDx4HCT640 High-Speed CMOS Logic Octal Three-State Bus Transceiver, Inverting

1 Features

- Buffered inputs
- Three-state outputs
- Applications in multiple-data-bus architecture
- Fanout (over temperature range)
  - Standard outputs : 10 LSTTL loads
  - Bus driver outputs : 15 LSTTL loads
- Wide operating temperature range : -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic IC's
- HC types
  - 2 V to 6 V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V(Max), V_{IH} = 2 V(Min)
  - CMOS input compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

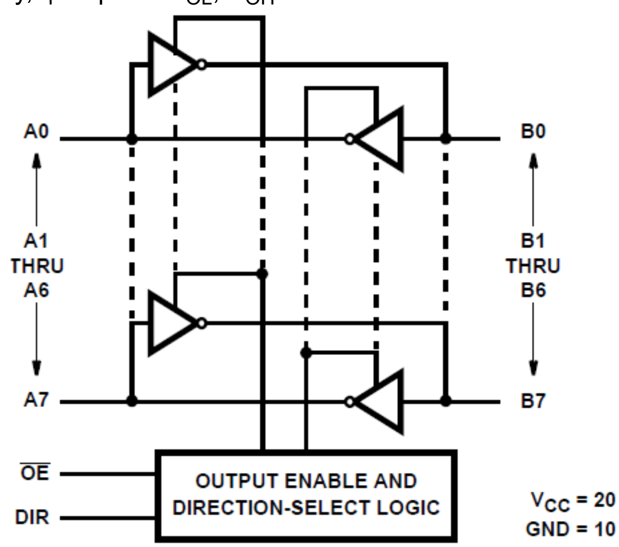
2 Description

The CDx4HC640 and CDx4HCT640 are inverting octal bus transceivers with 3-state outputs.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD54HC640	J (CDIP, 20)	26.92 mm × 6.92 mm
CD74HC640	N (PDIP, 20)	25.4 mm × 6.35 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm
CD54HCT640	J (CDIP, 20)	26.92 mm × 6.92 mm
CD74HCT640	N (PDIP, 20)	25.40 mm × 6.35 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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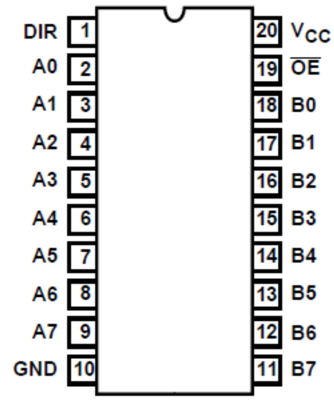
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2003) to Revision C (July 2022) **Page**

- Updated the numbering, formatting, tables, figures and cross-references throughout the document to reflect modern data sheet standards......1

4 Pin Configuration and Functions



J, N and DW Package
20-Pin CDIP, PDIP or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
I_{IK}	Input diode current	For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$		±20	mA
I_{OK}	Output diode current	For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$		±20	mA
I_O	Drain current, per output	For $-0.5V < V_O < V_{CC} + 0.5V$		±35	mA
I_O	Output source or sink current per output pin	For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C
	Lead temperature (Soldering 10s)(SOIC - lead tips only)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	HC types	2	6	V
		HCT types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input rise and fall time	V_{CC} = 2V		1000	ns
		V_{CC} = 4.5V		500	
		V_{CC} = 6V		400	
T_A	Temperature range		-55	125	°C

5.3 Thermal Information

THERMAL METRIC		N (PDIP)	DW (SOIC)	UNIT
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[(1)]	69	58	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[1]	V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V_{IL}	Low-level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	V
V_{OH}	High-level output voltage CMOS loads	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		V
	High-level output voltage TTL loads	I_{OH}= – 6 mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 7.8 mA	6	5.48			5.34		5.2		V
V_{OL}	Low-level output voltage CMOS loads	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
		I_{OL} = 20 µA	6			0.1		0.1		0.1	V
	Low-level output voltage TTL loads	I_{OL}= 6 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 7.8 mA	6			0.26		0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	V_I = V_{CC} or GND	6			8		80		160	µA
I_{OZ}	Three-state leakage current	V_O = V_{CC} or GND	6			±0.5		±5		±10	µA
HCT TYPES											
V_{IH}	High-level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low-level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High-level output voltage CMOS loads	V_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL loads	V_{OH} = – 6 mA	4.5	3.98			3.84		3.7		V
V_{OL}	Low-level output voltage CMOS loads	V_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low-level output voltage TTL	V_{OL} = 6 mA	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	V_I = V_{CC} or GND	5.5			8		80		160	µA
I_{OZ}	Three-state leakage current	V_O = V_{CC} or GND	5.5			±0.5		±5		±10	
ΔI_{CC} [1]	Additional quiescent device current per input pin	DIR input held at V_{CC} – 2.1	4.5 to 5.5		100	324		405		441	µA
		$\overline{OE}$ and A inputs held at V_{CC} – 2.1	4.5 to 5.5		100	540		675		735	µA
		B input held at V_{CC} – 2.1	4.5 to 5.5		100	540		675		735	µA

(1) For dual-supply systems theoretical worst case (VI = 2.4V, VCC = 5.5V) specification is 1.8mA

5.5 Switching Characteristics[(2)]

Input t_t = 6ns. Unless otherwise specified, C_L = 50pF

PARAMETER		V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t_{pd}	Propagation delay A to $\overline{B}$ B to $\overline{A}$	2			90		115		135	ns
		4.5		7 (1)	18		23		27	
		6			15		20		23	
t_{pd}	Propagation delay Output High-Z To high level, low level	2			150		190		225	ns
		4.5		12 (1)	30		38		45	
		6			26		33		38	
t_{pd}	Propagation delay Output high level Output lowe level to high Z	2			150		190		225	ns
		4.5		12 (1)	30		38		45	
		6			26		33		38	
t_t	Output transition time	2			60		75		90	ns
		4.5			12		15		18	
		6			10		13		15	
C_i	Input Capacitance		10		10		10		10	pF
C_O	Three-state output capacitance				20		20		20	pF
C_{pd}	Power dissipation capacitance (3) (4)	5		38						pF
HCT TYPES										
t_{pd}	Propagation delay A to $\overline{B}$ B to $\overline{A}$	4.5		9 (1)	22		28		33	ns
t_{pd}	Propagation delay Output High-Z To high level, low level	4.5		12 (1)	30		38			ns
t_{pd}	Propagation delay Output high level Output lowe level to high Z	4.5		12 (1)	30		38			ns
t_t	Transition times	4.5			12		15			ns
C_i	Input capacitance		10		10		10			pF
C_O	Three-state output capacitance				20		20			pF
C_{pd}	Power dissipation capacitance (3) (4)	5		41						pF

(1) Typical value tested at 5V, C_L = 15pF.
(2) For details on CMOS power calculation see, SCAA053B
(3) CPD is used to determine the dynamic power consumption, per channel
(4) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

6 Parameter Measurement Information

t_{PD} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

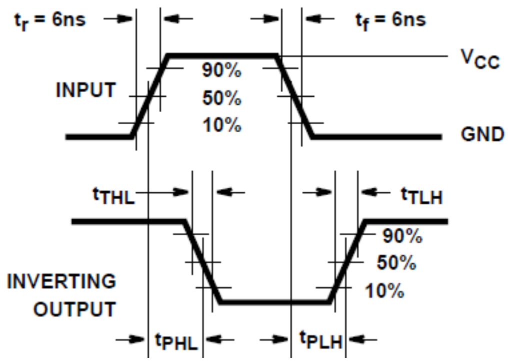


Figure 6-1. HC transition times and propagation delay times, combination logic

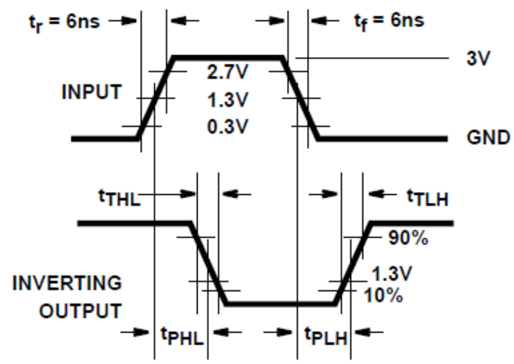


Figure 6-2. HCT transition times and propagation delay times, combination logic

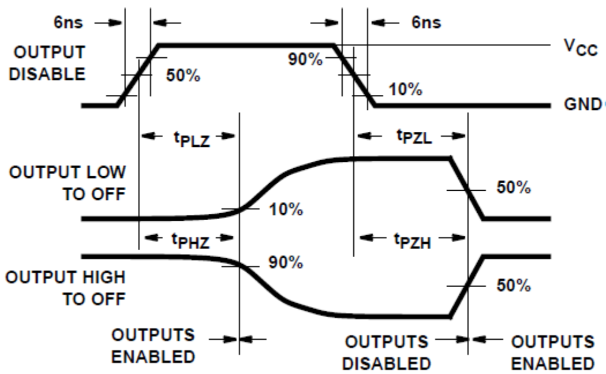


Figure 6-3. HC three-state propagation delay waveform

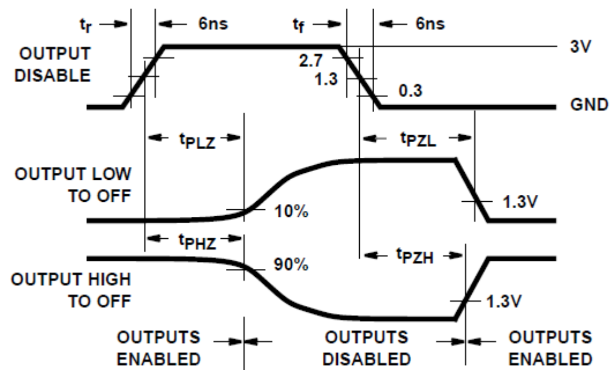
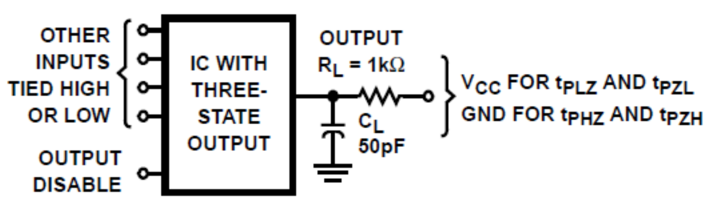


Figure 6-4. HCT three-state propagation delay waveform



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is output R_L = 1kΩ to V_{CC}, C_L = 50pF.

Figure 6-5. HC and HCT three-state propagation delay test circuit

7 Detailed Description

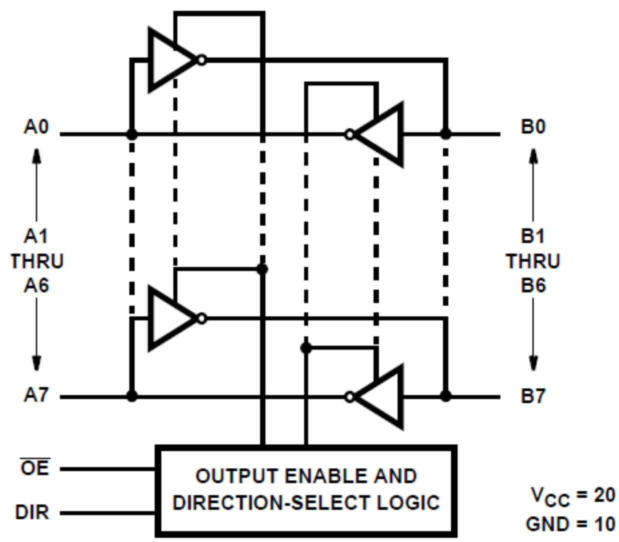
7.1 Overview

The CDx4HC640 and CDx4HCT640 silicon-gate CMOS three-state bidirectional inverting and non-inverting buffers are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits, and have speeds comparable to low power Schottky TTL circuits. They can drive 15 LSTTL loads. The CDx4HC640 and CDx4HCT640 devices have inverting buffers.

The direction of data flow (A to B, B to A) is controlled by the DIR input.

Outputs are enabled by a low on the Output Enable input ($\overline{OE}$); a high $\overline{OE}$ puts these devices in the high impedance mode.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Function Table(2)

Control Inputs(1)		Data Port Status	
$\overline{OE}$	DIR	A_n	B_n
L	L	$\overline{O}$	I
H	H	Z	Z
H	L	Z	Z
L	H	I	$\overline{O}$

(1) H = High level. L = Low level. I = Input. $\overline{O}$ = Output (inversion of input level). Z = High impedance.
(2) To prevent excess currents in the High-Z modes all I/O terminals should be terminated with 1kΩ to 1MΩ resistors.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8974001RA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974001RA CD54HCT640F3A
CD54HC640F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780901RA CD54HC640F3A
CD54HC640F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780901RA CD54HC640F3A
CD54HCT640F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974001RA CD54HCT640F3A
CD54HCT640F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974001RA CD54HCT640F3A
CD74HC640E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC640E
CD74HC640E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC640E
CD74HC640M	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC640M
CD74HC640M.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC640M
CD74HCT640E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT640E
CD74HCT640E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT640E
CD74HCT640M	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT640M
CD74HCT640M.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT640M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC640, CD54HCT640, CD74HC640, CD74HCT640 :

- Catalog : CD74HC640, CD74HCT640

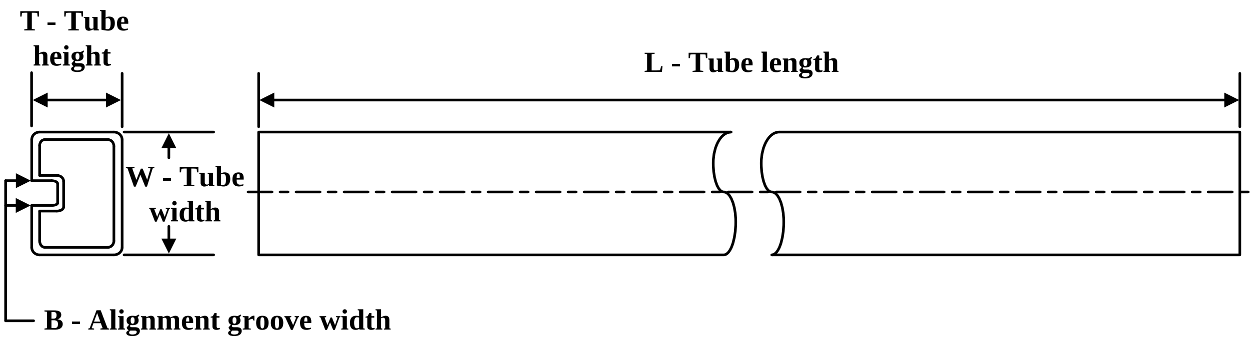
- Military : CD54HC640, CD54HCT640

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TUBE

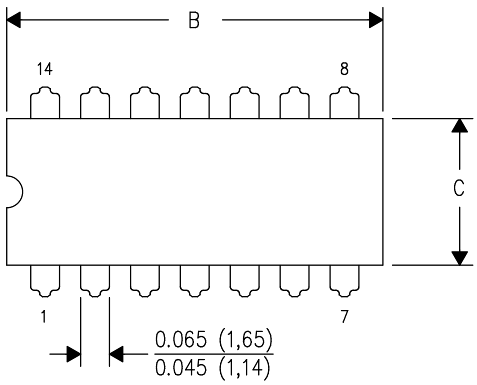


*All dimensions are nominal

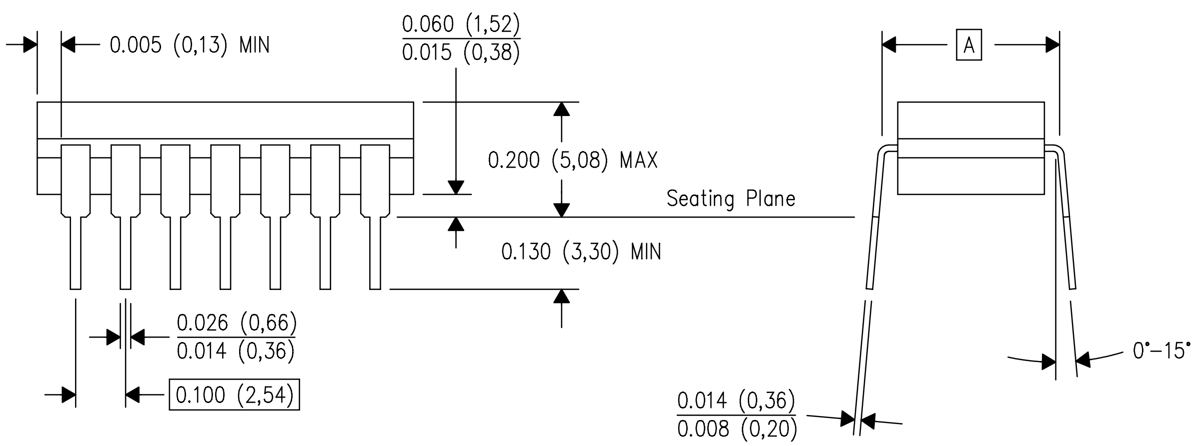
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC640E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC640E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC640M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HC640M.A	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT640E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT640E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT640M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT640M.A	DW	SOIC	20	25	507	12.83	5080	6.6

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

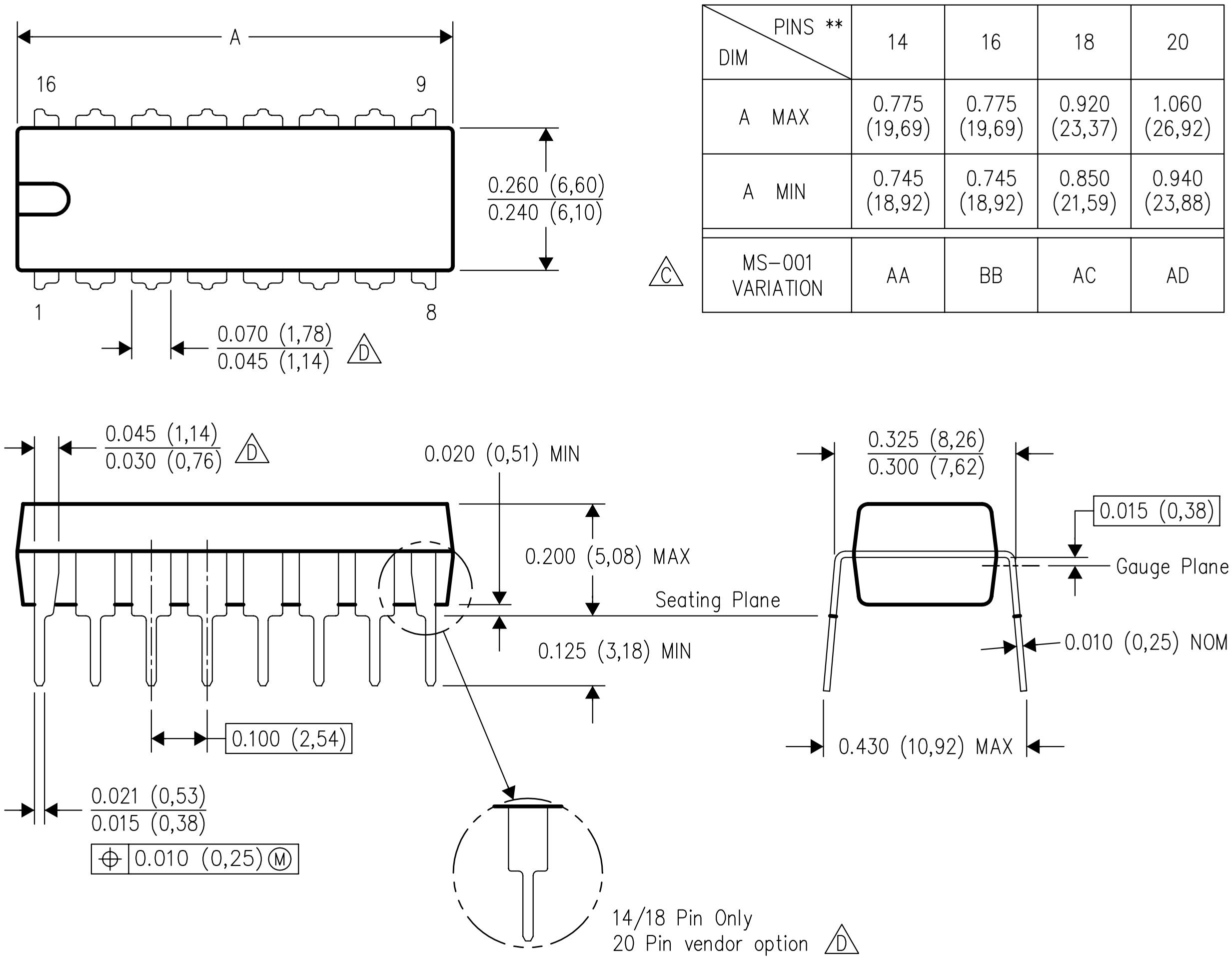


4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

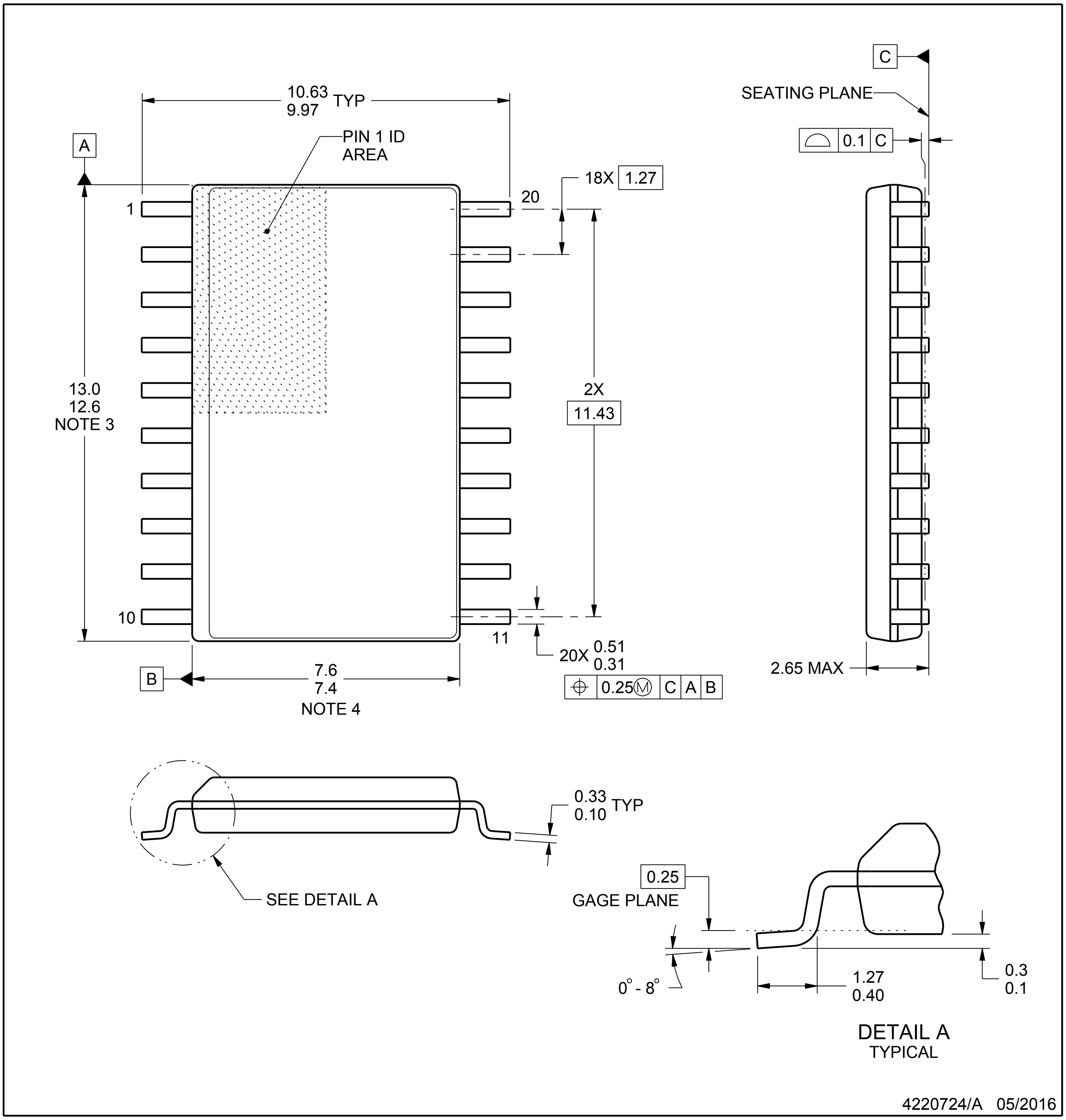
16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

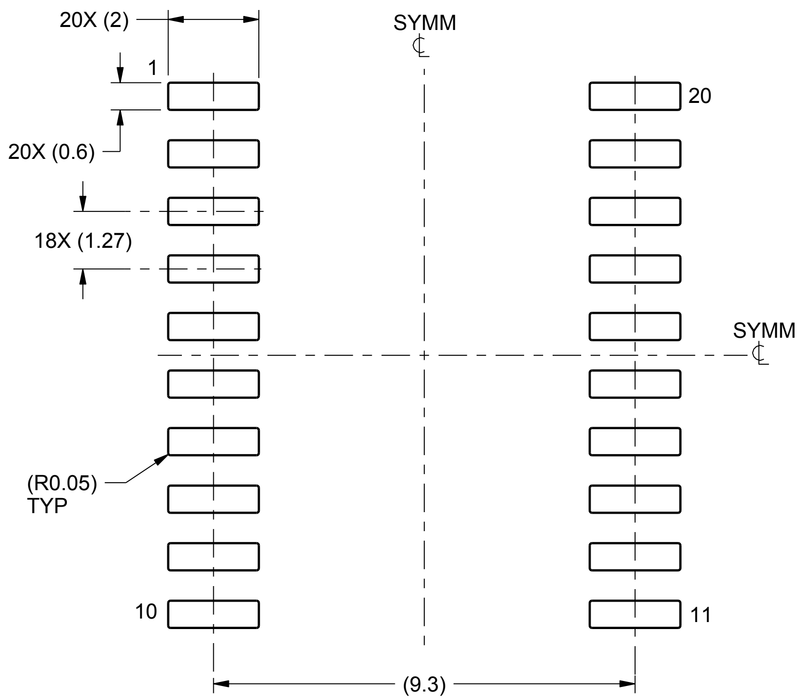
4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

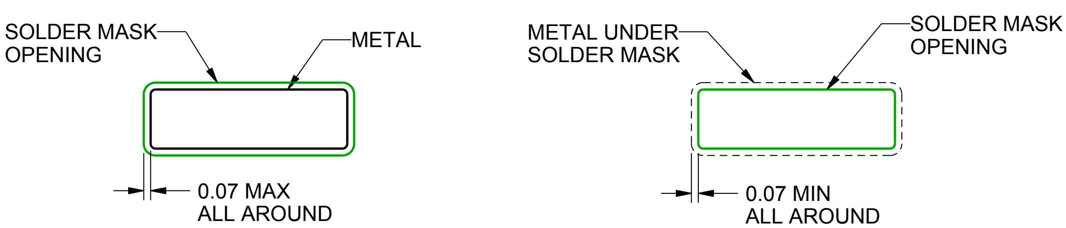


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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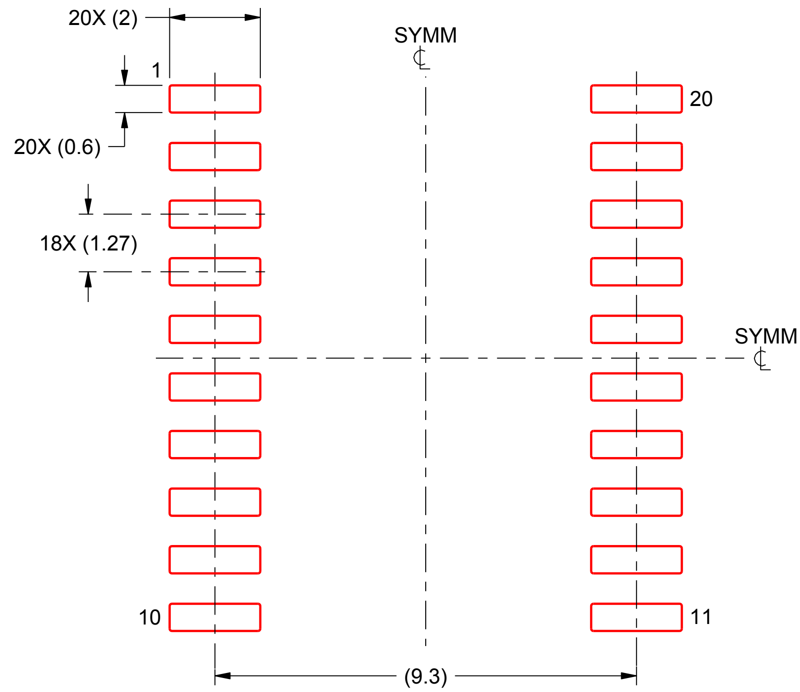
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.