CD74HCx4067-Q1 Automotive High-Speed CMOS Logic 16-Channel Analog Mulitplexer and Demultiplexer

1 Features

- Qualified for automotive applications
- AEC-Q100 test guidance with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD Classification Level H1A
  - Device CDM ESD Classification Level C2
- Wide analog input voltage range
- Low ON resistance
  - 70Ω typical (V_{CC} = 4.5V)
- Fast switching and propagation speeds
- Break-before-make switching
  - 6ns typical (V_{CC} = 4.5V)
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- 4.5V to 5.5V operation
- Direct LSTTL input logic compatibility: V_{IL} = 0.8V maximum, V_{IH} = 2V minimum
- CMOS input compatibility: $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

2 Applications

- Automotive
- Analog switch
- Analog multiplexer and demultiplexer

3 Description

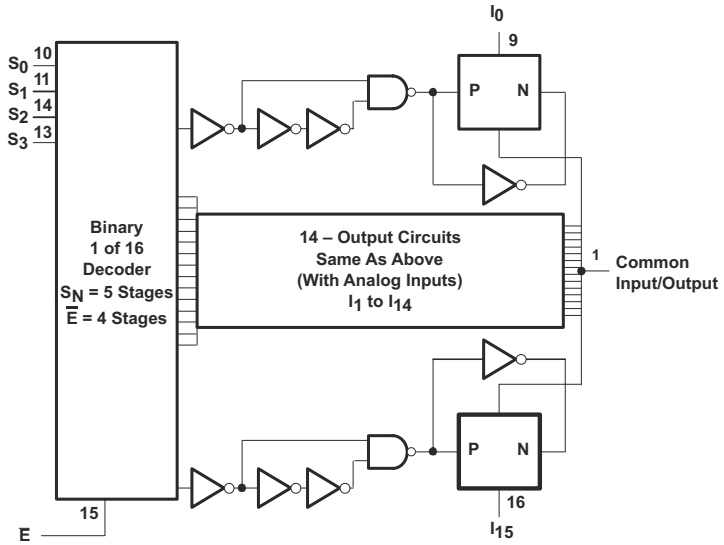
The CD74HCx4067-Q1 device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer and demultiplexer controls analog voltages that may vary across the voltage supply range. It is a bidirectional switch, thus allowing any analog input to be used as an output and vice-versa. The switch has low (on) resistance and low (off) leakages. In addition, the device has an enable control that, when high, disables all switches to their off state.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
CD74HCx4067QM96Q1	DW (SOIC, 24)	15.5mm × 10.3mm
CD74HCx4067QRGYRQ1	RGY (QFN, 24)	5.5mm × 3.5mm
CD74HCx4067QDGSRQ1	DGS (VSSOP, 24)	6.1mm × 3mm
CD74HCx4067QPWRQ1	PW (TSSOP, 24)	4.4mm × 7.8mm

(1) For more information, see Section 18.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

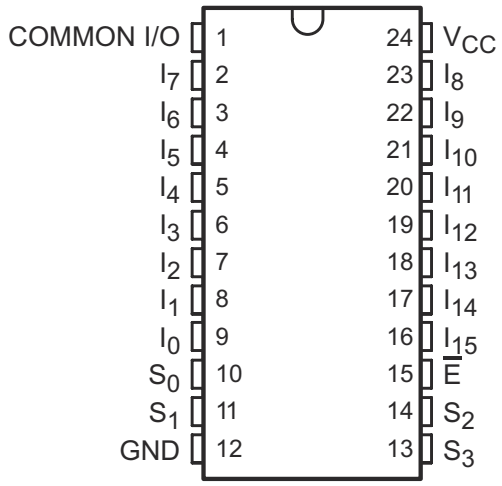


Figure 4-1. DW Package, 24-Pin SOIC (Top View)

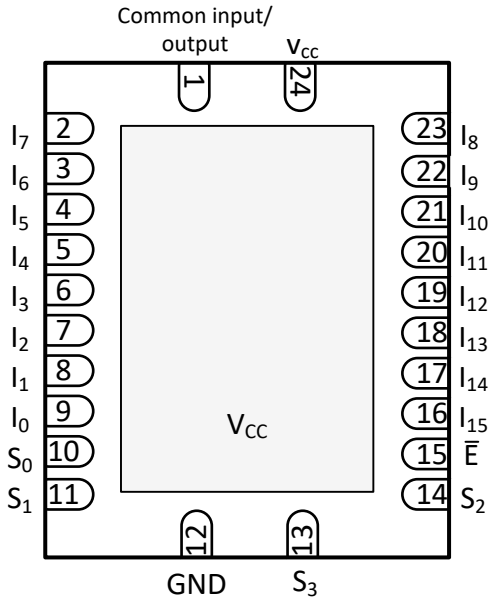


Figure 4-2. RGY Package, 24-Pin QFN (Top View) (Pad on Bottom)

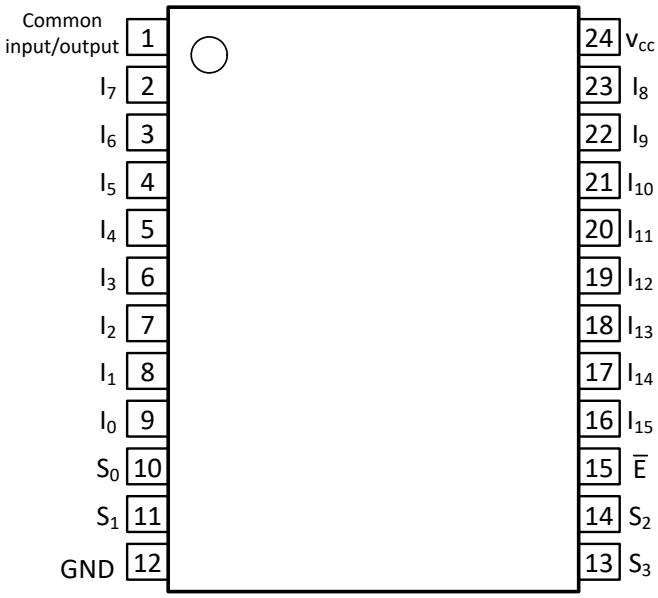


Figure 4-3. PW Package, 24-Pin TSSOP (Top View)

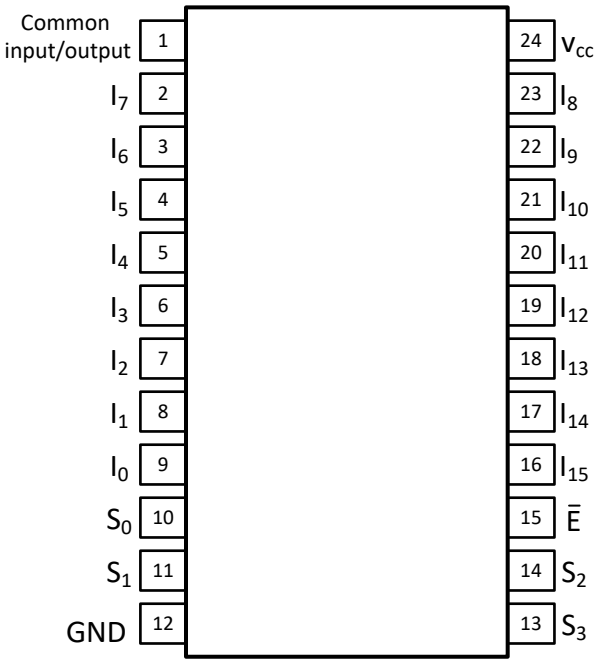


Figure 4-4. DGS Package, 24-Pin VSSOP (Top View)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
COMMON INPUT/ OUTPUT	1	IO	Common input or output.
I_7	2	IO	Switch input/output
I_6	3	IO	Switch input/output
I_5	4	IO	Switch input/output
I_4	5	IO	Switch input/output
I_3	6	IO	Switch input/output
I_2	7	IO	Switch input/output
I_1	8	IO	Switch input/output
I_0	9	IO	Switch input/output
S_0	10	I	Select/Address pin
S_1	11	I	Select/Address pin
GND	12	P	Ground pin
S_3	13	I	Select/Address pin
S_2	14	I	Select/Address pin
$\overline{E}$	15	I	Enable for all switches ON/OFF
I_{15}	16	IO	Switch input/output
I_{14}	17	IO	Switch input/output
I_{13}	18	IO	Switch input/output
I_{12}	19	IO	Switch input/output
I_{11}	20	IO	Switch input/output
I_{10}	21	IO	Switch input/output
I_9	22	IO	Switch input/output
I_8	23	IO	Switch input/output
V_{CC}	24	P	Power pin
Thermal Pad		-	The thermal pad is not electrically connected and can be floated, grounded or tied to V_{CC}

(1) I = input, O = output. P = power

5 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC} HC	DC Supply voltage		-0.5	7	V
V_{CC} HCT			–0.5	7	V
I_{IK}	DC input diode current	For V_I < -0.5V or V_I > V_{CC} + 0.5V	–20	20	mA
I_{OK}	DC output diode current	For V_O < -0.5V or V_O > V_{CC} + -0.5V	–20	20	mA
I_{CC}	DC V_{CC} or ground current		–50	50	mA
DC Output Source or Sink Current per Output Pin, I_O	For V_O > -0.5V or V_O < V_{CC} + -0.5V		–25	25	mA
T_{JMAX}	Maximum junction temperature (Plastic Package)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

6 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins(1)	400	V
		Charged device model (CDM), per AEC Q100-011, all pins	250	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7 Thermal Information

THERMAL METRIC (1)		CD74HCx4067				UNIT
		DW (SOIC)	RGY (QFN)	DGS (VSSOP)	PW (TSSOP)	
		24 PINS	24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.8	67.1	96.8	97.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.0	59.2	43.4	45.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	45.4	58.7	62.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29.0	9.3	3.9	5.20	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.0	45.1	58.2	62.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	34.7	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range (T_A = full package temperature range)	74HC types	2		6	V
V_{CC}	Supply voltage range (T_A = full package temperature range)	74HCT types	4.5		5.5	V
V_{IS}	Analog switch I/O voltage		0		V_{CC}	V
T_A	Ambient temperature	Ambient temperature	–40		125	°C
t_r , t_f	Input rise and fall times	2V	0		1000	ns
		4.5V	0		500	
		6V	0		400	

9 Electrical Characteristics: HC Devices

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
Analog Switch									
		V_{IS} (V)	V_I (V)	V_{CC} (V)	T_A				
High Level Input Voltage	V_{IH}			2	–40°C to 125°C	1.5			V
				4.5		3.15			
				6		4.2			
Low Level Input Voltage	VIL			2				0.5	V
				4.5				1.35	
				6				1.8	
"ON" Resistance IO = 1mA	R_{ON}	V_{CC} or GND	V_{CC} or GND	4.5	25°C		70	160	Ω
					–40°C to 125°C			200	
				6	25°C		60	140	
					–40°C to 125°C			175	
		V_{CC} to GND	V_{CC} to GND	4.5	25°C		90	180	
					–40°C to 125°C			225	
				6	25°C		80	160	
					–40°C to 125°C			200	
"ON" Resistance Between Any Two Switches	ΔR_{ON}			4.5	25°C		10		Ω
				6	25°C		8.5		
Off-Switch Leakage Current	I_Z	$\overline{E}$ = V_{CC}	V_{CC} or GND	6	25°C			±0.8	μA
					–40°C to 125°C			±8	
Input Leakage Current (Any Control)	I_{IL}		V_{CC} or GND(1)	6	25°C			±0.1	μA
					–40°C to 125°C			±1	
Quiescent Device Current	I_{CC}		V_{CC} or GND	6	25°C			8	μA
					–40°C to 125°C			160	

(1) Any voltage between V_{CC} and GND.

10 Electrical Characteristics: HCT Devices

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS				MIN	TYP	MAX	UNIT
Analog Switch										
			V_{IS} (V)	**V_I (V)**	**V_{CC} (V)**	**T_A**				
High Level Input Voltage		V_{IH}			4.5	25°C	2			V
Low Level Input Voltage		V_{IL}				–40°C to 125°C			0.8	V
"ON" Resistance IO = 1mA		R_{ON}	V_{CC} or GND	V_{CC} or GND	4.5	25°C		70	160	Ω
						–40°C to 125°C			200	
			VCC to GND	VCC to GND		25°C		90	180	
						–40°C to 125°C			225	
"ON" Resistance Between Any Two Switches		ΔR_{ON}			4.5	25°C		10		Ω
Off-Switch Leakage Current		I_Z	$\overline{E}$ = V_{CC}	V_{CC} or GND	5.5	25°C			±0.8	µA
						–40°C to 125°C			±8	
Input Leakage Current (Any Control)		I_{IL}		V_{CC} or GND	5.5	25°C			±0.1	µA
						–40°C to 125°C			±1	
Quiescent Device Current		I_{CC}		V_{CC} or GND	5.5	25°C			8	µA
						–40°C to 125°C			80	
Additional Quiescent Device Current Per Input Pin: 1 Unit Load		ΔI_{CC} (1)		V_{CC} - 2.1	4.5 to 5.5	25°C		100	360	µA
						–40°C to 125°C			450	
C_I	Control inputs					25°C			10	pF
						–55°C to 85°C			10	
						–55°C to 125°C			10	

(1) For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA

11 Switching Characteristics HC

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		C_L (pF)	MIN	NOM	MAX	UNIT
	FROM (INPUT) TO (OUTPUT)	V_{CC} (V)	T_A					
t_{pd}	I_n TO Common I/O	2	25°C	50			75	ns
			-40°C to 125°C				110	
		4.5	25°C				15	ns
			-40°C to 125°C				22	
		6	25°C				13	ns
			-40°C to 125°C				19	
		5	25°C	15		6		ns
t_{en}	$\overline{E}$ TO Common I/O	2	25°C	50			275	ns
			-40°C to 125°C				415	
		4.5	25°C				55	ns
			-40°C to 125°C				83	
		6	25°C				47	ns
			-40°C to 125°C				71	
		5	25°C	15		23		ns
t_{en}	S_n TO Common I/O	2	25°C	50			300	ns
			-40°C to 125°C				450	
		4.5	25°C				60	ns
			-40°C to 125°C				90	
		6	25°C				51	ns
			-40°C to 125°C				76	
		5	25°C	15		25		ns
t_{dis}	$\overline{E}$ TO Common I/O	2	25°C	50			275	ns
			-40°C to 125°C				415	
		4.5	25°C				55	ns
			-40°C to 125°C				83	
		6	25°C				47	ns
			-40°C to 125°C				71	
		5	25°C	15		23		ns
t_{dis}	S_n TO Common I/O	2	25°C	50			290	ns
			-40°C to 125°C				435	
		4.5	25°C				58	ns
			-40°C to 125°C				87	
		6	25°C				49	ns
			-40°C to 125°C				74	
		5	25°C	15		21		ns

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		C_L (pF)	MIN	NOM	MAX	UNIT
C_{PD} Power dissipation capacitance(1)	C_{PD}	5	25°C			93		pF

12 Switching Characteristics HCT

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		C_L (pF)	MIN	NOM	MAX	UNIT
	FROM (INPUT) TO (OUTPUT)	V_{CC} (V)	T_A					
t_{pd}	I_n TO Common I/O	5	25°C	15		6		ns
		4.5	25°C	50			15	
			-40°C to 125°C				19	
t_{en}	$\overline{E}$ TO Common I/O	5	25°C	15		25		ns
		4.5	25°C	50			60	
			-40°C to 125°C				75	
t_{en}	S_n TO Common I/O	5	25°C	15		25		ns
		4.5	25°C	50			60	
			-40°C to 125°C				75	
t_{dis}	$\overline{E}$ TO Common I/O	5	25°C	15		23		ns
		4.5	25°C	50			55	
			-40°C to 125°C				69	
t_{dis}	S_n TO Common I/O	5	25°C	15		21		ns
		4.5	25°C	50			58	
			-40°C to 125°C				73	
C_{PD} Power dissipation capacitance(1)	C_{PD}	5	25°C			96		pF

13 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

Parameter	Test Conditions		V_{CC} (V)	HC	HCT	UNIT
Switch Frequency Response Bandwidth at -3dB			4.5	89	89	MHz
Total Harmonic Distortion	1kHz, V_{IS}= $4V_{PP}$		4.5	0.051	0.051	%
Switch "OFF" signal feedthrough			4.5	-75	-75	dB
C_S Switch input capacitance				5	5	pF
C_{COM} Common Capacitance				50	50	pF

14 Parameter Measurement Information

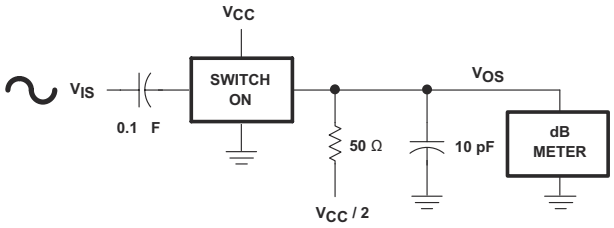


Figure 14-1. Frequency-Response Test Circuit

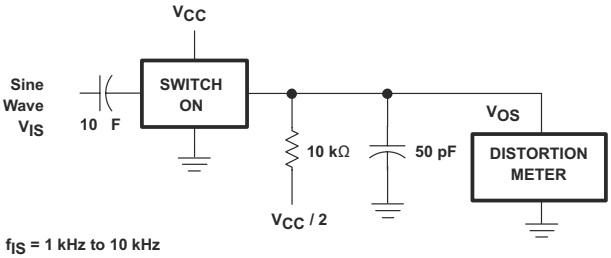


Figure 14-2. Sine-Wave Distortion Test Circuit

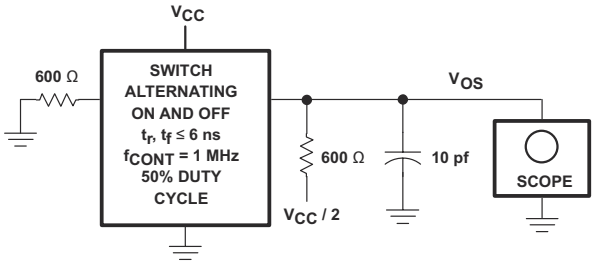


Figure 14-3. Control-to-Switch Feedthrough Noise Test Circuit

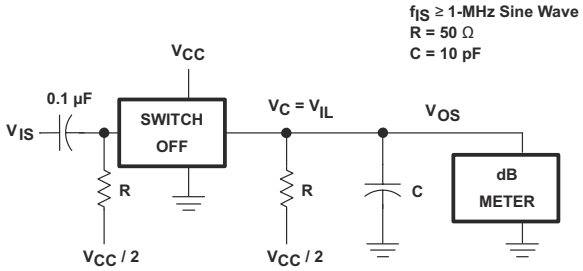
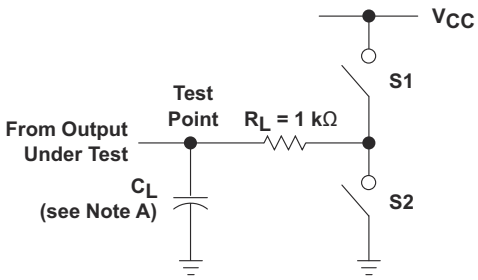
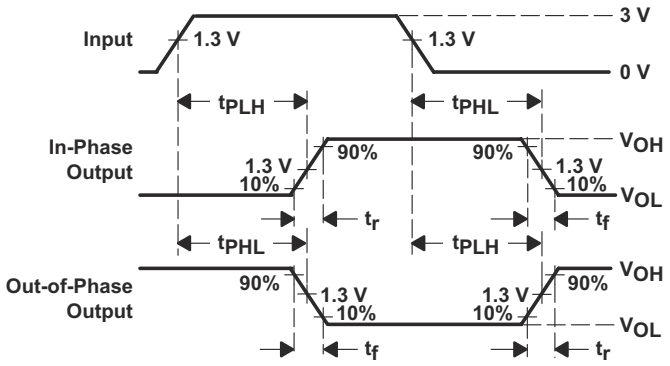


Figure 14-4. Switch OFF Signal Feedthrough Test Circuit

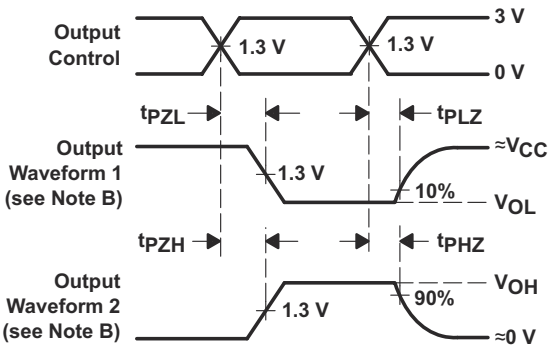


LOAD CIRCUIT

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 14-5. Load Circuit and Voltage Waveforms

15 Detailed Description

15.1 Functional Block Diagram

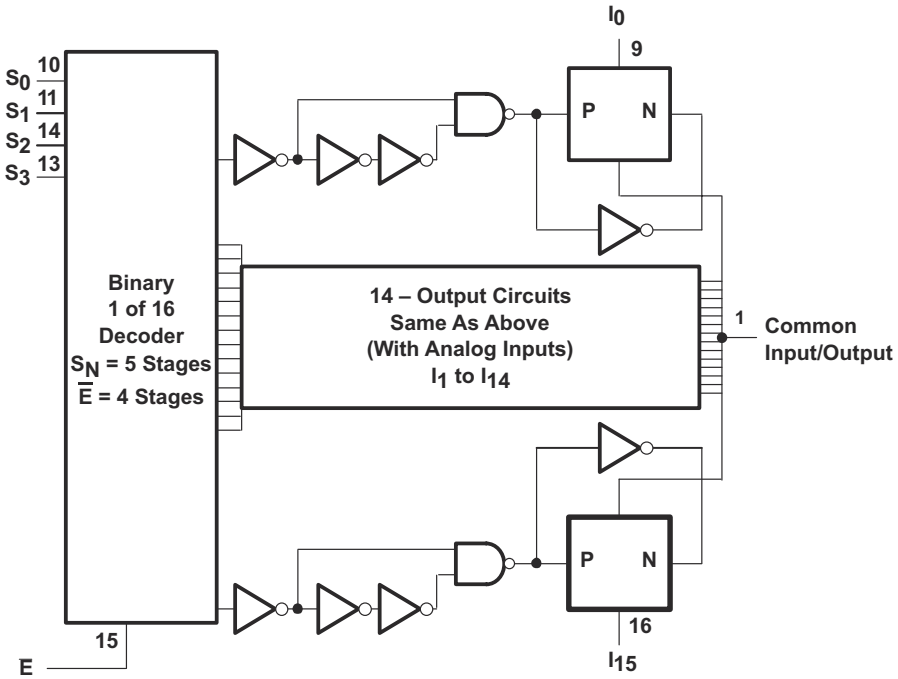


Figure 15-1. Logic Diagram (Positive Logic)

15.2 Device Functional Modes

Table 15-1. Function Table (1)

S0	S1	S2	S3	$\overline{E}$	SELECTED CHANNEL
X	X	X	X	H	None
L	L	L	L	L	0
H	L	L	L	L	1
L	H	L	L	L	2
H	H	L	L	L	3
L	L	H	L	L	4
H	L	H	L	L	5
L	H	H	L	L	6
H	H	H	L	L	7
L	L	L	H	L	8
H	L	L	H	L	9
L	H	L	H	L	10
H	H	L	H	L	11
L	L	H	H	L	12
H	L	H	H	L	13
L	H	H	H	L	14
H	H	H	H	L	15

(1) H = High level
L = Low level
X = Don't Care

16 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

16.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

16.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

16.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

16.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

16.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

17 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2025) to Revision D (April 2025)	Page
• Added CD74HC4067-Q1	1

Changes from Revision B (April 2008) to Revision C (February 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated Thermal parameters for DW package	6
• Added RGY, DGS, and PW packages	6
• Added HC Electrical characteristics	7
• Added HC Switching characteristics	9

Changes from Revision A (April 2008) to Revision B (August 2012)	Page
• Changed H2 to H1A and C3B to C2 throughout document	1
• Added AEC-Q100 info to Features	1
• Removed from Features: Wide Operating Temperature Range: –40°C to 85°C	1
• Added applications	1
• Replaced SOIC-M package info in ordering info table with new row for DW-SOIC-M package	1

18 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4067QDGSRQ1	Active	Production	VSSOP (DGS) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	H4067Q
CD74HC4067QPWRQ1	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067Q
CD74HC4067QPWRQ1.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067Q
CD74HC4067QRGYRQ1	Active	Production	VQFN (RGY) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	HC4067Q
CD74HC4067QRGYRQ1.A	Active	Production	VQFN (RGY) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	HC4067Q
CD74HCT4067QDGSRQ1	Active	Production	VSSOP (DGS) | 24	5000 | LARGE T&R	-	Call TI	Level-1-260C-UNLIM	-40 to 125	T4067Q
CD74HCT4067QM96Q1	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4067I
CD74HCT4067QM96Q1.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4067I
CD74HCT4067QPWRQ1	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4067Q
CD74HCT4067QPWRQ1.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4067Q
CD74HCT4067QRGYRQ1	Active	Production	VQFN (RGY) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HCT4067Q
CD74HCT4067QRGYRQ1.A	Active	Production	VQFN (RGY) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HCT4067Q
D24067IM96G4Q1	Obsolete	Production	SOIC (DW) | 24	-	-	Call TI	Call TI	-40 to 85	HCT4067I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD74HC4067-Q1, CD74HCT4067-Q1 :

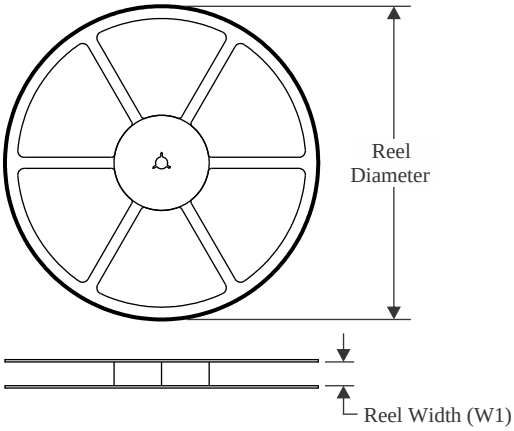
- Catalog : CD74HC4067, CD74HCT4067

NOTE: Qualified Version Definitions:

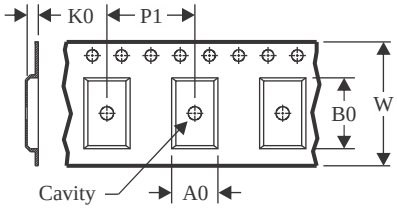
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

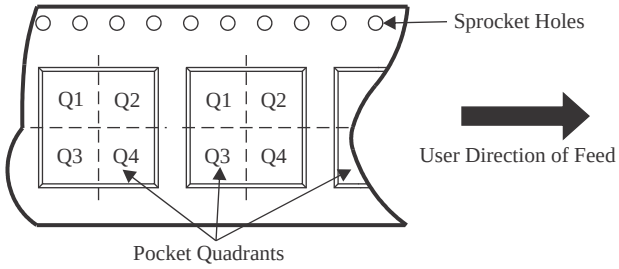


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

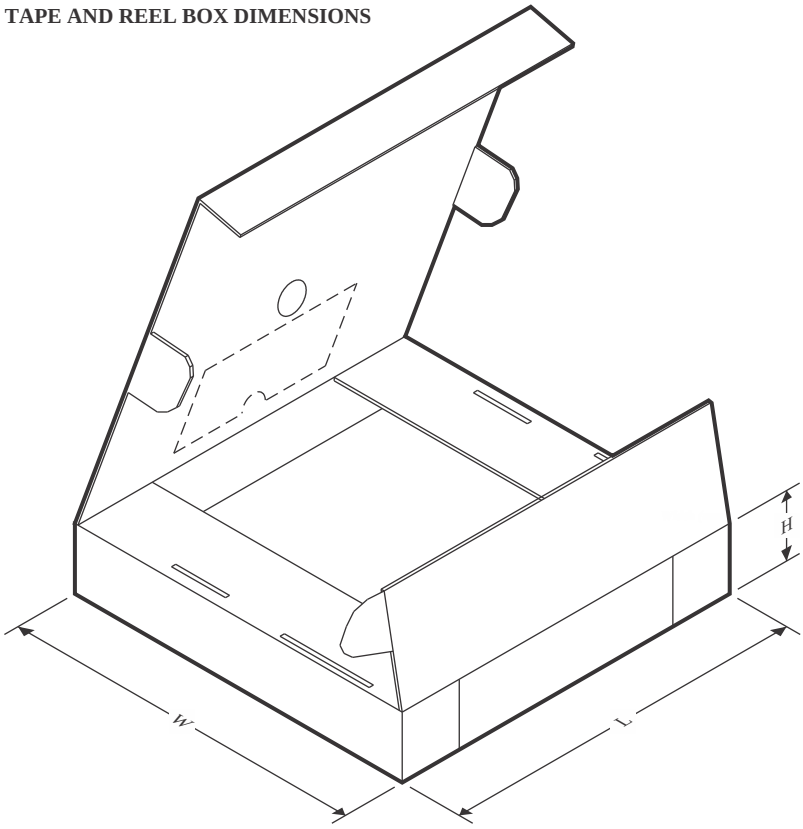
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4067QDGSRQ1	VSSOP	DGS	24	5000	330.0	16.4	5.44	6.4	1.45	8.0	16.0	Q1
CD74HC4067QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
CD74HC4067QRGYRQ1	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
CD74HCT4067QDGSRQ1	VSSOP	DGS	24	5000	330.0	16.4	5.44	6.4	1.45	8.0	16.0	Q1
CD74HCT4067QM96Q1	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74HCT4067QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
CD74HCT4067QRGYRQ1	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

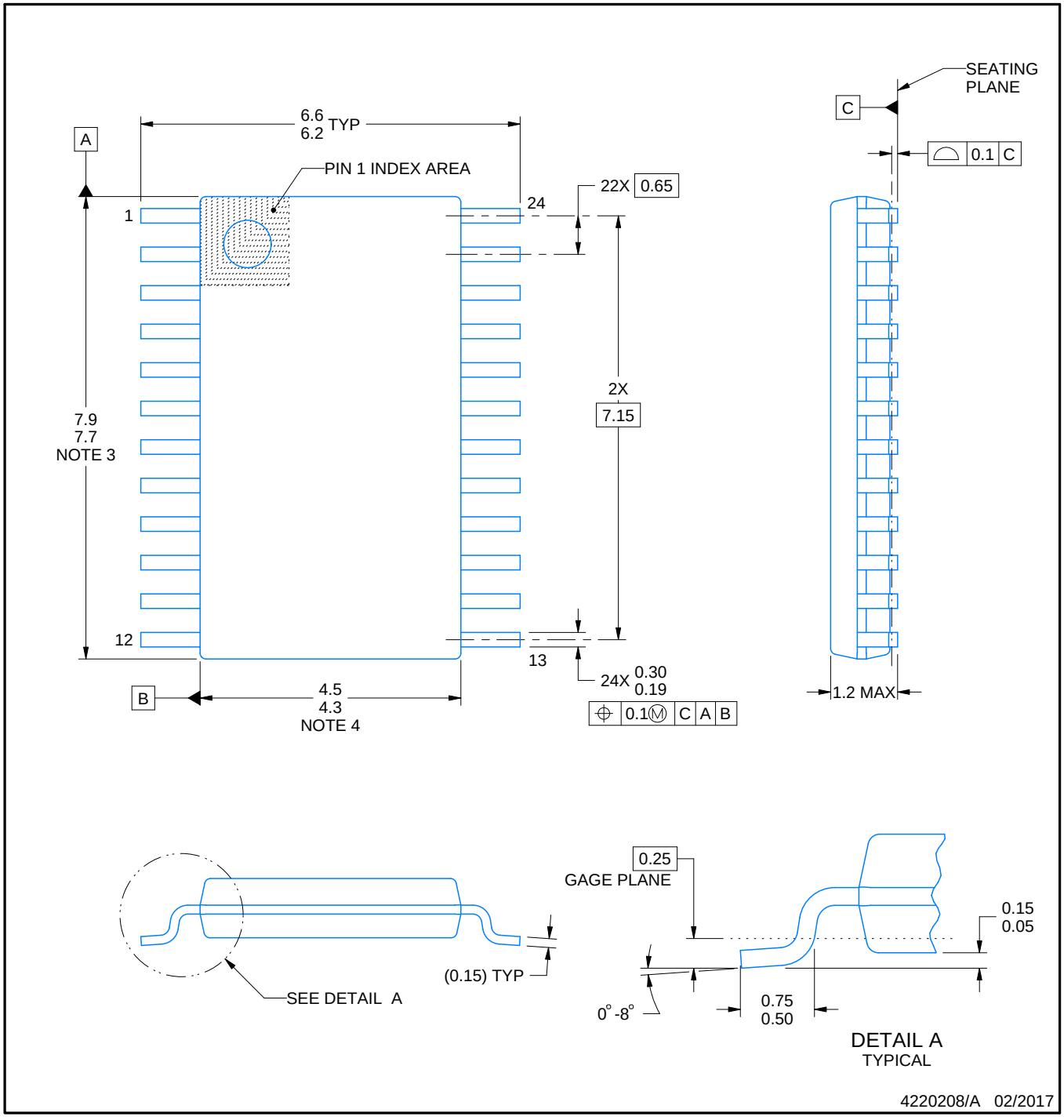
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4067QDGSRQ1	VSSOP	DGS	24	5000	353.0	353.0	32.0
CD74HC4067QPWRQ1	TSSOP	PW	24	2000	353.0	353.0	32.0
CD74HC4067QRGYRQ1	VQFN	RGY	24	3000	367.0	367.0	35.0
CD74HCT4067QDGSRQ1	VSSOP	DGS	24	5000	353.0	353.0	32.0
CD74HCT4067QM96Q1	SOIC	DW	24	2000	350.0	350.0	43.0
CD74HCT4067QPWRQ1	TSSOP	PW	24	2000	353.0	353.0	32.0
CD74HCT4067QRGYRQ1	VQFN	RGY	24	3000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0024A

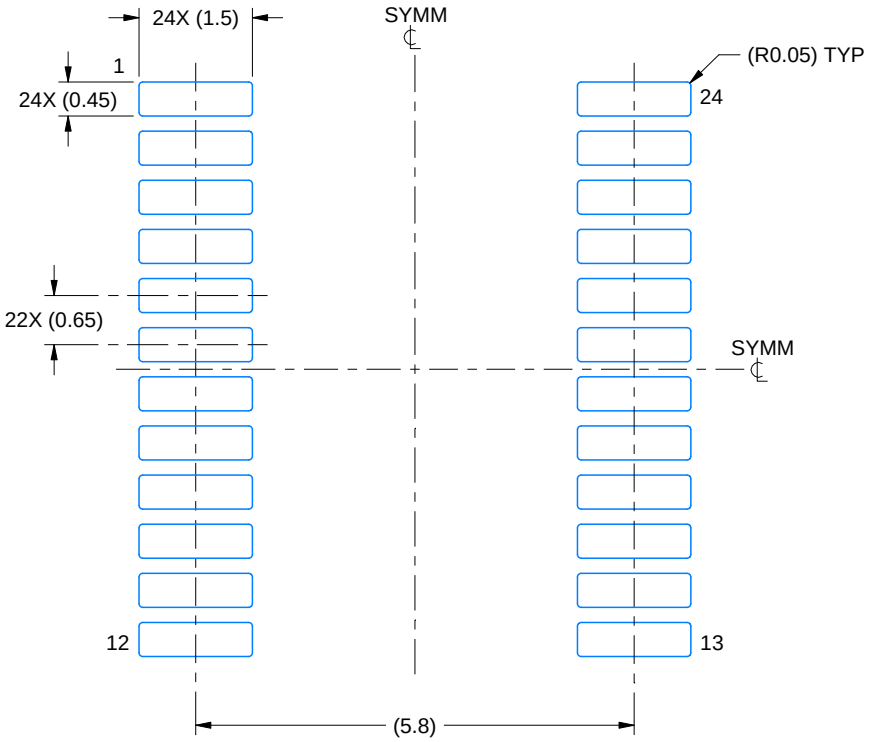
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

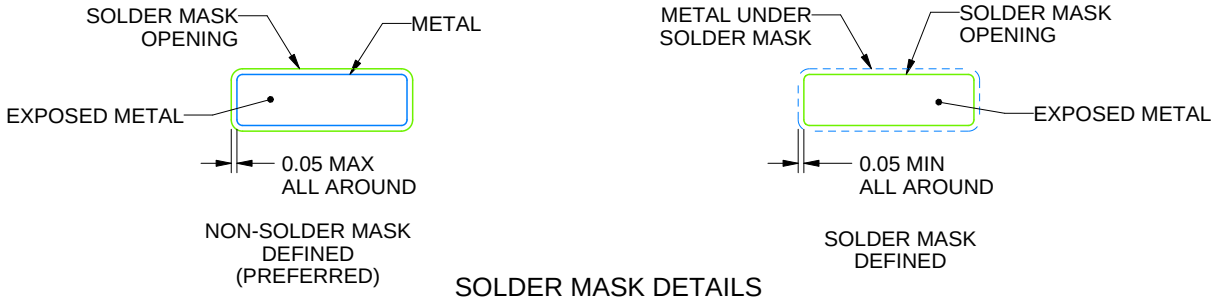


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

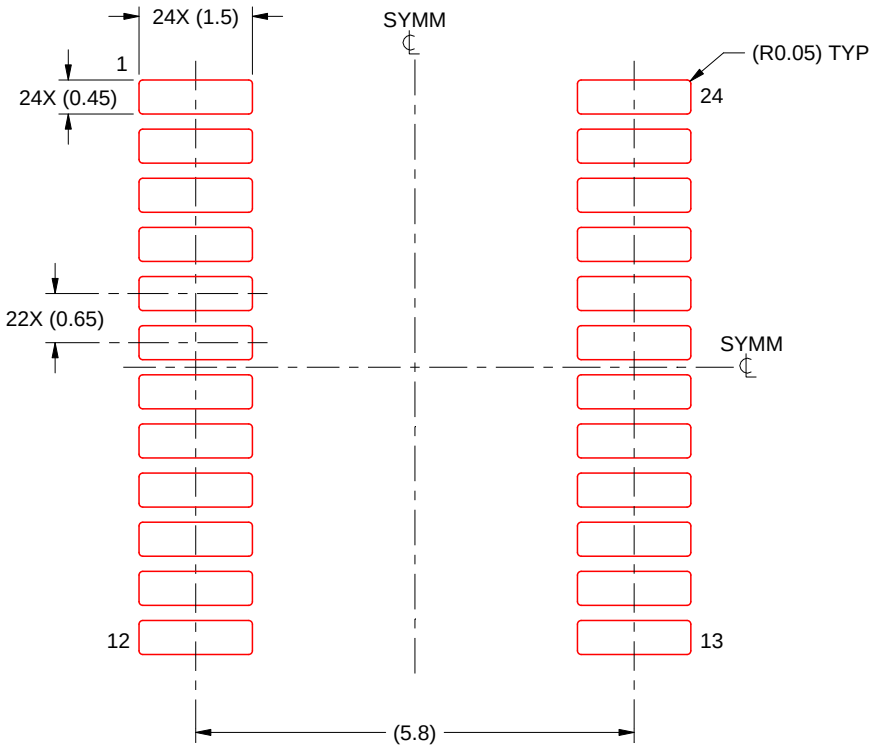


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

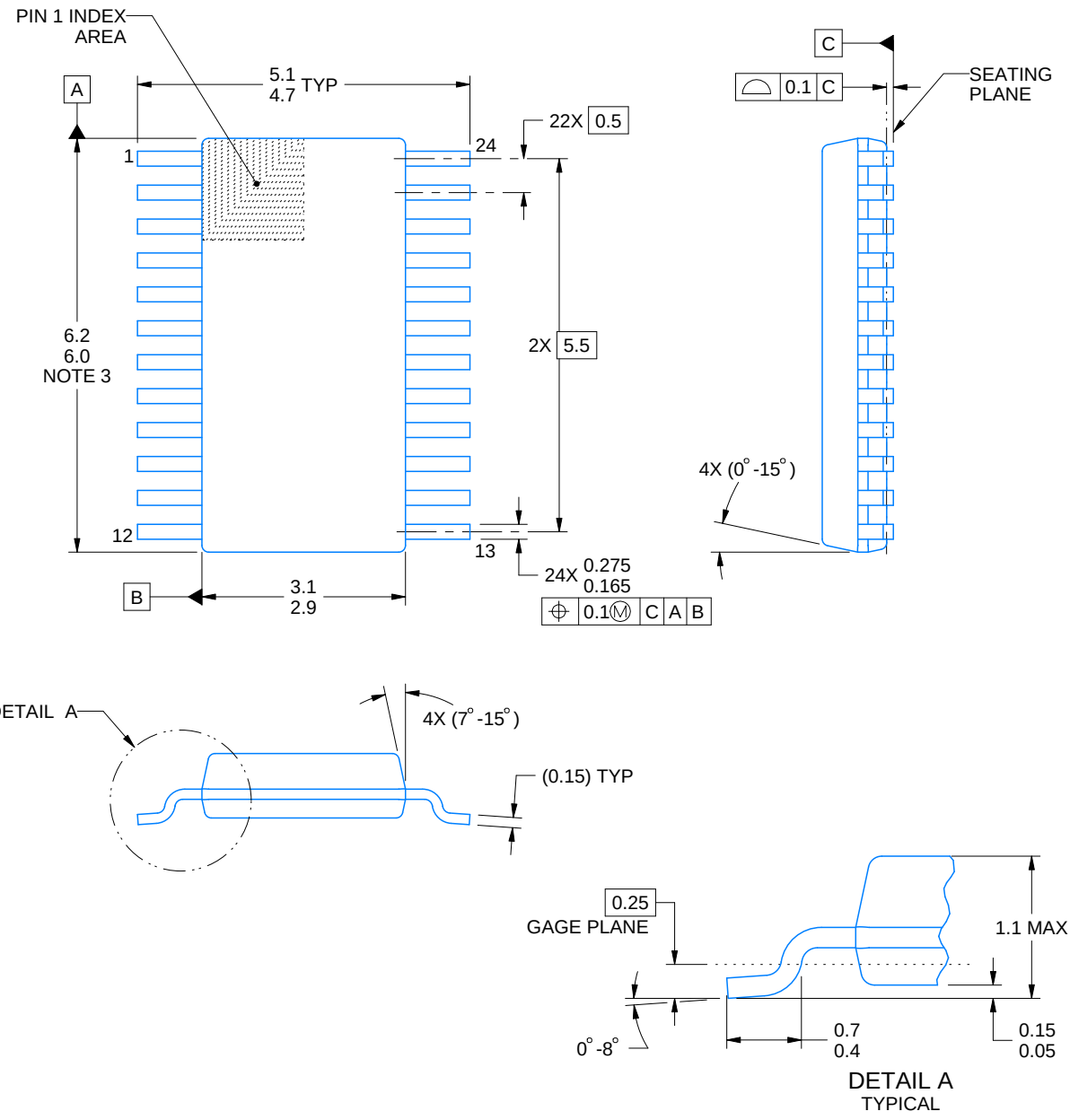
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0024A

VSSOP - 1.1 mm max height

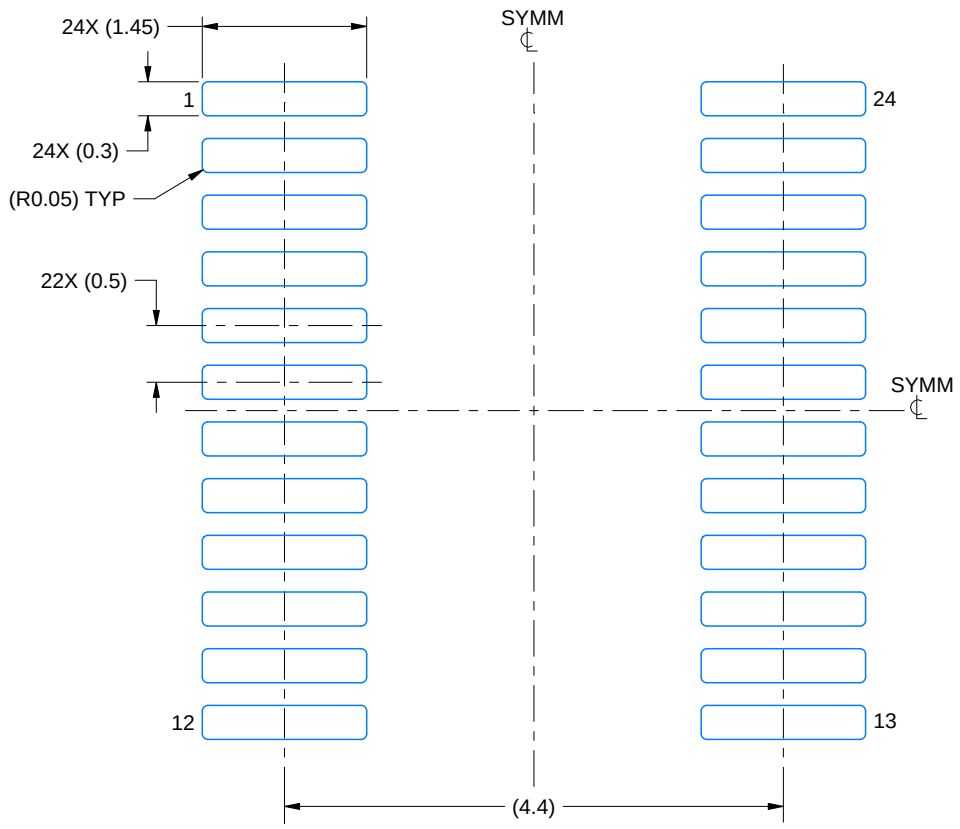
SMALL OUTLINE PACKAGE



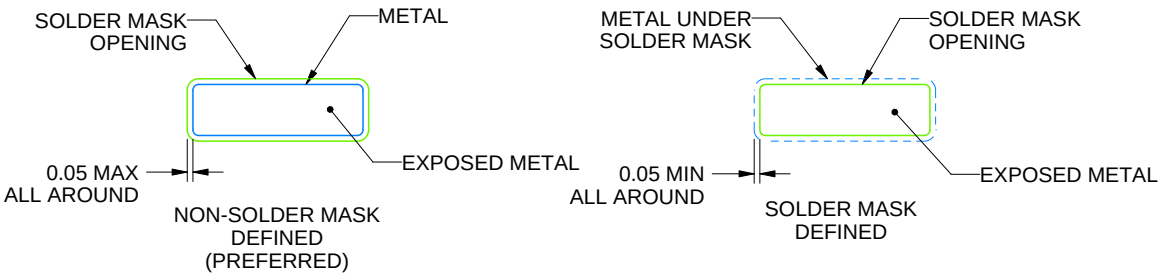
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 15X

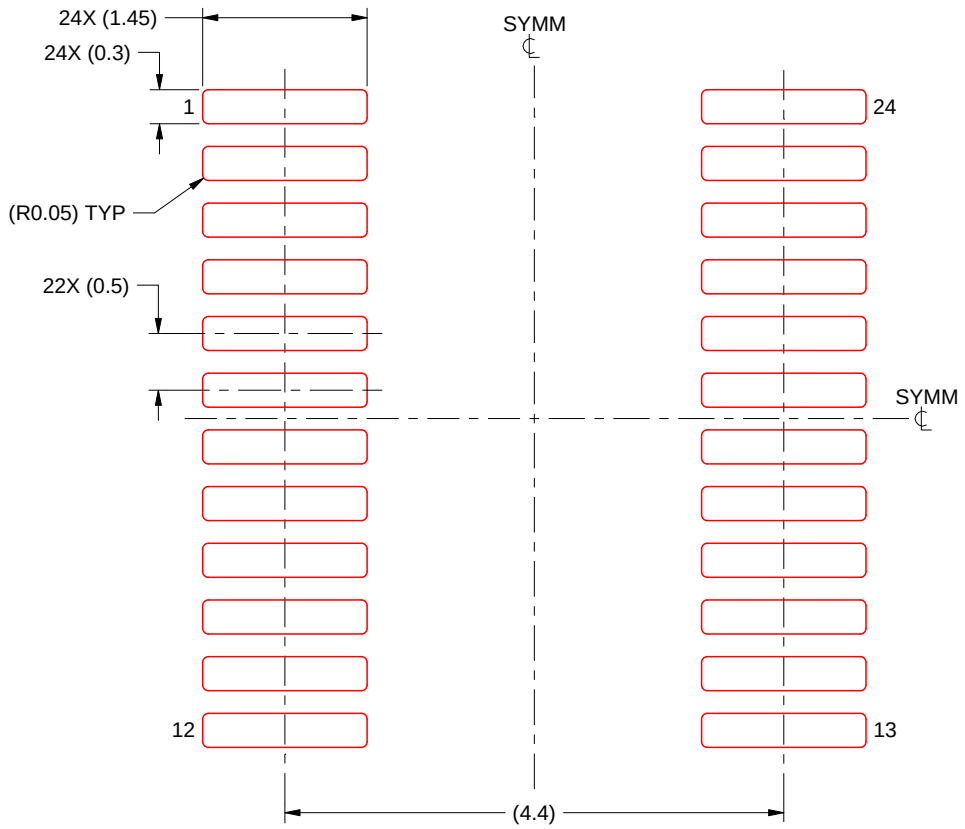


SOLDER MASK DETAILS

4226366/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



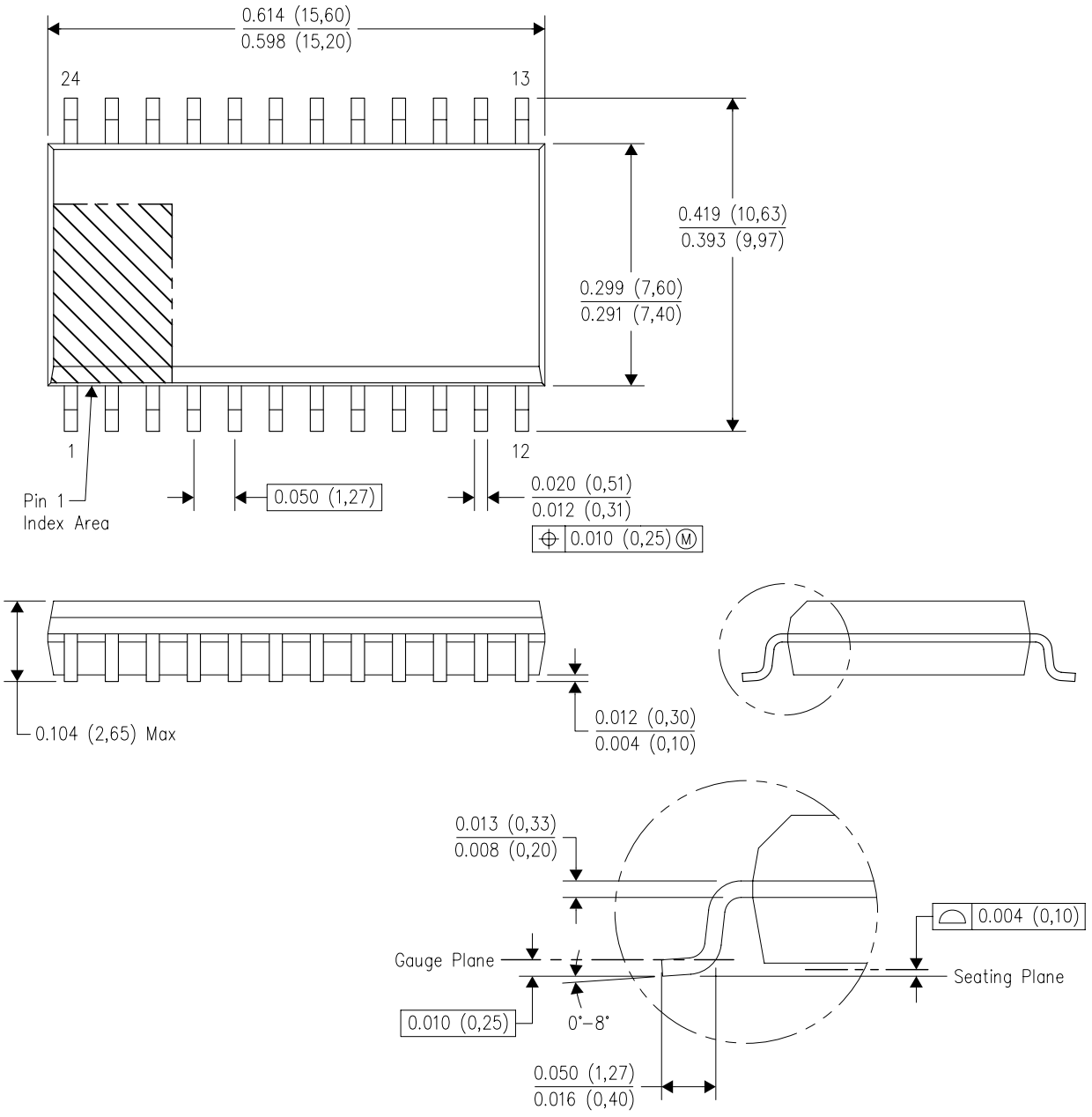
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

4226366/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



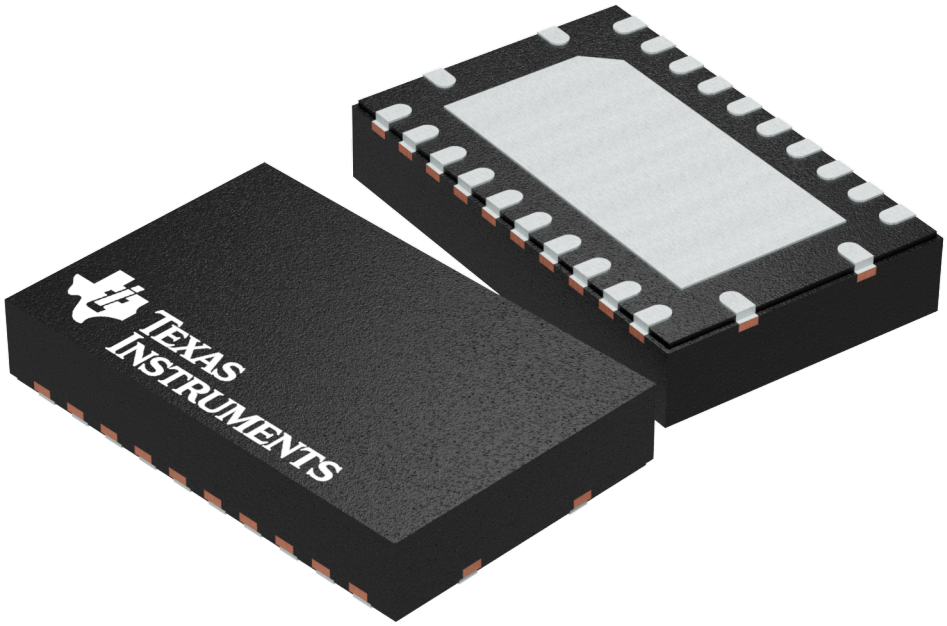
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

RGY 24

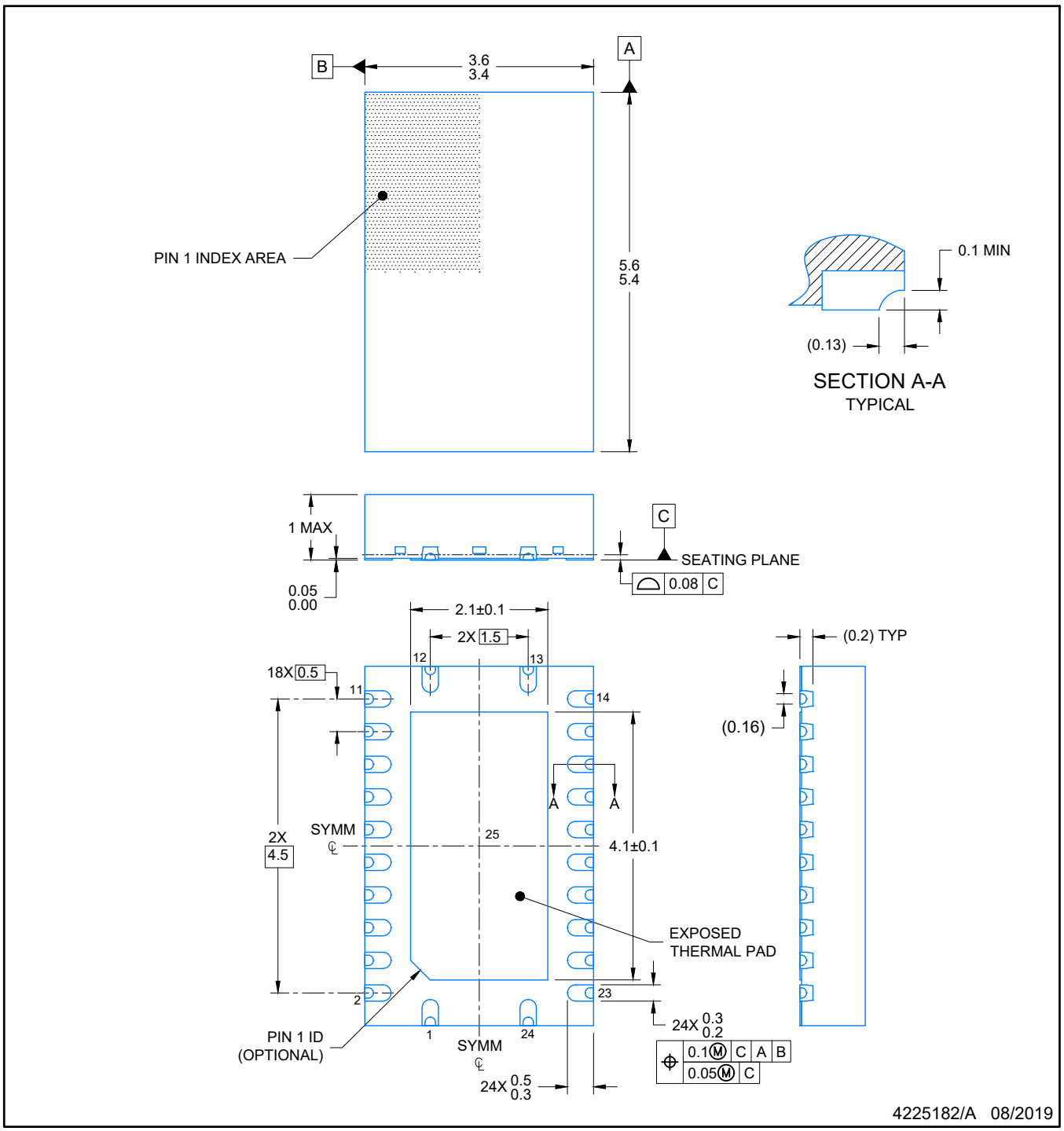
VQFN - 1 mm max height

5.5 x 3.5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

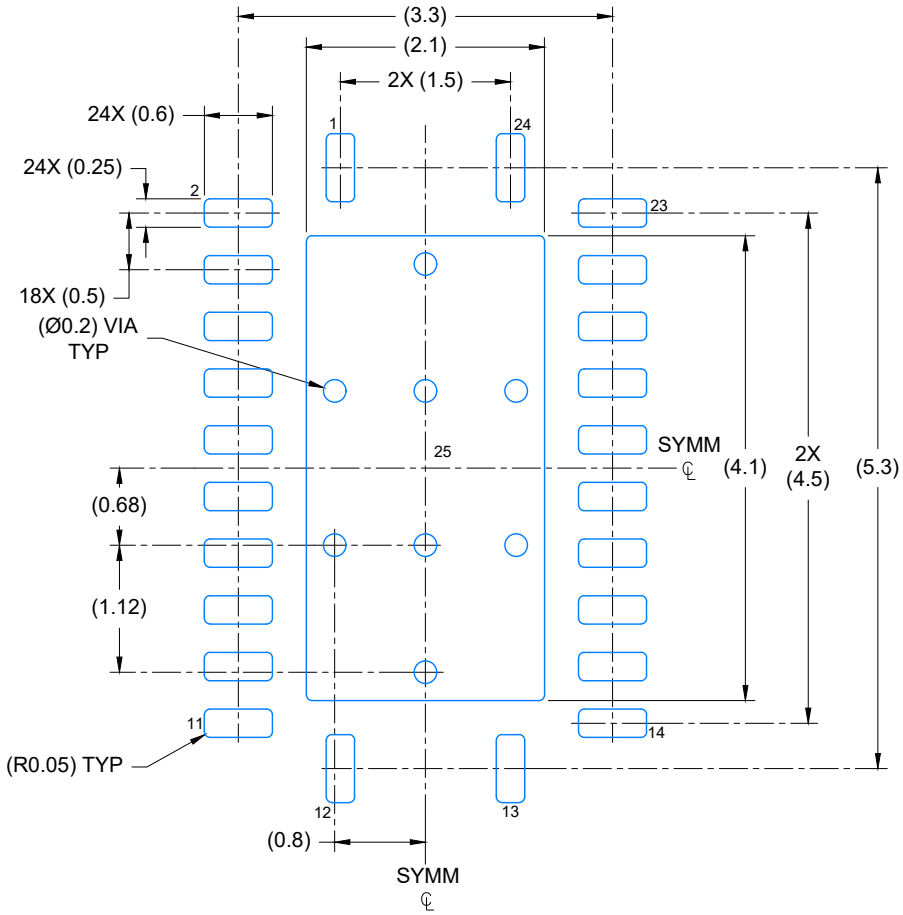


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

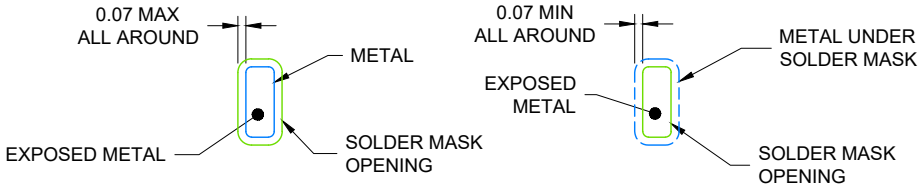


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

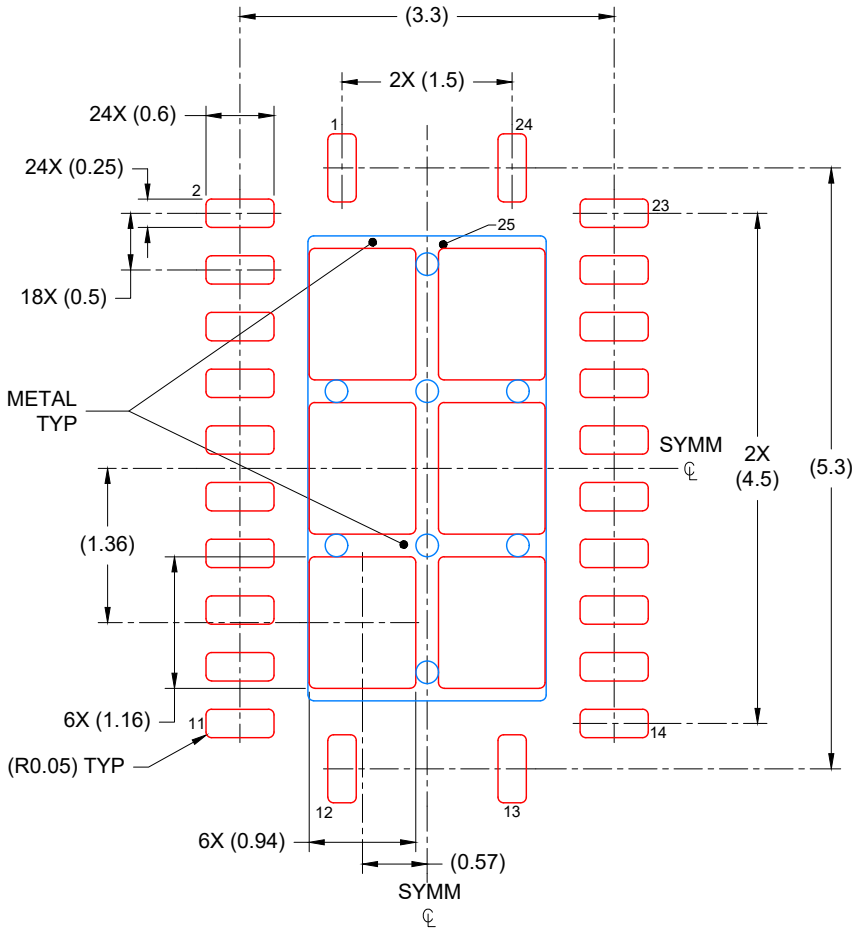
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4225182/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
76% PRINTED COVERAGE BY AREA
SCALE: 15X

4225182/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025