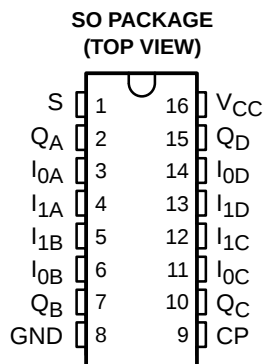


- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- 64-mA Output Sink Current
32-mA Output Source Current



description

The CY74FCT399T is a high-speed quad 2-input register that selects four bits of data from either of two sources (ports) under control of a common select (S) input. Selected data are transferred to a 4-bit output register synchronous with the low-to-high transition of the clock (CP) input. The 4-bit D-type output register is fully edge triggered. The data inputs (I_{0X} , I_{1X}) and S input must be stable only one setup time prior to, and hold time after, the low-to-high transition of CP for predictable operation. The CY74FCT399T has noninverted outputs.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION
S	Common select input
CP	Clock-pulse input (active rising edge)
I ₀	Data inputs from source 0
I ₁	Data inputs from source 1
Q	Register noninverted outputs

ORDERING INFORMATION

T _A	PACKAGE [†]		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – SO	Tube	6.1	CY74FCT399CTSOC	FCT399C
		Tape and reel	6.1	CY74FCT399CTSOCT	
	SOIC – SO	Tube	7	CY74FCT399ATSOC	FCT399A
		Tape and reel	7	CY74FCT399ATSOCT	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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CY74FCT399T
QUAD 2-INPUT REGISTER

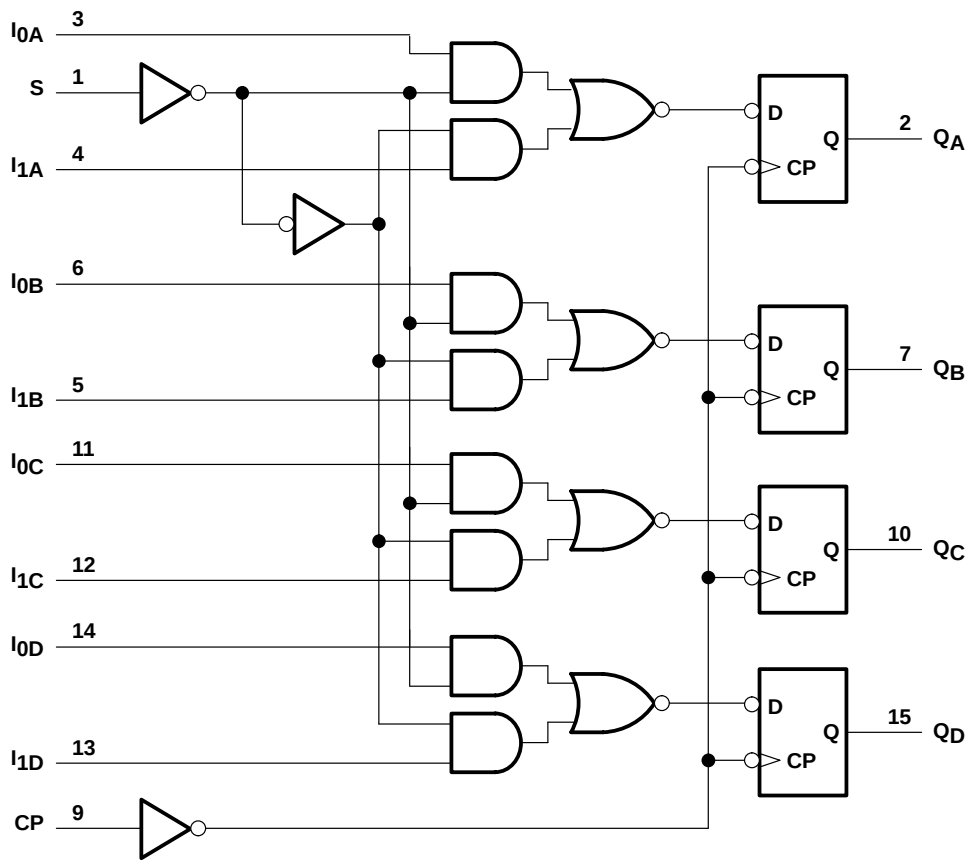
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FUNCTION TABLE

INPUTS			OUTPUT Q
S	I ₀	I ₁	
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

H = High logic level, h = High logic level
one setup time prior to the low-to-high
clock transition, L = Low logic level,
l = Low logic level one setup time prior
to the low-to-high clock transition,
X = Don't care

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1)	57°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			–32	mA
I_{OL} Low-level output current			64	mA
T_A Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

CY74FCT399T

QUAD 2-INPUT REGISTER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP [†]	MAX	UNIT
V _{IK}	V _{CC} = 4.75,	I _{IN} = −18 mA			−0.7	−1.2	V
V _{OH}	V _{CC} = 4.75	I _{OH} = −32 mA		2			V
		I _{OH} = −15 mA		2.4	3.3		
V _{OL}	V _{CC} = 4.75,	I _{OL} = 64 mA			0.3	0.55	V
V _H	All inputs				0.2		V
I _I	V _{CC} = 5.25 V,	V _{IN} = V _{CC}				5	μA
I _{IH}	V _{CC} = 5.25 V,	V _{IN} = 2.7 V				±1	μA
I _{IL}	V _{CC} = 5.25 V,	V _{IN} = 0.5 V				±1	μA
I _{OS} [‡]	V _{CC} = 5.25 V,	V _{OUT} = 0 V		−60	−120	−225	mA
I _{off}	V _{CC} = 0 V,	V _{OUT} = 4.5 V				±1	μA
I _{CC}	V _{CC} = 5.25 V,	V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} − 0.2 V			0.1	0.2	mA
ΔI _{CC}	V _{CC} = 5.25 V, V _{IN} = 3.4 V [§] , f ₁ = 0, Outputs open				0.5	2	mA
I _{CCD}	V _{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V				0.06	0.12	mA/MHz
I _C [#]	V _{CC} = 5.25 V, f ₀ = 10 MHz, Outputs open, S = Steady state	One input switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V		0.7	1.4	mA
			V _{IN} = 3.4 V or GND		1.2	3.4	
		Four inputs switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V		1.6	3.2	
			V _{IN} = 3.4 V or GND		2.9	8.2	
C _i					5	10	pF
C _o					9	12	pF

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

^{\S} Per TTL-driven input ($V_{IN} = 3.4 \text{ V}$); all other inputs at V_{CC} or GND

^{\parallel} This parameter is derived for use in total power-supply calculations.

^{\#} $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4 \text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

CY74FCT399T QUAD 2-INPUT REGISTER

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timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			CY74FCT399AT		CY74FCT399CT		UNIT
			MIN	MAX	MIN	MAX	
t _W	Pulse duration, CP high or low		5		5		ns
t _{SU}	Setup time, high or low	I _N before CP↑	3.5		3.5		ns
		S before CP↑	8.5		8.5		
t _H	Hold time, high or low	I _N after CP↑	1		1		ns
		S after CP↑	0		0		

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT399AT		CY74FCT399CT		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	CP	Q	2.5	7	2.5	6.1	ns
t_{PHL}			2.5	7	2.5	6.1	



CY74FCT399T

QUAD 2-INPUT REGISTER

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY74FCT399ATSOC	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT399A
CY74FCT399ATSOC.B	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT399A
CY74FCT399ATSOCT	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT399A
CY74FCT399ATSOCT.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT399A
CY74FCT399CTSOC	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT399C
CY74FCT399CTSOC.B	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT399C

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT399ATSOCT	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT399ATSOCT	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY74FCT399ATSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT399ATSOC.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT399CTSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT399CTSOC.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

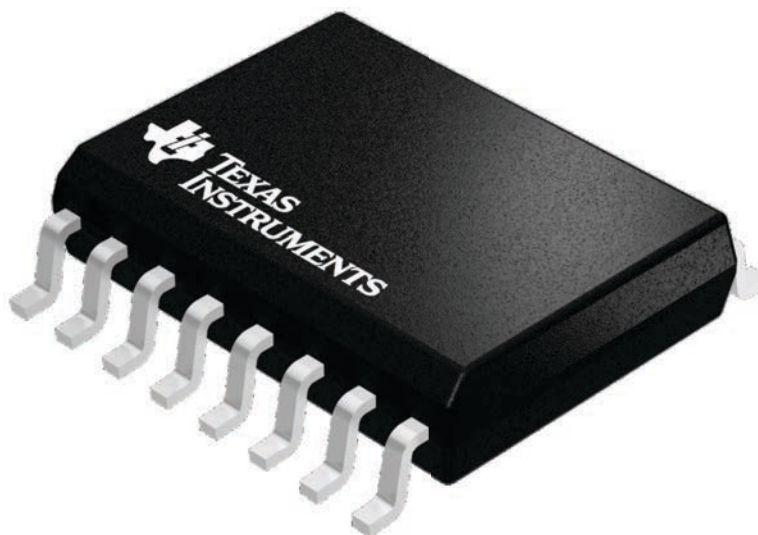
DW 16

SOIC - 2.65 mm max height

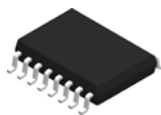
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

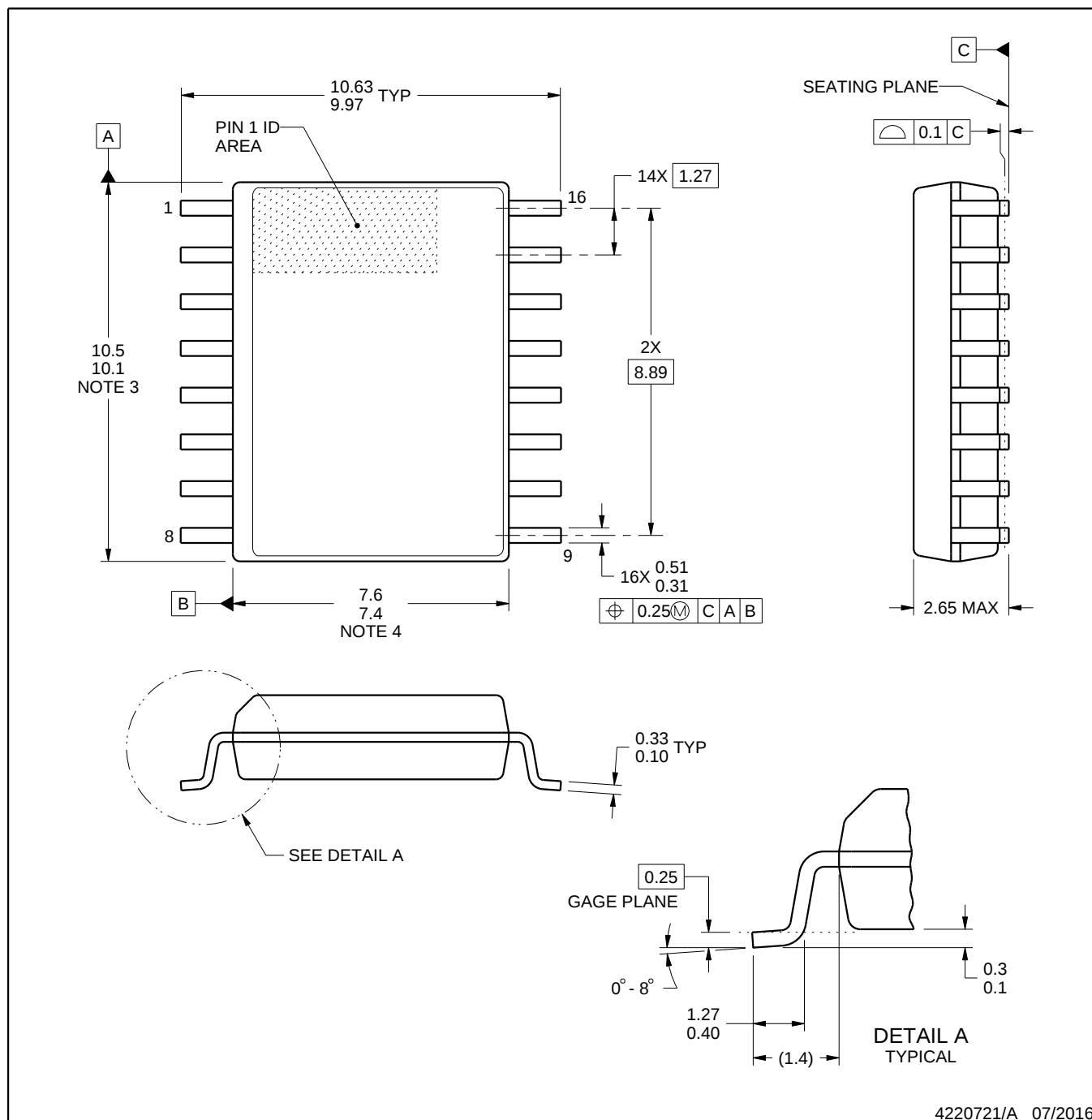


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

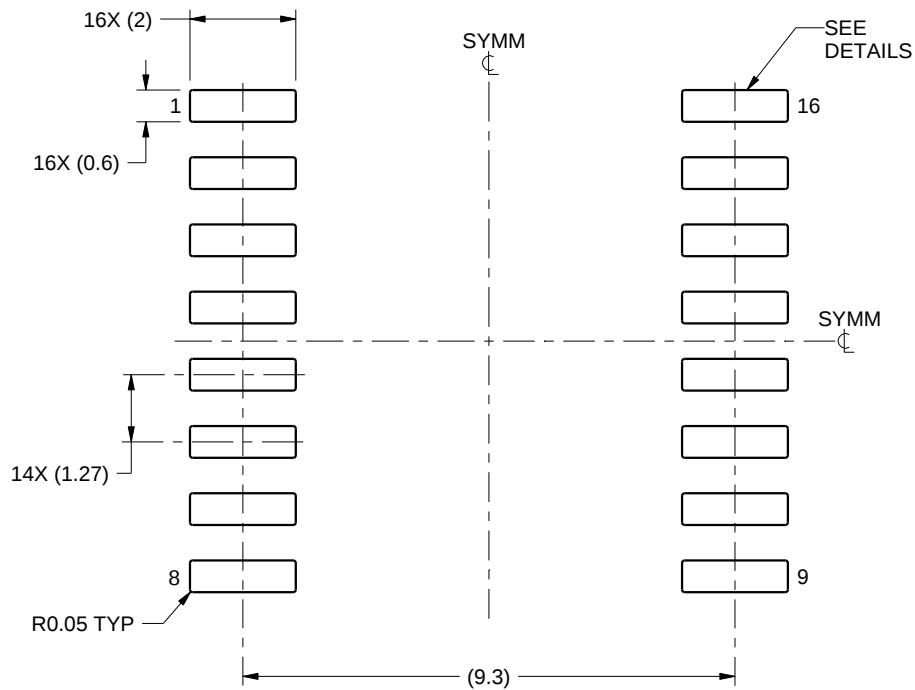
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

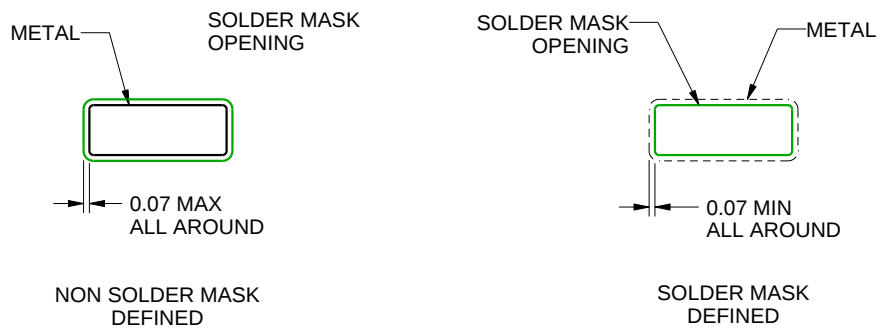
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

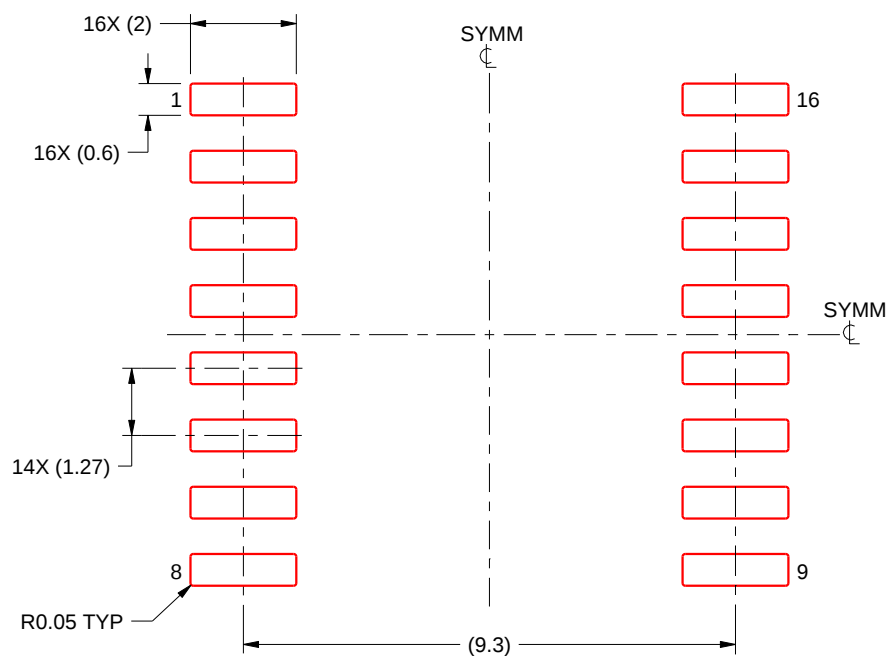
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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