10-BIT 165-MSPS DIGITAL-TO-ANALOG CONVERTER

Check for Samples: DAC900-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Single +5V OR +3V Operation**
- **High SFDR: 5MHz Output at 100MSPS: 68dBc**
- **Low Glitch: 3pV-s**
- **Low Power: 170mW at +5V**
- **Internal Reference: Optional External Reference Adjustable Full-Scale Range Multiplying Option**
- **Latch-Up Performance Meets 100 mA Per JESD 78, Class I**

APPLICATIONS

- **Communication Transmit Channels**
  - **WLL, Cellular Base Station**
  - **Digital Microwave Links**
  - **Cable Modems**
- **Waveform Generation**
  - **Direct Digital Synthesis (DDS)**
  - **Arbitrary Waveform Generation (ARB)**
- **Medical/Ultrasound**
- **High-Speed Instrumentation and Control**
- **Video, Digital TV**

DESCRIPTION

The DAC900 is a high-speed, Digital-to-Analog Converter (DAC) offering a 10-bit resolution option within the SpeedPlus family of high-performance converters. Featuring pin compatibility among family members, the DAC908, DAC902, and DAC904 provide a component selection option to an 8-, 12-, and 14-bit resolution, respectively. All models within this family of DACs support update rates in excess of 165MSPS with excellent dynamic performance, and are especially suited to fulfill the demands of a variety of applications.

The advanced segmentation architecture of the DAC900 is optimized to provide a high Spurious-Free Dynamic Range (SFDR) for single-tone, as well as for multi-tone signals—essential when used for the transmit signal path of communication systems.

The DAC900 has a high impedance (200kΩ) current output with a nominal range of 20mA and an output compliance of up to 1.25V. The differential outputs allow for both a differential or singleended analog signal interface. The close matching of the current outputs ensures superior dynamic performance in the differential configuration, which can be implemented with a transformer.

Utilizing a small geometry CMOS process, the monolithic DAC900 can be operated on a wide, single-supply range of +2.7V to +5.5V. Its low power consumption allows for use in portable and batteryoperated systems. Further optimization can be realized by lowering the output current with the adjustable full-scale option.

For noncontinuous operation of the DAC900, a power-down mode results in only 45mW of standby power.

The DAC900 comes with an integrated 1.24V bandgap reference and edge-triggered input latches, offering a complete converter solution. Both +3V and +5V CMOS logic families can be interfaced to the DAC900.

The reference structure of the DAC900 allows for additional flexibility by utilizing the on-chip reference, or applying an external reference. The full-scale output current can be adjusted over a span of 2mA to 20mA, with one external resistor, while maintaining the specified dynamic performance.

The DAC900 is available in a TSSOP-28 (PW) package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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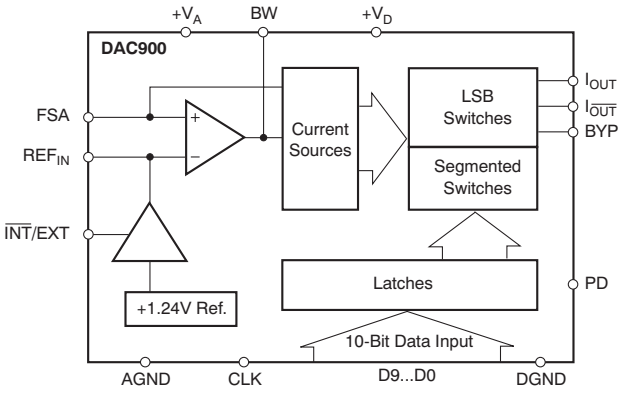
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	TSSOP – PW	Reel of 2500	DAC900TPWRQ1	DAC900T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

$+V_A$ to AGND	–0.3V to +6V
$+V_D$ to DGND	–0.3V to +6V
AGND to DGND	–0.3V to +0.3V
$+V_A$ to +VD	–6V to +6V
CLK, PD to DGND	–0.3V to V_D + 0.3V
D0-D9 to DGND	–0.3V to V_D + 0.3V
IOUT, IOUT to AGND	–1V to V_A + 0.3V
BW, BYP to AGND	–0.3V to V_A + 0.3V
REFIN, FSA to AGND	–0.3V to V_A + 0.3V
INT/EXT to AGND	–0.3V to V_A + 0.3V
Junction temperature	+150°C
Storage temperature	+150°C

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ELECTRICAL CHARACTERISTICS

At T_A = -40°C to +105°C, $+V_A$ = +5V, $+V_D$ = +5V, differential transformer coupled output, 50Ω doubly terminated, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION			10		bits
OUTPUT UPDATE RATE					
Output Update Rate (f_{CLOCK})	2.7V to 3.3V	125	165		MSPS
	4.5V to 5.5V	165	200		MSPS
STATIC ACCURACY(1)	T_A = +25°C				
Differential Nonlinearity (DNL)	f_{CLOCK} = 25MSPS, f_{OUT} = 1.0MHz	-0.75	±0.3	+0.75	LSB
Integral Nonlinearity (INL)	T_A = +25°C	-1	±0.5	+1	LSB
	T_A = -40°C to +105°C	-1.5		+1.5	
DYNAMIC PERFORMANCE	T_A = +25°C				
Spurious-Free Dynamic Range (SFDR)	To Nyquist				
f_{OUT} = 1.0MHz, f_{CLOCK} = 25MSPS	T_A = +25°C	70	76		dBc
	T_A = -40°C to +105°C	60	76		
f_{OUT} = 2.1MHz, f_{CLOCK} = 50MSPS			75		dBc
f_{OUT} = 5.04MHz, f_{CLOCK} = 50MSPS			68		dBc
f_{OUT} = 5.04MHz, f_{CLOCK} = 100MSPS			68		dBc
f_{OUT} = 20.2MHz, f_{CLOCK} = 100MSPS			62		dBc
f_{OUT} = 25.3MHz, f_{CLOCK} = 125MSPS			62		dBc
f_{OUT} = 41.5MHz, f_{CLOCK} = 125MSPS			53		dBc
f_{OUT} = 27.4MHz, f_{CLOCK} = 165MSPS			59		dBc
f_{OUT} = 54.8MHz, f_{CLOCK} = 165MSPS			53		dBc
Spurious-Free Dynamic Range within a Window					
f_{OUT} = 5.04MHz, f_{CLOCK} = 50MSPS	2MHz Span		78		dBc
f_{OUT} = 5.04MHz, f_{CLOCK} = 100MSPS	4MHz Span		78		dBc
Total Harmonic Distortion (THD)					
f_{OUT} = 2.1MHz, f_{CLOCK} = 50MSPS			-74		dBc
f_{OUT} = 2.1MHz, f_{CLOCK} = 125MSPS			-73		dBc
Two Tone					
f_{OUT1} = 13.5MHz, f_{OUT2} = 14.5MHz, f_{CLOCK} = 100MSPS			60		dBc
Output Settling Time(2)	to 0.1%		30		ns
Output Rise Time(2)	10% to 90%		2		ns
Output Fall Time(2)	90% to 10%		2		ns
Glitch Impulse			3		pV-s
DC-ACCURACY					
Full-Scale Output Range(3) (FSR)	All Bits High, I_{OUT}	2		20	mA
Output Compliance Range		-1		+1.25	V
Gain Error With Internal Reference	T_A = +25°C	-10	±1	+10	%FSR
	T_A = -40°C to +105°C	-25		+25	
Gain Error With External Reference		-10	±2	+10	%FSR
Gain Drift With Internal Reference			±120		ppmFSR/°C
Offset Error With Internal Reference	T_A = +25°C	-0.06		+0.06	%FSR
	T_A = -40°C to +105°C	-0.1		+0.1	

(1) At output I_{OUT}, while driving a virtual ground.
(2) Measured single-ended into 50Ω Load.
(3) Nominal full-scale output current is 32x I_{REF}; see Application Section for details.

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ELECTRICAL CHARACTERISTICS (continued)

At T_A = -40°C to +105°C, $+V_A$ = +5V, $+V_D$ = +5V, differential transformer coupled output, 50Ω doubly terminated, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset Drift With Internal Reference			±0.1		ppmFSR/°C
Power-Supply Rejection, $+V_A$	T_A = +25°C	-0.2		+0.2	%FSR/V
	T_A = -40°C to +105°C	-1.4		+1.4	
Power-Supply Rejection, $+V_D$	T_A = +25°C	-0.025		+0.025	%FSR/V
	T_A = -40°C to +105°C	-0.4		+0.4	
Output Noise	I_{OUT} = 20mA, R_{LOAD} = 50Ω		50		pA/√Hz
Output Resistance			200		kΩ
Output Capacitance	I_{OUT}, $I_{\overline{OUT}}$ to Ground		12		pF
REFERENCE					
Reference Voltage			+1.24		V
Reference Tolerance			±10		%
Reference Voltage Drift			±50		ppmFSR/°C
Reference Output Current			10		µA
Reference Input Resistance			1		mΩ
Reference Input Compliance Range		0.1		1.25	V
Reference Small-Signal Bandwidth(4)			1.3		MHz
DIGITAL INPUTS					
Logic Coding			Straight Binary		
Latch Command			Rising Edge of Clock		
Logic High Voltage, V_{IH}	$+V_D$ = +5V	3.5	5		V
Logic Low Voltage, V_{IL}	$+V_D$ = +5V		0	1.2	V
Logic High Voltage, V_{IH}	+v = +3V	2	3		V
Logic Low Voltage, V_{IL}	$+V_D$ = +3V		0	0.8	V
Logic High Current, I_{IH}(5)	$+V_D$ = +5V		±20		V
Logic Low Current, I_{IL}	$+V_D$ = +5V		±20		µA
Input Capacitance			5		pF
POWER SUPPLY					
Supply Voltages					
$+V_A$		+2.7	+5	+5.5	V
$+V_D$		+2.7	+5	+5.5	V
Supply Current(6)					
I_{VA}			24	30	mA
I_{VA}, Power-Down Mode			1.1	2	mA
I_{VD}			8	15	mA
Power Dissipation	+5V, I_{OUT} = 20mA		170	230	mW
	+3V, I_{OUT} = 2mA		50		mW
	Power-Down Mode		45		mW
Thermal Resistance, θ_{JA}					
TSSOP-28			50		°C/W

(4) Reference bandwidth depends on size of external capacitor at the BW pin and signal level.
(5) Typically 45µA for the PD pin, which has an internal pulldown resistor.
(6) Measured at f_{CLOCK} = 50MSPS and f_{OUT} = 1.0MHz.

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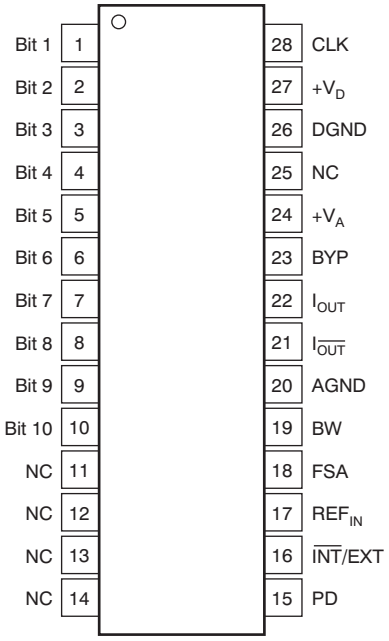
PW PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1	Bit 1	Data Bit 1 (D9), MSB
2	Bit 2	Data Bit 2 (D8)
3	Bit 3	Data Bit 3 (D7)
4	Bit 4	Data Bit 4 (D6)
5	Bit 5	Data Bit 5 (D5)
6	Bit 6	Data Bit 6 (D4)
7	Bit 7	Data Bit 7 (D3)
8	Bit 8	Data Bit 8 (D2)
9	Bit 9	Data Bit 9 (D1)
10	Bit 10	Data Bit 10 (D0), LSB
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	NC	No Connection
15	PD	Power Down, Control Input; Active HIGH. Contains internal pull-down circuit; may be left unconnected if not used.
16	$\overline{INT}$/EXT	Reference Select Pin; Internal (= 0) or External (= 1) Reference Operation.
17	REF_{IN}	Reference Input/Ouput. See Applications section for further details.
18	FSA	Full-Scale Output Adjust
19	BW	Bandwidth/Noise Reduction: Bypass with 0.1μF to $+V_A$ for Optimum Performance.
20	AGND	Analog Ground
21	$I_{\overline{OUT}}$	Complementary DAC Current Output
22	I_{OUT}	DAC Current Output
23	BYP	Bypass Node: Use 0.1μF to AGND
24	$+V_A$	Analog Supply Voltage, 2.7V to 5.5V
25	NC	No Connection
26	DGND	Digital Ground
27	$+V_D$	Digital Supply Voltage, 2.7V to 5.5V
28	CLK	Clock Input

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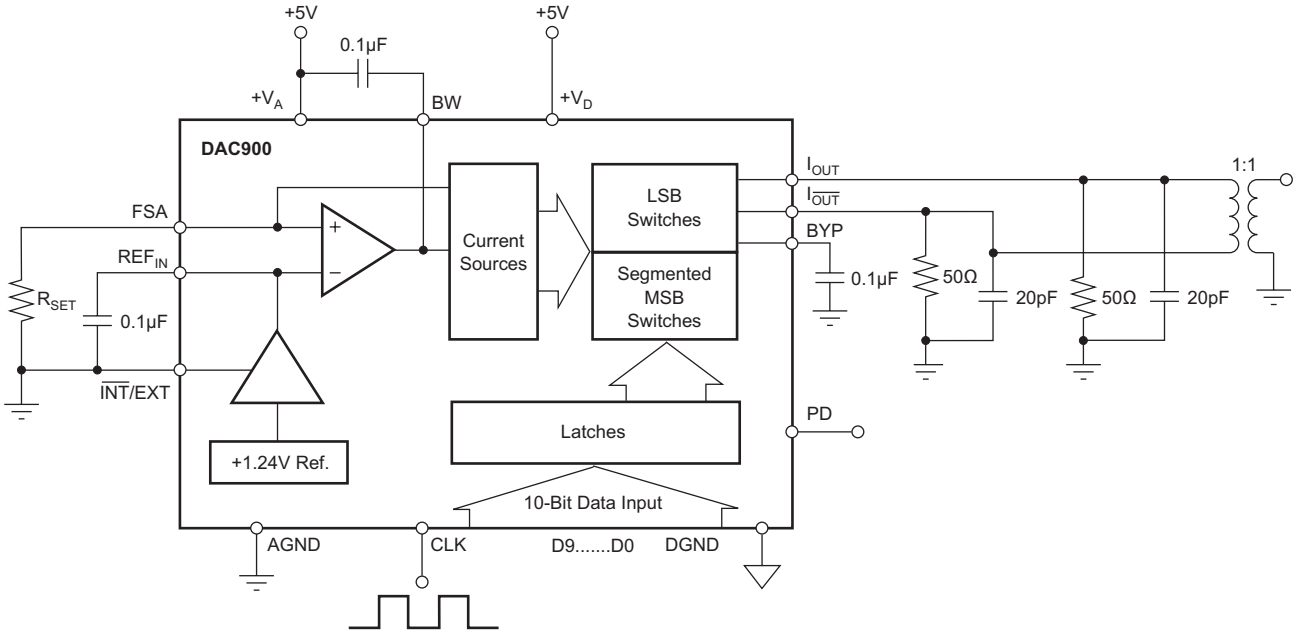
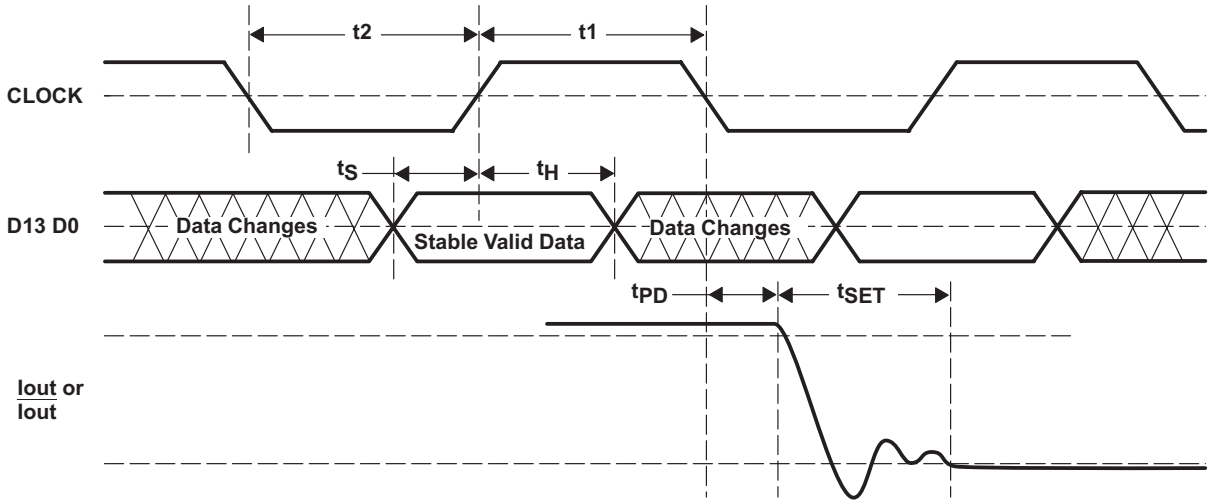
Typical Connection Circuit



Timing Diagram

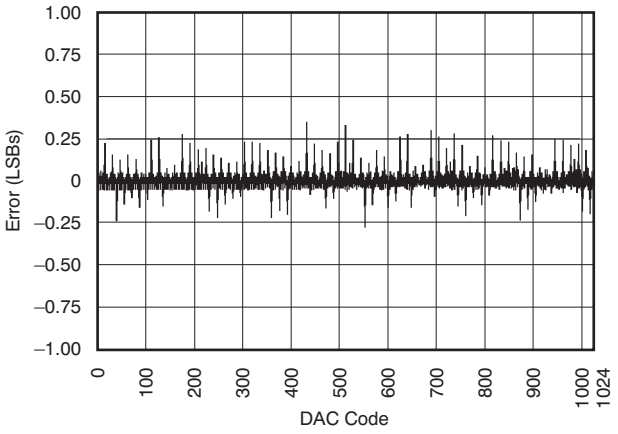


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Clock Pulse HIGH Time		3		ns
t_2	Clock Pulse LOW Time		3		ns
t_S	Data Setup Time		1.5		ns
t_H	Data Hold Time		1		ns
t_{PD}	Propagation Delay Time		1		ns
t_{SET}	Output Settling Time to 0.1%		30		ns

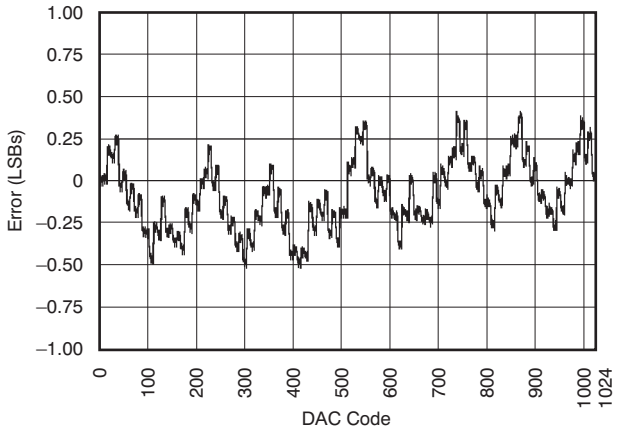
TYPICAL CHARACTERISTICS: $V_D = V_A = +5V$

At T_A = +25°C, Differential I_{OUT} = 20mA, 50Ω double-terminated load, SFDR up to Nyquist, unless otherwise specified

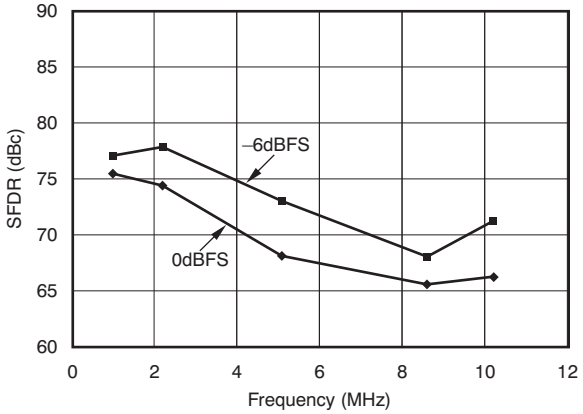
TYPICAL DNL



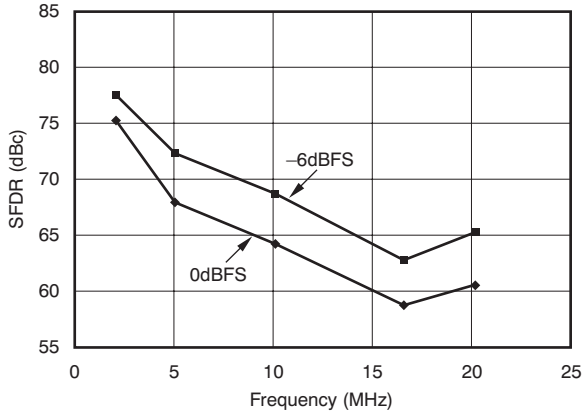
TYPICAL INL



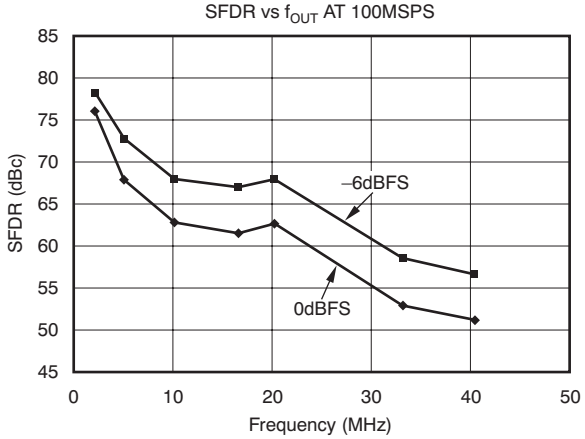
SFDR vs f_{OUT} AT 25MSPS



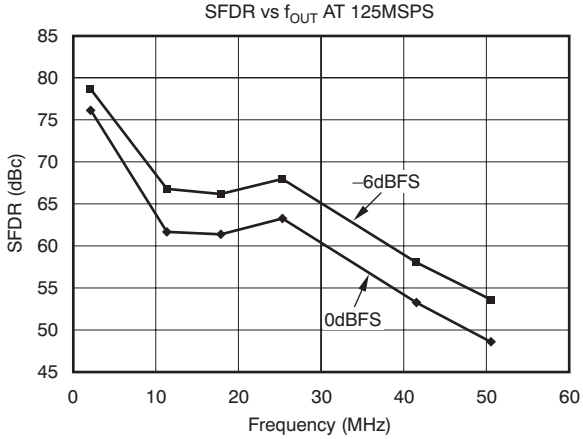
SFDR vs f_{OUT} AT 50MSPS



SFDR vs f_{OUT} AT 100MSPS



SFDR vs f_{OUT} AT 125MSPS



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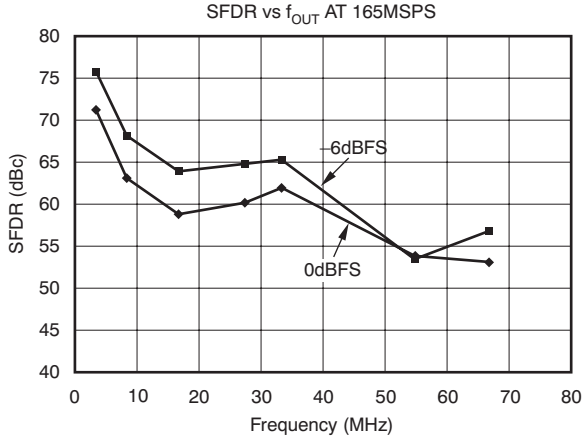
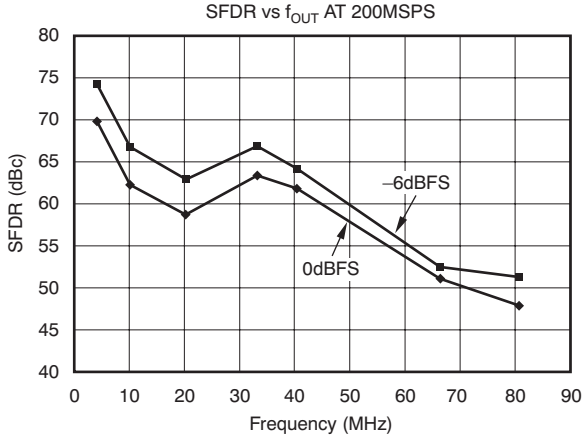
TYPICAL CHARACTERISTICS: $V_D = V_A = +5V$ (continued)

At T_A = +25°C, Differential I_{OUT} = 20mA, 50Ω double-terminated load, SFDR up to Nyquist, unless otherwise specified

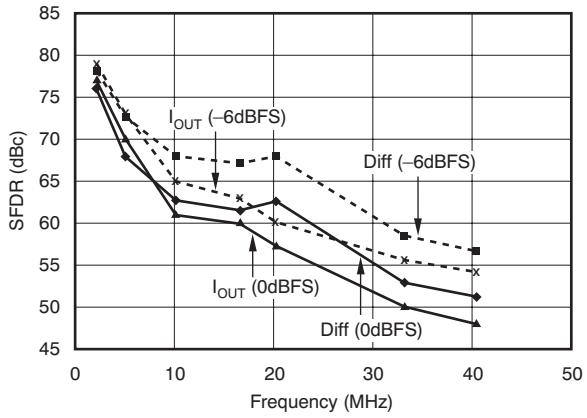
SFDR vs f_{OUT} AT 165MSPS



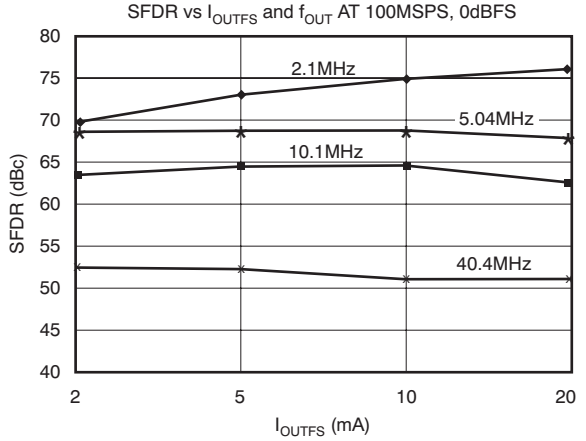
SFDR vs f_{OUT} AT 200MSPS



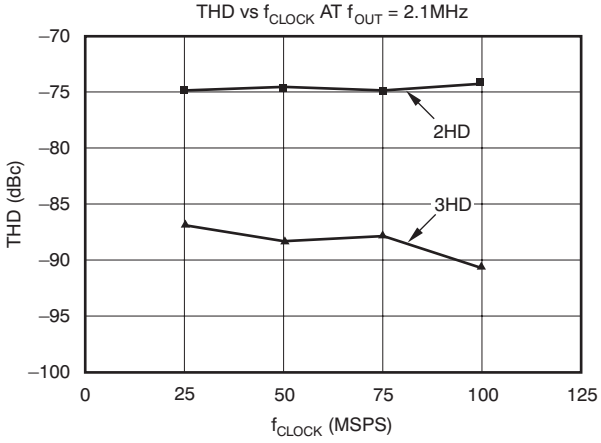
DIFFERENTIAL vs SINGLE-ENDED SFDR vs f_{OUT} AT 100MSPS



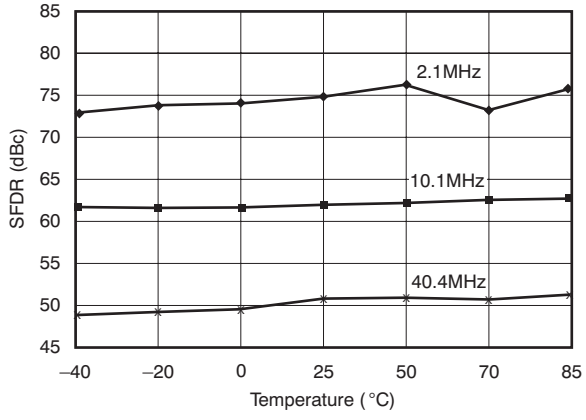
SFDR vs I_{OUTFS} and f_{OUT} AT 100MSPS, 0dBFS



THD vs f_{CLOCK} AT f_{OUT} = 2.1MHz



SFDR vs TEMPERATURE AT 100MSPS, 0dBFS



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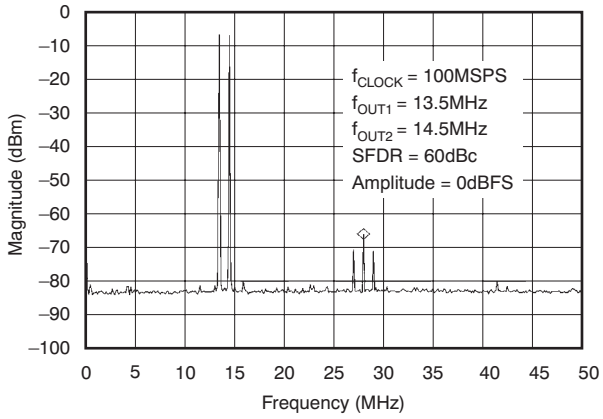
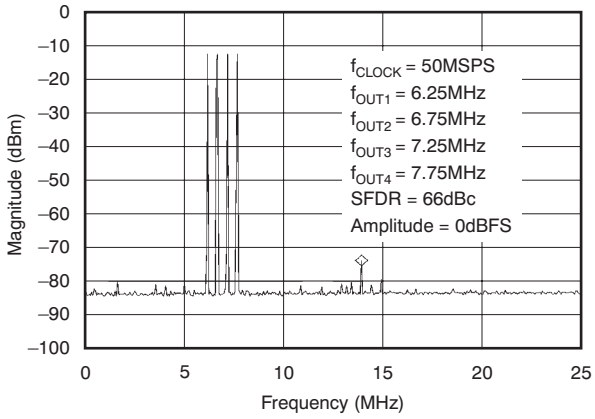
TYPICAL CHARACTERISTICS: $V_D = V_A = +5V$ (continued)

At T_A = +25°C, Differential I_{OUT} = 20mA, 50Ω double-terminated load, SFDR up to Nyquist, unless otherwise specified

DUAL-TONE OUTPUT SPECTRUM



FOUR-TONE OUTPUT SPECTRUM



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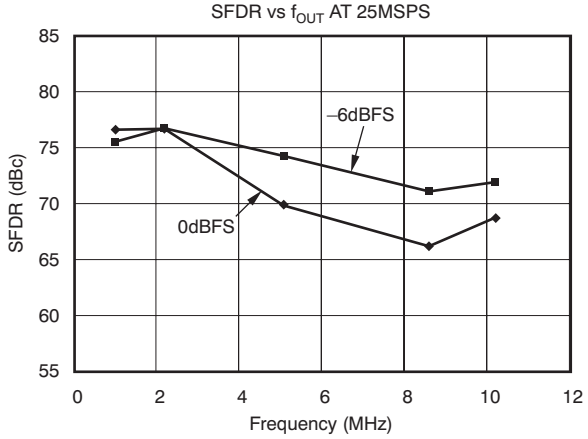
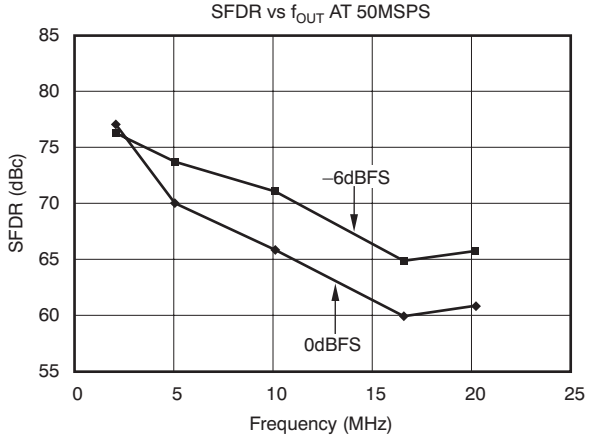
TYPICAL CHARACTERISTICS: $V_D = V_A = +3V$

At T_A = +25°C, Differential I_{OUT} = 20mA, 50Ω double-terminated load, SFDR up to Nyquist, unless otherwise specified

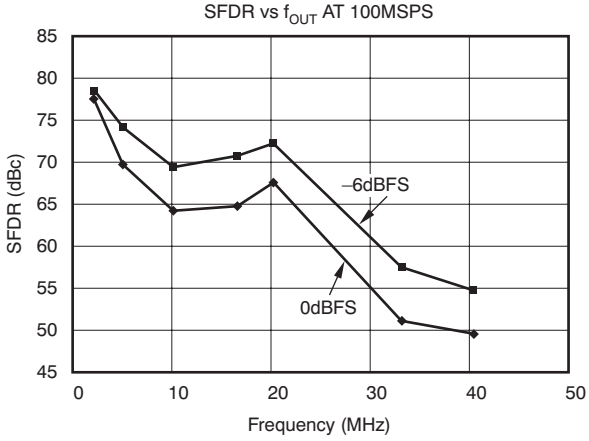
SFDR vs f_{OUT} AT 25MSPS



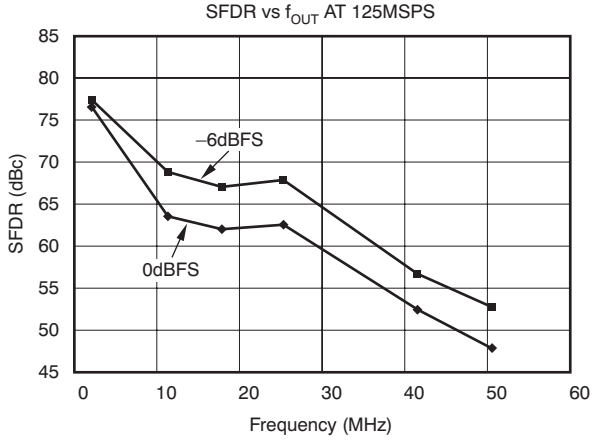
SFDR vs f_{OUT} AT 50MSPS



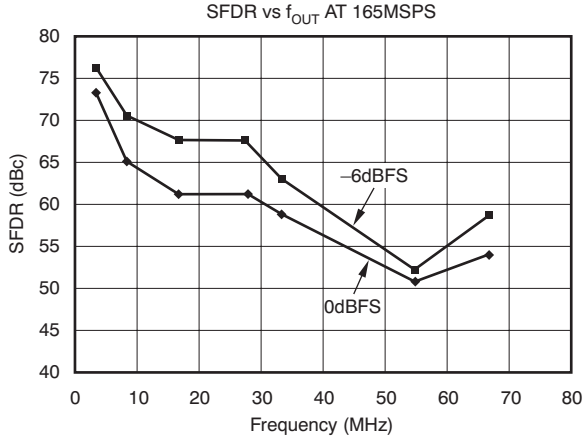
SFDR vs f_{OUT} AT 100MSPS



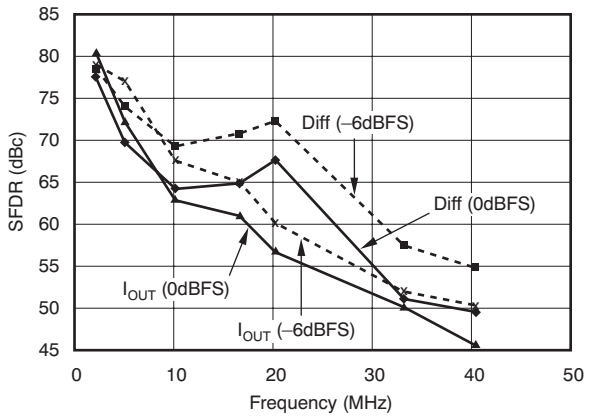
SFDR vs f_{OUT} AT 125MSPS



SFDR vs f_{OUT} AT 165MSPS



DIFFERENTIAL vs SINGLE-ENDED SFDR vs f_{OUT} AT 100MSPS



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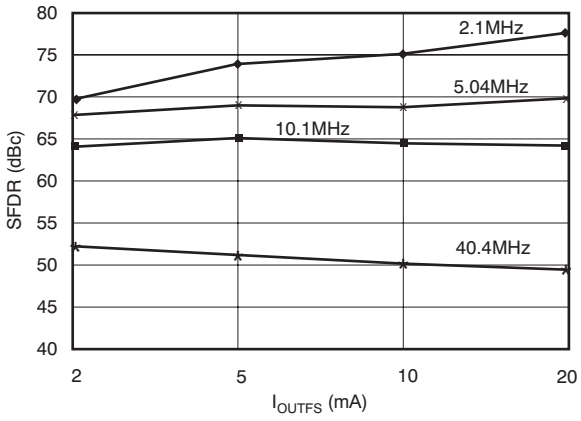
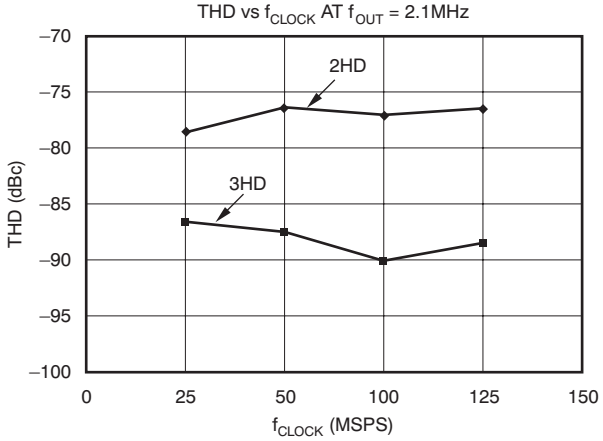
TYPICAL CHARACTERISTICS: $V_D = V_A = +3V$ (continued)

At T_A = +25°C, Differential I_{OUT} = 20mA, 50Ω double-terminated load, SFDR up to Nyquist, unless otherwise specified

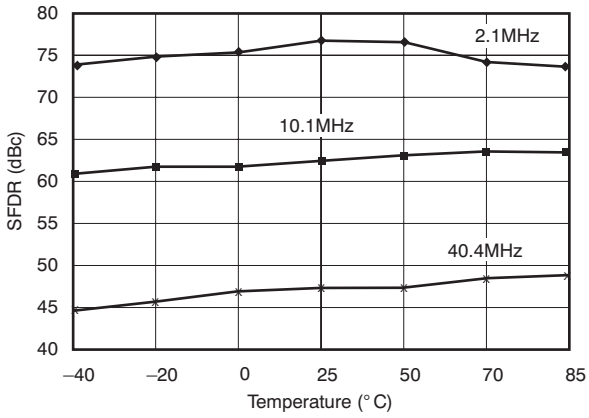
SFDR vs I_{OUTFS} and f_{OUT} AT 100MSPS



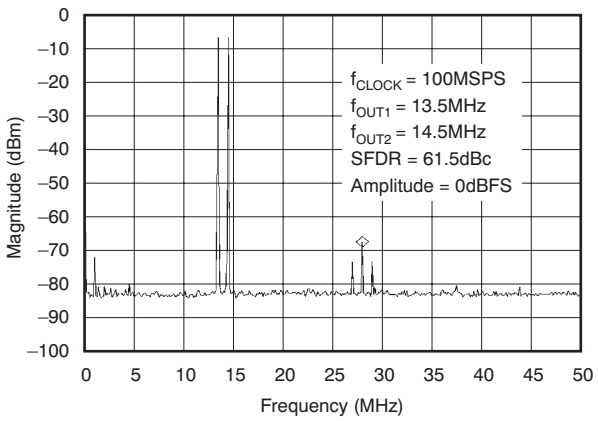
THD vs f_{CLOCK} AT f_{OUT} = 2.1MHz



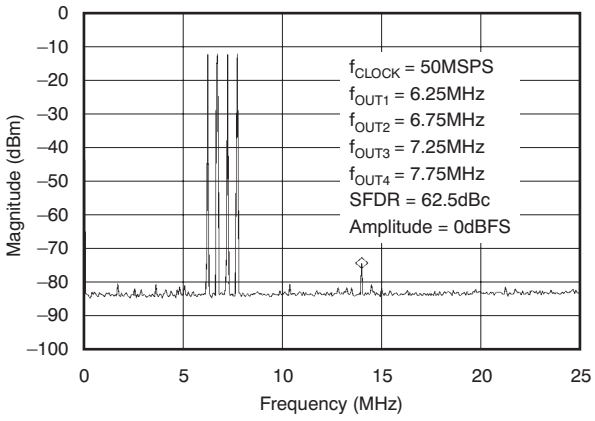
SFDR vs TEMPERATURE AT 100MSPS, 0dBFS



DUAL-TONE OUTPUT SPECTRUM



FOUR-TONE OUTPUT SPECTRUM



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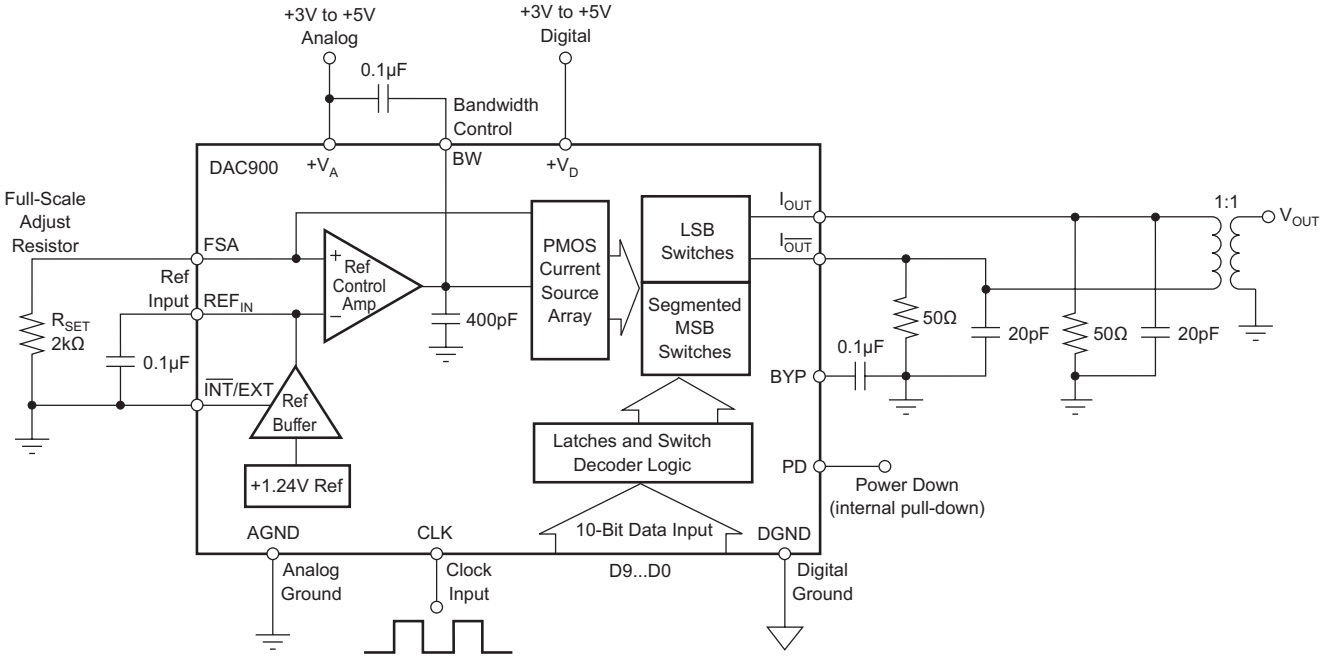
APPLICATION INFORMATION

Theory of Operation

The architecture of the DAC900 uses the current steering technique to enable fast switching and a high update rate. The core element within the monolithic DAC is an array of segmented current sources, which are designed to deliver a full-scale output current of up to 20mA, as shown in Figure 1. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node, I_{OUT} or $I_{\overline{OUT}}$. The complementary outputs deliver a differential output signal that improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, compared to singleended operation.



NOTE: Supply bypassing not shown.

Figure 1. Functional Block Diagram

The segmented architecture results in a significant reduction of the glitch energy, and improves the dynamic performance (SFDR) and DNL. The current outputs maintain a very high output impedance of greater than 200kΩ.

The full-scale output current is determined by the ratio of the internal reference voltage (1.24V) and an external resistor, R_{SET}. The resulting I_{REF} is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2mA to 20mA, depending on the value of R_{SET}.

The DAC900 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises the current source array with its associated switches and the reference circuitry.

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DAC Transfer Function

The total output current, I_{OUTFS}, of the DAC900 is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT} + I_{\overline{OUT}} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT} = I_{OUTFS} \times \frac{Code}{1024} \quad (2)$$

$$I_{\overline{OUT}} = I_{OUTFS} \times \left(1023 - \frac{Code}{1024}\right) \quad (3)$$

Where,

Code is the decimal representation of the DAC data input word.

Additionally, I_{OUTFS} is a function of the reference current I_{REF}, which is determined by the reference voltage and the external setting resistor, R_{SET}.

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (4)$$

In most cases the complementary outputs will drive resistive loads or a terminated transformer. A signal voltage will develop at each output according to:

$$V_{OUT} = I_{OUT} \times R_{LOAD} \quad (5)$$

$$V_{\overline{OUT}} = I_{\overline{OUT}} \times R_{LOAD} \quad (6)$$

The value of the load resistance is limited by the output compliance specification of the DAC900. To maintain specified linearity performance, the voltage for I_{OUT} and $I_{\overline{OUT}}$ should not exceed the maximum allowable compliance range. The two single-ended output voltages can be combined to find the total differential output swing:

$$V_{OUTDIFF} = V_{OUT} - V_{\overline{OUT}} = \frac{2 \times Code - 1023}{1024} \times I_{OUTFS} \times R_{LOAD} \quad (7)$$

Analog Outputs

The DAC900 provides two complementary current outputs, I_{OUT} and $I_{\overline{OUT}}$. The simplified circuit of the analog output stage representing the differential topology is shown in Figure 2. The output impedance of 200kΩ || 12pF for I_{OUT} and $I_{\overline{OUT}}$ results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

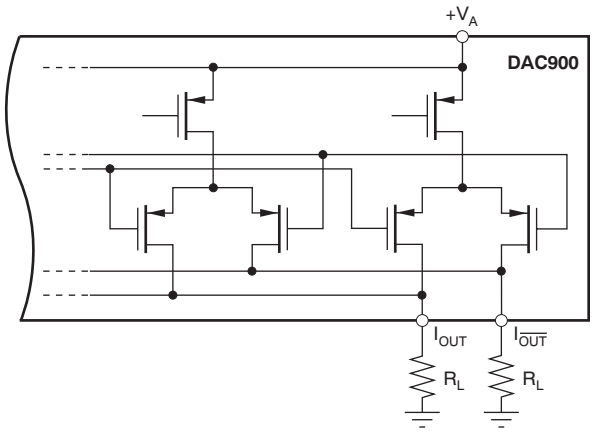

Figure 2. Equivalent Analog Output

The signal voltage swing that may develop at the two outputs, I_{OUT} and $I_{\overline{OUT}}$, is limited by a negative and positive compliance. The negative limit of –1V is given by the breakdown voltage of the CMOS process, and exceeding it

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will compromise the reliability of the DAC900, or even cause permanent damage. With the full-scale output set to 20mA, the positive compliance equals 1.25V, operating with $+V_D$ = 5V. Note that the compliance range decreases to about 1V for a selected output current of I_{OUTFS} = 2mA. Care should be taken that the configuration of DAC900 does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately 0.5V. This is the case for a 50Ω doubly-terminated load and a 20mA full-scale output current. A variety of loads can be adapted to the output of the DAC900 by selecting a suitable transformer while maintaining optimum voltage levels at I_{OUT} and $I_{\overline{OUT}}$. Furthermore, using the differential output configuration in combination with a transformer will be instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies and/or output amplitudes below full-scale.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20mA. A lower full-scale range down to 2mA may be considered for applications that require a low power consumption, but can tolerate a reduced performance level.

Table 1. Input Coding vs Analog Output Current

INPUT CODE (D9 - D0)	I_{OUT}	$I_{\overline{OUT}}$
11 1111 1111	20mA	0mA
10 0000 0000	10mA	10mA
00 0000 0000	0mA	20mA

Output Configurations

The current output of the DAC900 allows for a variety of configurations, some of which are illustrated in the following sections. As mentioned previously, utilizing the converter's differential outputs will yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer (see Figure 3) or a differential amplifier configuration (see Figure 4). The transformer configuration is ideal for most applications with ac coupling, while op amps will be suitable for a DC-coupled configuration.

The single-ended configuration (see Figure 6) may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground will convert the output current into a ground-referenced voltage signal. To improve on the DC linearity, an I-to-V converter can be used instead. This will result in a negative signal excursion and, therefore, requires a dual supply amplifier.

Differential With Transformer

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance (see Figure 3). The appropriate transformer should be carefully selected based on the output frequency spectrum and impedance requirements. The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio), the transformer can be used to provide optimum impedance matching while controlling the compliance voltage for the converter outputs. The model shown in Figure 3 has a 1:1 ratio and may be used to interface the DAC900 to a 50Ω load. This results in a 25Ω load for each of the outputs, I_{OUT} and $I_{\overline{OUT}}$. The output signals are ac coupled and inherently isolated because of the transformer's magnetic coupling.

As shown in Figure 3, the transformer's center tap is connected to ground. This forces the voltage swing on I_{OUT} and $I_{\overline{OUT}}$ to be centered at 0V. In this case the two resistors, R_S, may be replaced with one, R_{DIFF}, or omitted altogether. This approach should only be used if all components are close to each other, and if the V_{SWR} is not important. A complete power transfer from the DAC output to the load can be realized, but the output compliance range should be observed. Alternatively, if the center tap is not connected, the signal swing will be centered at $R_S \times I_{OUTFS} / 2$. However, in this case, the two resistors (R_S) must be used to enable the necessary DC-current flow for both outputs.

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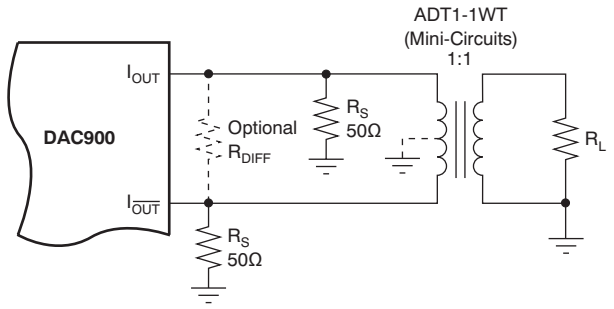

Figure 3. Differential Output Configuration Using an RF Transformer

Differential Configuration Using an Op Amp

If the application requires a DC-coupled output, a difference amplifier may be considered, as shown in Figure 4. Four external resistors are needed to configure the voltage-feedback op amp OPA680 as a difference amplifier performing the differential to single-ended conversion. Under the shown configuration, the DAC900 generates a differential output signal of 0.5Vp-p at the load resistors, R_L. The resistor values shown were selected to result in a symmetric 25Ω loading for each of the current outputs since the input impedance of the difference amplifier is in parallel to resistors R_L, and should be considered.

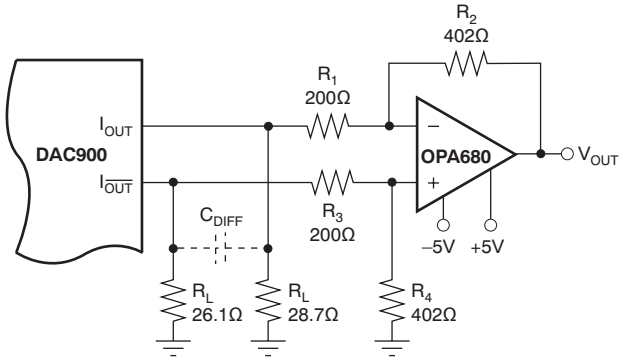

Figure 4. Difference Amplifier Provides Differential to Single-Ended Conversion and DC-Coupling

The OPA680 is configured for a gain of two. Therefore, operating the DAC900 with a 20mA full-scale output will produce a voltage output of ±1V. This requires the amplifier to operate off of a dual power supply (±5V). The tolerance of the resistors typically sets the limit for the achievable common-mode rejection. An improvement can be obtained by fine tuning resistor R_4.

This configuration typically delivers a lower level of ac performance than the previously discussed transformer solution because the amplifier introduces another source of distortion. Suitable amplifiers should be selected based on their slew-rate, harmonic distortion, and output swing capabilities. High-speed amplifiers like the OPA680 or OPA687 may be considered. The ac performance of this circuit may be improved by adding a small capacitor, C_{DIFF}, between the outputs I_{OUT} and $I_{\overline{OUT}}$, as shown in Figure 4. This will introduce a real pole to create a low-pass filter in order to slewlimit the DACs fast output signal steps that otherwise could drive the amplifier into slew-limitations or into an overload condition; both would cause excessive distortion. The difference amplifier can easily be modified to add a level shift for applications requiring the single-ended output voltage to be unipolar, i.e., swing between 0V and +2V.

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Dual Transimpedance Output Configuration

The circuit example of Figure 5 shows the signal output currents connected into the summing junction of the OPA2680, which is set up as a transimpedance stage, or I-to-V converter. With this circuit, the DAC's output will be kept at a virtual ground, minimizing the effects of output impedance variations, and resulting in the best DC linearity (INL). However, as mentioned previously, the amplifier may be driven into slew-rate limitations, and produce unwanted distortion. This may occur especially at high DAC update rates.

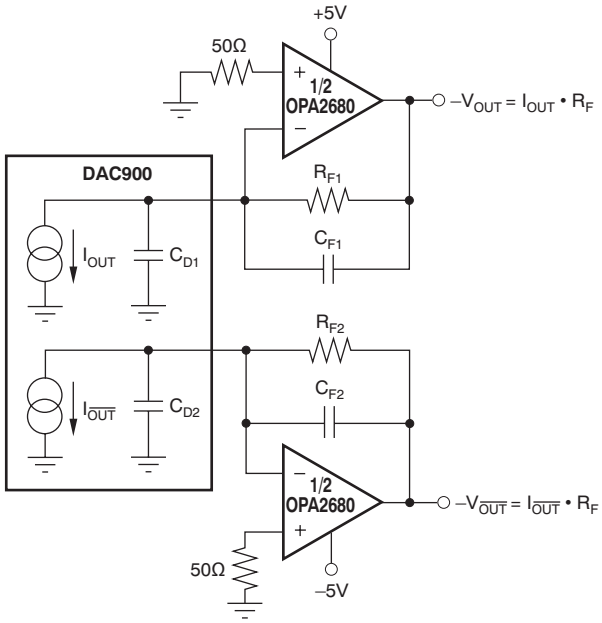

Figure 5. Dual Voltage-Feedback Amplifier OPA2680 Forms Differential Transimpedance Amplifier

The DC gain for this circuit is equal to feedback resistor RF. At high frequencies, the DAC output impedance (CD1, CD2) will produce a zero in the noise gain for the OPA2680 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise-gain peaking. To achieve a flat transimpedance frequency response, the pole in each feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \frac{\sqrt{GBP}}{4\pi R_F C_D} \quad (8)$$

Where,

GBP = Gain Bandwidth Product of OPA

This gives a corner frequency f_{-3dB} of approximately:

$$f_{-3dB} = \frac{\sqrt{GBP}}{2\pi R_F C_D} \quad (9)$$

The full-scale output voltage is defined by the product of $I_{OUTFS} \times R_F$, and has a negative unipolar excursion. To improve on the ac performance of this circuit, adjustment of R_F and/or I_{OUTFS} should be considered. Further extensions of this application example may include adding a differential filter at the OPA2680's output followed by a transformer, in order to convert to a single-ended signal.

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Single-Ended Configuration

Using a single load resistor connected to the one of the DAC outputs, a simple current-to-voltage conversion can be accomplished. The circuit in Figure 6 shows a 50Ω resistor connected to IOUT, providing the termination of the further connected 50Ω cable. Therefore, with a nominal output current of 20mA, the DAC produces a total signal swing of 0V to 0.5V into the 25Ω load.

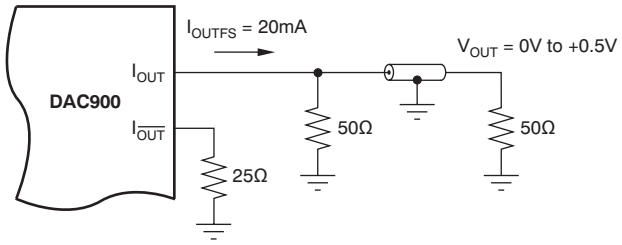

Figure 6. Driving a Doubly-Terminated 50Ω Cable Directly

Different load resistor values may be selected as long as the output compliance range is not exceeded. Additionally, the output current, IOUTFS, and the load resistor may be mutually adjusted to provide the desired output signal swing and performance.

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Internal Reference Operation

The DAC900 has an on-chip reference circuit that comprises a 1.24V bandgap reference and a control amplifier. Grounding pin 16, $\overline{INT}$/EXT, enables the internal reference operation. The full-scale output current, I_{OUTFS}, of the DAC900 is determined by the reference voltage, V_{REF}, and the value of resistor R_{SET}. I_{OUTFS} can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (10)$$

As shown in Figure 7, the external resistor RSET connects to the FSA pin (Full-Scale Adjust). The reference control amplifier operates as a V-to-I converter producing a reference current, I_{REF}, which is determined by the ratio of V_{REF} and R_{SET}, as shown in Equation 10. The full-scale output current, I_{OUTFS}, results from multiplying I_{REF} by a fixed factor of 32.

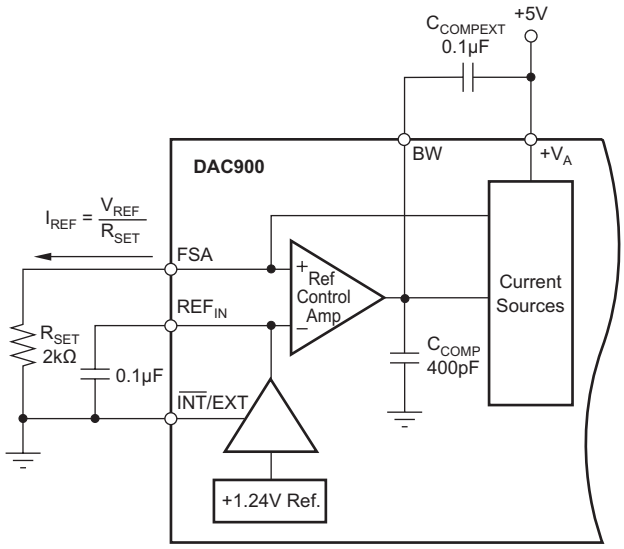

Figure 7. Internal Reference Configuration

Using the internal reference, a 2kΩ resistor value results in a 20mA full-scale output. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the converter output can be adjusted from 20mA down to 2mA. Operating the DAC900 at lower than 20mA output currents may be desirable for reasons of reducing the total power consumption, improving the distortion performance, or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the REF_{IN} pin with a ceramic chip capacitor of 0.1µF or more. The control amplifier is internally compensated, and its small signal bandwidth is approximately 1.3MHz. To improve the ac performance, an additional capacitor ($C_{COMPEXT}$) should be applied between the BW pin and the analog supply, $+V_A$, as shown in Figure 7. Using a 0.1µF capacitor, the small-signal bandwidth and output impedance of the control amplifier is further diminished, reducing the noise that is fed into the current source array. This also helps shunting feedthrough signals more effectively, and improving the noise performance of the DAC900.

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External Reference Operation

The internal reference can be disabled by applying a logic HIGH ($+V_A$) to pin $\overline{\text{INT}}$/EXT. An external reference voltage can then be driven into the REF_{IN} pin, which in this case functions as an input, as shown in Figure 8. The use of an external reference may be considered for applications that require higher accuracy and drift performance, or to add the ability of dynamic gain control.

While a 0.1µF capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, REF_{IN}, has a high input impedance (1MΩ) and can easily be driven by various sources. Note that the voltage range of the external reference should stay within the compliance range of the reference input (0.1V to 1.25V).

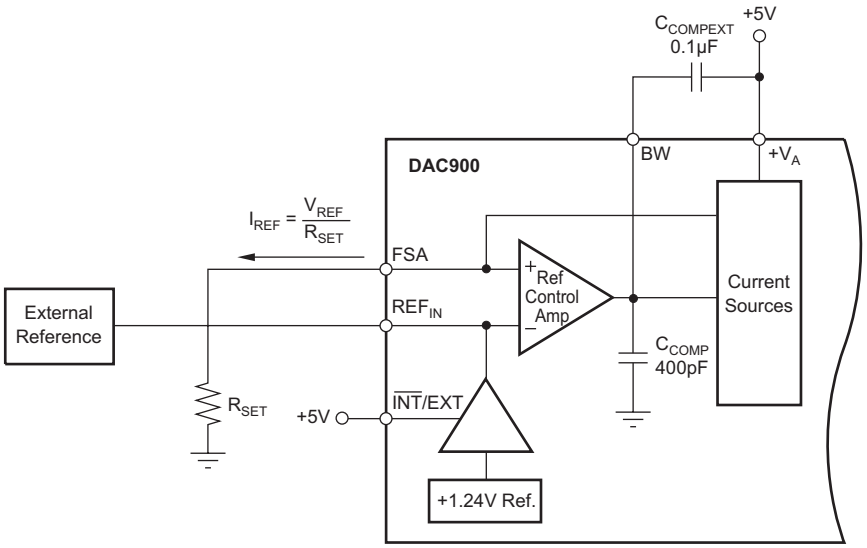

Figure 8. External Reference Configuration

Digital Inputs

The digital inputs, D0 (LSB) through D9 (MSB) of the DAC900 accepts standard-positive binary coding. The digital input word is latched into a master-slave latch with the rising edge of the clock. The DAC output becomes updated with the following falling clock edge (refer to the specification table and timing diagram for details). The best performance will be achieved with a 50% clock duty cycle, however, the duty cycle may vary as long as the timing specifications are met. Additionally, the setup and hold times may be chosen within their specified limits. All digital inputs are CMOS compatible. The logic thresholds depend on the applied digital supply voltage such that they are set to approximately half the supply voltage; $V_{th} = +V_D/2$ (±20% tolerance). The DAC900 is designed to operate over a supply range of 2.7V to 5.5V.

Power-Down Mode

The DAC900 features a power-down function that can be used to reduce the supply current to less than 9mA over the specified supply range of 2.7V to 5.5V. Applying a logic HIGH to the PD pin will initiate the power-down mode, while a logic LOW enables normal operation. When left unconnected, an internal active pull-down circuit will enable the normal operation of the converter.

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Grounding, Decoupling, and Layout Information

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high frequency designs. Multilayer pc-boards are recommended for best performance since they offer distinct advantages such as minimization of ground impedance, separation of signal layers by ground layers, etc.

The DAC900 uses separate pins for its analog and digital supply and ground connections. The placement of the decoupling capacitor should be such that the analog supply ($+V_A$) is bypassed to the analog ground (AGND), and the digital supply bypassed to the digital ground (DGND). In most cases 0.1uF ceramic chip capacitors at each supply pin are adequate to provide a low impedance decoupling path. Keep in mind that their effectiveness largely depends on the proximity to the individual supply and ground pins. Therefore, they should be located as close as physically possible to those device leads. Whenever possible, the capacitors should be located immediately under each pair of supply/ ground pins on the reverse side of the pc-board. This layout approach will minimize the parasitic inductance of component leads and pcb runs.

Further supply decoupling with surface mount tantalum capacitors (1µF to 4.7µF) may be added as needed in proximity of the converter.

Low noise is required for all supply and ground connections to the DAC900. It is recommended to use a multilayer pcboard utilizing separate power and ground planes. Mixed signal designs require particular attention to the routing of the different supply currents and signal traces. Generally, analog supply and ground planes should only extend into analog signal areas, such as the DAC output signal and the reference signal. Digital supply and ground planes must be confined to areas covering digital circuitry, including the digital input lines connecting to the converter, as well as the clock signal. The analog and digital ground planes should be joined together at one point underneath the DAC. This can be realized with a short track of approximately 1/8" (3mm).

The power to the DAC900 should be provided through the use of wide pcb runs or planes. Wide runs will present a lower trace impedance, further optimizing the supply decoupling. The analog and digital supplies for the converter should only be connected together at the supply connector of the pc-board. In the case of only one supply voltage being available to power the DAC, ferrite beads along with bypass capacitors may be used to create an LC filter. This will generate a low-noise analog supply voltage that can then be connected to the $+V_A$ supply pin of the DAC900.

While designing the layout, it is important to keep the analog signal traces separate from any digital line, in order to prevent noise coupling onto the analog signal path.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC900TPWRQ1	Active	Production	TSSOP (PW) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC900T
DAC900TPWRQ1.B	Active	Production	TSSOP (PW) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAC900T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF DAC900-Q1 :

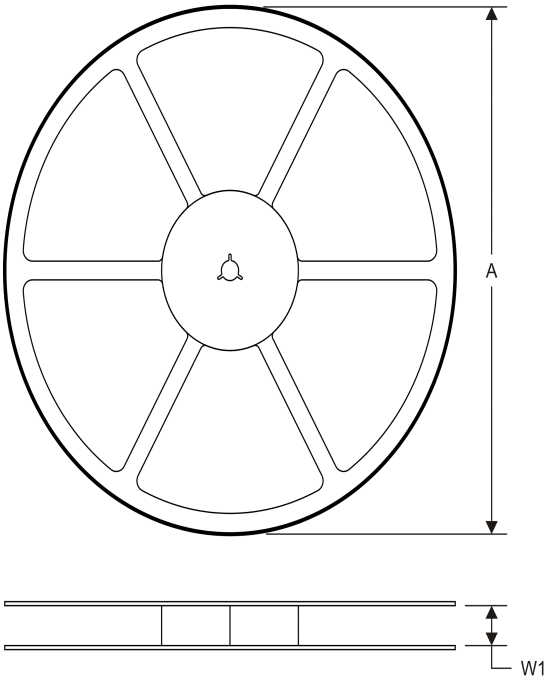
- Catalog : DAC900

NOTE: Qualified Version Definitions:

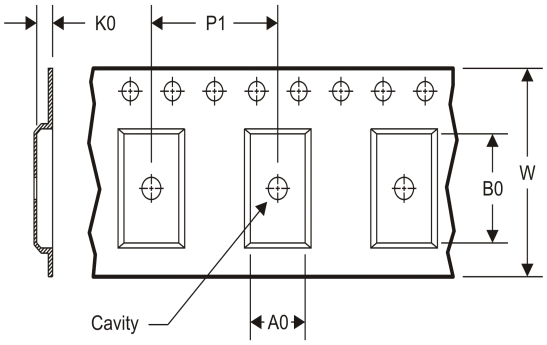
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



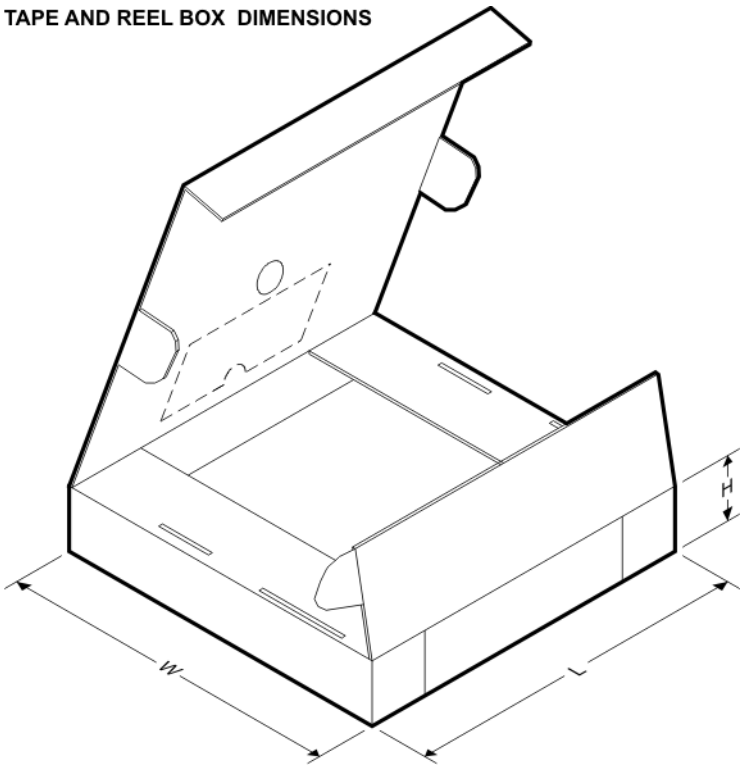
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC900TPWRQ1	TSSOP	PW	28	2500	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

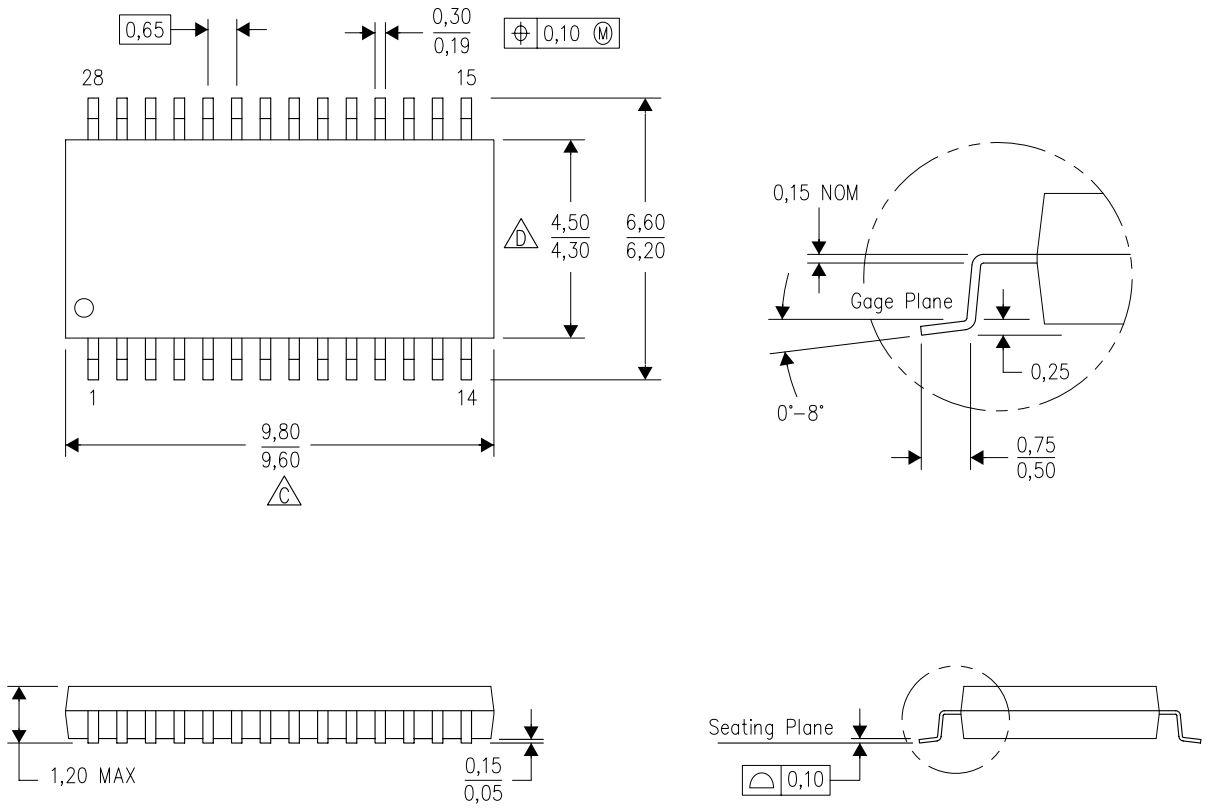
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC900TPWRQ1	TSSOP	PW	28	2500	367.0	367.0	38.0

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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