

DDC3512 512-Channel, Current-Input Analog-To-Digital Converter

1 Features

- Single-chip design to directly measure 512 low-level currents simultaneously
- Adjustable full-scale charge range up to 600pC
- Input current: 1μA (maximum)
- Adjustable speed with integration times as low as 50μs (20 KSPS per channel)
- Resolution: 24 bit
- Low power dissipation: 1.2mW/channel
- Integral non-linearity: ±0.025% of reading ±1ppm of full scale range (all channels active)
- Low noise: 0.26 fCrms at 600pC FSR with 20pF sensor capacitance
- No charge loss
- On-chip temperature sensor
- Serial LVDS output interface
- Single 1.85V supply
- In-package bypass capacitors and reference buffer to reduce PCB area and design complexity

2 Applications

- [CT scanner](#) data acquisition system
- Photodiode sensors
- [X-ray](#) detection systems
- Optical fiber power monitoring
- Multi-channel current, voltage instrumentation

3 Description

The DDC3512 is a 24-bit, 512-channel, current-input analog-to-digital (A/D) converter. The device combines both, current-to-voltage conversion by current integration, and A/D conversion. The device is a stacked-die version of DDC3256, with one die of the latter sitting on top of the other.

Up to 512 individual low-level current output devices, such as photodiodes, can be directly connected to the inputs and digitized in parallel (simultaneously).

For each of the 512 inputs, the device has one low noise and low power integrator designed to capture all the charge from the sensor. The integration time is adjustable from 50μs to 1.6ms, allowing currents in the order of fA to μA to be continuously measured with outstanding precision. The outputs of the integrators are digitized by on-chip low power ADCs and the converted digital codes are transmitted over a single LVDS pair designed to minimize noise coupling in environments with high channel count.

The DDC3512 operates from single 1.85V supply. The device is specified from 0°C to 70°C operating temperature and available in a 13.2 × 17.2mm² 656-ball 0.8mm row-pitch and 0.4mm column-pitch BGA. The on-chip reference buffer and bypass capacitors (on the BGA) help minimize the external component requirements and further reduce board space.

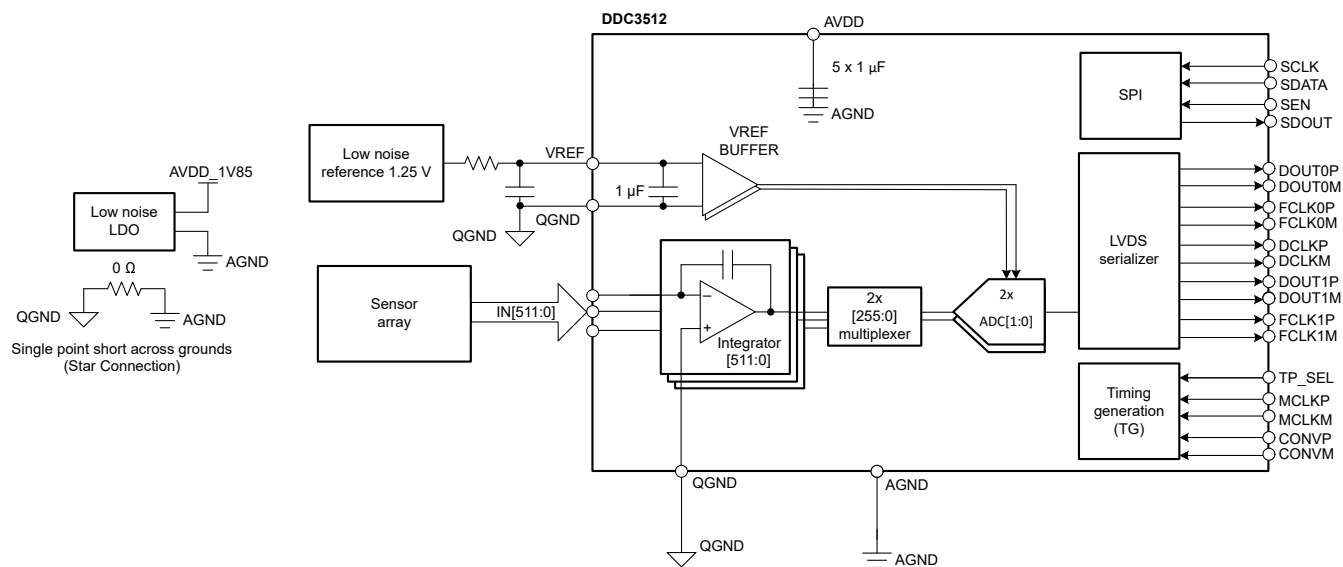
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
DDC3512	ZWR (NFBGA, 656)	17.2mm × 13.2mm

(1) For more information, see [Section 6](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.





Simplified Schematic

4 Device and Documentation Support

4.1 Documentation Support

4.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [TPS7A84 High-Current \(3 A\), High-Accuracy \(1%\), Low-Noise \(4.4 \$\mu\$ VRMS\), LDO Voltage Regulator data sheet](#)
- Texas Instruments, [REF70 2 ppm/ \$^{\circ}\$ C Maximum Drift, 0.23 ppmp-p 1/f Noise, Precision Voltage Reference data sheet](#)

4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.4 Trademarks

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4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

DATE	REVISION	NOTES
October 2025	*	Initial Release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DDC3512ZWR	Active	Production	NFBGA (ZWR) 656	108 EIAJ TRAY (10+1)	Yes	SNAGCUNI	Level-3-260C-168 HR	0 to 70	DDC3512

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

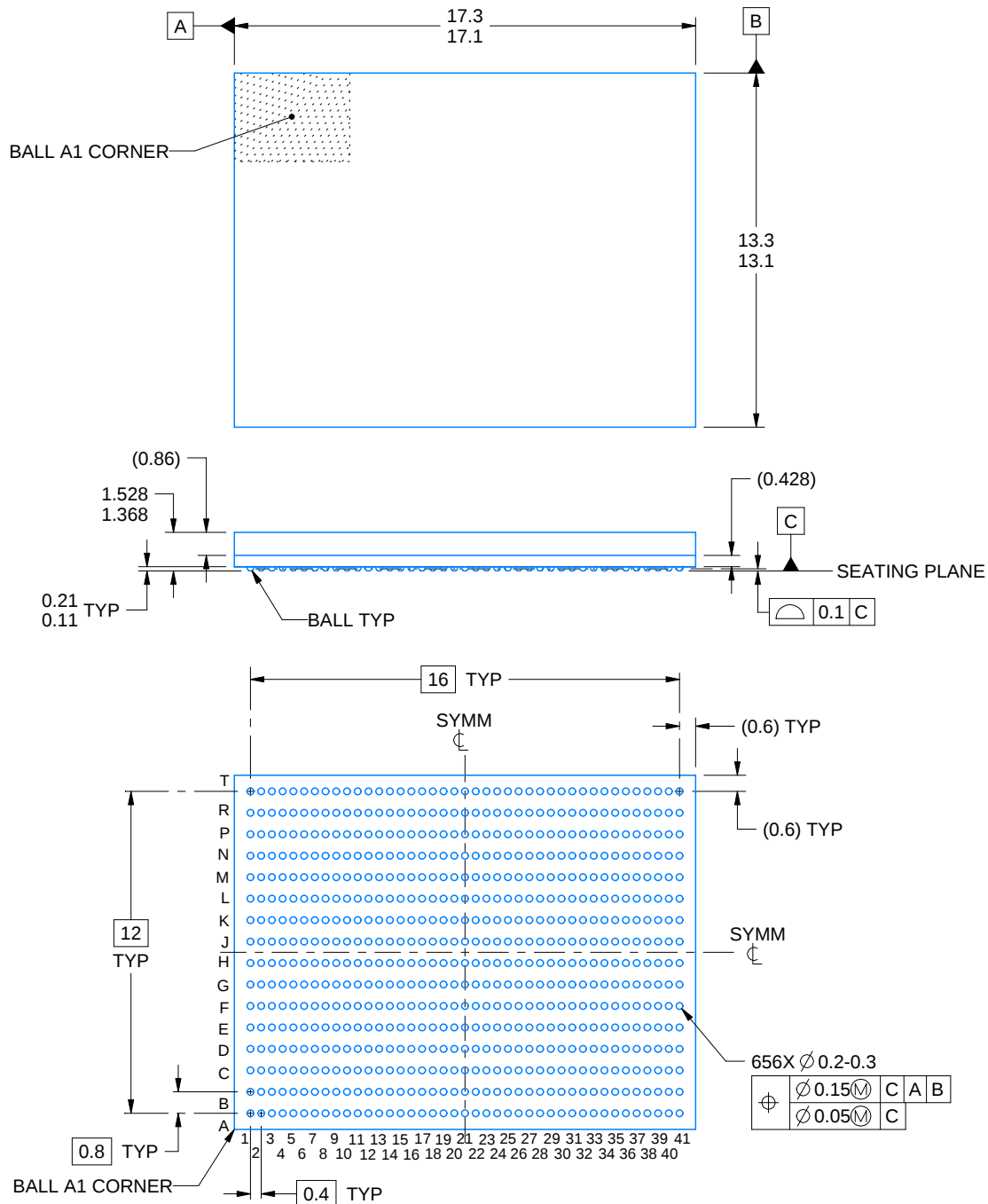
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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NOTES:

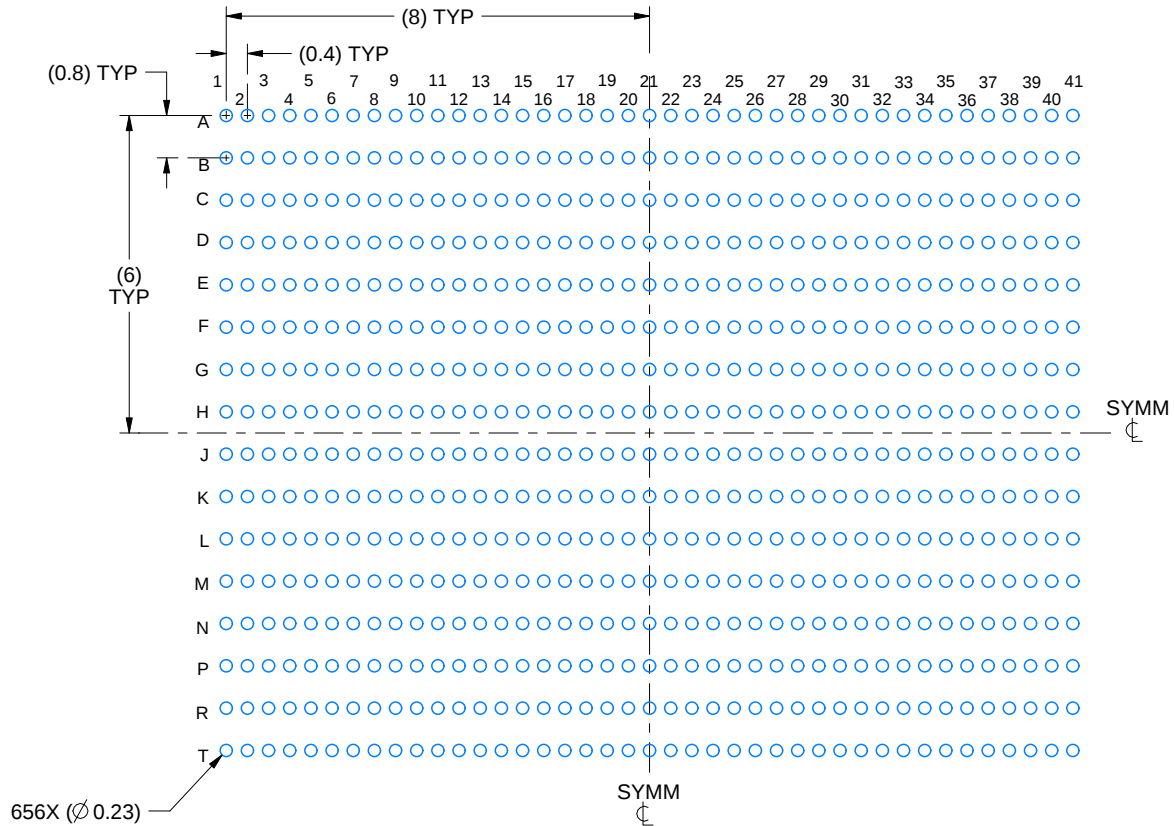
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

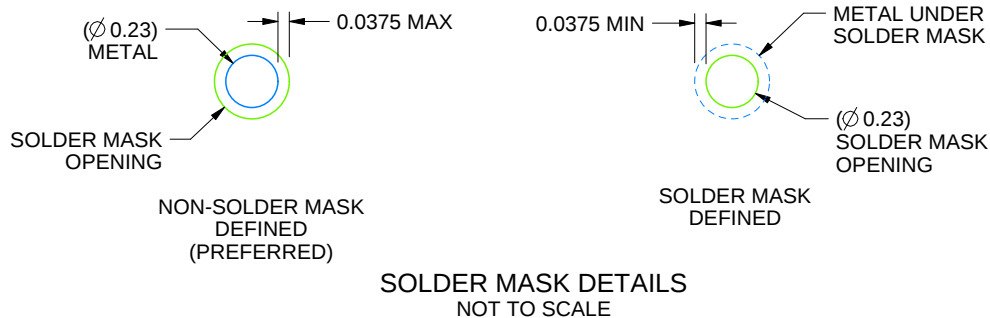
ZWR0656A

NFBGA - 1.53 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:7X



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NOTES: (continued)

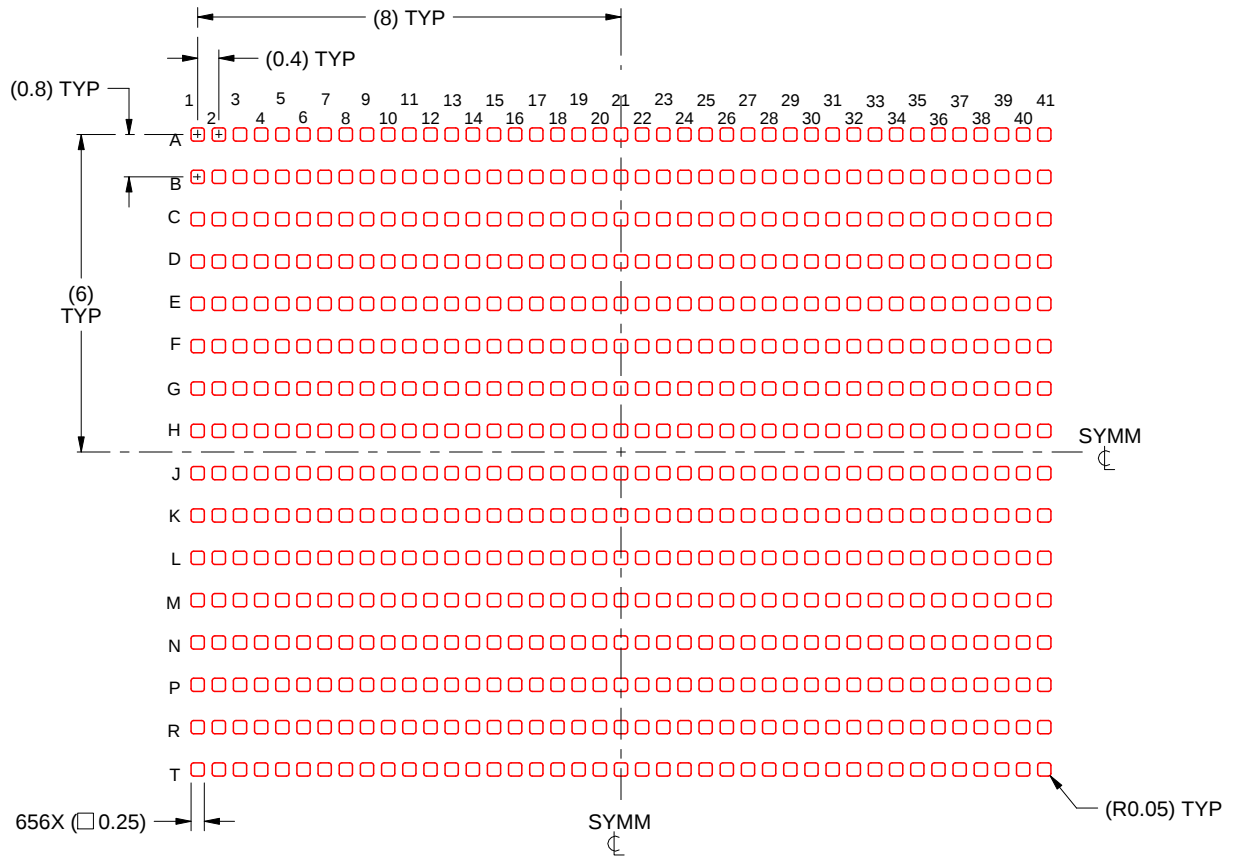
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZWR0656A

NFBGA - 1.53 mm max height

PLASTIC BALL GRID ARRAY



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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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