DLP391TP 0.39-Inch 4K UHD Digital Micromirror Device

1 Features

- 0.39" diagonal micromirror array
  - 4K UHD (3840 × 2160) display resolution
  - 4.5µm micromirror pitch
  - ±14.5° micromirror tilt (relative to flat surface)
  - Side illumination
- SubLVDS input data bus
- Supports 4K UHD at 60Hz
- Supports 1080p up to 240Hz
- LED operation is supported by DLPC8445V display controller, DLPA3085 / DLPA3082 power management IC (PMIC) and illumination driver

2 Applications

- Mobile smart TV
- Mobile projector
- Digital signage

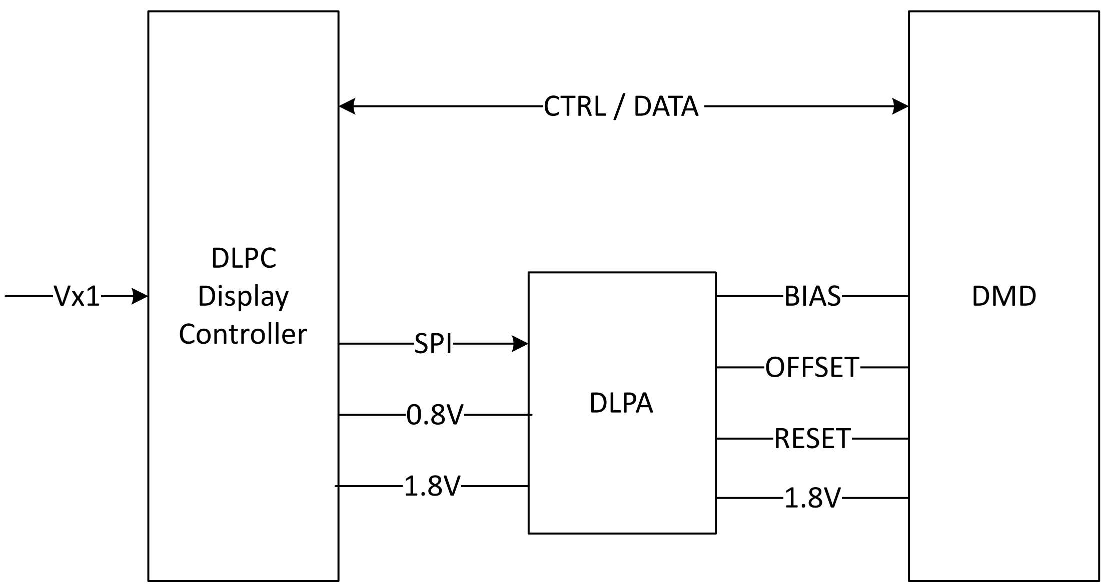
3 Description

The DLP391TP digital micromirror device (DMD) is a digitally controlled micro-electro-mechanical system (MEMS) spatial light modulator (SLM) that enables bright 4K UHD display systems. The TI DLP® Products 0.39" 4K UHD chipset is composed of the DMD, DLPC8445V display controller, and DLPA3085 / DLPA3082 PMIC and illumination driver. The compact physical size of the chipset provides a complete system solution that enables small form factor 4K UHD displays.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE
DLP391TP	FSB (154)	18.35mm × 9.60mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.



Simplified Application

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4 Pin Configuration and Functions

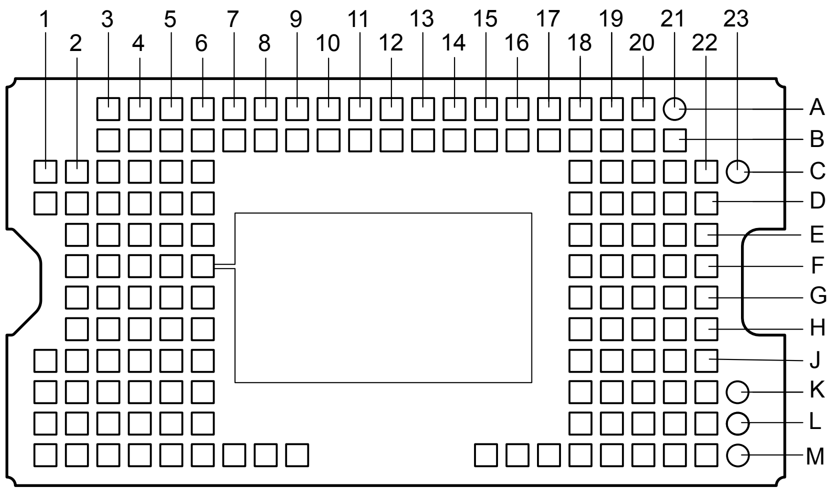


Figure 4-1. FSB Package 154-Pin LGA (Bottom View)

Table 4-1. Pin Functions

PIN [(2)]		TYPE[(1)]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_AP(0)	C2	I	High-Speed Differential Data Pair lane A0	Differential 100Ω	1.123
D_AN(0)	C3	I	High-Speed Differential Data Pair lane A0	Differential 100Ω	1.414
D_AP(1)	D2	I	High-Speed Differential Data Pair lane A1	Differential 100Ω	1.212
D_AN(1)	D3	I	High-Speed Differential Data Pair lane A1	Differential 100Ω	1.626
D_AP(2)	C4	I	High-Speed Differential Data Pair lane A2	Differential 100Ω	3.011
D_AN(2)	C5	I	High-Speed Differential Data Pair lane A2	Differential 100Ω	3.388
D_AP(3)	D5	I	High-Speed Differential Data Pair lane A3	Differential 100Ω	3.682
D_AN(3)	D6	I	High-Speed Differential Data Pair lane A3	Differential 100Ω	3.912
D_AP(4)	G5	I	High-Speed Differential Data Pair lane A4	Differential 100Ω	3.542
D_AN(4)	G6	I	High-Speed Differential Data Pair lane A4	Differential 100Ω	3.662
D_AP(5)	E2	I	High-Speed Differential Data Pair lane A5	Differential 100Ω	0.972
D_AN(5)	E3	I	High-Speed Differential Data Pair lane A5	Differential 100Ω	1.335
D_AP(6)	E5	I	High-Speed Differential Data Pair lane A6	Differential 100Ω	4.520
D_AN(6)	E6	I	High-Speed Differential Data Pair lane A6	Differential 100Ω	4.634
D_AP(7)	H5	I	High-Speed Differential Data Pair lane A7	Differential 100Ω	3.200
D_AN(7)	H6	I	High-Speed Differential Data Pair lane A7	Differential 100Ω	3.515
DCLK_AP	F4	I	High-Speed Differential Clock A	Differential 100Ω	2.610
DCLK_AN	F5	I	High-Speed Differential Clock A	Differential 100Ω	3.068
D_BP(0)	C20	I	High-Speed Differential Data Pair lane B0	Differential 100Ω	2.563
D_BN(0)	C19	I	High-Speed Differential Data Pair lane B0	Differential 100Ω	2.636
D_BP(1)	D21	I	High-Speed Differential Data Pair lane B1	Differential 100Ω	2.329
D_BN(1)	D20	I	High-Speed Differential Data Pair lane B1	Differential 100Ω	2.487
D_BP(2)	C18	I	High-Speed Differential Data Pair lane B2	Differential 100Ω	4.300
D_BN(2)	D18	I	High-Speed Differential Data Pair lane B2	Differential 100Ω	4.569

Table 4-1. Pin Functions (continued)

PIN (2)		TYPE(1)	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_BP(3)	E20	I	High-Speed Differential Data Pair lane B3	Differential 100Ω	3.112
D_BN(3)	E19	I	High-Speed Differential Data Pair lane B3	Differential 100Ω	3.485
D_BP(4)	F22	I	High-Speed Differential Data Pair lane B4	Differential 100Ω	1.073
D_BN(4)	F21	I	High-Speed Differential Data Pair lane B4	Differential 100Ω	1.239
D_BP(5)	H18	I	High-Speed Differential Data Pair lane B5	Differential 100Ω	4.146
D_BN(5)	G18	I	High-Speed Differential Data Pair lane B5	Differential 100Ω	4.330
D_BP(6)	F18	I	High-Speed Differential Data Pair lane B6	Differential 100Ω	4.241
D_BN(6)	E18	I	High-Speed Differential Data Pair lane B6	Differential 100Ω	4.494
D_BP(7)	G22	I	High-Speed Differential Data Pair lane B7	Differential 100Ω	0.663
D_BN(7)	G21	I	High-Speed Differential Data Pair lane B7	Differential 100Ω	1.054
DCLK_BP	F20	I	High-Speed Differential Clock B	Differential 100Ω	2.404
DCLK_BN	F19	I	High-Speed Differential Clock B	Differential 100Ω	2.610
D_CP(0)	G2	I	High-Speed Differential Data Pair lane C0	Differential 100Ω	1.052
D_CN(0)	G3	I	High-Speed Differential Data Pair lane C0	Differential 100Ω	1.112
D_CP(1)	M7	I	High-Speed Differential Data Pair lane C1	Differential 100Ω	6.519
D_CN(1)	M8	I	High-Speed Differential Data Pair lane C1	Differential 100Ω	6.611
D_CP(2)	H2	I	High-Speed Differential Data Pair lane C2	Differential 100Ω	0.921
D_CN(2)	H3	I	High-Speed Differential Data Pair lane C2	Differential 100Ω	1.376
D_CP(3)	M5	I	High-Speed Differential Data Pair lane C3	Differential 100Ω	5.196
D_CN(3)	M6	I	High-Speed Differential Data Pair lane C3	Differential 100Ω	5.318
D_CP(4)	K3	I	High-Speed Differential Data Pair lane C4	Differential 100Ω	1.579
D_CN(4)	K4	I	High-Speed Differential Data Pair lane C4	Differential 100Ω	1.648
D_CP(5)	M3	I	High-Speed Differential Data Pair lane C5	Differential 100Ω	3.414
D_CN(5)	M4	I	High-Speed Differential Data Pair lane C5	Differential 100Ω	3.857
D_CP(6)	L4	I	High-Speed Differential Data Pair lane C6	Differential 100Ω	2.460
D_CN(6)	L5	I	High-Speed Differential Data Pair lane C6	Differential 100Ω	2.566
D_CP(7)	K1	I	High-Speed Differential Data Pair lane C7	Differential 100Ω	1.114
D_CN(7)	L1	I	High-Speed Differential Data Pair lane C7	Differential 100Ω	1.707
DCLK_CP	K5	I	High-Speed Differential Clock C	Differential 100Ω	3.744
DCLK_CN	K6	I	High-Speed Differential Clock C	Differential 100Ω	3.883
D_DP(0)	J19	I	High-Speed Differential Data Pair lane D0	Differential 100Ω	4.189
D_DN(0)	J18	I	High-Speed Differential Data Pair lane D0	Differential 100Ω	4.435
D_DP(1)	M18	I	High-Speed Differential Data Pair lane D1	Differential 100Ω	6.588
D_DN(1)	M17	I	High-Speed Differential Data Pair lane D1	Differential 100Ω	6.867
D_DP(2)	H21	I	High-Speed Differential Data Pair lane D2	Differential 100Ω	1.754
D_DN(2)	H20	I	High-Speed Differential Data Pair lane D2	Differential 100Ω	1.936
D_DP(3)	J22	I	High-Speed Differential Data Pair lane D3	Differential 100Ω	1.339
D_DN(3)	J21	I	High-Speed Differential Data Pair lane D3	Differential 100Ω	1.634
D_DP(4)	L20	I	High-Speed Differential Data Pair lane D4	Differential 100Ω	3.329
D_DN(4)	L19	I	High-Speed Differential Data Pair lane D4	Differential 100Ω	3.436
D_DP(5)	M20	I	High-Speed Differential Data Pair lane D5	Differential 100Ω	3.631
D_DN(5)	M19	I	High-Speed Differential Data Pair lane D5	Differential 100Ω	3.738
D_DP(6)	M22	I	High-Speed Differential Data Pair lane D6	Differential 100Ω	2.420
D_DN(6)	M21	I	High-Speed Differential Data Pair lane D6	Differential 100Ω	2.573

Table 4-1. Pin Functions (continued)

PIN [2]		TYPE[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_DP(7)	K22	I	High-Speed Differential Data Pair lane D7	Differential 100Ω	1.406
D_DN(7)	K21	I	High-Speed Differential Data Pair lane D7	Differential 100Ω	1.881
DCLK_DP	K19	I	High-Speed Differential Clock D	Differential 100Ω	3.916
DCLK_DN	K18	I	High-Speed Differential Clock D	Differential 100Ω	4.022
TEMP_N	M2	I	Temp Diode N		1.133
TEMP_P	M1	I	Temp Diode P		1.237
LS_RDATA_D	B7	O	LPSDR Output		4.978
LS_RDATA_C	A4	O	LPSDR Output		2.897
LS_WDATA	B5	I	LPSDR Input		2.524
LS_RDATA_B	A7	O	LPSDR Output		5.103
LS_RDATA_A	A3	O	LPSDR Output		1.725
LS_CLK	A5	I	LPSDR Input		2.454
DMD_DEN_ARSTZ	D1	I	ARSTZ	17.5kΩ pulldown	0.735
VDD	A6, A8, A10, A12, A14, A16, A18, B4, B11, B13, B15, B19, B21, C21, D22, E21, G4, J1, J4, J6, L2, M15	P	Digital Core Supply Voltage		8.350
VBIAS	A20, B6	P	Supply Voltage for Positive Bias of Micromirror reset signal		7.409
VRESET	B8, B17	P	Supply Voltage for Negative Bias of Micromirror reset signal		3.374
VOFFSET	B9, M16	P	Supply voltage for HVCMOS logic,stepped up logic level		1.797
VDDI	C22, E4, F2, G20, J2,L22	P			19.977
VSS	A9, A11, A13, A15, A17, A19, B3, B10, B12, B14, B16, B18, B20, C1, C6, D4, D19, E22, F3, F6, G19, H4, H19, H22, J3, J5, J20, K2, K20, L3, L6, L18, L21, M9	G	Ground		12.614
N/C	A21, C23, K23, L23, M23	NC	No Connect Pin		N/A

(1) I=Input, O=Output, P=Power, G=Ground, NC=No Connect
(2) Only 151 pins are electrically connected for functional use.

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{DD}	Supply voltage for LVCMOS core logic and low speed interface (LSIF)(1)	-0.5	2.3	V
V_{DDI}	Supply voltage for SubLVDS receivers(1)	-0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(1) (2)	-0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(1)	-0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(1)	-15	0.5	V
$\mid V_{DDI} - V_{DD} \mid$	Supply voltage delta, absolute value(3)		0.3	V
$\mid V_{BIAS} - V_{OFFSET} \mid$	Supply voltage delta, absolute value(4)		11	V
$\mid V_{BIAS} - V_{RESET} \mid$	Supply voltage delta, absolute value(5)		34	V
INPUT VOLTAGE				
	Input voltage for other inputs — LSIF and LVCMOS	-0.5	V_{DD} + 0.5	V
	Input voltage for other inputs — SubLVDS(1) (6)	-0.5	V_{DDI} + 0.5	V
SUBLVDS INTERFACE				
$\mid V_{ID} \mid$	SubLVDS input differential voltage (absolute value)(6)		810	mV
I_{ID}	SubLVDS input differential current		10	mA
CLOCK FREQUENCY				
f_{clock}	Clock frequency for low-speed interface LS_CLK	100	130	MHz
TEMPERATURE DIODE				
I_{TEMP_DIODE}	Max current source into the temperature diode		120	µA
ENVIRONMENTAL				
T_{ARRAY}	Temperature, operating(7)	0	90	°C
T_{ARRAY}	Temperature, non-operating(7)	-40	90	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) All voltage values are with respect to the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDI} and V_{DD} may result in excessive current draw and permanent damage to the device.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw and permanent damage to the device.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw and permanent damage to the device.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. SubLVDS differential inputs must not exceed the specified limit or damage to the internal termination resistors may result.
(7) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 6-2 using the Micromirror Array Temperature Calculation.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD temperature	-40	85	°C
$T_{DP\text{-}AVG}$	Average dew point temperature, non-condensing(1)		28	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range, non-condensing(2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	months

(1) The average temperature over time (including storage and operating temperatures) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification ANSI/ESDA/JEDEC JS-002(2)	±250	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

PARAMETER		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE RANGE					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface (1) (2)	1.71	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers (1) (2)	1.71	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode (1) (2) (3)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for mirror electrode (1) (2)	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode (1) (2)	–14.5	–14	–13.5	V
$\| V_{DDI} - V_{DD} \|$	Supply voltage delta (absolute value) (1) (2) (4)			0.3	V
$\| V_{BIAS} - V_{OFFSET} \|$	Supply voltage delta (absolute value) (1) (2) (5)			10.5	V
$\| V_{BIAS} - V_{RESET} \|$	Supply voltage delta (absolute value) (1) (2) (6)			33	V
LPSDR INTERFACE					
V_{IH}	High-level input voltage	$0.7 \times V_{DD}$			V
V_{IL}	Low-level input voltage			$0.3 \times V_{DD}$	V
V_{IH} (AC)	AC input high voltage	$0.8 \times V_{DD}$		$V_{DD} + 0.3$	V
V_{IL} (AC)	AC input low voltage	–0.3		$0.2 \times V_{DD}$	V
VHyst	Input Hysteresis	$0.1 \times V_{DD}$		$0.4 \times V_{DD}$	V
f_{max_LS}	Clock frequency for low speed interface LS_CLK (7)	108		130	MHz
DCD_{IN}	LSIF duty cycle distortion (LS_CLK) (7)	44		56	%
SUBLVDS INTERFACE					
f_{max_HS}	Clock frequency for high-speed interface DCLK (8)			720	MHz
DCD_{IN}	LVDS duty cycle distortion (DCLK)	48		52	%
$\| V_{ID} \|$	LVDS differential input voltage magnitude (8)	150	250	350	mV
V_{CM}	Common mode voltage (8)	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage (8)	525		1275	mV
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
TEMPERATURE DIODE					
I_{TEMP_DIODE}	Max current source into Temperature Diode			120	µA
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operation (9) (10) (11) (12)	0		40 to 70	°C
T_{DP-AVG}	Average dew point temperature, (non-condensing)(13)			28	°C
T_{DP-ELR}	Elevated dew point temperature range, (non-condensing)(14)		28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	months
Q_{AP-ILL}	Window aperture illumination overfill (15) (16) (17)			17	W/cm^2
ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 410nm (9) (19)			10	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths ≥ 410nm and ≤ 800nm (18) (19)			40	W/cm^2
ILL_{IR}	Illumination power at wavelengths > 800nm (19)			10	mW/cm^2
ILL_{BLU}	Illumination power at wavelengths ≥ 410nm and ≤ 475nm (18) (19)			12.8	W/cm^2
ILL_{BLU1}	Illumination power at wavelengths ≥ 410nm and ≤ 440nm (18) (19)			2.0	W/cm^2

(1) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All VSS connections are also required.
(2) All voltage values are with respect to the ground pins (VSS).

(3) VOFFSET supply transients must fall within the specified max voltages.
(4) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(6) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit.
(7) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(8) Refer to the SubLVDS timing requirements in Timing Requirements.
(9) Simultaneous exposure of the DMD to the maximum Recommended Operating Conditions for temperature and UV illumination reduces device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in Figure 6-2 and the package thermal resistance using the Micromirror Array Temperature Calculation
(11) Long-term is defined as the usable life of the device.
(12) Per Figure 5-1, the maximum operational array temperature is derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See Micromirror Landed-on/Landed-off Duty cycle for a definition of micromirror landed duty cycle.
(13) The average over time (including storage and operating) is that the device is not in the elevated dew point temperature range.
(14) Exposure to dew point temperatures in the elevated range during storage and operation is limited to less than a total cumulative time of CT_{ELR}.
(15) Applies to the region defined in Figure 5-2
(16) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly for normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects on the performance of an end application using the DMD. Minimizing the light flux incident outside the active array is a design requirement of the illumination optical system. Depending on the particular optical architecture and assembly tolerances of the optical system, the amount of overfill light on the outside of the active array may cause system performance degradation.
(17) To calculate, see Window Aperture Illumination Overfill Calculation.
(18) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
(19) To calculate, see Micromirror Power Density Calculation.

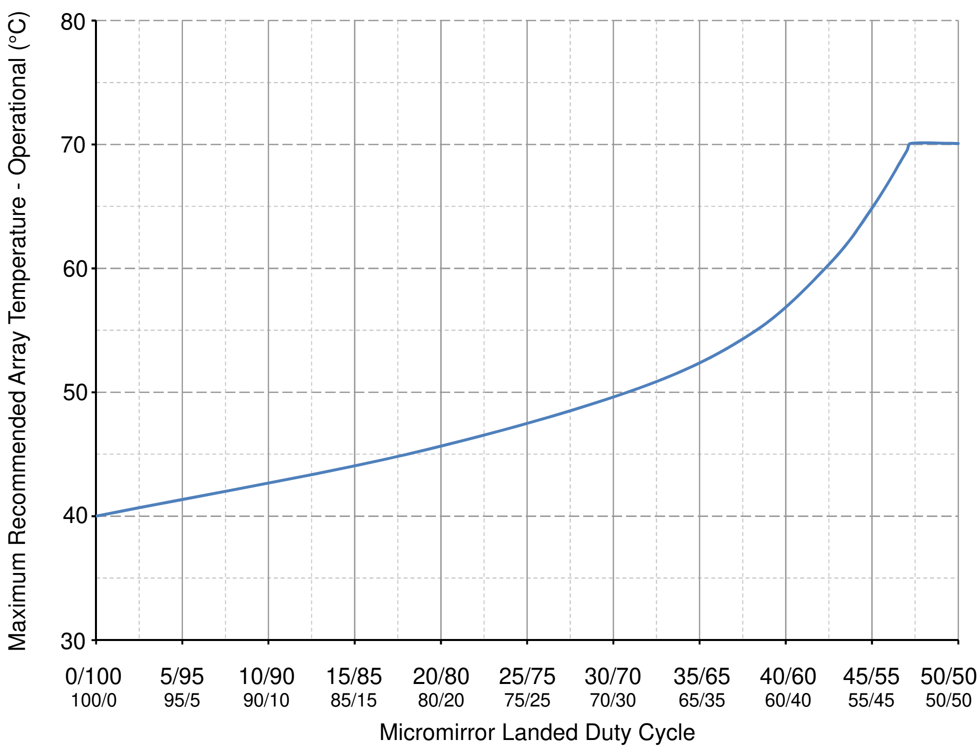


Figure 5-1. Maximum Recommended Array Temperature—Derating Curve

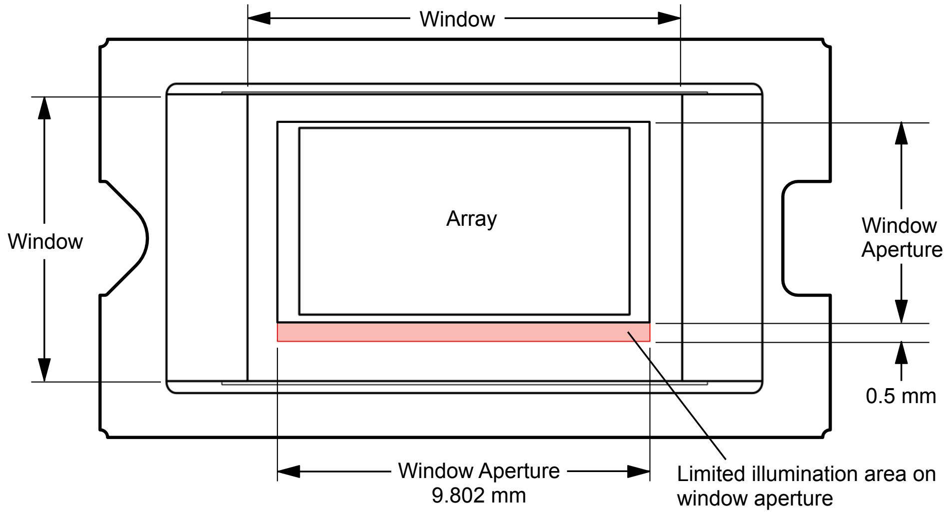


Figure 5-2. Illumination Overfill Diagram—Critical Area

5.5 Thermal Information

THERMAL METRIC	DLP391TP FSB 154 PIN	UNIT
THERMAL INFORMATION		
Thermal Resistance[1]	2.3	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the Recommended Operating Conditions. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER (6)		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: V_{DD} (3) (4)	Typical			140	mA
I_{DDI}	Supply current: V_{DDI} (3) (4)	Typical			45	mA
I_{OFFSET}	Supply current: V_{OFFSET} (5)	Typical			6	mA
I_{BIAS}	Supply current: V_{BIAS} (5)	Typical			0.6	mA
I_{RESET}	Supply current: V_{RESET}	Typical			1.8	mA
POWER						
P_{DD}	Supply power dissipation: V_{DD} (3) (4)	Typical			252	mW
P_{DDI}	Supply power dissipation: V_{DDI} (3) (4)	Typical			81	mW
P_{OFFSET}	Supply power dissipation: V_{OFFSET} (5)	Typical			60	mW
P_{BIAS}	Supply power dissipation: V_{BIAS} (5)	Typical			1.08	mW
P_{RESET}	Supply power dissipation: V_{RESET}	Typical			25.2	mW
P_{TOTAL}	Supply power dissipation Total	Typical			419.28	mW
LPSDR INPUT						
I_{IL}	Low level input current	V_{DD} = 1.95V, V_I = 0V	-100			nA
I_{IH}	High level input current	V_{DD} = 1.95V, V_I = 1.95V			135	uA
LPSDR OUTPUT						
V_{OH}	DC output high voltage (7) (8) (9)	I_{OH} = -2mA	0.8 x V_{DD}			V
V_{OL}	DC output low voltage (7) (8) (9)	I_{OL} = 2mA			0.2 x V_{DD}	V
CAPACITANCE						
C_{IN}	Input capacitance LVCMOS	F = 1MHz			10	pF
C_{IN}	Input capacitance SubLVDS	F = 1MHz			20	pF
C_{OUT}	Output capacitance	F = 1MHz			10	pF
C_{TEMP}	Temperature sense diode capacitance	F = 1MHz			20	pF

(1) Device electrical characteristics are over Section 5.4 unless otherwise noted.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta | V_{DDI} – V_{DD} | must be less than the specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta | V_{BIAS} – V_{OFFSET} | must be less than the specified limit.
(6) All power supply connections are required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, VRESET. All VSS connections are also required.
(7) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(8) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209-2F, Low-Power Double Data Rate (LPDDR) JESD209-2F.
(9) LPSDR output specification is for pins LS_RDATA_A, LS_RDATA_B, LS_RDATA_C, LS_RDATA_D.

5.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK input to LS_RDATA output. (1)	C_L = 15pF			15	ns
	Slew rate, LS_RDATA		0.3			V/ns
	Output duty cycle distortion, LS_RDATA		40		60	%

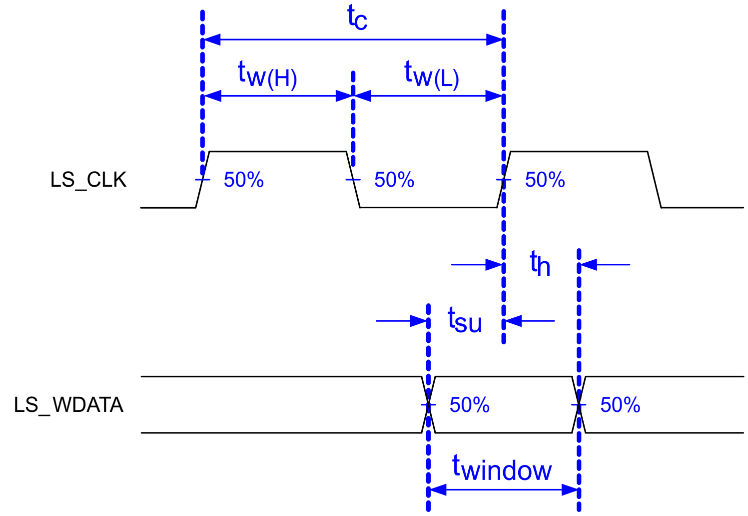
(1) Device electrical characteristics are over Section 5.4 unless otherwise noted.

5.8 Timing Requirements

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
LVCMOS						
LPSDR						
t_r	Rise slew rate (2)	(20% to 80%) × VDD(6)	0.25			V/ns
t_f	Fall slew rate (2)	(80% to 20%) × VDD(6)	0.25			V/ns
t_r	Rise slew rate (1)	(30% to 80%) × VDD(6)	1		3	V/ns
t_f	Fall slew rate (1)	(70% to 20%) × VDD(6)	1		3	V/ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points(5)	4.2			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points(5)	4.2			ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK(5)			1.5	ns
t_h	Hold time	LS_WDATA valid after LS_CLK(5)			1.5	ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points(7)	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points(7)	0.7	1		V/ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points(8)	0.7			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points(8)	0.7			ns
t_{WINDOW}	Window time (1) (3)	Setup time + Hold time(5)	0.25			ns
t_{su}	Setup time	HS_DATA valid before HS_CLK(8)			0.17	ns
t_h	Hold time	HS_DATA valid after HS_CLK(8)			0.17	ns
t_{POWER}	Power-up receiver(4)				200	ns

(1) The specification is for the DMD_DEN_ARSTZ pin. Refer to the LPSDR input rise and fall slew rate in Figure 5-4.
(2) The specification is for the LS_CLK and LS_WDATA pins. Refer to the LPSDR input rise and fall slew rate in Figure 5-4.
(3) Window time derating example: 0.5V/ns slew rate increases the window time by 0.7ns, from 3ns to 3.7ns. See Figure 5-6.
(4) The specification is for the SubLVDS receiver time only and does not take into account commanding and latency after commanding.
(5) See Figure 5-3.
(6) See Figure 5-4.
(7) See Figure 5-5.
(8) See Figure 5-7.



The low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

Figure 5-3. LPSDR Switching Parameters

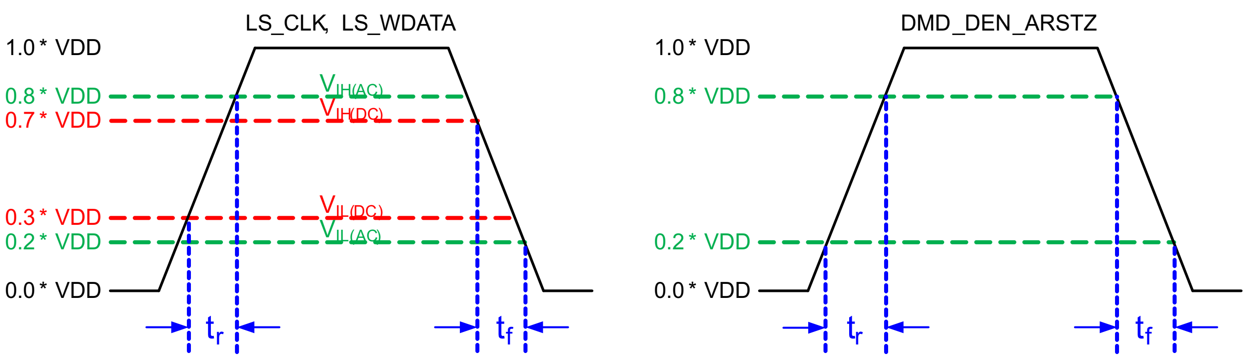


Figure 5-4. LPSDR Input Rise and Fall Slew Rate

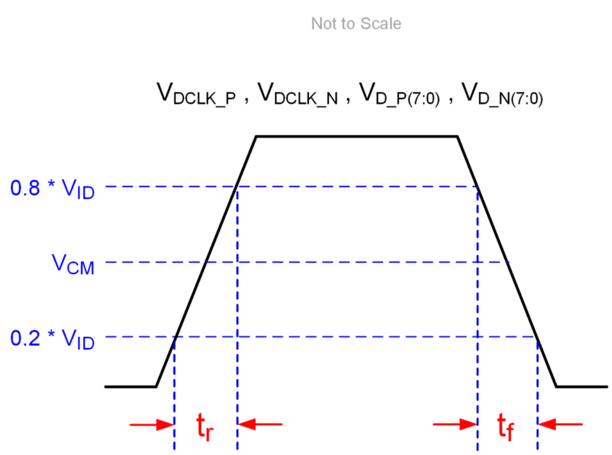


Figure 5-5. SubLVDS Input Rise and Fall Slew Rate

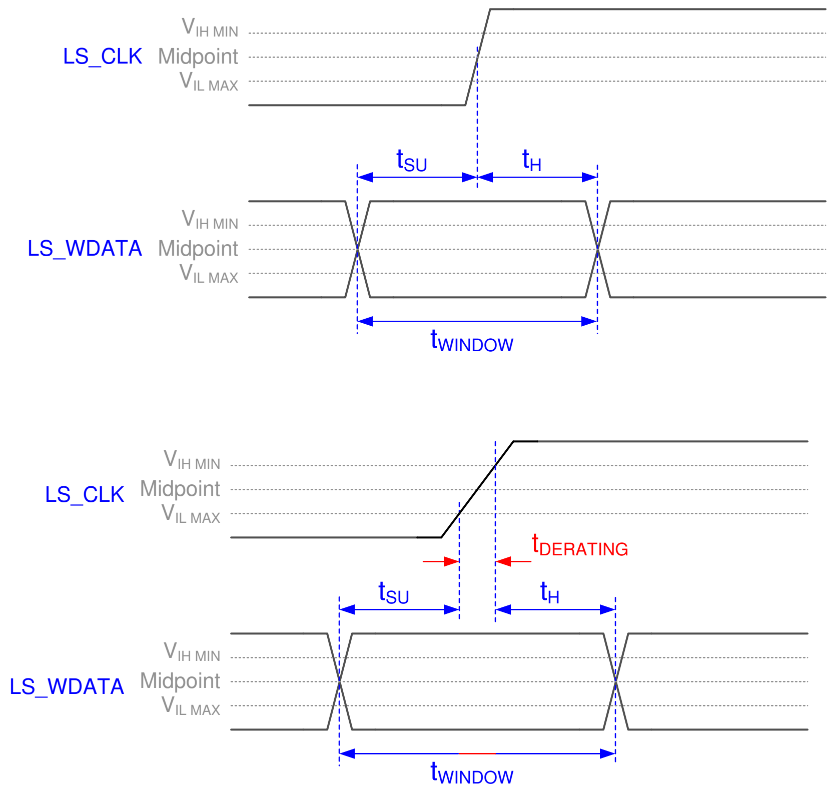


Figure 5-6. Window Time Derating Concept

Not to Scale

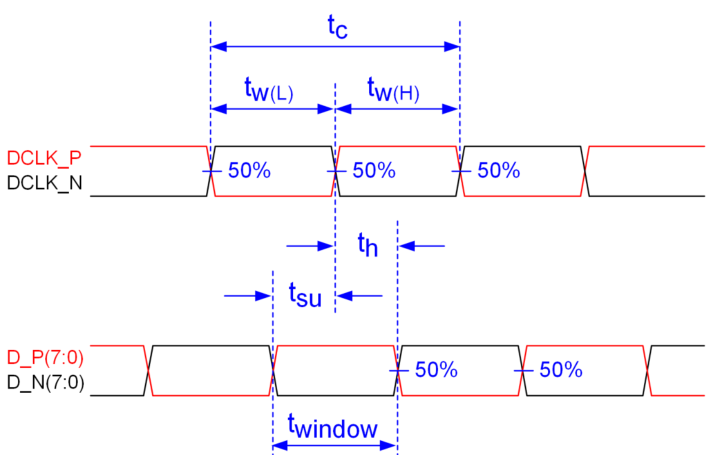
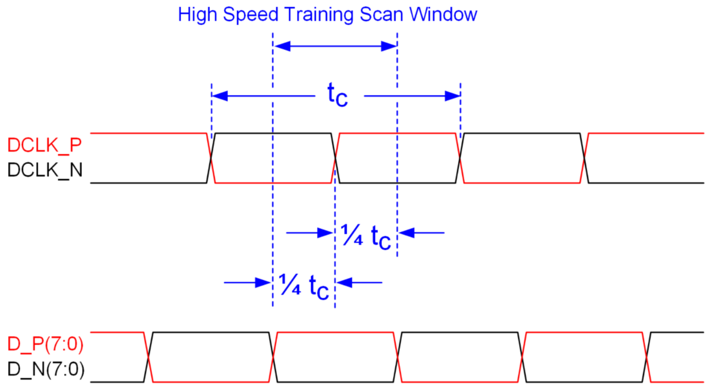


Figure 5-7. SubLVDS Switching Parameters



Refer to *Timing Requirements* for details.

Figure 5-8. High-Speed Training Scan Window

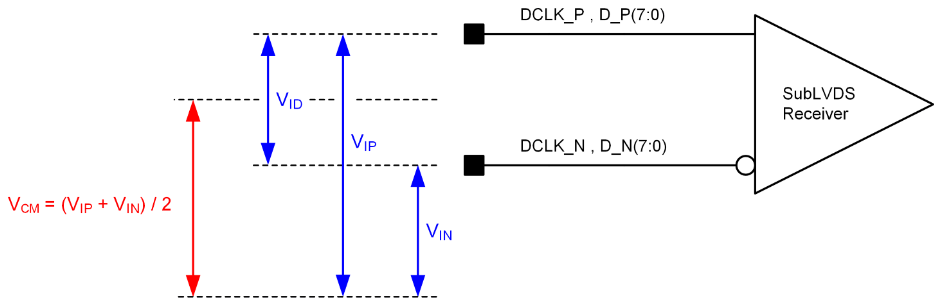


Figure 5-9. SubLVDS Voltage Parameters

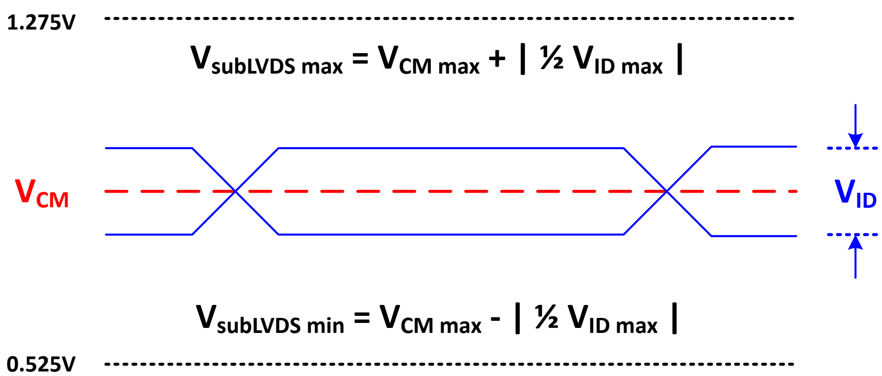


Figure 5-10. SubLVDS Waveform Parameters

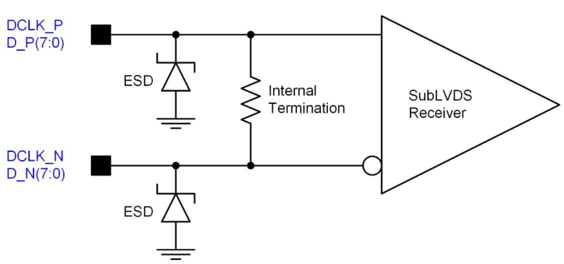


Figure 5-11. SubLVDS Equivalent Input Circuit

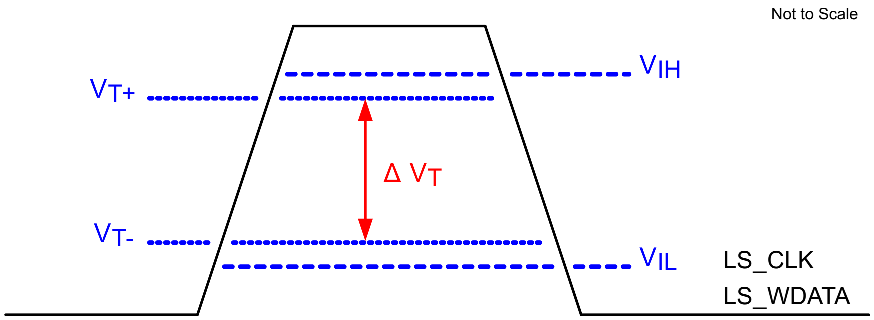


Figure 5-12. LPSDR Input Hysteresis

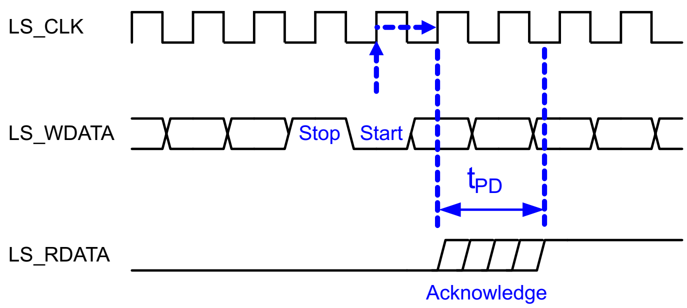
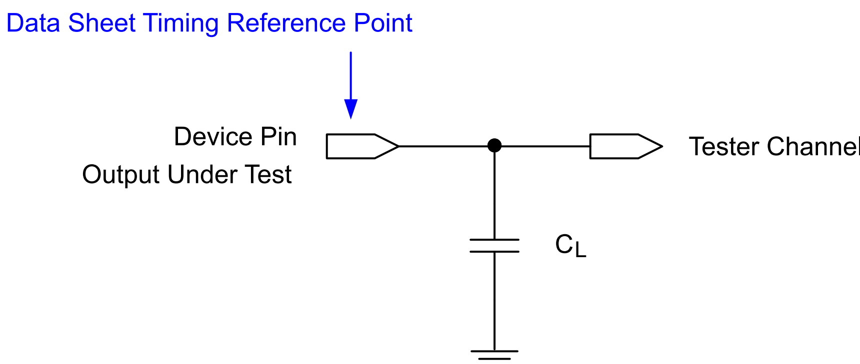


Figure 5-13. LPSDR Read Out



See Section 6.3.4 for more information.

Figure 5-14. Test Load Circuit for Output Propagation Measurement

5.9 System Mounting Interface Loads

PARAMETER	Condition	MIN	NOM	MAX	UNIT
Thermal Interface Area	Maximum load evenly distributed within each area [1]			50	N
Electrical Interface Area	Maximum load evenly distributed within each area [1]			143	

(1) See Figure 5-15.

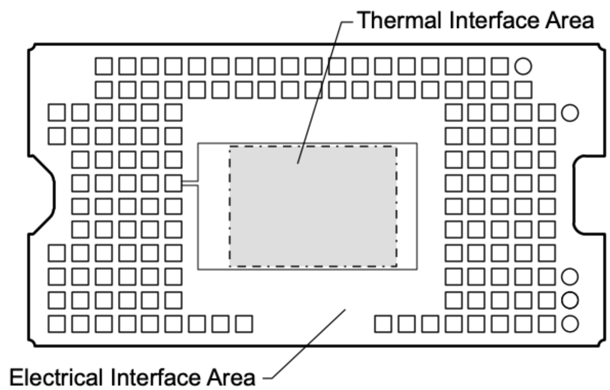


Figure 5-15. System Mounting Interface Loads

5.10 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION			VALUE	UNIT
M	Number of active columns (1) (2)		1360	micromirrors
N	Number of active rows (1) (2)		1536	micromirrors
Ɛ	Micromirror pitch, diagonal(1)		4.525	µm
P	Micromirror pitch, vertical and horizontal (1)		6.4	µm
	Micromirror active array width (1)	(P × M) + (P / 2)	8.7072	mm
	Micromirror active array height (1)	(P × N) / 2 + (P / 2)	4.9184	mm
	Micromirror active border (3)	Pond of micromirror (POM)	15	micromirrors/side

(1) See Figure 5-16.
(2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 x 2160 pixel image being displayed.
(3) The structure and qualities of the border around the active array include a band of partially functional micromirrors referred to as the *Pond of Micromirrors* (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

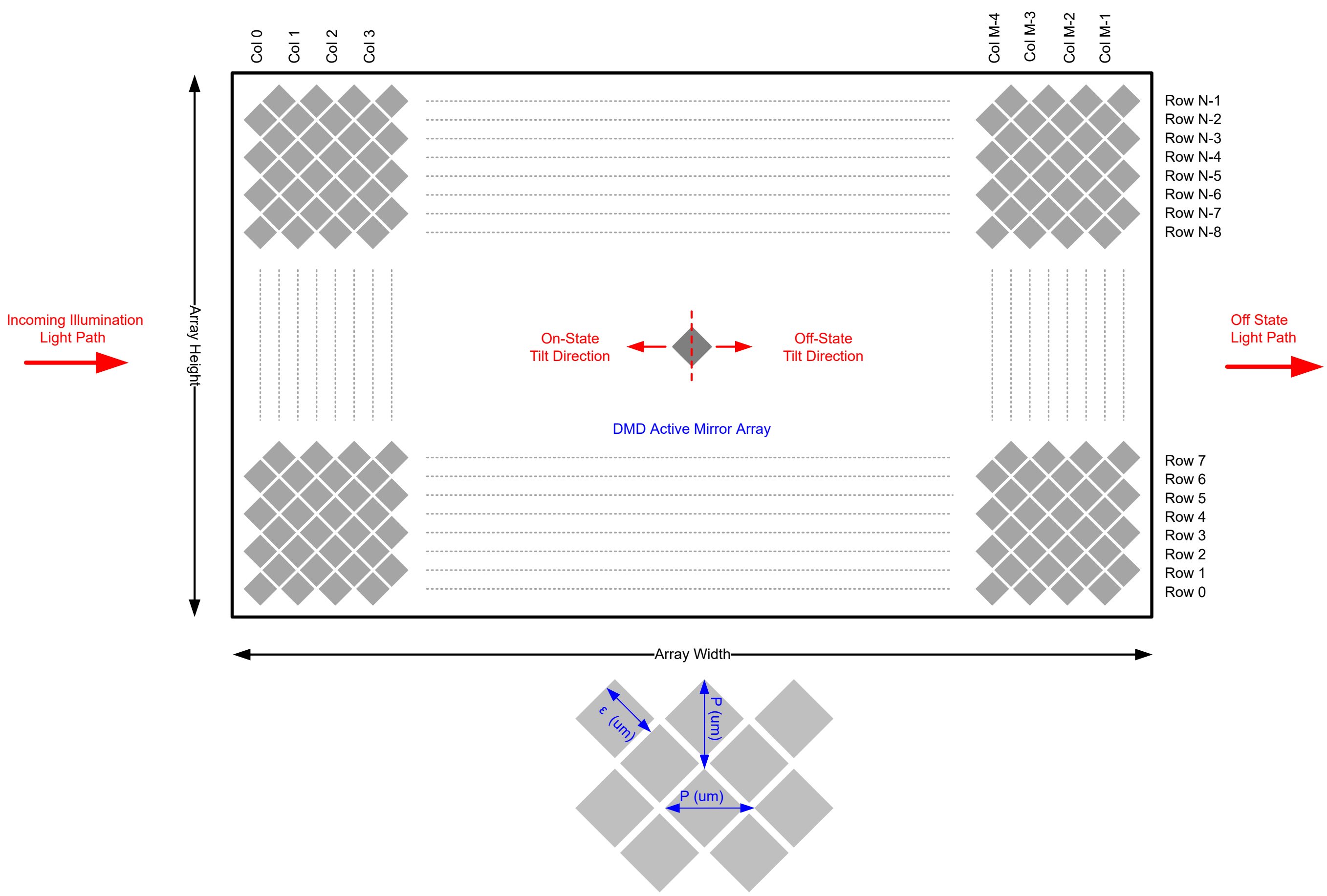


Figure 5-16. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle		DMD landed state [(1) (2) (3) (4)]	13.5	14.5	15.5	degrees
Micromirror crossover time[(5)]				1	3	μs
Micromirror switching time[(6)]			6			μs
Image Performance[(7)]	Bright pixel(s) in active area[(8)]	Gray 10 Screen[(9)]			0	Micromirrors
	Bright pixel(s) in the POM[(10)]	Gray 10 Screen[(9)]			1	
	Dark pixel(s) in the active area[(11)]	White Screen			4	
	Adjacent pixel(s)[(12)]	Any Screen			0	
	Unstable pixel(s) in active area[(13)]	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the variation that can occur between any two individual micromirrors, located on the same device or on different devices.
(4) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(5) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(6) The minimum time between successive transitions of a micromirror
(7) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear
Test set brightness and contrast shall be set to nominal
The diagonal size of the projected image shall be a minimum of 20 inches
The projection screen shall be unity gain
The projected image shall be inspected from a 38-inch minimum viewing distance
The image must be in focus during all image quality tests.
(8) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
(9) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(10) POM definition: Rectangular border of off-state mirrors surrounding the active area
(11) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
(12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
(13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

5.12 Window Characteristics

PARAMETER		MIN	NOM	MAX
Window material			Corning Eagle XG	
Window refractive index	at wavelength 546.1nm		1.5119	
Window aperture [(1)]				
Illumination overfill			See Section 6.5	

(1) See the mechanical package ICD for details regarding the size and location of the window aperture.

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP391TP DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

6 Detailed Description

6.1 Overview

The DLP391TP digital micromirror device (DMD) is a 0.39" diagonal spatial light modulator that consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors, combined with advanced DLP image processing algorithms, enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed. The electrical interface is low-voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the Section 6.2. The deflection of the micromirrors (positive or negative) is individually controlled by changing the address voltage of the underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.39" 4K UHD chipset is comprised of the DLP391TP DMD, DLPC8445V display controller, and the DLPA3085 / DLPA3082 PMIC and the LED driver. For reliable operation, the DLP391TP DMD must always be used with the DLP display controller and the PMIC specified in the chipset.

6.2 Functional Block Diagram

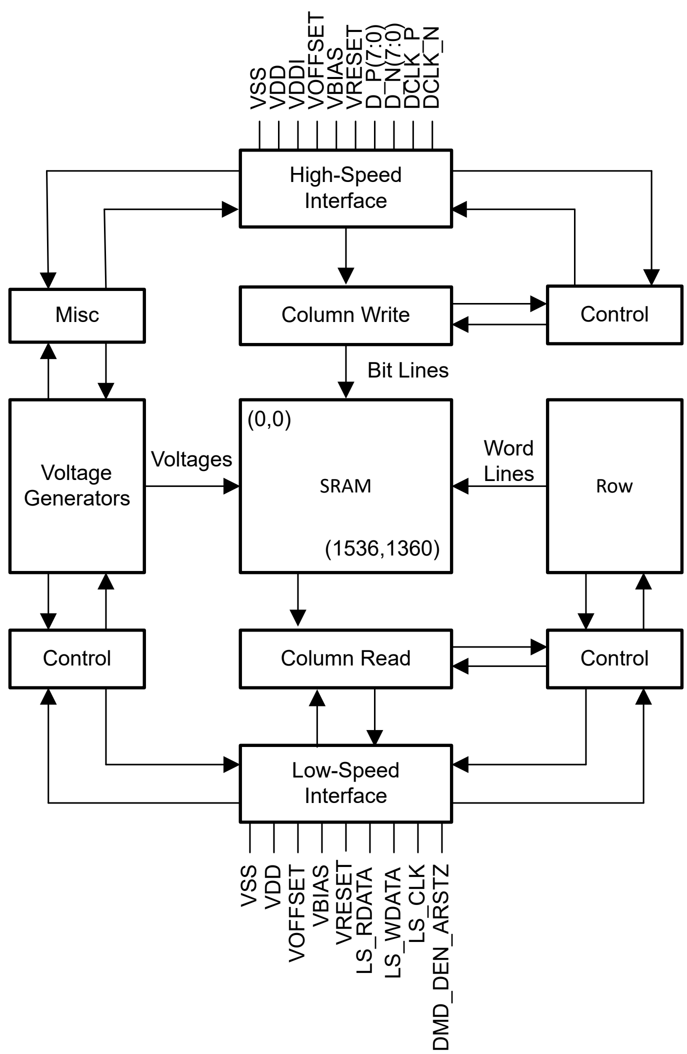


Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Power Interface

The DMD requires four DC voltages: 1.8V source (for V_{DD} and V_{DDI}), V_{OFFSET}, V_{RESET}, and V_{BIAS}. In a typical LED-based system, 1.8V, V_{OFFSET}, V_{RESET}, and V_{BIAS} are managed by the DLPA3085 / DLPA3082 PMIC and LED driver.

6.3.2 LPSDR Low-Speed Interface

The low-speed interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low-speed clock, and LS_WDATA is the low-speed data input.

6.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high-speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

6.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and their transmission line effects must be considered. Figure 5-14 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for the characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC8445V display controller. See the DLPC8445V display controller data sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trade-offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance are contingent on compliance with the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines the DMD's capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD, such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and active area could occur.

6.5.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, the overfill light on the window aperture may have to be further reduced below the suggested maximum 10% level in order to be acceptable.

6.6 Micromirror Array Temperature Calculation

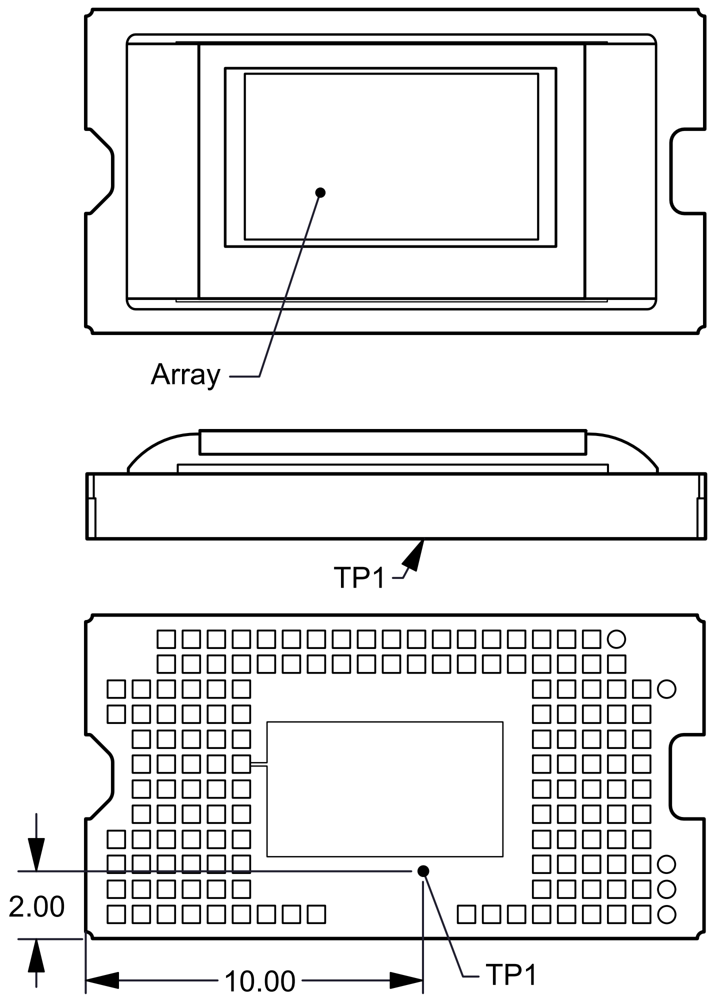


Figure 6-2. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore, it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in Figure 6-2) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of the package specified in Section 5.5 from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total (electrical + absorbed) DMD power on the array (Watts)
- $Q_{ELECTRICAL}$ = Nominal electrical power (Watts)
- $Q_{INCIDENT}$ = Incident illumination optical power (Watts)
- DMD average thermal absorptivity = 0.54
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (Watts)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.5W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single-chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the active array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 12.1W \text{ (measured)} \quad (1)$$

$$T_{CERAMIC} = 53.0°C \text{ (measured)} \quad (2)$$

$$Q_{ELECTRICAL} = 0.5W \quad (3)$$

$$Q_{ARRAY} = 0.5W + (0.54 \times 12.1W) = 7.034W \quad (4)$$

$$T_{ARRAY} = 53.0°C + (7.034W \times 2.3°C/W) = 69.2°C \quad (5)$$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000mW/W \div A_{ILL}$ (mW/cm^2)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000mW/W \div A_{ILL}$ (mW/cm^2)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)

- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm ^{2}) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR\text{-}RATIO}$ = ratio of the optical power for wavelengths >800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤475nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤445nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values, the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$Q_{INCIDENT}$ = 12.1W (measured)

A_{ARRAY} = ((8.7072mm × 4.9184mm) ÷ 100mm^2/cm^2) = 0.4283cm^2 (data sheet)

OV_{ILL} = 16.3% (optical model)

$OP_{UV\text{-}RATIO}$ = 0.00021 (spectral measurement)

$OP_{VIS\text{-}RATIO}$ = 0.99977 (spectral measurement)

$OP_{IR\text{-}RATIO}$ = 0.00002 (spectral measurement)

$OP_{BLU\text{-}RATIO}$ = 0.28100 (spectral measurement)

$OP_{BLU1\text{-}RATIO}$ = 0.03200 (spectral measurement)

A_{ILL} = 0.4283cm^2 ÷ (1 - 0.163) = 0.5117cm^2

ILL_{UV} = [0.00021 × 12.1W] × 1000 ÷ 0.5117cm^2 = 4.966mW/cm^2

ILL_{VIS} = [0.99977 × 12.1W] ÷ 0.5117cm^2 = 23.64W/cm^2

ILL_{IR} = [0.00002 × 12.1W] × 1000 ÷ 0.5117cm^2 = 0.473mW/cm^2

ILL_{BLU} = [0.28100 × 12.1W] ÷ 0.5117cm^2 = 6.64W/cm^2

ILL_{BLU1} = [0.03200 × 12.1W] ÷ 0.5117cm^2 = 0.757W/cm^2

6.8 Window Aperture Illumination Overfill Calculation

The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array, the amount is determined using the total measured incident optical power on the DMD, and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percentage of optical power on the window aperture critical area and estimate the size of the area.

- $Q_{AP\text{-}ILL}$ = [$Q_{INCIDENT}$ × $OP_{AP\_ILL\_RATIO}$] ÷ A_{AP_ILL} (W/cm^2)

where:

- $Q_{AP\text{-}ILL}$ = window aperture illumination overfill (W/cm^2)
- $Q_{INCIDENT}$ = total incident optical power on the DMD (Watts) (measured)
- $OP_{AP\_ILL\_RATIO}$ = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)
- $A_{AP\text{-}ILL}$ = size of the window aperture critical area (cm^2) (data sheet)
- OP_{CA_RATIO} = percent of the window aperture critical area with incident optical power (%) (optical model)

Sample calculation:

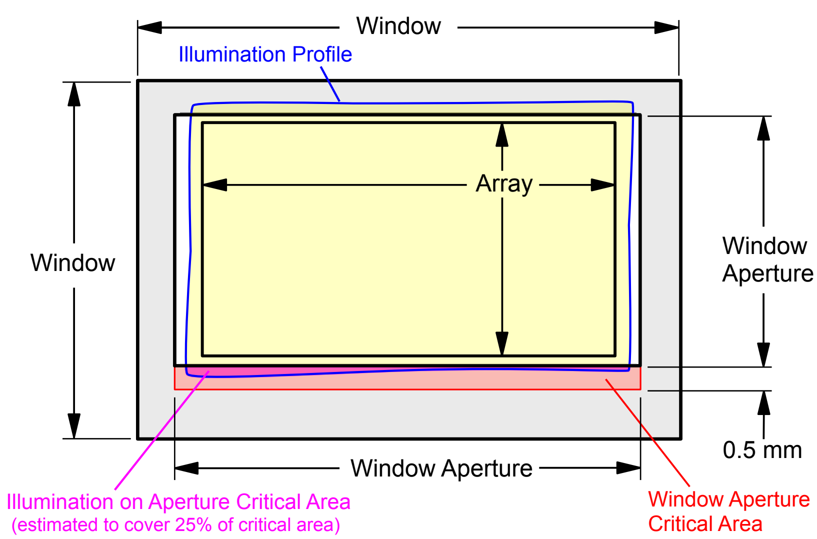


Figure 6-3. Window Aperture Overfill Example

See the above figure for the length of the critical aperture.

$$Q_{INCIDENT} = 12.1\text{W (measured)} \quad (6)$$

$$OP_{AP\_ILL\_RATIO} = 0.312\% \text{ (optical model)} \quad (7)$$

$$OV_{CA\_RATIO} = 25\% \text{ (optical model)} \quad (8)$$

Length of the window aperture for critical area = 0.9802cm (data sheet) (9)

Width of critical area = 0.050 cm (data sheet) (10)

$A_{AP\text{-}ILL}$ = 0.9802cm × 0.050 cm = 0.04901cm^2 (11)

$Q_{AP\text{-}ILL}$ = (12.1W × 0.00312) ÷ (0.04901cm^2 × 0.25) = 3.08W/cm^2 (W/cm^2) (12)

6.9 Micromirror Landed-On/Landed-Off Duty Cycle

6.9.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Because a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.9.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical, whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.9.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD's useful life. This is quantified in the derating curve shown in the *Recommended Operating Conditions*. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent a lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent a higher useful life (and the further away from the curve, the higher the useful life).

This curve specifies the maximum operating DMD temperature that the DMD should be operated at for a given long-term average landed duty cycle.

6.9.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring, for the moment, color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the grayscale value, as shown in Table 6-1.

Table 6-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use Equation 13 to calculate the landed duty cycle of a given pixel during a given time period.

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \tag{13}$$

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point.
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point.
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point.

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20%, respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in Table 6-2 and Table 6-3.

Table 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
GREEN	BLUE	RED
50%	20%	30%

Table 6-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
GREEN	BLUE	RED	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80

Table 6-3. Example Landed Duty Cycle for Full-Color (continued)

SCALE VALUE			LANDED DUTY CYCLE
GREEN	BLUE	RED	
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form $\text{Output\_Level} = A \times \text{Input\_Level}^{\text{Gamma}}$, where A is a scaling factor that is typically set to 1.

In the controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 6-4.

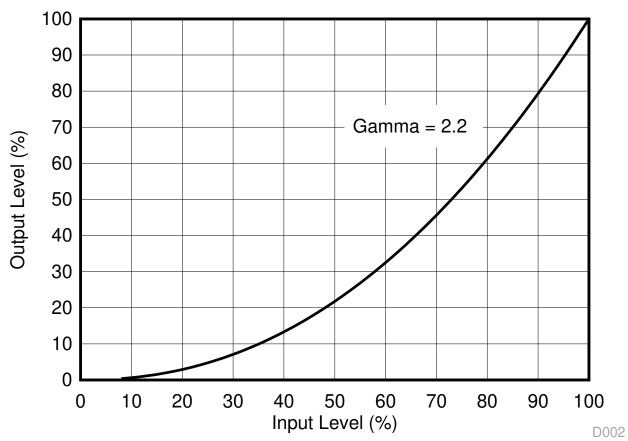


Figure 6-4. Example of Gamma = 2.2

From Figure 6-4, if the grayscale value of a given input pixel is 40% (before gamma is applied), then the grayscale value will be 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact on the displayed grayscale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing that occurs before the controller.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

DMDs are spatial light modulators that reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC8445V controller. The high tilt pixel in the bottom-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness-constrained applications. Typical applications using the DLP391TP include mobile smart TVs and digital signage.

DMD power-up and power-down sequencing is strictly controlled by the DLPA3085 / DLPA3082 . Refer to the *Power Supply Recommendations* for power-up and power-down specifications. For reliable operation, the DLP391TP DMD must always be used with the DLPC8445V controller and a DLPA3085 / DLPA3082 PMIC.

7.2 Typical Application

The DLP391TP DMD, combined with DLPC8445V digital controller and a power management device, provides full 4K UHD resolution for bright, colorful display applications. See Figure 7-1, which shows the system components needed along with the LED configuration of the DLP 0.39" 4K UHD chipset. The components include the DLP391TP DMD, the DLPC8445V display controller, and the DLPA3085 / DLPA3082 PMIC and LED driver.

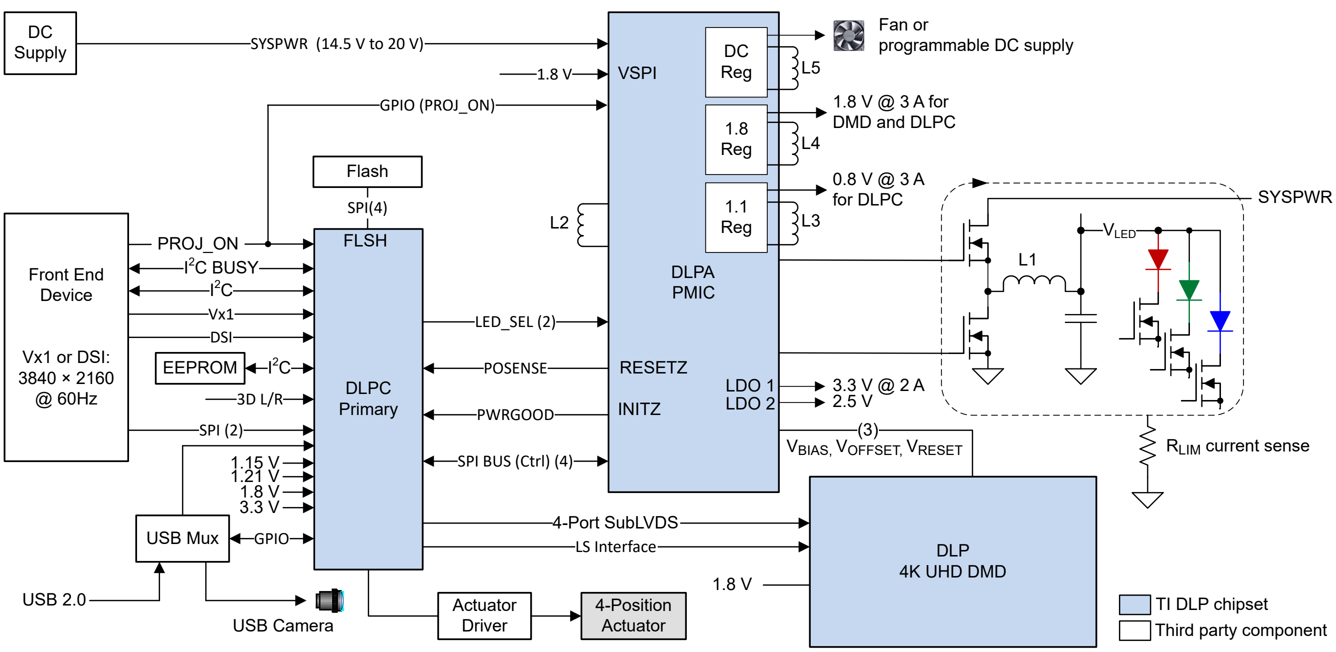


Figure 7-1. Typical 4K UHD LED Application Diagram

7.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and the desired brightness have a major effect on the overall system design and size.

The display system uses the DLP391TP as the core imaging device and contains a 0.39" array of micromirrors. The DLPC8445V controller is the digital interface between the DMD and the rest of the system, taking digital input from the front-end receiver and driving the DMD over a high-speed interface. The DLPA3085 / DLPA3082 PMIC serves as a voltage regulator for the DMD, controller, and LED illumination functionality.

7.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP391TP DMD, associated illumination sources, optical elements, and necessary mechanical components.

For reliable operation, use the DMD with the DLPC8445V display controller and the DLPA3085 / DLPA3082 PMIC driver.

7.2.3 Application Curve

The typical LED-current-to-luminance relationship when LED illumination is used is shown in Figure 7-2.

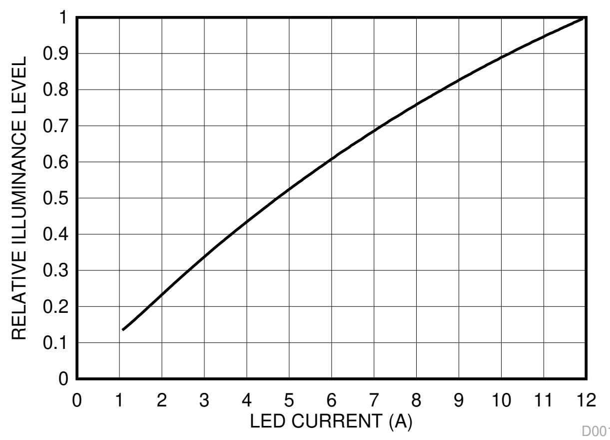


Figure 7-2. Luminance vs Current

7.3 Temperature Sensor Diode

The software application provides functions to configure the TMP411 to read the DLP391TP DMD temperature sensor diode. Use this data to incorporate additional functionality in the overall system design, such as adjusting illumination, fan speeds, and so on. All communication between the TMP411 and the DLPC8445V controller is completed using the I^2C interface. The TMP411 connects to the DMD through the pins outlined in Section 4.

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{DDA}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in Figure 8-1.

V_{BIAS}, V_{DD}, V_{DDA}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

Table 8-1. DMD Power Supply Sequence Requirements

SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DELAY1} (1)	Power up delay requirement	from V_{OFFSET} settled at recommended operating voltage to V_{BIAS} and V_{RESET} power up	2			ms
t_{DELAY2} (1)	Power down delay requirement	Delay V_{DD} must be held high from V_{OFFSET}, V_{BIAS} and V_{RESET} powering down.	50			us
V_{OFFSET}	Supply voltage level	at beginning of power-up sequence delay			6	V
V_{BIAS}	Supply voltage level	at end of power-up sequence delay			6	V

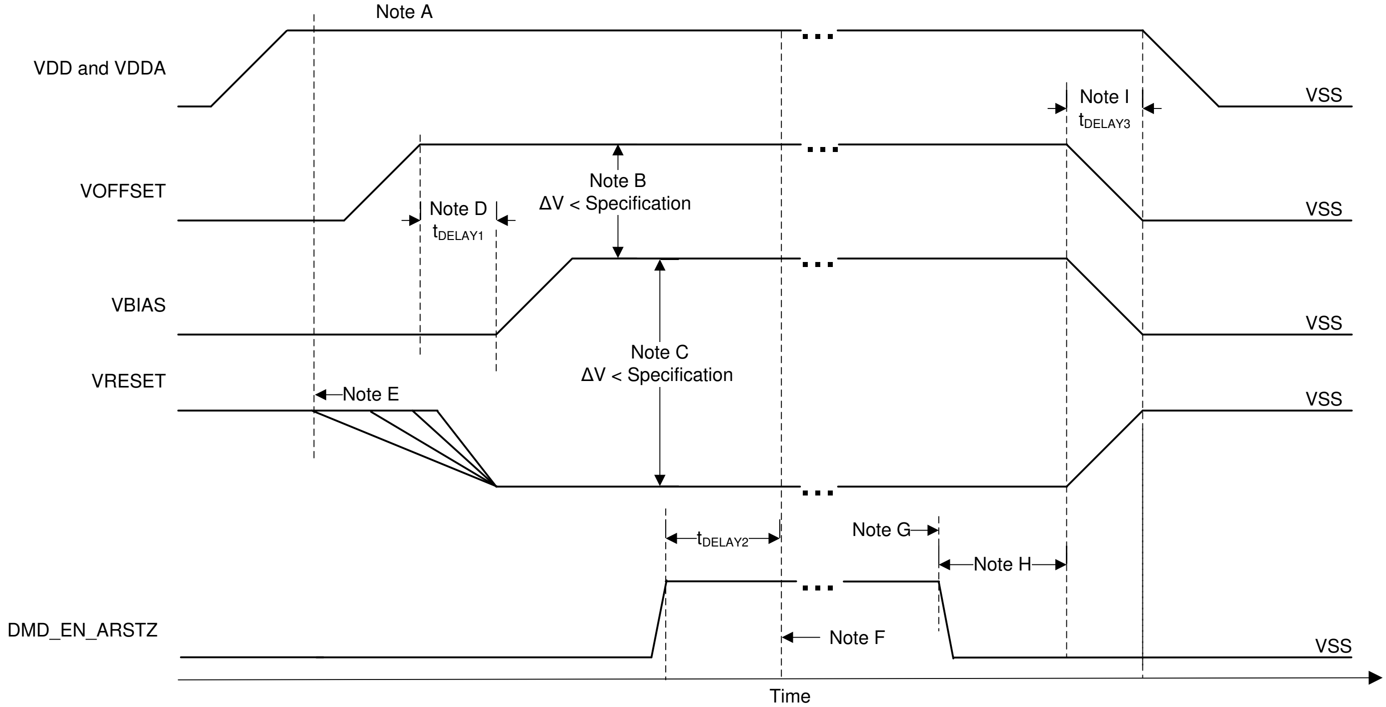
(1) See Figure 8-1.

8.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDA} must always start and settle before V_{OFFSET} plus Delay1, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in the Section 5.4.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in Section 5.1, Section 5.4, and in Figure 8-1.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} have settled at the operating voltages listed in *Recommended Operating Conditions*.

8.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} and V_{DDA} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in Section 5.4.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in the Section 5.1, Section 5.4, and Figure 8-1.
- During power-down, LVCMOS input pins must be less than specified in the Section 5.4.



A. See Section 4 for the *Pin Functions Table*.
B. To prevent excess current, the supply voltage difference $|V_{OFFSET} – V_{BIAS}|$ must be less than the specified limit in the Section 5.4.
C. To prevent excess current, the supply difference $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit in Section 5.4.
D. V_{BIAS} should power up after V_{OFFSET} has powered up, per the Delay1 specification.
E. DLP controller software initiates the global V_{BIAS} command.
F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS}, V_{RESET}, and V_{OFFSET}.
G. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, DMD_EN_ARSTZ will go low.
H. V_{DD} must remain high until after V_{OFFSET}, V_{BIAS}, V_{RESET} go low, per Delay2 specification.
I. To prevent excess current, the supply voltage delta $|V_{DDA} – V_{DD}|$ must be less than the specified limit in Section 5.4.

Figure 8-1. DMD Power Supply Requirements

9 Layout

9.1 Layout Guidelines

The DLP391TP DMD connects to a PCB or a flex circuit using an interposer. For additional layout guidelines regarding length matching and impedance, see the DLPC8445V controller data sheet. For a detailed layout example, refer to the layout design files. Some layout guidelines for routing to the DLP391TP DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals, as specified in the DLPC8445V controller data sheet.
- Match lengths for the HS_bus differential signals as specified in the DLPC8445V controller data sheet.
- Minimize vias, layer changes, and turns for the HS bus signals.
- Supply capacitance needs can vary per design. Refer to the layout design file for a general guideline. Verify all supplies on the design are operating in the recommended operating range at the DMD.

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

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10.2 Device Support

10.2.1 Device Nomenclature

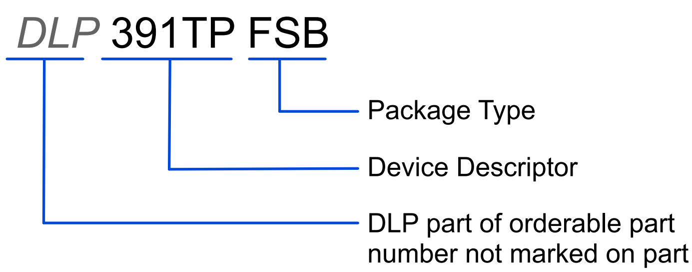

Figure 10-1. Part Number Description

10.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 10-2 and includes the legible character string GHJJJJK DLP391TPFSB. GHJJJJK is the lot trace code, and DLP391TPFSB is the device marking.

Example: GHJJJJK DLP391TPFSB

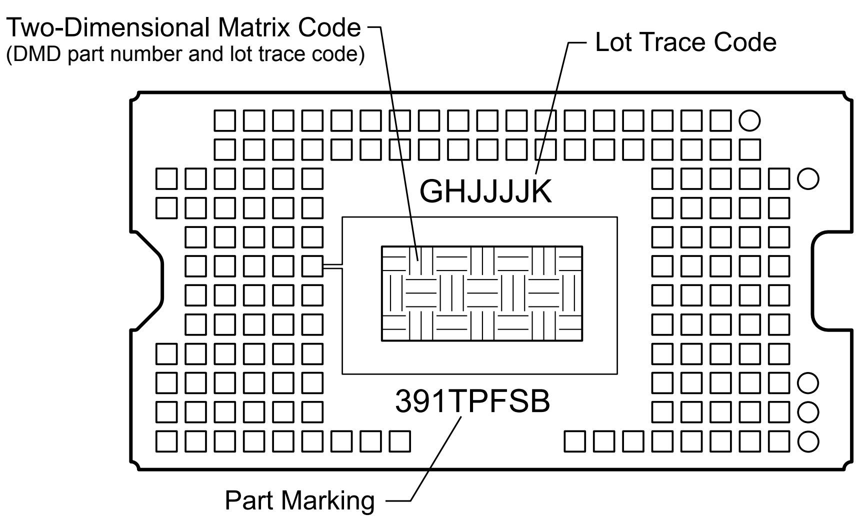

Figure 10-2. DMD Marking Locations

10.3 Documentation Support

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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DLP® is a registered trademark of Texas Instruments.
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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	A	Changed the document status From: *Advance Information* To: *Production Data*

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP391TPFSB	Active	Production	CLGA (FSB) | 154	96 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 70	
XDLP391TPFSB.B	Active	Preproduction	CLGA (FSB) | 154	96 | JEDEC TRAY (5+1)	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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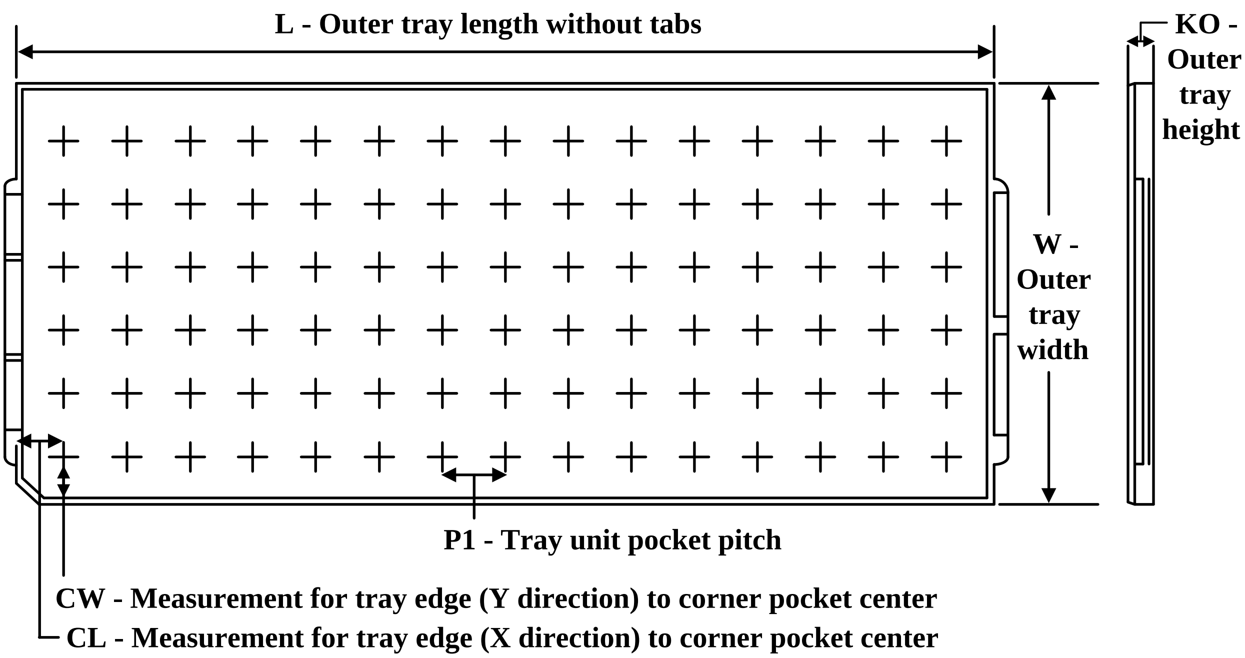
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP391TPFSB	FSB	CLGA	154	96	8 x 12	150	315	135.9	12190	23	31	15.45

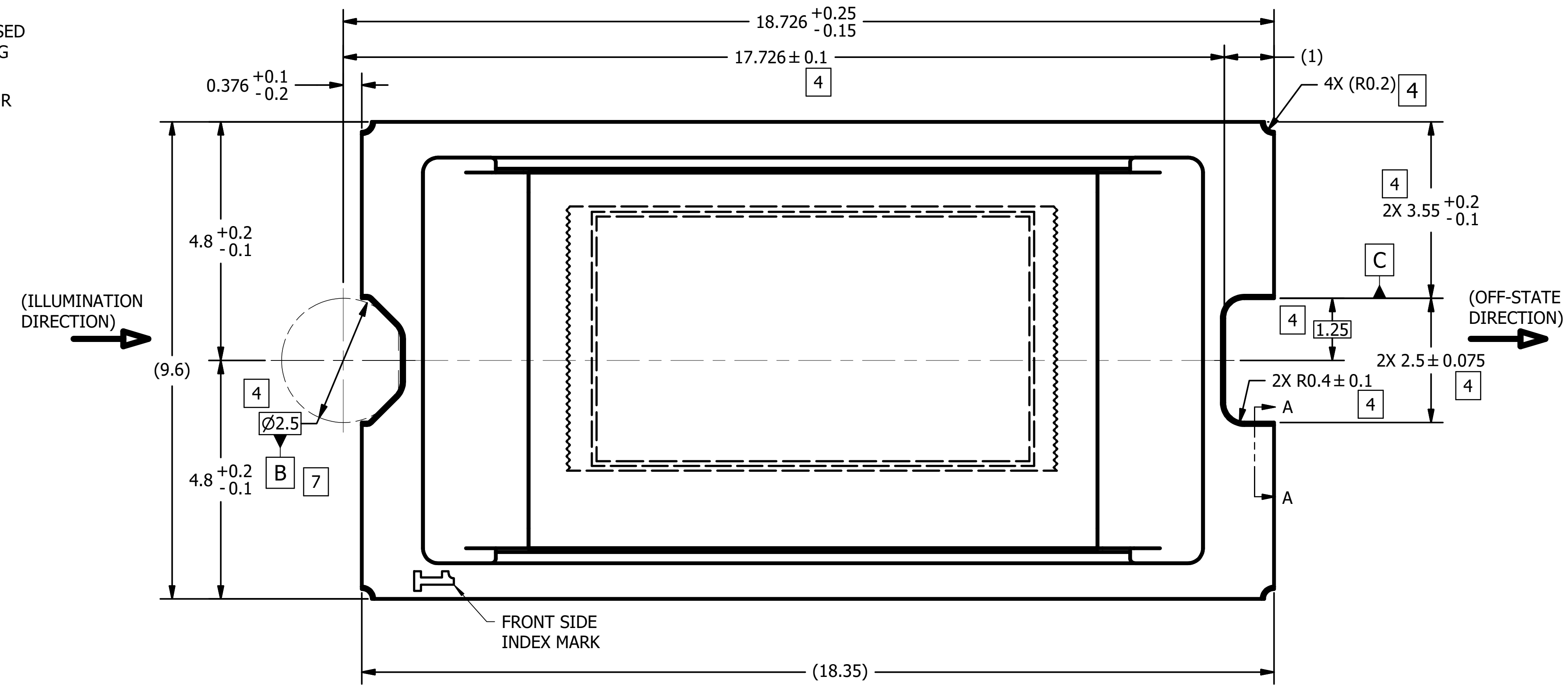
DWG NO. 2519203 SH 1

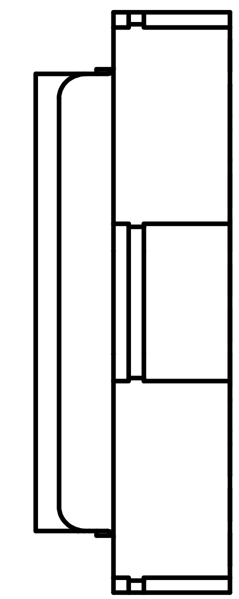
REVISIONS

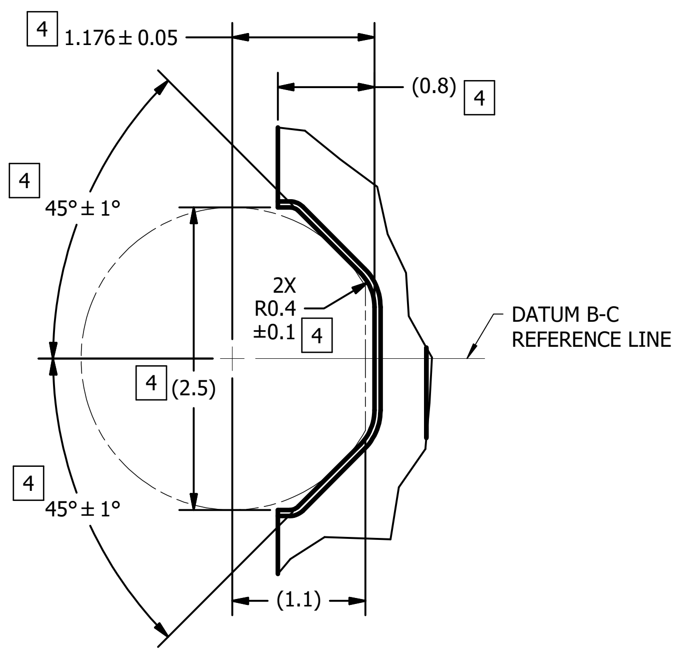
REV	DESCRIPTION	DATE	BY
A	ECO 2209009: INITIAL RELEASE	6/19/2024	BMH

NOTES UNLESS OTHERWISE SPECIFIED:

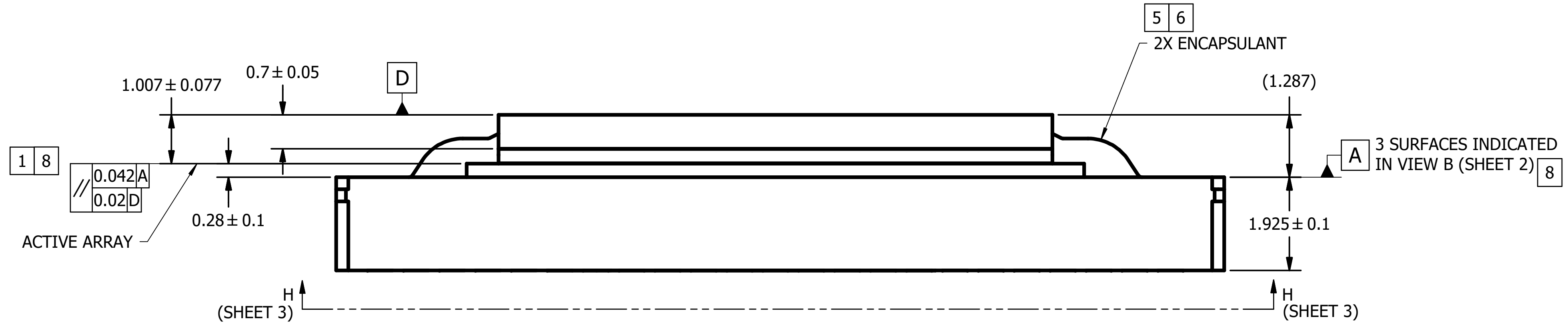
1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY SECOND LAYER OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW D (SHEET 3). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. SEE DETAIL B FOR "V-NOTCH" DIMENSIONS.
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.
9. SHORTING TEST PADS AND SYMBOLIZATION PAD TO EACH OTHER AND/OR TO VSS IS ACCEPTABLE.

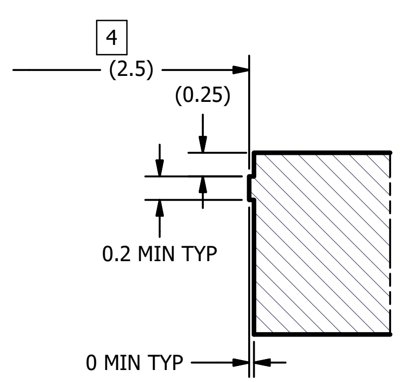






DETAIL B
V-NOTCH
SCALE 32 : 1





SECTION A-A
NOTCH OFFSETS
SCALE 25 : 1
(ROTATED 90°)

	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

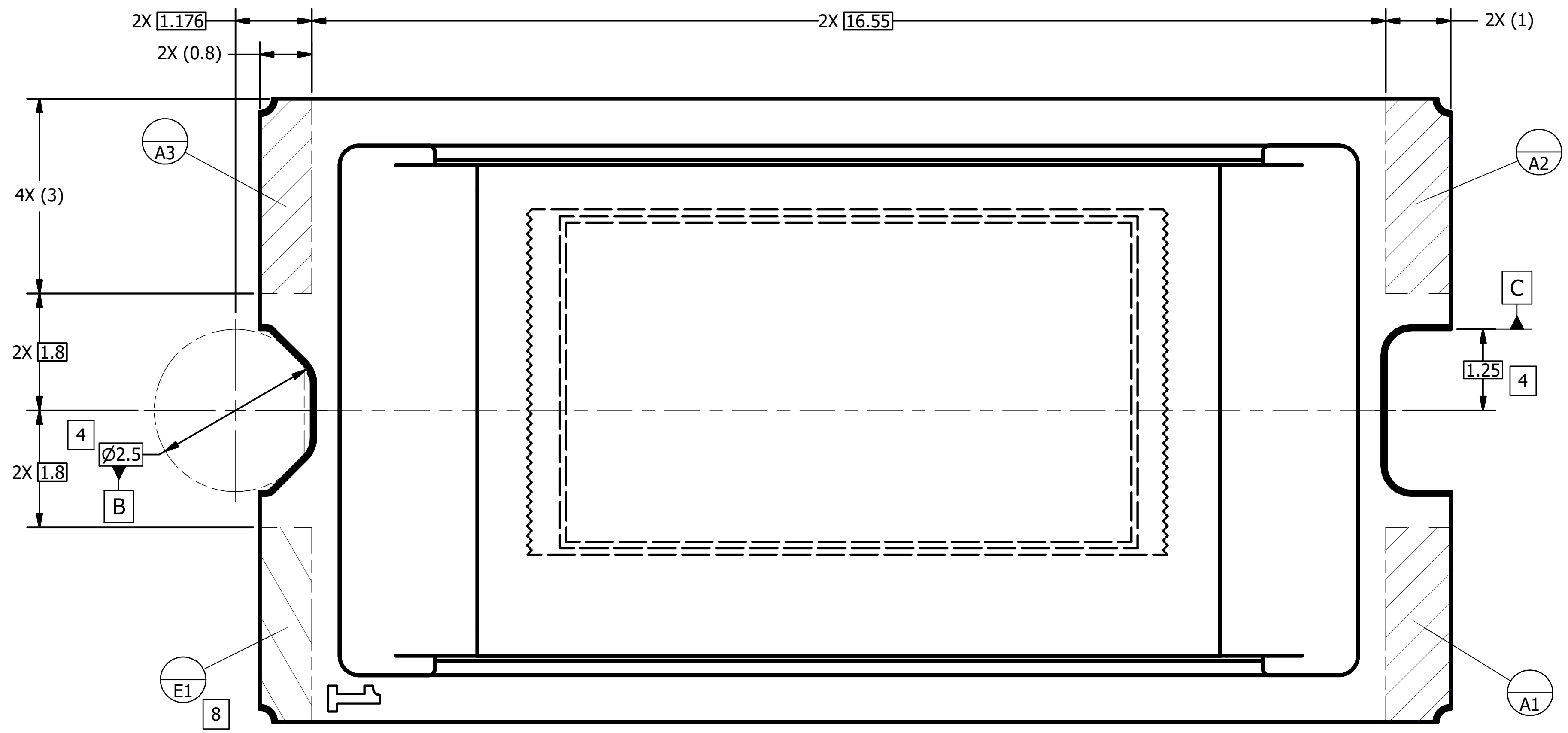
	NAME	DATE
DRAWN	B. HASKETT	6/19/2024
ENGINEER	B. HASKETT	6/19/2024
QA/CE	P. KONRAD	6/20/2024
CM	J. McKINLEY	6/24/2024
APPROVED	M. GARCIA	6/26/2024

TEXAS INSTRUMENTS
Dallas Texas

TITLE ICD, MECHANICAL, DMD, .39 4K SERIES 323 (FSB PACKAGE)

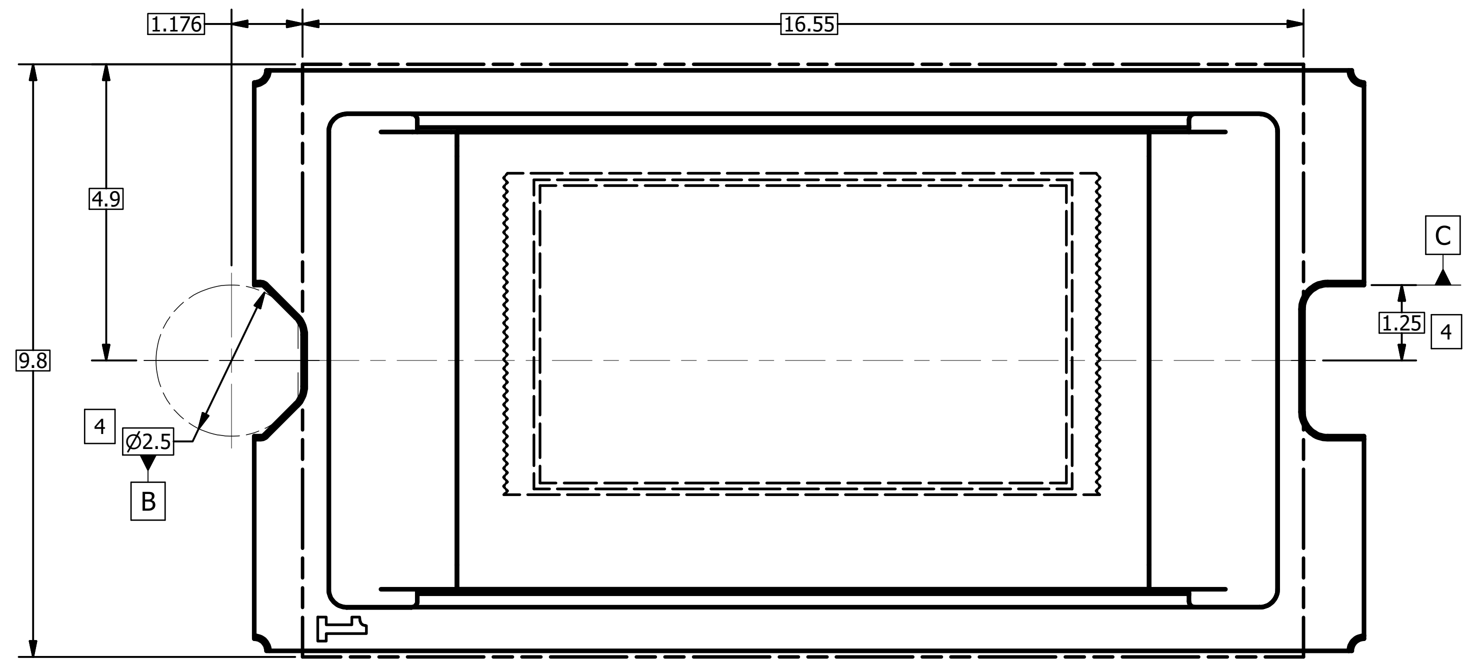
SIZE D | DWG NO 2519203 | REV A
SCALE 16:1 | SHEET 1 OF 5

INV11-2006a

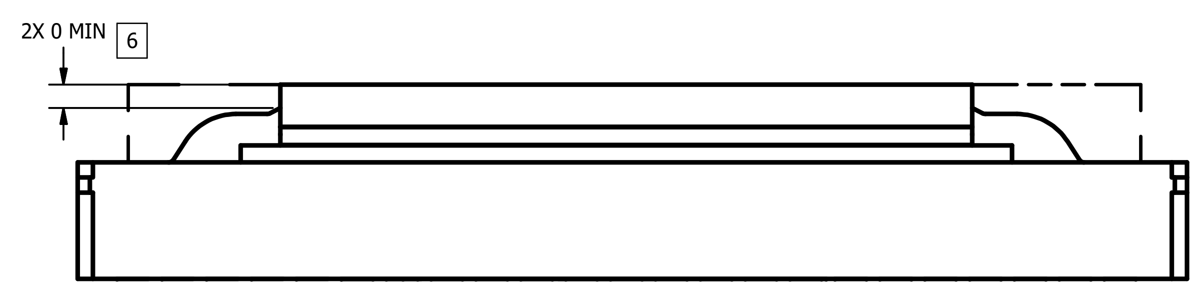


VIEW C
DATUMS A AND E
SCALE 20 : 1
(FROM SHEET 1)

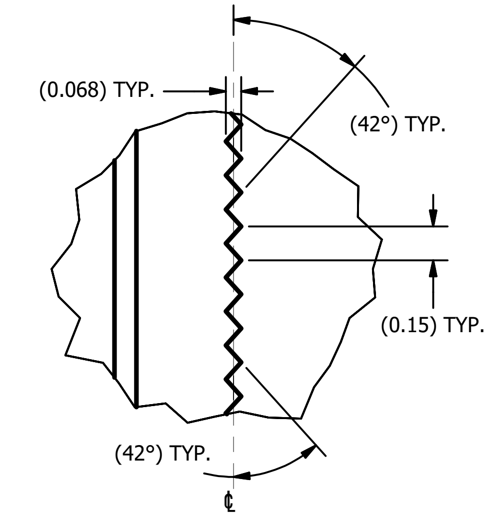
TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 6/19/2024	SIZE D	DWG NO 2519203	REV A
			SCALE		SHEET 2 OF 5



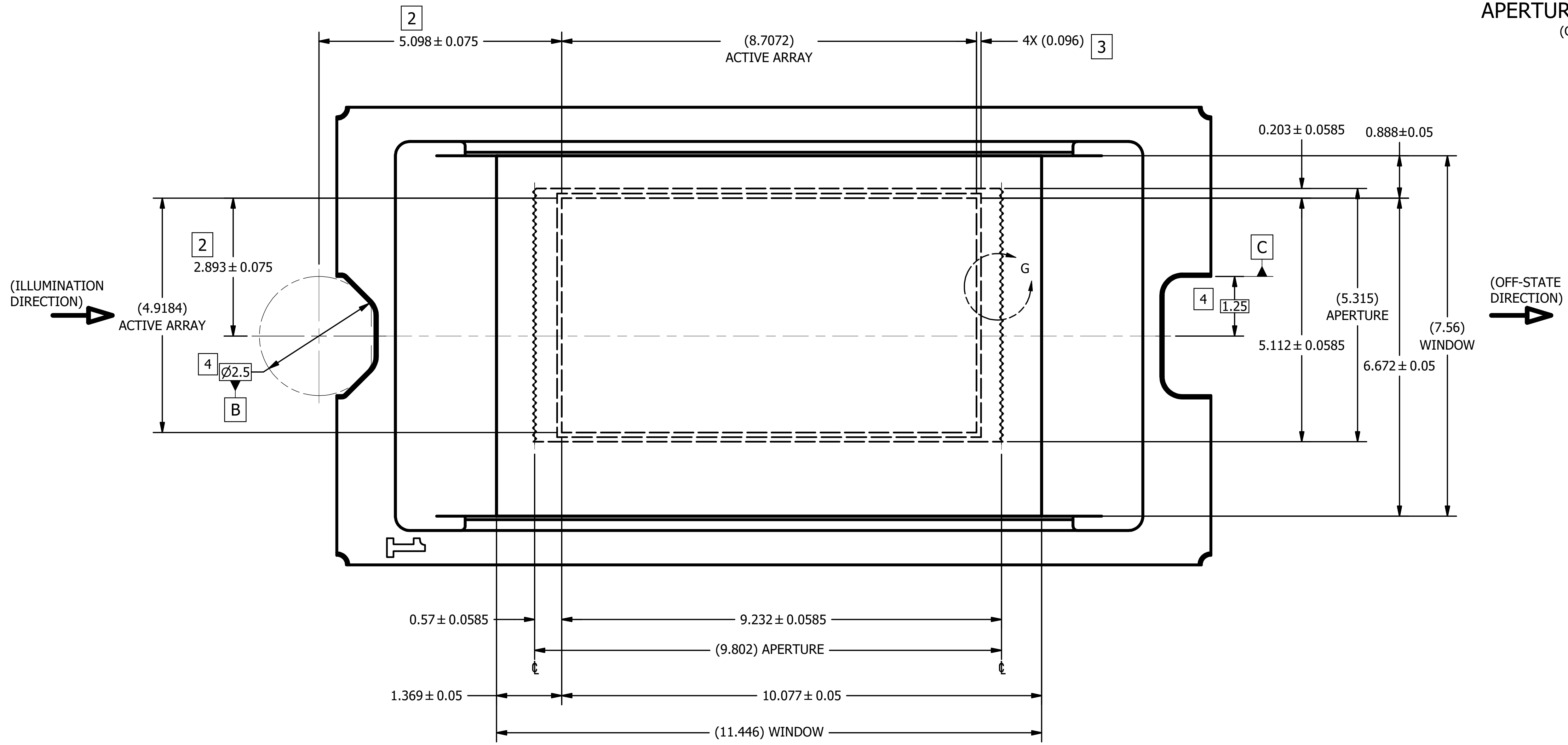
VIEW D
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
(FROM SHEET 1)



VIEW E
ENCAPSULANT MAXIMUM HEIGHT

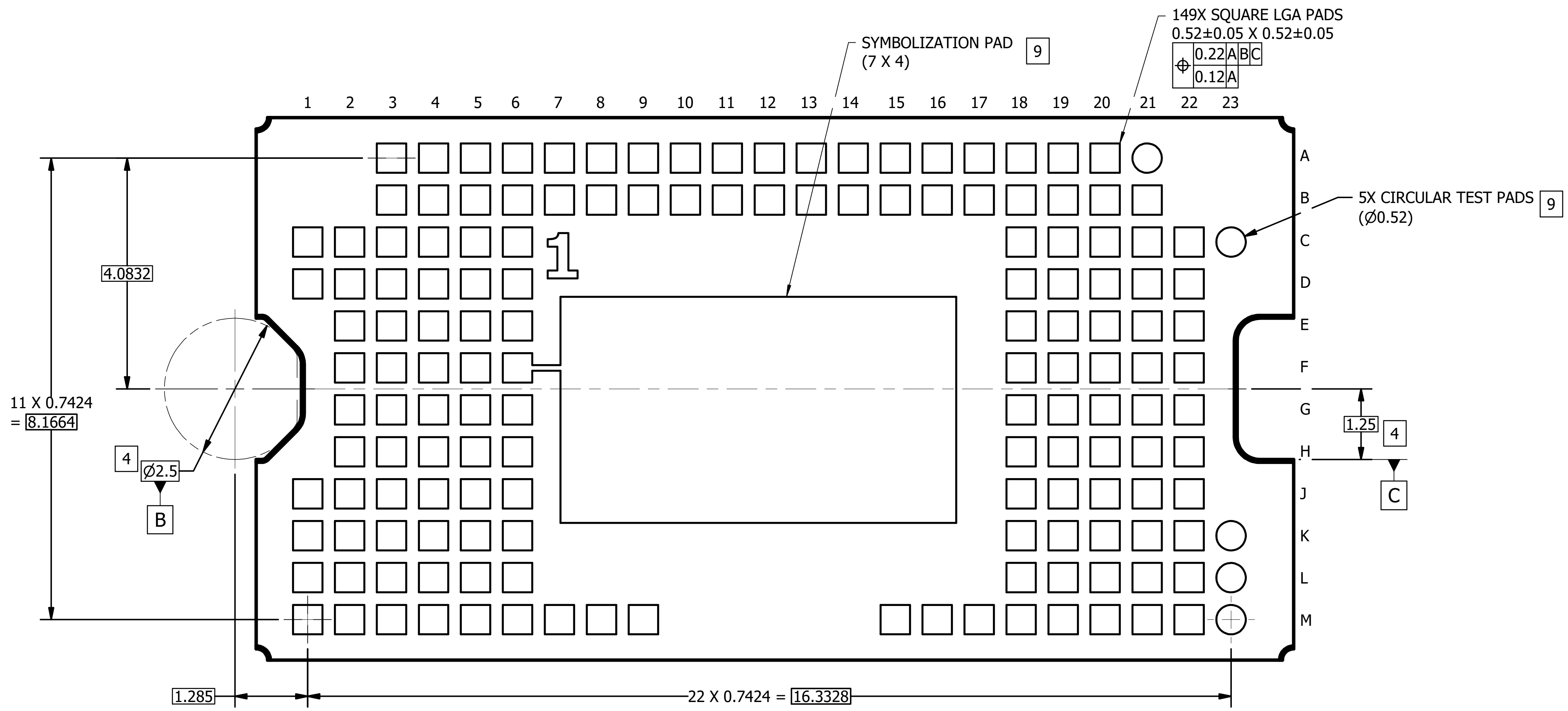


DETAIL G
APERTURE LEFT AND RIGHT EDGES
(GLASS OMITTED FOR CLARITY)
SCALE 60 : 1



VIEW F
WINDOW AND ACTIVE ARRAY
SCALE 20 : 1
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 6/19/2024	SIZE D	DWG NO 2519203	REV A
			SCALE	SHEET 4 OF 5	



VIEW H-H
BACK SIDE METALLIZATION
SCALE 20 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 6/19/2024	SIZE D	DWG NO 2519203	REV A
			SCALE	SHEET 5 OF 5	