ISOUSB211-Q1 High/Full/Low Speed Isolated USB Repeater

1 Features

- Compliant to USB 2.0
- Supports low speed (1.5Mbps), full speed (12Mbps), and high speed (480Mbps) signaling
- Does not need external crystal or clock input
- Automatic speed and connection detection
- Supports L1 (sleep) and L2 (suspend) low-power states
- Programmable equalization to compensate board trace loss in high speed mode
- CDP advertising on downstream side
- Supply OK indication on opposite side
- Supports automatic role reversal for USB On-The-Go (OTG) and Type-C™ Dual Role Port (DRP) designs
- High CMTI: 100kV/µs
- ±8kV IEC 61000-4-2 contact discharge protection across isolation barrier
- V_{BUS} voltage range: 4.25V to 5.5V
  - 3.3V and 1.8V internal LDOs
- Meets CISPR32 class B emissions limits
- Ambient temperature range: –40°C to +125°C
- Small footprint 28-SSOP package
- Safety-related certifications:
  - 7071V_{PK} V_{IOTM} and 2121V_{PK} V_{IORM} (Reinforced) per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5700V_{RMS} isolation for 1 minute per UL 1577
  - IEC 62368-1, IEC 60601-1 and IEC 61010-1 certifications
  - CQC, TUV and CSA certifications

2 Applications

- USB Hub, Host, Peripheral and Cable Isolation
- Medical and healthcare
- Factory automation
- Motor drives
- Grid infrastructure
- Power delivery
- USB Audio

Reinforced Isolation Option

FEATURE	ISOUSB211-Q1
Protection Level	Reinforced
Surge Isolation Voltage	12800V_{PK}
Isolation Rating	5700V_{RMS}
Isolation Working Voltage	1500V_{RMS} / 2121V_{PK}

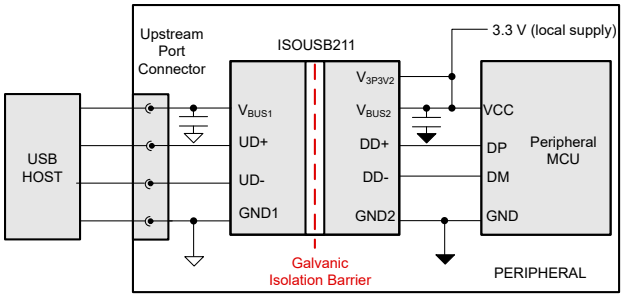
3 Description

ISOUSB211-Q1 is a galvanically-isolated USB 2.0 compliant repeater supporting low speed (1.5Mbps), full speed (12Mbps) and high speed (480Mbps) signaling rates. The device supports automatic connect and speed detection, reflection of pullups/ pulldowns, and link power management, allowing drop-in USB hub, host, peripheral, and cable isolation. The device also supports automatic role reversal. If, after disconnect, a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. This feature enables the device to support USB On-The-Go (OTG) and Type-C Dual Role Port (DRP) implementations. The ISOUSB211-Q1 has inbuilt programmable equalization to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates. This device uses a silicon dioxide (SiO_2) insulation barrier with a withstand voltage of up to 5700V_{RMS} and a working voltage of 1500V_{RMS}. Used in conjunction with isolated power supplies, the device protects against high voltage and prevents noise currents from the bus from entering the local ground. The ISOUSB211-Q1 device is available for reinforced isolation. The device supports a wide ambient temperature range of –40°C to +125°C. The device is available in the small foot-print SSOP-28 (28-DP) package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ISOUSB211-Q1	DP (SSOP, 28)	10.30mm × 7.50mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Diagram

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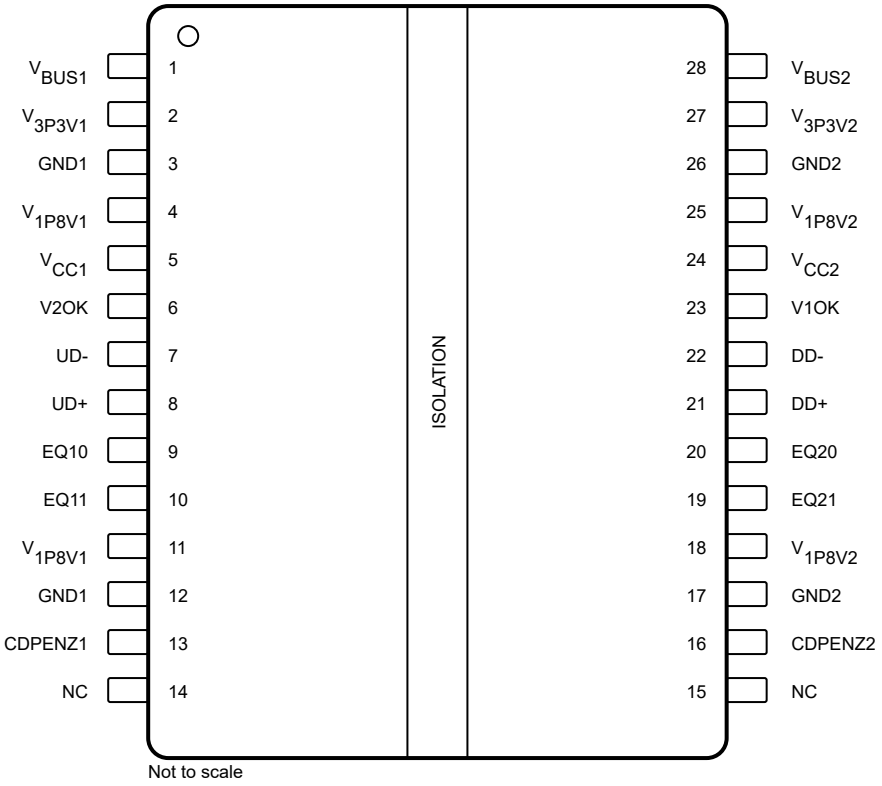
4 Pin Configuration and Functions



Not to scale

Figure 4-1. DP Package 28-Pin SSOP Top View

Table 4-1. Pin Functions—28 Pins

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	V_{BUS1}	—	Input Power Supply for Side 1. If a 4.25V to 5.5V (example USB power bus) supply is available, connect the supply to V_{BUS1}. In this case, an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3V power supply.
2	V_{3P3V1}	—	Power Supply for Side 1. If a 4.25V to 5.5V supply is connected to V_{BUS1} connect a bypass capacitor between V_{3P3V1} and GND1. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3V power supply.
3	GND1	—	Ground 1. Ground reference for Isolator Side 1.
4	V_{1P8V1}	—	Power Supply for Side 1. If a 2.4V to 5.5V supply is connected to V_{CC1} connect a bypass capacitor between V_{1P8V1} and GND1. In this case an internal LDO generates V_{1P8V1}. Else, connect V_{CC1} and V_{1P8V1} to an external 1.8V power supply.
5	V_{CC1}	—	Input Power Supply for Side 1. If a 2.4V to 5.5V (example USB power bus, or a DC/DC supply derived from USB power bus) supply is available, connect the supply to V_{CC1}. In this case an internal LDO generates V_{1P8V1}. Else, connect V_{CC1} and V_{1P8V1} to an external 1.8V power supply.
6	V2OK	O	High level on this pin indicates that side 2 is powered up.
7	UD-	I/O	Upstream facing port D-.
8	UD+	I/O	Upstream facing port D+.
9	EQ10	I	Equalization setting for Side 1, LSB. Logic Input.
10	EQ11	I	Equalization setting for Side 1, MSB. Logic Input.
11	V_{1P8V1}	—	Connect pin 11 to pin 4, with local bypass capacitors near pin 11.
12	GND1	—	Ground 1. Ground reference for Isolator Side 1.
13	CDPENZ1	I	Active low signal. Enables CDP advertising on UD+/UD- pins.
14	NC	—	Leave floating or connect to V_{3P3V1}.

Table 4-1. Pin Functions—28 Pins (continued)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
15	NC	—	Leave floating or connect to V_{3P3V2}.
16	CDPENZ2	I	Active low signal. Enables CDP advertising on DD+/DD- pins.
17	GND2	—	Ground 2. Ground reference for Isolator Side 2.
18	V_{1P8V2}	—	Connect pin 18 to pin 25, with local bypass capacitors near pin 18.
19	EQ21	I	Equalization setting for Side 2, MSB. Logic Input.
20	EQ20	I	Equalization setting for Side 2, LSB. Logic Input.
21	DD+	I/O	Downstream facing port D+.
22	DD-	I/O	Downstream facing port D-.
23	V1OK	O	High level on this pin indicates that side 1 is powered up.
24	V_{CC2}	—	Input Power Supply for Side 2. If a 2.4V to 5.5V (example USB power bus, or a DC/DC supply derived from USB power bus) supply is available, connect the supply to V_{CC2}. In this case, an internal LDO generates V_{1P8V2}. Else, connect V_{CC2} and V_{1P8V2} to an external 1.8V power supply.
25	V_{1P8V2}	—	Power Supply for Side 1. If a 2.4V to 5.5V supply is connected to V_{CC2}, connect a bypass capacitor between V_{1P8V2} and GND2. In this case, an internal LDO generates V_{1P8V2}. Else, connect V_{CC2} and V_{1P8V2} to an external 1.8V power supply.
26	GND2	—	Ground 2. Ground reference for Isolator Side 2.
27	V_{3P3V2}	—	Power Supply for Side 2. If a 4.25V to 5.5V supply is connected to V_{BUS2} connect a bypass capacitor between V_{3P3V2} and GND1. In this case, an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3V power supply.
28	V_{BUS2}	—	Input Power Supply for Side 2. If a 4.25V to 5.5V (example USB power bus) supply is available, connect the supply to V_{BUS2}. In this case, an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3V power supply.

(1) I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{BUS1}, V_{BUS2}	V_{BUS} supply voltage	-0.3	6	V
V_{CC1}, V_{CC2}	V_{CC} supply voltage	-0.3	6	V
V_{3P3V1}, V_{3P3V2}	3.3V input supply voltage	–0.3	4.25	V
V_{1P8V1}, V_{1P8V2}	1.8V input supply voltage	–0.3	2.1	V
V_{DPDM}	Voltage on bus pins (UD+, UD-, DD+, DD-) 1000 total number of short events and cumulative duration of 1000 hrs.	–0.3	6	V
V_{IO}	IO voltage range (V*OK, EQ*, CDPENZ*)	–0.3	V_{3P3Vx}+0.3(3)	V
I_O	Output current on output pins (V*OK)	-10	10	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 4.25V

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) (3)	UD and DD pins with respect to GND	±1500	V
			All other pins	±2000	
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) Pins UDP, UDM, DDP, and DDM are rated for 1500V HBM

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BUSx}	V_{BUS} input voltage (inclusive of any ripple)	4.25	5	5.5	V
V_{3P3Vx}	3.3V input supply voltage (inclusive of any ripple)	3.0	3.3	3.6	V
V_{CCx}	Input voltage to internal 1.8V LDO (inclusive of any ripple)	2.4	3	5.5	V
V_{1P8Vx}	1.8V input supply voltage (inclusive of any ripple)	1.71	1.8	1.94	V
T_A	Operating free-air temperature	–40		125	°C
T_J	Junction temperature	–55		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		ISOUSB211 DP (SSOP) 28 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	44.2	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	13.9	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	19.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.4	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISOUSB211						
P_D	Maximum power dissipation (both sides)	V_{BUS1} = V_{BUS2} = V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, R_L = 50Ω each on DD- and DD+ to GNDx, input a 240MHz 50% duty cycle a differential 0 to 400mV swing signal on UD- and UD+			1232	mW
P_{D1}	Maximum power dissipation (side-1)	V_{BUS1} = V_{BUS2} = V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, R_L = 50Ω each on DD- and DD+ to GNDx, input a 240MHz 50% duty cycle a differential 0 to 400mV swing signal on UD- and UD+			616	mW
P_{D2}	Maximum power dissipation (side-2)	V_{BUS1} = V_{BUS2} = V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, R_L = 50Ω each on DD- and DD+ to GNDx, input a 240MHz 50% duty cycle a differential 0 to 400mV swing signal on UD- and UD+			616	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS DP-28	UNIT
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	>8	mm
CPG	External Creepage(1)	Side 1 to side 2 distance across package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)	8000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50us waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge(5)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10s	≤ 5	
		Method b: At routine test (100% production); V_{ini} = 1.2 × V_{IOTM}, tini = 1s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 πft), f = 1MHz	1.2	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} , t = 60s (qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1s (100% production)	5700	V_{RMS}

(1) Care must be taken during board design so that the mounting pads of the isolator on the printed-circuit board (PCB) do not reduce creepage and clearance. Inserting grooves, ribs or both can help increase creepage distance on the PCB.
(2) ISOUSB211 is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Certificate number: 40040142	Master contract: 220991	File number: E181974	Certificate: CQC15001121716	Client ID: 77311

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DP-28 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 44.2°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			514	mA
		$R_{\theta JA}$ = 44.2°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			785	mA
		$R_{\theta JA}$ = 44.2°C/W, V_I = 1.94V, T_J = 150°C, T_A = 25°C			1457	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 44.2°C/W, T_J = 150°C, T_A = 25°C			2828	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

5.9 Electrical Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5V, V_{3P3Vx} = 3.3V, V_{1P8Vx} = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - High Speed (HS) mode	Receive side HS Active (240MHz signal rate), EQxx = 00, R_L = 45Ω to ground on D+ and D-		11.0	13.5	mA
		Transmit side HS Active (240MHz signal rate), EQxx = 00, R_L= 45Ω to ground on D+ and D-		10.5	13.5	mA
		HS Idle State, EQxx = 00, R_L = 45Ω to ground on D+ and D-		10.5	13.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - Full Speed (FS) and Low Speed (LS) modes	Receive side FS Active (6MHz signal rate), Figure 7-9, C_L = 50pF		12	15.3	mA
		Transmit side FS Active (6MHz signal rate), Figure 7-9, C_L = 50pF		9.5	13	mA
		Receive side LS Active (750kHz signal rate), Figure 7-10, C_L = 450pF		11	13.5	mA
		Transmit side LS Active (750kHz signal rate), Figure 7-10, C_L = 450pF		9.5	13	mA
		FS/LS Idle State (US side or DS side)		7.4	11	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - L1 Sleep mode	Upstream Facing side		7.5	9.8	mA
		Downstream Facing side		7.3	9.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - L2 Suspend mode	Upstream Facing side		1.07	1.55	mA
		Downstream Facing side		5.6	7.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - Not attached	Upstream Facing side		6.2	8.5	mA
		Downstream Facing side		6.2	8.9	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - High Speed (HS) mode	Receive side HS Active (240MHz signal rate), EQxx = 00, R_L = 45Ω to ground on D+ and D-		80	96	mA
		Transmit side HS Active (240MHz signal rate), EQxx = 00, R_L = 45Ω to ground on D+ and D-		85	96	mA
		HS Idle State, EQxx = 00, R_L = 45Ω to ground on D+ and D-.		77	90	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - Full Speed (FS) and Low Speed (LS) modes	Receive side FS Active (6MHz signal rate), Figure 7-9, C_L = 50pF		0.4	0.55	mA
		Transmit side FS Active (6MHz signal rate), Figure 7-9, C_L = 50pF		0.4	0.55	mA
		Receive side LS Active (750kHz signal rate), Figure 7-10, C_L = 450pF		0.4	0.55	mA
		Transmit side LS Active (750kHz signal rate), Figure 7-10, C_L = 450pF		0.4	0.55	mA
		FS/LS Idle State		0.4	0.55	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - L1 Sleep mode	Upstream Facing side		0.4	0.55	mA
		Downstream Facing side		0.4	0.55	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - L2 Suspend mode	Upstream Facing side		0.4	0.55	mA
		Downstream Facing side		0.4	0.55	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - Not attached	Upstream Facing side		0.4	0.55	mA
		Downstream Facing side		0.4	0.55	mA
$UV+_{(VBUSx)}$ (1)	Under voltage threshold when supply voltage is rising, V_{BUS}				4.0	V

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5V, V_{3P3Vx} = 3.3V, V_{1P8Vx} = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$UV-_{(VBUSx)}$ (1)	Under voltage threshold when supply voltage is falling, V_{BUS}		3.6			V
$UVHYS_{(VBUSx)}$ (1)	Under voltage threshold hysteresis, V_{BUS}			0.08		V
$UV+_{(V3P3Vx)}$	Under voltage threshold when supply voltage is rising, V_{3P3V}				2.95	V
$UV-_{(V3P3Vx)}$	Under voltage threshold when supply voltage is falling, V_{3P3V}		1.95			V
$UVHYS_{(V3P3Vx)}$	Under voltage threshold hysteresis, V_{3P3V}			0.11		V
$UV+_{(VCCx)}$ (2)	Under voltage threshold when supply voltage is rising, V_{CC}				2.35	V
$UV-_{(VCCx)}$ (2)	Under voltage threshold when supply voltage is falling, V_{CC}		2			V
$UVHYS_{(VCCx)}$ (2)	Under voltage threshold hysteresis, V_{CC}			0.07		V
$UV+_{(V1P8Vx)}$	Under voltage threshold when supply voltage is rising, V_{1P8V}				1.66	V
$UV-_{(V1P8Vx)}$	Under voltage threshold when supply voltage is falling, V_{1P8V}		1.25			V
$UVHYS_{(V1P8Vx)}$	Under voltage threshold hysteresis, V_{1P8V}			0.05		V
DIGITAL INPUTS						
V_{IH}	High-level input voltage		0.7 x V_{3PV3x}			V
V_{IL}	Low-level input voltage				0.3 x V_{3PV3x}	V
V_{IHYS}	Input transition threshold hysteresis		0.3			V
I_{IH}	High-level input current				1	µA
I_{IL}	Low-level input current				10	µA
DIGITAL OUTPUTS (V1OK, V2OK)						
V_{OH}	High-level output voltage	I_O = -3mA for 3.0V ≤ V_{3P3Vx} ≤ 3.6V	V_{3P3Vx} - 0.2			V
V_{OL}	Low-level output voltage	I_O = 3mA for 3.0V ≤ V_{3P3Vx} ≤ 3.6V			0.2	V
UDx, DDx, INPUT CAPACITANCE AND TERMINATION						
Z_{INP_xDx}	Impedance to GND, no pull up/down	Vin = 3.6V, V_{3P3Vx} = 3.0V, T_J < 125 °C, USB 2.0 Spec Section 7.1.6	300			kΩ
C_{IO_xDx}	Capacitance to GND	Measured with VNA at 240MHz, Driver Hi-Z			10	pF
R_{PUI}	Bus Pull up Resistor on Upstream Facing Port (idle)	USB 2.0 Spec Section 7.1.5	0.9	1.1	1.575	kΩ
R_{PUR}	Bus Pull up Resistor on Upstream Facing Port (receiving)	USB 2.0 Spec Section 7.1.5	1.5	2.2	3	kΩ
R_{PD}	Bus Pull-down Resistor on Downstream Facing Port	USB 2.0 Spec Section 7.1.5	14.25	19	24.8	kΩ
V_{TERM}	Termination voltage for Upstream facing port pullup (RPU)	USB 2.0 Spec Section 7.1.5, measured on D+ or D-, pullup enabled on upstream port, external load disconnected.	3		3.6	V
V_{HSTERM}	Termination voltage in high speed	USB 2.0 Spec Section 7.1.6.2, output voltage in high-speed idle state	–10		10	mV

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5V, V_{3P3Vx} = 3.3V, V_{1P8Vx} = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{HSTERM}	Driver Output Resistance (which also serves as high-speed termination)	(VOH= 0 to 600mV) USB 2.0 Spec Section 7.1.1.1 and Figure 7-5	40.5	45	49.5	Ω
UDx, DDx, INPUT LEVELS LS/FS						
V_{IH}	High (driven)	USB 2.0 Spec Section 7.1.4 (measured at connector)	2			V
V_{IHZ}	High (floating)	USB 2.0 Spec Section 7.1.4 (Downstream port pulldown, and upstream port pullup resistors enabled).	2.7		3.6	V
V_{IL}	Low	USB 2.0 Spec Section 7.1.4			0.8	V
V_{DI}	Differential Input Sensitivity	|(xD+)-(xD-)|; USB 2.0 Spec Figure 7-19; (measured at connector)	0.2			V
V_{CM}	Common Mode Range	Includes VDI range; USB 2.0 Spec Figure 7-19; (measured at connector)	0.8		2.5	V
UDx, DDx, OUTPUT LEVELS LS/FS						
V_{OL}	Low	USB 2.0 Spec Section 7.1.1, measured with RL of 0.9kΩ to 3.6V	0		0.3	V
V_{OH}	High (Driven)	USB 2.0 Spec Section 7.1.1, measured with RL of 14.25kΩ to GND	2.8		3.6	V
V_{OSE1}	SE1	USB 2.0 Spec Section 7.1.1	0.8			V
Z_{FSTERM}	Driver Series Output Resistance	USB 2.0 Spec Section 7.1.1 and Figure 7-4, measured during VOL or VOH	28		44	Ω
V_{CRS}	Output Signal Crossover Voltage	USB 2.0 Spec Section 7.1.1 Figures 7-8, 7-9 and 7-10; Excluding the first transition from the Idle state	1.3		2	V
UDx, DDx, INPUT LEVELS HS						
V_{HSSQ}	High-speed squelch/no-squelch detection threshold	USB 2.0 Spec Section 7.1.7.2, measured at 240MHz with increasing amplitude, V_{CM} = -50mV to 500mV	100	116	150	mV
V_{HSDSC}	High-speed disconnect detection threshold $_{HSDC}$ typical values	USB 2.0 Spec Section 7.1.7.2, V_{CM} = -50mV to 500mV	525	575	625	mV
V_{CHIRP_TH}	Chirp detection threshold	Chirp detection threshold, V_{CM} = -50mV to 500mV	70	215	365	mV
V_{HSRX}	High-speed differential input signaling levels data sensitivity	Peak-to-peak at 240MHz			100	mV
V_{HSCM}	High-speed data signaling common mode voltage range	USB 2.0 Spec Section 7.1.4.2	–50	200	500	mV
UDx, DDx, OUTPUT LEVELS HS						
V_{HSOH}	High-speed data signaling high	USB 2.0 Spec Section 7.1.7.2, EQxx = 00, Test load: 45Ω to GND on D+, D-	360	400	440	mV
V_{HSOL}	High-speed data signaling low	USB 2.0 Spec Section 7.1.7.2, EQxx = 00, Test load: 45Ω to GND on D+, D-	–10		10	mV
V_{HSOI}	High-speed data signaling idle, driver is off termination is on (measured single ended)	USB 2.0 Spec Section 7.1.7.2, EQxx = 00, Test load: 45Ω to GND on D+, D-	–10		10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	USB 2.0 Spec Section 7.1.7.2, EQxx = 00, Test load: 45Ω to GND on D+, D-, 2.2kΩ pullup to 3.3V on D+	700	850	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	USB 2.0 Spec Section 7.1.7.2, EQxx = 00, Test load: 45Ω to GND on D+, D-, 2.2kΩ pullup to 3.3V on D+	–900	–750	–500	mV
$U2\_TX_{CM}$	High-speed TX DC Common Mode	Test load: 45Ω to GND on D+, D-	–50	200	500	mV

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5V, V_{3P3Vx} = 3.3V, V_{1P8Vx} = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EQUALIZATION AND PRE-EMPHASIS						
EQ_{HS}	High-speed RX Equalization	EQ1=low, EQ0=low, 240MHz	-0.24	0.46	0.75	dB
EQ_{HS}	High-speed RX Equalization	EQ1=low, EQ0=float, 240MHz	0.27	0.98	1.5	dB
EQ_{HS}	High-speed RX Equalization	EQ1=low, EQ0=high, 240MHz	0.70	1.50	2.2	dB
EQ_{HS}	High-speed RX Equalization	EQ1=float, EQ0=low, 240MHz	1.04	2.00	2.81	dB
EQ_{HS}	High-speed RX Equalization	EQ1=float, EQ0=float, 240MHz	1.45	2.68	3.8	dB
EQ_{HS}	High-speed RX Equalization	EQ1=float, EQ0=high, 240MHz	1.73	3.09	4.4	dB
EQ_{HS}	High-speed RX Equalization	EQ1=high, EQ0=low, 240MHz	2.00	3.46	4.7	dB
EQ_{HS}	High-speed RX Equalization	EQ1=high, EQ0=float, 240MHz	2.25	3.80	5.1	dB
EQ_{HS}	High-speed RX Equalization	EQ1=high, EQ0=high, 240MHz	2.25	3.80	5.1	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=low, EQ0=low, 240MHz	0.25	0.48	0.75	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=low, EQ0=float, 240MHz	0.62	0.9	1.2	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=low, EQ0=high, 240MHz	0.89	1.36	1.5	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=float, EQ0=low, 240MHz	1.4	1.7	2.0	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=float, EQ0=float, 240MHz	1.7	2.1	2.5	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=float, EQ0=high, 240MHz	2.1	2.5	2.9	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=high, EQ0=low, 240MHz	2.7	3.2	3.7	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=high, EQ0=float, 240MHz	3.4	4.0	4.6	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=high, EQ0=high, 240MHz	3.4	4.0	4.6	dB
CDP						
V_{DM_SRC}	VDM_SRC Voltage	Load Current in the range of 0 to 250µA	0.5		0.7	V
I_{DP_SINK}	IDP_SINK (D+)	D+ Voltage = 0V to 0.7V	25		175	µA
V_{DAT_REF+}	VDAT_REF comparator rising threshold		300		400	mV
V_{DAT_REF-}	VDAT_REF comparator falling threshold		275		385	mV
THERMAL SHUTDOWN						
TSD+	Thermal shutdown turn-on temperature		160	170	180	°C
TSD-	Thermal shutdown turn-off temperature		150	160	170	°C
TSD_{HYS}	Thermal shutdown hysteresis			10		°C

(1) If V_{BUSx} pins are externally connected to the corresponding V_{3P3Vx} pins, then UVLO thresholds on V_{BUSx} are governed by $UV+_{(V3P3Vx)}$, $UV-_{(V3P3Vx)}$ and $UVHYS_{(V3P3Vx)}$

(2) If V_{CCx} pins are externally connected to the corresponding V_{1P8Vx} pins, then UVLO thresholds on V_{CCx} are governed by $UV+_{(V1P8Vx)}$, $UV-_{(V1P8Vx)}$ and $UVHYS_{(V1P8Vx)}$

5.10 Switching Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5V, V_{3P3Vx} = 3.3V, V_{1P8Vx} = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-UP TIMING						
T_{PWRUP}	Time taken for the device to power up, and recognize USB signaling, after valid power supply is provided on both side 1 and side 2.	All external power supplies are ramped up together with 5µs power-up time.		3.6	8	ms
UDx, DDx, HS Driver Switching Characteristics						
T_{HSR}	Rise Time (10% - 90%)	USB 2.0 Spec Section 7.1.2, 45Ω to GND loads on D+ and D-, EQxx = 00	310	370	510	ps
T_{HSF}	Fall Time (10% - 90%)	USB 2.0 Spec Section 7.1.2, 45Ω to GND loads on D+ and D-, EQxx = 00	310	370	510	ps
UDx, DDx, FS Driver Switching Characteristics						
T_{FR}	Rise Time (10% - 90%)	USB 2.0 Spec Figures 7-8, 7-9, C_L = 50pF	4		20	ns
T_{FF}	Fall Time (10% - 90%)	USB 2.0 Spec Figures 7-8, 7-9, C_L = 50pF	4		20	ns
T_{FRFM}	Differential Rise and Fall Time Matching (T_{FR}/T_{FM})	USB 2.0 Spec 7.1.2, Excluding first transition from Idle state, Figure 7-9, C_L = 50pF	90		111.1	%
UDx, DDx, LS Driver Switching Characteristics						
T_{LR}	Rise Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50pF to 600pF.	75		300	ns
T_{LF}	Fall Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50pF to 600pF.	75		300	ns
T_{LRFM}	Rise and Fall Time Matching (TLR/TFM), Excluding first transition from idle state.	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50pF to 600pF.	80		125	%
REPEATER TIMING - CONNECT, DISCONNECT, RESET, L1, L2						
$T_{FILTCONN}$	Debounce filter on FS or LS Connect Detection		45	70	80	µs
T_{DDIS}	Time to detect disconnect at the DS facing port in LS/FS L0 mode.		2		7	µs
T_{DETRST}	Time taken to detect reset on US port in LS/FS L0 mode		0		7	µs
T_{2SUSP}	Time taken by the US side to detect suspend (L2) and draw less than 2.5 mA current when bus is continuously in Idle		3		10	ms
$t_{DRESUMEL1}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from sleep/L1 state.				1	µs
$t_{DRESUMEL2}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from suspend/L2 state.				130	µs
$t_{DWAKEL1}$	Maximum time to detect and propagate remote wake when in sleep/L1 state.				5	µs
$t_{DWAKEL2}$	Maximum pulse width of remote wake that is guaranteed to be detected when in suspend/L2 state.				900	µs
$t_{DRSMPROP}$	Minimum duration of resume driven upstream and downstream after detecting remote wake when in suspend/L2 state.		1			ms
CMTI	Common mode transient immunity	PK-PK common mode noise, V_{CMPKPK} = 1200 V, with (xD+, xD-) set to (V_{3P3Vx}, 0), (0, V_{3P3Vx}) or (0,0). See Figure 6-3	50	100		kV/µs

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5V, V_{3P3Vx} = 3.3V, V_{1P8Vx} = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REPEATER TIMING - LS, FS						
T_{LSDD}	Low-speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			358	ns
T_{LSOP}	LS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-40		25	ns
T_{LSJP}	LS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–5		5	ns
T_{LSJN}	LS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–7.0		7.0	ns
T_{LST}	Minimum width of SE0 interval during LS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	210			ns
T_{LEOPD}	Repeater EOP delay relative to T_{LSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		200	ns
T_{LESK}	SE0 skew caused by the repeater during LS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-100		100	ns
T_{FSDD}	Full-Speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			70	ns
T_{FSOP}	FS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-10		10	ns
T_{FSJP}	FS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–2		2	ns
T_{FSJN}	FS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–6.0		6.0	ns
T_{FST}	Minimum width of SE0 interval during FS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	14			ns
T_{FEOPD}	Repeater EOP delay relative to T_{FSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		17	ns
T_{FESK}	SE0 skew caused by the repeater during FS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-15		15	ns
REPEATER TIMING - HS						
T_{HSSOPT}	High-speed Start of Packet Truncation	USB 2.0 spec, section 7.1.10.		6	8	UI
T_{HSEOPD}	High-speed End of Packet Dribble	USB 2.0 spec, section 7.1.13.		7	8	UI
T_{HSPD}	High-speed Propagation Delay	USB 2.0 spec, section 7.1.14.	2	3	4	ns
T_{HSTJ}	High-speed total additive jitter (output jitter - input jitter) of repeater (includes all complete SOP bits), EQxx=00				120	ps
T_{HSRJ}	High-speed additive random jitter (output jitter - input jitter) of repeater (includes all complete SOP bits), EQxx=00				35	ps
T_{HSDJ}	High-speed additive deterministic jitter (output jitter - input jitter) of repeater (includes all complete SOP bits), EQxx=00.				82	ps
T_{HSDIS}	Time window of continuous no transition during which the HS Disconnect Detector output is be sampled		36		82	ns
T_{FILT}	Time for which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	USB 2.0 spec, section 7.1.7.5.	2.5			µs
CDP TIMING						
$T_{VDMSRCEN}$	Time taken to enable VDMSRC on D- after detecting VDPSRC connection on D+				0.1	ms
$T_{VDMSRCDIS}$	Time taken to disable VDMSRC on D- after detecting VDPSRC disconnection on D+				0.1	ms
$T_{CON\_IDPSINK\_DIS}$	Time taken to disable IDP_SINK on D+ after detecting connect				0.1	ms

5.11 Insulation Characteristics Curves

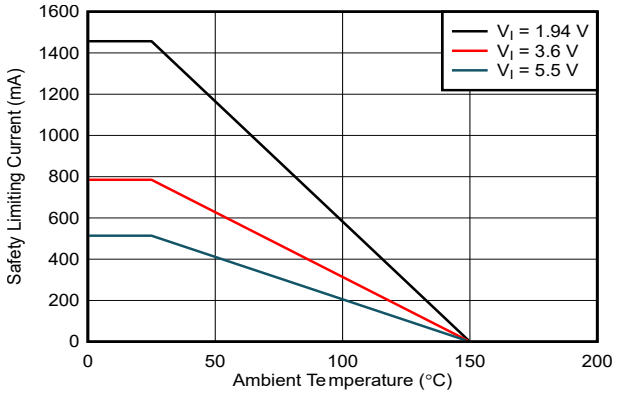


Figure 5-1. Thermal Derating Curve for Limiting Current per VDE for DP-28 Package

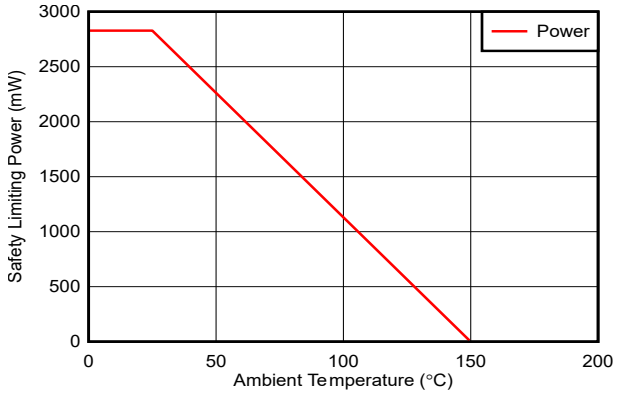


Figure 5-2. Thermal Derating Curve for Limiting Power per VDE for DP-28 Package

5.12 Typical Characteristics

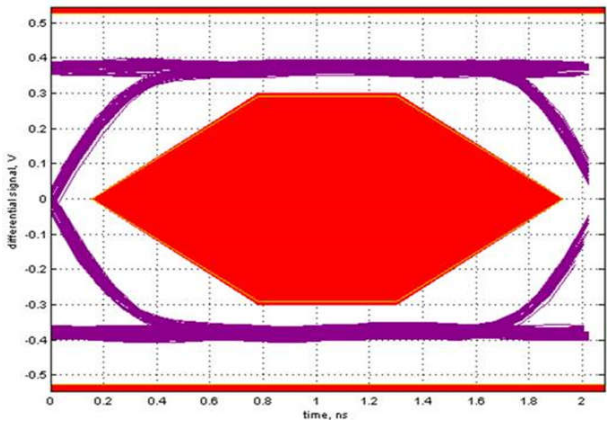


Figure 5-3. Typical High-Speed (480Mbps) Eye-Diagram through ISOUSB211-Q1

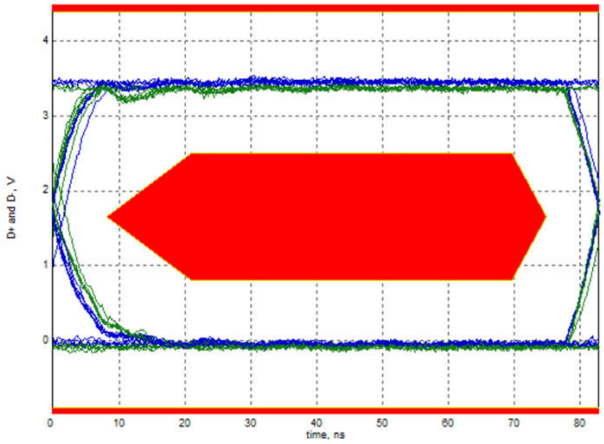


Figure 5-4. Typical Full-Speed (12Mbps) Eye-Diagram through ISOUSB211-Q1

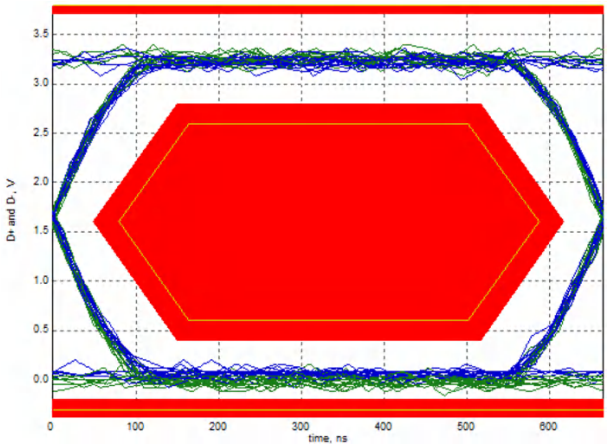


Figure 5-5. Typical Low-Speed (1.5Mbps) Eye-Diagram through ISOUSB211-Q1

6 Parameter Measurement Information

6.1 Test Circuits

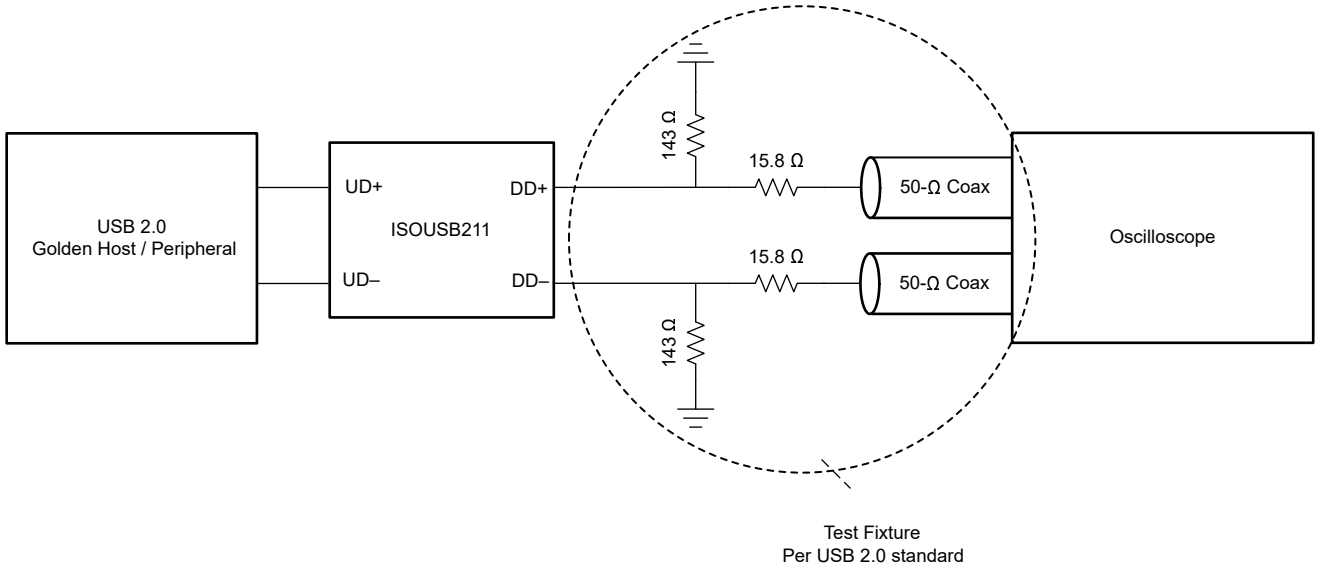


Figure 6-1. Upstream and Downstream Packet Parameter and Eye-Diagram Measurements for HS

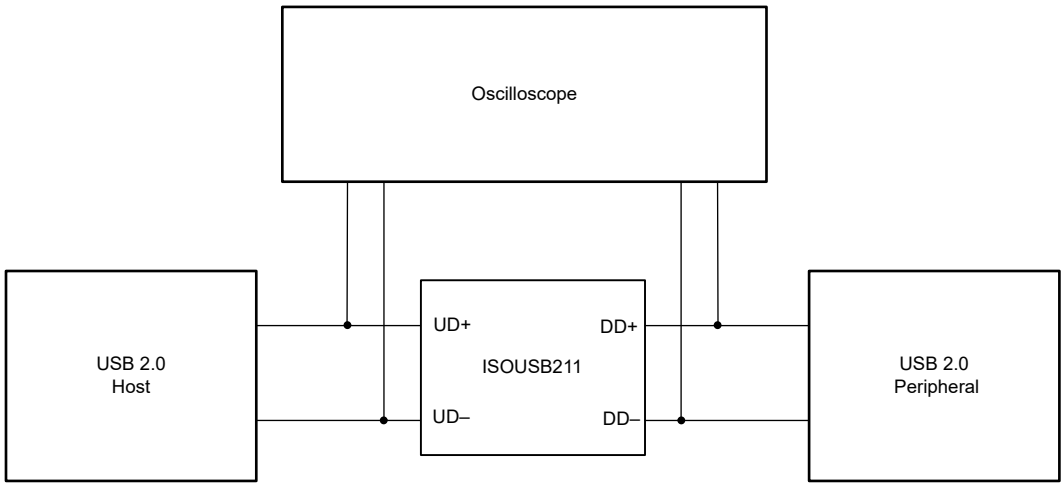


Figure 6-2. Upstream and Downstream Packet Parameter and Eye-Diagram Measurements for LS, FS

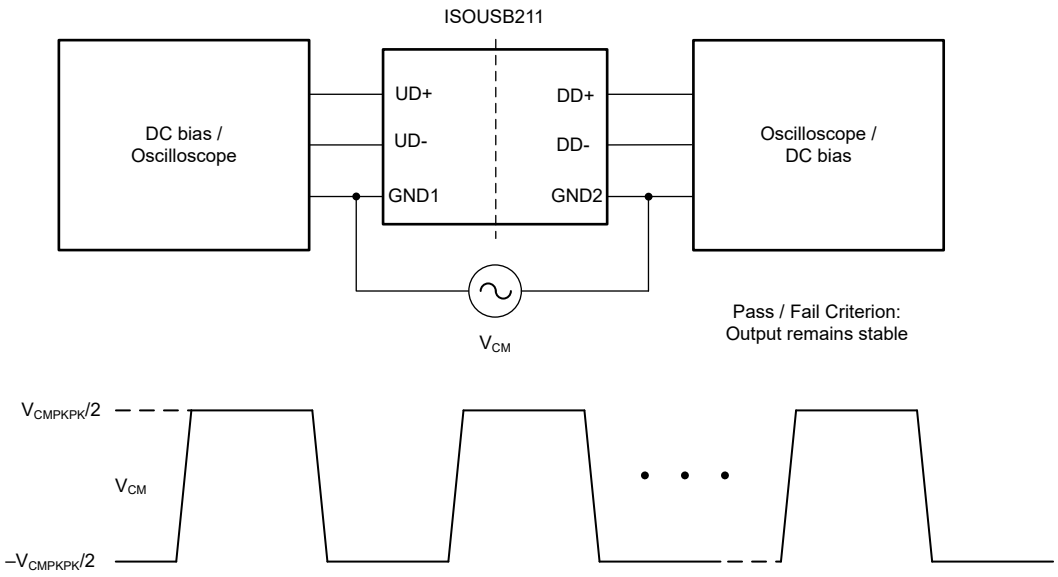


Figure 6-3. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

ISOUSB211-Q1 is a galvanically-isolated USB2.0 compliant repeater supporting Low Speed (1.5Mbps), Full Speed (12Mbps) and High Speed (480Mbps) signaling rates. The device supports automatic speed and connection detection, reflection of pullups/pulldowns, and link power management allowing drop-in USB hub, host, peripheral, and cable isolation. Most microcontrollers integrate the USB PHY, and so offer only D+ and D- bus lines as external pins. ISOUSB211-Q1 can isolate these pins from the USB bus without needing any other intervention from the microcontroller. The device also supports automatic role reversal. If, after disconnect, a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. The ISOUSB211-Q1 has inbuilt programmable equalization to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates. High Speed (HS) Test Mode entry is also automatically detected, as required by the USB2.0 standard, to enable HS compliance tests.

ISOUSB211-Q1 is available in reinforced isolation option with isolation withstand voltage of $5700V_{RMS}$ respectively, and with surge test voltage of $12.8kV_{PK}$ respectively. The device can operate completely off a 4.25V to 5.5V supply (USB VBUS power) or from local 3.3V and 1.8- supplies, if available, on both side 1 and side 2. This flexibility in supply voltages allows optimization for thermal performance based on power rails available in the system.

7.2 Functional Block Diagram

A simplified functional block diagram of ISOUSB211-Q1 is shown in Figure 7-1. The device comprises the following:

1. Transmit and receive circuits and pullup and pulldown resistors according to the USB standard.
2. Digital logic to handle bidirectional communication, and various state-transitions.
3. Internal LDOs to generate V_{3P3Vx} and V_{1P8Vx} supplies from the V_{BUSx} and V_{CCx} supplies respectively.
4. Galvanic isolation.

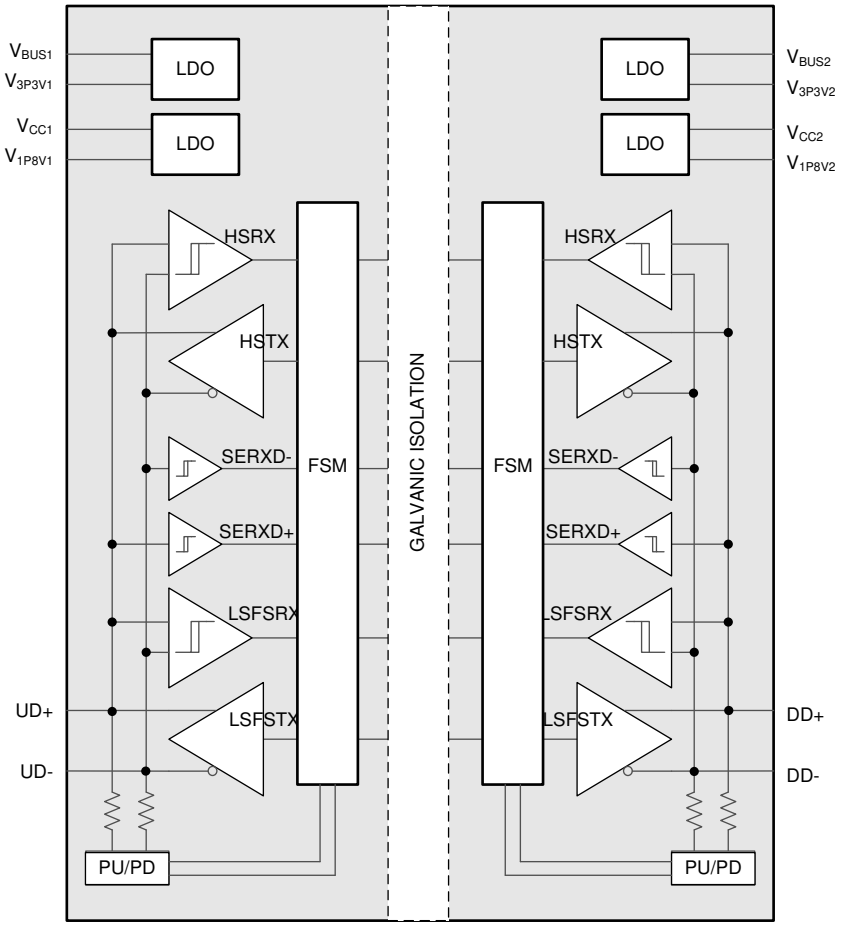


Figure 7-1. ISOUSB211-Q1 Simplified Functional Block Diagram

7.3 Feature Description

7.3.1 Power Supply Options

The ISOUSB211-Q1 can be powered by connecting a 4.25V to 5.5V supply on V_{BUSx} pins, in which case an internal LDO generates V_{3P3Vx} voltage. This option is designed for the side facing the USB connector, where a 5V VBUS supply is available. Alternatively, V_{BUSx} and V_{3P3Vx} pins can be shorted together and an external 3.3V power supply can be connected to both. This second option is designed for the side facing the microcontroller, where a 5V supply can be unavailable.

The ISOUSB211-Q1 also needs a 1.8V supply for operation. A 2.4V to 5.5V supply can be connected on V_{CCx} pins, in which case internal LDOs generate the V_{1P8Vx} supplies. In the simplest implementation, V_{CCx} can be connected to the USB VBUS on the side facing the connector, and to the 3.3V local supply on the side facing the microcontroller. In this implementation, there is power dissipation on the internal LDOs of ISOUSB, which limits the maximum ambient temperature supported by ISOUSB211-Q1.

To reduce power dissipation inside the ISOUSB211-Q1, an external 1.8V supply can be connected to both V_{CCx} and V_{1P8Vx} pins shorted together, in which case the internal 1.8V LDOs of ISOUSB211-Q1 are bypassed. In this implementation, some of the power dissipation is transferred to the external 1.8V supply, and overall higher ambient temperature operation is achieved for the ISOUSB211-Q1. If the external 1.8V supply is an LDO, the effect is to reduce power dissipation inside ISOUSB211-Q1, but overall no reduction in system current or power dissipation is achieved. Alternatively, if the external 1.8V supply is a DC-DC (buck) converter, both system power and ISOUSB211-Q1 power dissipation can be reduced.

A third option is to include external resistors between VCCx pins and VBUS and 3.3V local supplies. These resistors can be accommodated since V_{CCx} pins operate down to 2.4V. The resistors drop voltage and dissipate

power and serve a similar purpose as external 1.8V LDOs; that is, reduce power dissipation inside ISOUSB211-Q1 and allow higher ambient temperature operation.

Refer to the Thermal Considerations section for further details on how to optimize ISOUSB211-Q1 internal power dissipation according to the maximum ambient temperature required in the system and for recommendations on external resistors, LDOs and buck converters.

7.3.2 Power Up

Until all power supplies on both sides of ISOUSB211-Q1 are above the respective UVLO thresholds, the device ignores any activity on the bus lines on both the upstream and downstream sides. Once the power supplies are above the UVLO thresholds, the device is ready to respond to activity on the bus lines. When the power supplies on side 1 are up, this is indicated on side 2 by V1OK = High. Similarly, V2OK = High indicates that Side 2 is fully powered up.

7.3.3 Symmetric Operation, Dual-Role Port and Role-Reversal

ISOUSB211-Q1 supports symmetric operation. Typically, UD+ and UD- are upstream facing ports and connect to a host or hub. DD+ and DD- are downstream facing ports and connect to a peripheral. However, UD+ and UD- can also be connected to a peripheral and DD+ and DD- to a host or hub. Whichever side sees a connect first (D+ or D- pulled up to 3.3V) becomes the downstream facing side. This feature enables implementation of dual-role port (for example, Type-C dual-role port) and role-reversal (for example, OTG Host Negotiation Protocol - HNP). Refer to the *How to Implement an Isolated USB 2.0 High-Speed, Type-C® DRP* analog design journal for details. In the rest of this document, DD+/DD- are treated as downstream facing ports, and UD+/UD- as upstream facing ports, but the various operations and features described are equally applicable if this assignment is swapped.

7.3.4 Connect and Speed Detection

When there is no peripheral device connected to the downstream side of ISOUSB211-Q1, internal 15kΩ pulldown resistors on DD+ and DD- pins pull the bus lines to zero, creating an SE0 state. When either the DD+ or DD- lines is pulled up higher than the V_{IH} threshold, for a time period higher than $T_{FILTCONN}$, the ISOUSB211-Q1 device treats this as a connect. The ISOUSB211-Q1 device configures internal pull-up on the upstream side to match the pull-up detected on the downstream side. After connect is detected, the ISOUSB211-Q1 device waits for a reset to be asserted by the host/hub on the upstream side. Depending on whether DD+ or DD- is pulled up at the start of reset, the speed of the ISOUSB211-Q1 repeater is set. Once set, the speed of the repeater can only be changed after a power down or disconnect event.

A high-speed (HS) capable device is attached to the ISOUSB211-Q1 device and proceeds to perform high-speed handshake using chirp signaling as specified in the USB2.0 standard. This is followed by chirp signals from the host. The ISOUSB211-Q1 device reflects these chirp signals across the barrier, including HS idle (SE0) states from downstream to upstream and vice versa. Upon successful completing of the HS handshake, ISOUSB211-Q1 speed is set to High speed. Once set to high-speed, the speed of the repeater can only be changed after power down, HS disconnect event, or if the peripheral or host or hub do not perform HS handshake after a reset.

7.3.5 Disconnect Detection

When in Full-speed (FS) and Low-speed (LS) modes, disconnection of a peripheral is indicated when the host/hub is not driving any signal on the upstream side, and when the downstream bus is in the SE0 state (Both DD+ and DD- are below the V_{IL}threshold) for a time period higher than T_{DDIS}. Upon disconnect detection in FS and LS modes, the ISOUSB211-Q1 device removes the pullup resistor from the upstream side, thus allowing the upstream UD+ and UD- lines to discharge to zero. The ISOUSB211-Q1 then waits for the next connect event to occur.

When in High Speed (HS) mode, if the ISOUSB211-Q1 detects a continuous period of no transitions lasting T_{HSDIS}, the devices samples the DD+ and DD- lines using the HS Disconnect detector. If the input differential voltage crosses V_{HSDSC} during T_{HSDIS}, the repeater removes the HS termination from both the downstream and

upstream terminals and transitions to a disconnect state. The ISOUSB211-Q1 then waits for the next connect event to occur.

7.3.6 Reset

The ISOUSB211-Q1 device detects Reset assertion (prolonged SE0 state) on the upstream facing side of the device, and transmits the same to the downstream facing side. In HS state, an extended HS idle state can be the beginning of reset, or an entry into L2 Power Management state. ISOUSB211-Q1 is able to make the distinction between the two, and accordingly either continue to drive HS idle (same as reset) on the downstream side or transition to the L2 suspend state.

7.3.7 LS/FS Message Traffic

The ISOUSB211-Q1 device monitors the state of the bus on both upstream and downstream sides. The direction of communication is set by which side transitions from the LS/FS idle state first (J to K transition). After that, data is transferred digitally across the barrier, and reconstructed on the other side. Data transmission continues until either an end-of-packet (EOP) or a long idle is seen. At this point, the ISOUSB211-Q1 device tri-states the LS/FS transmitters, and waits for the next transition from the LS/FS idle state.

7.3.8 HS Message Traffic

The ISOUSB211-Q1 device monitors the state of the bus on both upstream and downstream sides. The direction of communication is set by which side transitions from the HS idle state first. Transition from HS idle state to valid HS data is detected by the HS squelch detector. After that, data is transferred digitally across the barrier, and reconstructed on the other side. Data transmission continues until the bus returns to HS idle state, also indicated by the HS squelch detector. At this point, the ISOUSB211-Q1 device tri-states the HS transmitters, and waits for the next transition from the HS idle state.

7.3.9 Equalization and Pre-Emphasis

The ISOUSB211-Q1 has inbuilt programmable receive equalization and transmit pre-emphasis to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates. These settings are controlled by EQ11 and EQ10 on side 1 and EQ21 and EQ20 on side 2. The EQxx pins can be connected to ground, connected to 3.3V supply or left floating, together creating nine different equalization levels. EQ11 and EQ10 can be chosen based on the length of D+/D- board trace and corresponding channel loss estimated on side 1, and similarly EQ21 and EQ20 for side 2. Typical 45Ω trace in FR4 has about 0.15dB/inch for 480Mbps signaling. Further adjustments to the EQ settings can be made by observing the transmit eye-diagram at the connector. If the trace lengths are very small, no equalization is needed, and the EQxx pins can be connected to ground.

ISOUSB211-Q1 samples EQxx pins only at power up, so do not change the EQxx settings on the fly after power up.

7.3.10 L2 Power Management State (Suspend) and Resume

The ISOUSB211-Q1 device supports Suspend low power state, also called L2 state in the USB 2.0 Link Power Management engineering change notice (ECN). Suspend mode is detected if the bus stays in the LS/FS/HS idle state for more than 3ms. When Suspend is detected from LS and FS idle state, the ISOUSB211-Q1 continues in the LS or FS idle state, at the same time reducing internal power consumption. If Suspend is detected from HS idle state, the ISOSUB211 detects the DS port transition to FS idle state (FS J), and reflects this upstream, while disabling all high-speed circuits to reduce power consumption. The transition to the L2 low-power mode is completed within 10ms.

Exit from L2 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB211-Q1, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB211-Q1 followed by Resume signaling from the host/hub on the upstream facing side. Start of Resume or Wake are signaled by a ‘K’ state by the host or the device respectively. The end of resume is signaled by the host by driving two low-speed bit times of SE0 followed by a 'J' state. If the port was operating in high speed before entering the low power state, end of resume is signaled by the host by transitioning to the high speed idle state. ISOUSB211-Q1 is able to replicate the resume and wake signaling appropriately both upstream and downstream. After Resume/Wake

signaling, the device returns to LS, FS or HS idle state, depending on the state the device was in before entering the L2 state.

7.3.11 L1 Power Management State (Sleep) and Resume

The ISOUSB211-Q1 device supports the additional L1 or Sleep low power state defined in the USB 2.0 Link Power Management ECN. When L1 entry is detected from the LS and FS idle state, the ISOUSB211-Q1 continues in the LS or FS idle state, at the same time reducing internal power consumption. If L1 entry is detected from HS idle state, the ISOSUB211 disables all high-speed circuits to reduce power consumption. The transition to the L1 low-power mode is completed within 50µs.

Exit from L1 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB211-Q1, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB211-Q1 followed by Resume signaling from the host or hub on the upstream facing side. Start of Resume or Wake are signaled by a ‘K’ state by the host or the device respectively. The end of resume is signaled by the host by driving two low-speed bit times of SE0 followed by a 'J' state. If the port is operating in high speed before entering the low power state, end of resume is signaled by the host by transitioning to the high speed idle state. ISOUSB211-Q1 is able to replicate the K signaling appropriately both upstream and downstream. After Resume/Wake signaling, the device returns to LS, FS or HS idle state, depending on the state the device was in before entering the L1 state.

7.3.12 HS Test Mode Support

USB2.0 standards needs test mode support, where the host/hub or peripheral is expected to enter High Speed test-modes based on commands received. ISOUSB211-Q1 is able to automatically detect test mode entry to enable HS compliance tests.

7.3.13 CDP Advertising

The ISOUSB211-Q1 device supports CDP advertising on both downstream and upstream facing side according to Battery Charger standard BC 1.2. CDP advertizing is useful when isolating a host or hub, to indicate to the connected peripheral that the port is capable of supplying 1.5A of current on VBUS. CDP advertising can be enabled by connecting the downstream side CDPENZx pin to ground (active low).

7.4 Device Functional Modes

Function Table lists the functional modes for the ISOUSB211-Q1 device.

Table 7-1. Function Table

SIDE 1 SUPPLY V_{BUS1}, V_{3P3V1} V_{CC1}, V_{1P8V1} (1)	BUS1 (UD+, UD-)	SIDE 2 SUPPLY V_{BUS2}, V_{3P3V2} V_{CC2}, V_{1P8V2}	BUS2 (DD+, DD-)	COMMENTS
Powered	Active	Powered	Active	When both sides are powered, the state-of the bus is reflected correctly from upstream to downstream and vice versa.
Powered	15kΩ PD	Powered	15kΩ PD	Disconnected state is presented on both upstream and downstream
Powered	15kΩ PD	Unpowered	Z	If a side is not powered, the bus lines on that side are in high-impedance state.
Unpowered	Z	Powered	15kΩ PD	
Unpowered	Z	Unpowered	Undetermined	

(1) Powered =((V_{BUSx} ≥ $UV+_{(VBUSx)}$) || (V_{BUSx} = V_{3P3Vx} ≥ $UV+_{(V3P3Vx)}$)) & ((V_{CCx} ≥ $UV+_{(VCCx)}$) || (V_{CCx} = V_{1P8Vx} ≥ $UV+_{(V1P8Vx)}$)) ; Unpowered = ((V_{BUSx} < $UV-_{(VBUSx)}$) & (V_{3P3Vx} < $UV-_{(V3P3Vx)}$)) || ((V_{CCx} < $UV-_{(VCCx)}$) & (V_{1P8Vx} < $UV-_{(V1P8Vx)}$)); X = Irrelevant; H = High level; L = Low level; Z = High impedance

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

ISOUSB211-Q1 is a galvanically-isolated USB 2.0 compliant repeater supporting low speed (1.5Mbps), full speed (12Mbps) and high speed (480Mbps) signaling rates. The device supports automatic connect and speed detection, reflection of pullups and pulldowns, and link power management, allowing drop-in USB hub, host, peripheral and cable isolation. The device also supports automatic role reversal; if, after disconnect, a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. This feature enables the device to support USB On-The-Go (OTG) and Type-C Dual Role Port (DRP) implementations. The ISOUSB211-Q1 has inbuilt programmable equalization to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates.

8.2 Typical Application

8.2.1 Isolated Host or Hub

Figure 8-1 shows an application for isolating a host or a hub using ISOUSB211-Q1. In this example, on the microcontroller side, V_{3P3V1} and V_{BUS1} are together connected to an external 3.3V supply. The V_{1P8V1} supply is generated using the internal 1.8V LDO by providing 3.3V supply to V_{CC1}. On the connector side, the VBUS from the USB connector is connected to V_{BUS2} and the V_{3P3V2} supply is generated using the internal 3.3V LDO. V_{CC2} and V_{1P8V2} are together connected to an external 1.8V supply derived from VBUS. Please refer to Thermal Considerations for options on optimizing power dissipation inside ISOUSB211-Q1 as required.

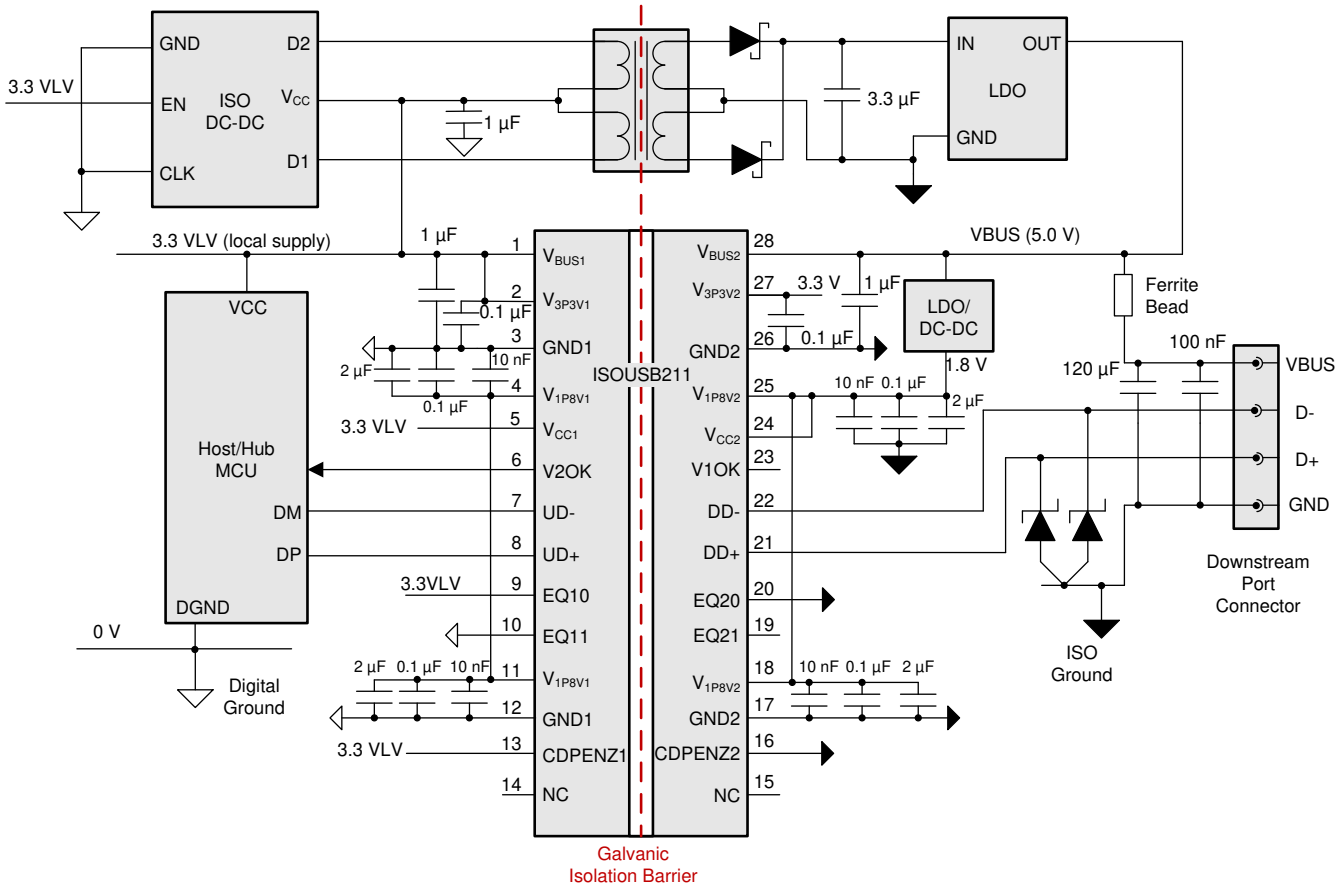


Figure 8-1. Isolated Host or Hub with ISOUSB211-Q1

8.2.1.1 Design Requirements

Decoupling capacitors are placed next to ISOUSB211-Q1 according to the recommendations provided in the Power Supply Recommendations section. An isolated DC-DC converter (such as the SN6505) is to provide power to the VBUS using the 3.3V local supply. Note that, for a host or hub, the USB standard requires a 120µF capacitor to be placed on the VBUS to provide in-rush current when a downstream peripheral is attached. In addition, a 100nF capacitor is recommended close to the VBUS pin to handle transient currents.

For more details about meeting USB2.0 design requirements, see Section 8.3.

8.2.1.2 Detailed Design Procedure

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, can be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100mΩ, can be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB211-Q1, as shown in Figure 8-1, to suppress transients such as ESD.

If the isolated power supply used is capable of providing >1.5A current on the VBUS, the port can be configured as a CDP port according to Battery Charger specification BC 1.2. To do this, the CDPENZ2 pin of ISOUSB211-Q1 must be connected to ground as shown. Under this condition ISOUSB211-Q1 responds to BC 1.2 signaling from a connected peripheral indicating to the peripheral that the port is capable of supply 1.5A current on VBUS.

8.2.2 Isolated Peripheral - Self-Powered

Figure 8-2 shows an application for isolating a self-powered peripheral using ISOUSB211-Q1.

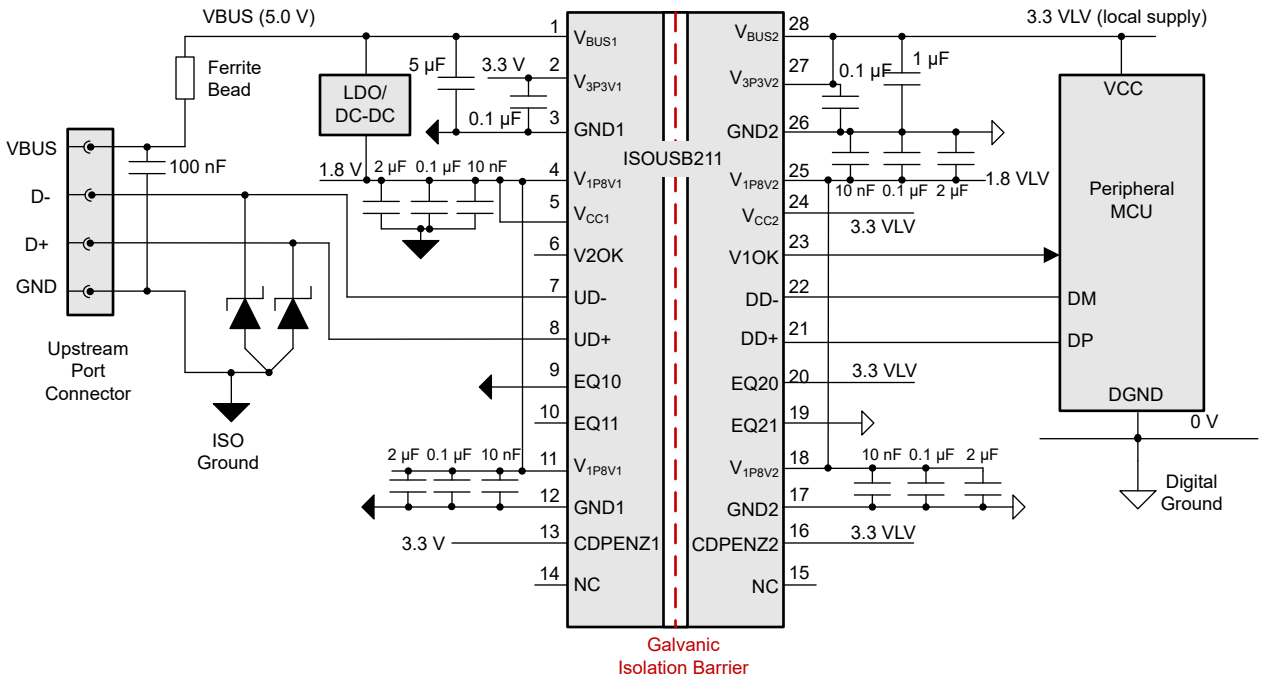


Figure 8-2. Isolated Self-Powered Peripheral with ISOUSB211-Q1

8.2.2.1 Design Requirements

In this example, on the microcontroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3V supply. The V_{1P8V2} supply is generated using the internal 1.8V LDO by providing 3.3V supply to V_{CC1}. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3V LDO. V_{CC1} and V_{1P8V1} are together connected to an external 1.8V supply derived from VBUS. Please refer to Thermal Considerations for options on optimizing power dissipation inside ISOUSB211-Q1 as required.

For more details about the meeting USB2.0 design requirements, see Section 8.3.

8.2.2.2 Detailed Design Procedure

Decoupling capacitors are placed next to ISOUSB211-Q1 according to the recommendations provided in the Power Supply Recommendations section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS must be less than 10µF. However, a total of at least 5µF capacitance is recommended on VBUS. A 100nF capacitor is recommended close to the VBUS pin to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, can be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100mΩ, can be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB211-Q1, as shown in the figure, to suppress transients such as ESD.

8.2.3 Isolated Peripheral - Bus-Powered

Figure 8-3 shows an application for isolating a self-powered peripheral using ISOUSB211-Q1.

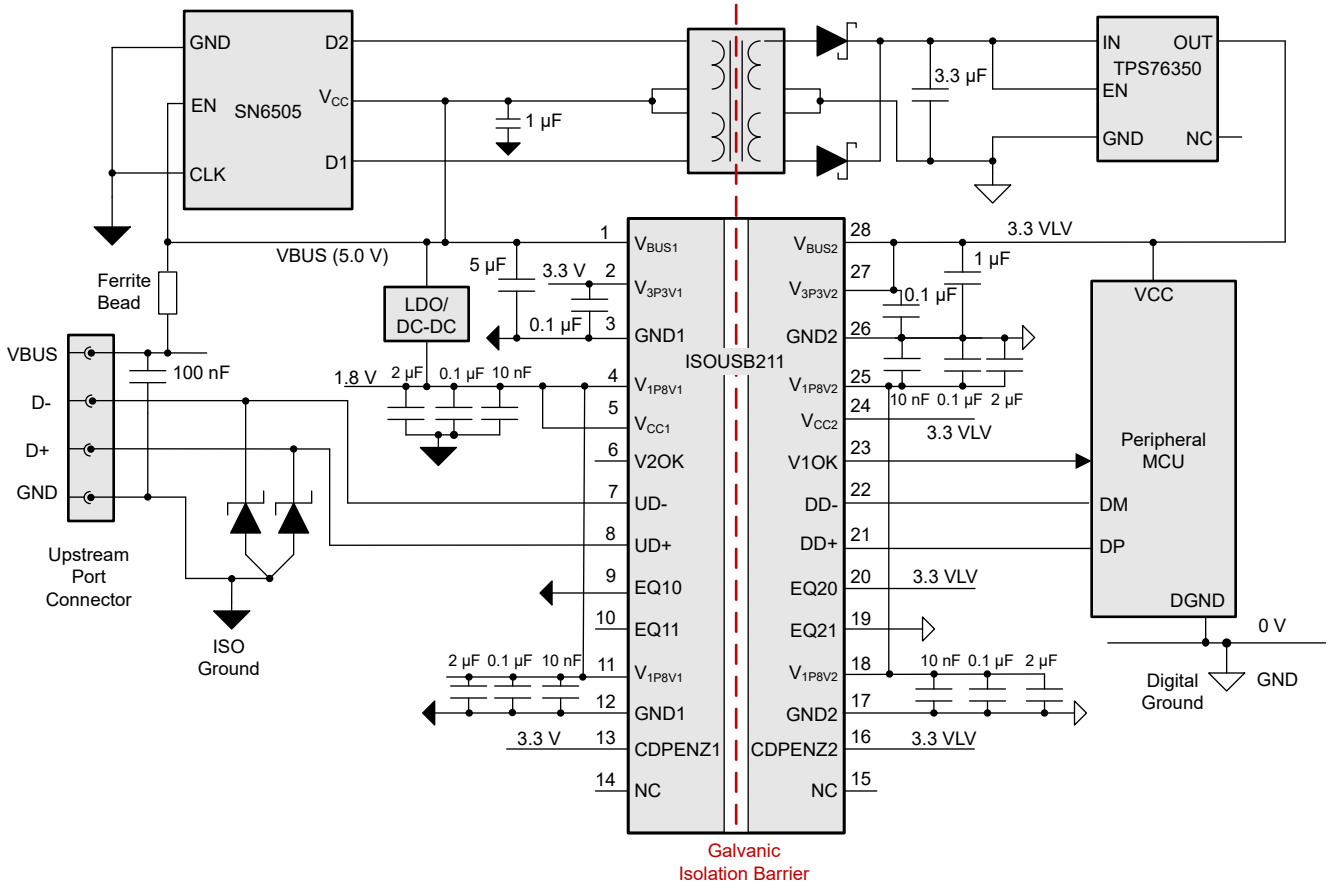


Figure 8-3. Isolated Bus-Powered Peripheral using ISOUSB211-Q1

8.2.3.1 Design Requirements

In this example, an isolated DC-DC converter (for example: SN6505) is used to create a 3.3V local supply while deriving power from the USB VBUS. On the microcontroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3V supply. The V_{1P8V2} supply is generated using the internal 1.8V LDO by connecting the 3.3V local supply to V_{CC1}. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3V LDO. V_{CC1} and V_{1P8V1} are connected together connected to an external 1.8V supply derived from VBUS. Please refer to Thermal Considerations for options on optimizing power dissipation inside ISOUSB211-Q1 as required.

For more details about the meeting USB2.0 design requirements, see Section 8.3.

8.2.3.2 Detailed Design Procedure

Decoupling capacitors are placed next to ISOUSB211-Q1 according to the recommendations provided in the Power Supply Recommendations section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS, including any decoupling capacitors reflected from the secondary side through the isolated DC-DC converter, must be less than 10µF. However, a total of at least 5µF capacitance is recommended on VBUS. A 100nF capacitor is recommended close to the VBUS connector to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, can be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100mΩ, can be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB211-Q1, as shown in the figure, to suppress transients such as ESD.

8.2.4 Application Curve

8.2.4.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 8-4 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that is 20% higher than the specified value.

Figure 8-5 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the isolation barrier. Based on the TDDB data, the intrinsic capability of the insulation is $1500V_{RMS}$ with a lifetime of 169 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DP-28 package is specified up to $1500V_{RMS}$. At the lower working voltages, the corresponding insulation lifetime is much longer than 169 years.

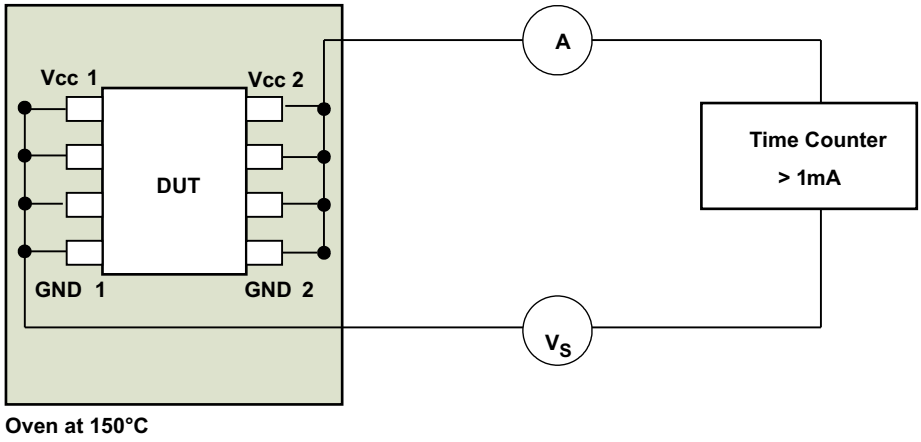


Figure 8-4. Test Setup for Insulation Lifetime Measurement

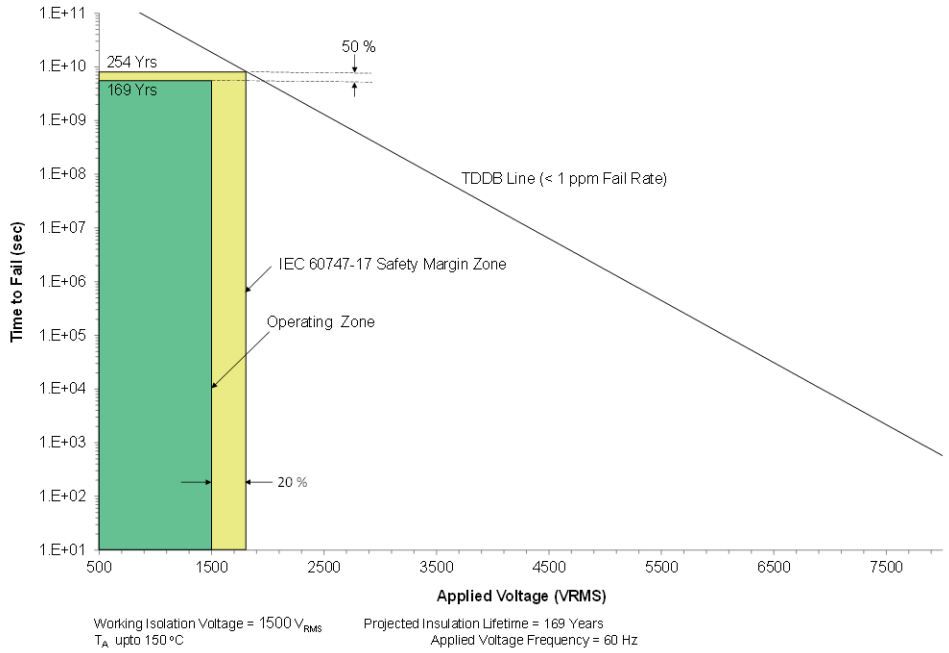


Figure 8-5. Insulation Lifetime Projection Data

8.3 Meeting USB2.0 HS Eye-Diagram Specifications

The USB2.0 standards specify TX and RX eye-diagram templates that must be met at the connector. The horizontal eye-opening achieved at the connector is a combination of the performance at the microcontroller, the additive jitter of the ISOUSB211-Q1, and the inter-symbol interference resulting from the insertion loss of D+/D- board traces. For best performance, minimize the length of D+/D- board traces from the MCU to ISOUSB211-Q1, and from ISOUSB211-Q1 to the connector. Vias and stubs on D+/D- lines must be avoided.

The ISOUSB211-Q1 has inbuilt programmable receive equalization and transmit pre-emphasis to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagrams. EQ11 and EQ10 can be chosen based on the length of D+/D- board traces and corresponding channel loss estimated on side 1, and similarly EQ21 and EQ20 for side 2. The EQxx pins can be connected to ground, connected to 3.3V supply or left floating, together creating 9 different equalization levels.

Typical 45Ω traces in FR4 have an insertion loss of approximately 0.15dB/inch for 480Mbps signaling. This number can be used to arrive at an estimate for the amount of Equalization/Pre-emphasis needed and the corresponding EQ settings. Further adjustments to the EQxx settings can be made by observing the transmit eye-diagram at the connector, and choosing the setting that gives the best eye opening. Choosing the right setting for the transmit path also results in an optimum performance for the receive path. Refer to Compensate for Channel Loss with Equalizer Settings on High-Speed USB Isolators application note for details. If the trace lengths are very small, no equalization is needed, and the EQxx pins can be connected to ground.

8.4 Thermal Considerations

ISOUSB211-Q1 offers different power supply input options, including internal LDOs, that can be used to optimize thermal performance in HS mode. If the 3.3V and 1.8V supplies are supplied using external regulators, the power dissipated inside the ISOUSB chip is lower. The internal power dissipated, when taken with the junction-to-air thermal resistance defined in the Thermal Information table can be used to determine the junction temperature for a given ambient temperature. The junction temperature must not exceed 150°C. This section describes different power supply configurations for ISOUSB211-Q1 and explains how the power dissipated inside ISOUSB211-Q1 and the internal temperature rise can be calculated in each case.

For best thermal performance, connect small ground planes to the GNDx pins, and connect these planes to the ground layer with multiple vias as shown in Layout Example.

8.4.1 V_{BUS} / V_{3P3V} Power

If VBUS is connected to external 5.0V supply, with V3P3V generated through an internal LDO, the power dissipated is $V_{BUSx} \times I_{VBUSx}$.

If VBUSx and V3P3Vx are shorted together and connected to an external 3.3V supply, the power dissipated due to this supply is $V_{3P3Vx} \times I_{3P3Vx}$.

8.4.2 V_{CCx} / V_{1P8Vx} Power

If V_{CCx} is connected to external 2.4 to 5.0V supply, with V_{1P8Vx} generated through the internal 1.8V LDO, the power dissipated is $V_{CCx} \times I_{VCCx}$.

If V_{CCx} and V_{1P8Vx} are shorted together and connected to an external 1.8V supply, the power dissipated due to this supply is $V_{1P8Vx} \times I_{1P8Vx}$.

8.4.3 Example Configuration 1

In the application example shown in Figure 8-6, ISOUSB211-Q1 is powered using USB VBUS on the connector side, and a local 3.3V digital supply on the microcontroller side. No other external regulators or power supplies are used.

In this scenario, the total power consumption inside ISOUSB211-Q1 from both sides taken together is:

$V_{BUS1} \times I_{VBUS1} + V_{BUS1} \times I_{VCC1} + V_{3P3V2} \times I_{3P3V2} + V_{3P3V2} \times I_{VCC2}$

Assuming 5.25V as the maximum value of VBUS1, and 3.5V as the maximum value of the 3.3V local supply, the internal power dissipation is calculated as:

5.25V × 13.5mA + 5.25V × 96mA + 3.5V × 13.5mA + 3.5V × 96mA = 960mW.

Since the junction-to-air thermal resistance is 44.2°C/W, this power dissipation results in a 42.5°C internal temperature rise. Ambient temperature up to 107°C can be supported for this configuration.

This configuration offers the simplest implementation, but the ambient temperature supported is lower than other configurations.

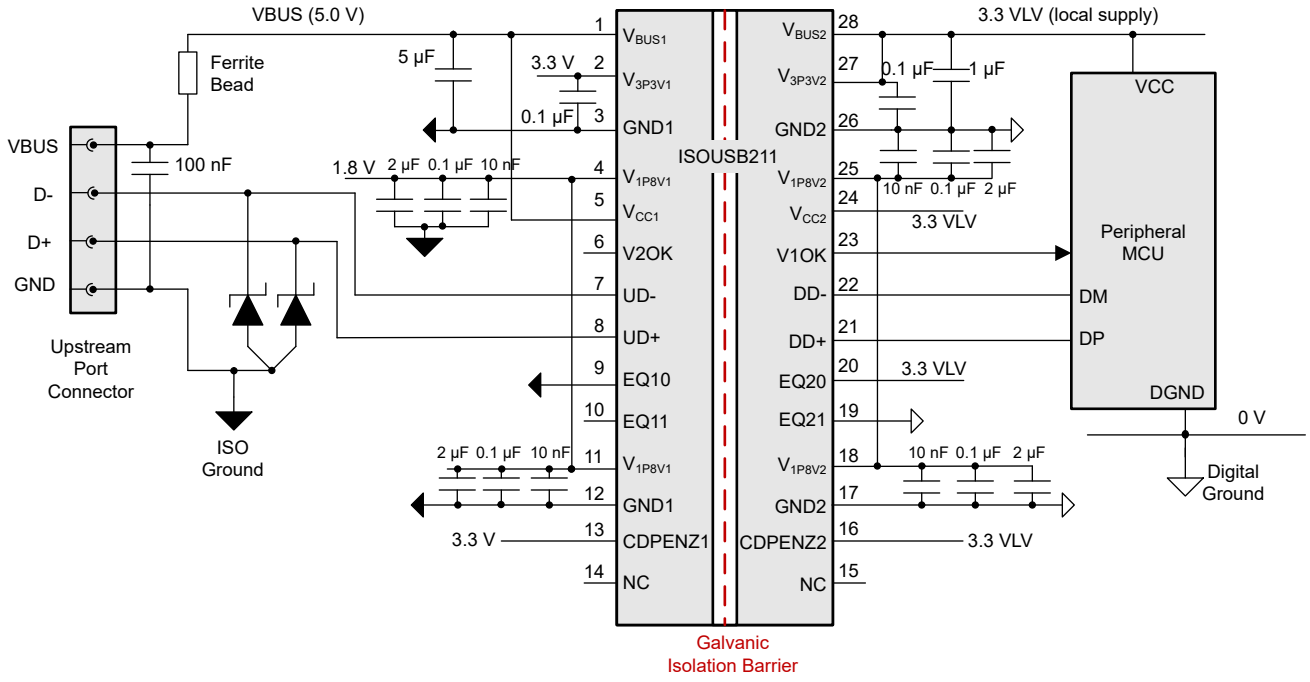


Figure 8-6. Using ISOUSB211-Q1 Without External 1.8V Regulators

8.4.4 Example Configuration 2

In the application example shown in Figure 8-7, ISOUSB211-Q1 is powered using USB VBUS on the connector side, and a local 3.3V digital supply on the microcontroller side to generate V_{3P3Vx}. An external LDO or DC-DC buck converter is used to generate V_{1P8Vx} on both sides.

In this scenario, the total power consumption from both sides taken together is:

$V_{BUS1} \times I_{VBUS1} + V_{1P8V1} \times I_{1P8V1} + V_{3P3V2} \times I_{3P3V2} + V_{1P8V2} \times I_{1P8V2}$

Assuming 5.25V as the maximum value of VBUS, and 1.89V as the maximum value of the external 1.8V power supply, the internal power dissipation is calculated as

5.25V × 13.5mA + 1.89V × 96mA + 3.5V × 13.5mA + 1.89V × 96mA = 481mW.

Since the junction-to-air thermal resistance is 44.2°C/W, this power dissipation results in a 22°C internal temperature rise. Ambient temperature up to 128°C can be supported for this configuration.

TLV741P and TLV62568 are examples of low-cost LDO and buck converters, respectively, that can be used in this application. Both options reduce the power dissipation in ISOUSB211-Q1. However, the buck converter additionally reduces power dissipation at the system level, and the current drawn from VBUS and local 3.3V supplies.

This configuration offers the lowest power dissipation and the highest ambient temperature operation using external regulators.

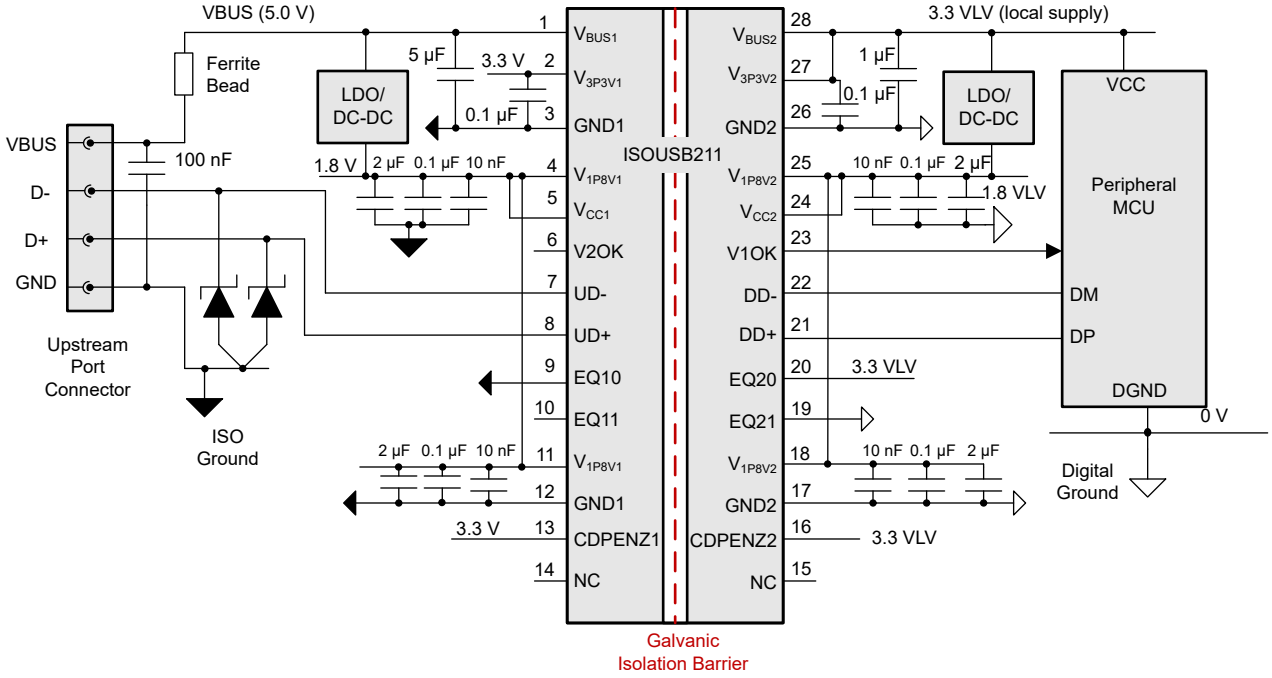


Figure 8-7. Using ISOUSB211-Q1 with 1.8V Supplied with External Regulators

8.4.5 Example Configuration 3

In the application example shown in Figure 8-8, ISOUSB211-Q1 is powered using USB VBUS on the connector side, and a local 3.3V digital supply on the microcontroller side to generate V_{3P3Vx}. The internal LDOs are used to generate V_{1P8Vx} on both sides like in Example Configuration 1. However, the V_{CC1} and V_{CC2} are connected to VBUS and 3.3 VLV, not directly like in Example Configuration 1, but through resistors R1 (20Ω, 250mW) and R2 (5Ω, 50mW) respectively.

The external resistors drop voltage, and dissipate power, helping reduce the power dissipation within ISOUSB211-Q1, and the corresponding temperature rise. The resistor values are decided keeping in mind that the V_{CCx} voltage can be as low as 2.4V. Additional 1µF capacitors are needed on V_{CCx} pins.

In this scenario, the total power consumption inside the IC from both sides taken together is:

$V_{BUS1} \times I_{VBUS1} + V_{BUS1} \times I_{VCC1} - 20\Omega \times I_{VCC1} \times I_{VCC1} + V_{3P3V2} \times I_{3P3V2} + V_{3P3V2} \times I_{VCC2} - 5\Omega \times I_{VCC2} \times I_{VCC2}$

Assuming 5.25V as the maximum value of VBUS, and 3.5V as the maximum value of the 3.3V local supply, the internal power dissipation is calculated as

5.25V × 13.5mA + 5.25V × 96mA - 20Ω × 96mA × 96mA + 3.5V × 13.5mA + 3.5V × 96mA - 5Ω × 96mA × 96mA = 728mW.

Since the junction-to-air thermal resistance is 44.2°C/W, this power dissipation results in a 33°C internal temperature rise. Ambient temperature up to 117°C can be supported for this configuration.

This configuration offers a middle path between Example Configuration 1 and Example Configuration 2, achieving lower temperature rise, and higher ambient temperature operation, with the addition of only two resistors and two capacitors.

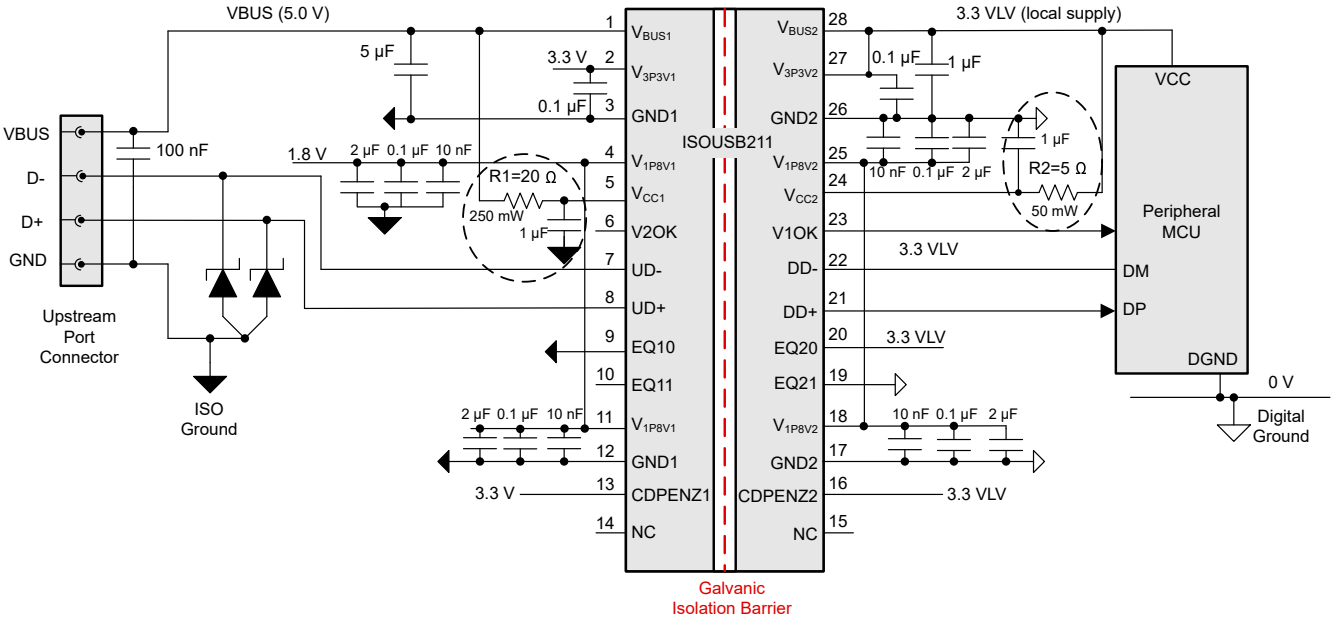


Figure 8-8. Using ISOUSB211-Q1 with Resistors in series with V_{CCx} Pins

8.5 Power Supply Recommendations

0.1µF capacitors are recommended to be placed very close to V_{3P3Vx} pins to GNDx. 1µF capacitors are recommended to be placed very close to V_{BUSx} pins to GNDx. 2µF, 0.1µF, and 10nF capacitors are recommended to be placed between V_{1P8Vx} and GNDx, between pins 4 and 3, between pins 25 and 26, between pins 11 and 12, and between pins 25 and 26 respectively, as close to the device as possible. Place the lower value capacitors closer to the IC. If V_{CCx} pins are connected through resistors as shown in Example Configuration 3, 1µF capacitors are recommended to be placed between V_{CCx} (pins 5, 24) and GNDx (pins 3, 26), as close to the device as possible, with higher priority being accorded to the capacitors on V_{1P8Vx} pins.

These decoupling capacitor recommendations are irrespective of whether the 3.3V and 1.8V supplies are provided externally or generated using internal LDOs.

Refer to Section 8.6.2 for recommended placement of the decoupling capacitors. Small footprint capacitors (0402/0201) are recommended so that these can be placed very close to the supply pins and corresponding

ground pins on the top layer without the use of vias. The capacitors on V_{1P8Vx} supplies are higher in priority when considering placement close to the IC.

While isolating a host or hub or bus-powered peripherals, isolated power is needed and can be generated with the help of a transformer driver such as TI's SN6505B. For such applications, detailed power supply design, and transformer selection recommendations are available in the *SN6505 Low-Noise 1A Transformer Drivers for Isolated Power Supplies* datasheet. If CDP functionality is enabled while isolation host/hub, the isolated power supply must be capable of delivering 1.5A on VBUS.

8.6 Layout

8.6.1 Layout Guidelines

Three layers are sufficient to accomplish a low EMI PCB design. Layer stacking must be in the following order (top to bottom): high-speed signal layer, ground plane, optional power layer, and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- For best performance, minimize the length of D+/D- board traces from the MCU to ISOUSB211-Q1, and from ISOUSB211-Q1 to the connector. Vias and stubs on D+/D- lines must be avoided. This is especially important for High Speed Operation.
- Placing a solid ground plane just below the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow. D+ and D- traces must be designed for 90Ω differential impedance and as close to 45Ω single ended impedance as possible.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Decoupling capacitors must be placed on the top layer, and the routing between the capacitors and the corresponding to supply and ground pins must be completed in the top layer. There must not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins.
- ESD structures must be placed on the top layer, close to the connector, and right on the D+/D- traces without vias. Ground routing for the ESD structures must be made in the top layer if possible, else must have a strong connection to the ground plane with multiple vias.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility, as these signal links typically have margin to tolerate discontinuities such as vias.
- Connect a small plane (for example, 2mm × 2mm) to the GND pins on the top layer to improve thermal performance. Connect this to the ground player in the second layer with multiple vias. See Layout Example for details.

8.6.1.1 PCB Material

For digital circuit boards operating at less than 500Mbps, (or rise and fall times greater than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over lower-cost alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.6.2 Layout Example

The layout example in this section shows the recommended placement for decoupling capacitors and ESD protection diodes. A continuous ground plane is recommended below the D+/D- signal traces. Small footprint capacitors (0402/0201) are recommended so that these can be placed very close to the supply pins and corresponding ground pins and connected using the top layer. There must not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins. The capacitors on V_{1P8Vx} supplies are higher in priority when considering placement close to the IC. The ESD protection diodes must be placed close to the connector with a strong connection to the ground plane. Pins 4 and 11 for V_{1P8V1} and pins 18 and 25 for V_{1P8V2} are connected together, but this connection is after the decoupling capacitors. If more than two layers are available in the PCB, this connection must be made in an inner or bottom layer (for example, Layer 3 or 4) to not interrupt the ground plane under the D+/D- traces. The example shown is for an isolated host or

hub, but similar considerations apply for isolated peripherals as well. The 120µF capacitor on VBUS only applies to host or hub and must not be used for peripherals. A ferrite bead, with dc resistance less than 100mΩ, can be optionally placed on the VBUS route, after the 100nF (and 120µF) capacitors to prevent transients such as ESD from affecting the rest of the circuits.

For best performance, minimize the length of D+/D- board traces from the MCU to ISOUSB211-Q1, and from ISOUSB211-Q1 to the connector. Vias and stubs on D+/D- lines must be avoided. This is especially important for High Speed Operation.

Connect a small plane (for example, 2mm × 2mm) to the GND pins on the top layer to improve thermal performance. Connect this to the ground player in the second layer with multiple vias.

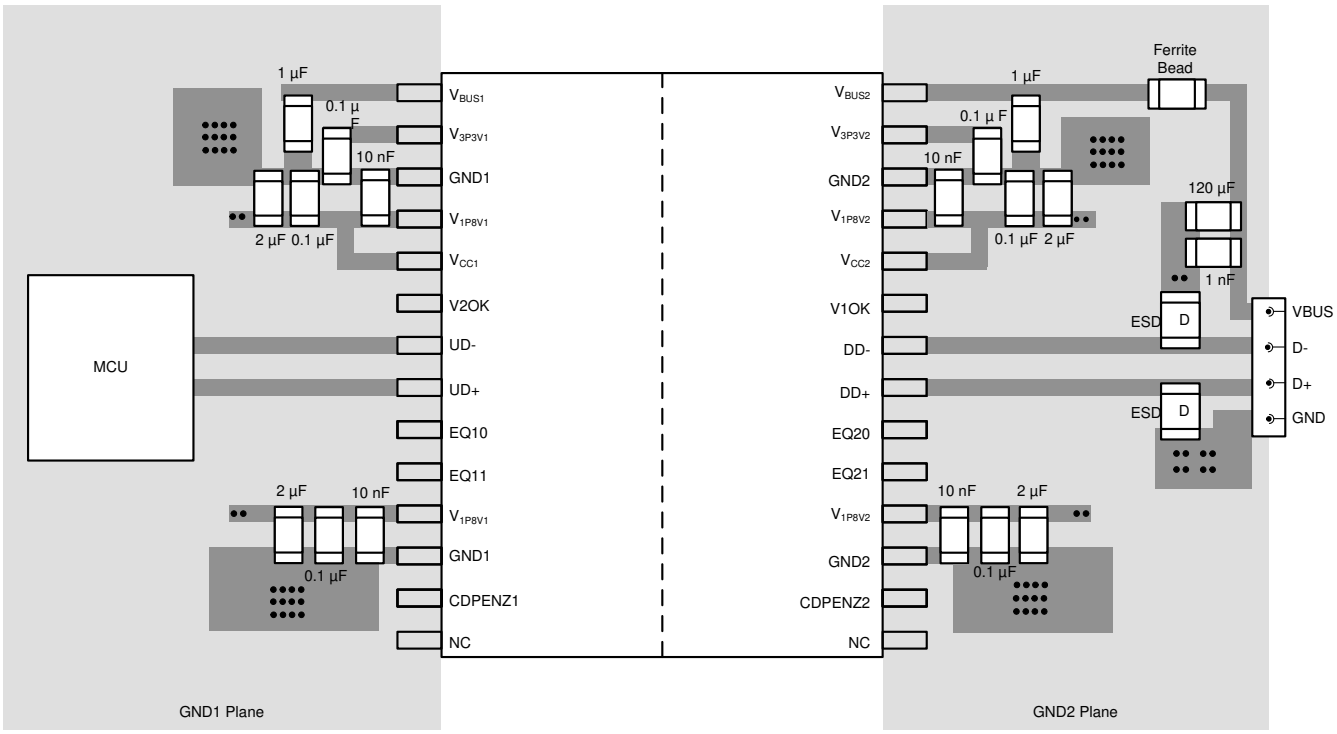


Figure 8-9. Layout Example for ISOUSB211-Q1

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2024) to Revision A (June 2026)	Page
• Changed the status of the datasheet from *Advanced Information* to: *Production Data*	1
• Added HBM ESD rating for bus pins	5
• Increased the Withstand isolation voltage from 5,000V to 5,700V	7
• Removed certification ratings row as this information is available in the certificates	8
• Added Application Information section	24
• Added Design Requirements section	25
• Added Detailed Design Procedure section	25

11 Mechanical, Packaging, and Orderable Information

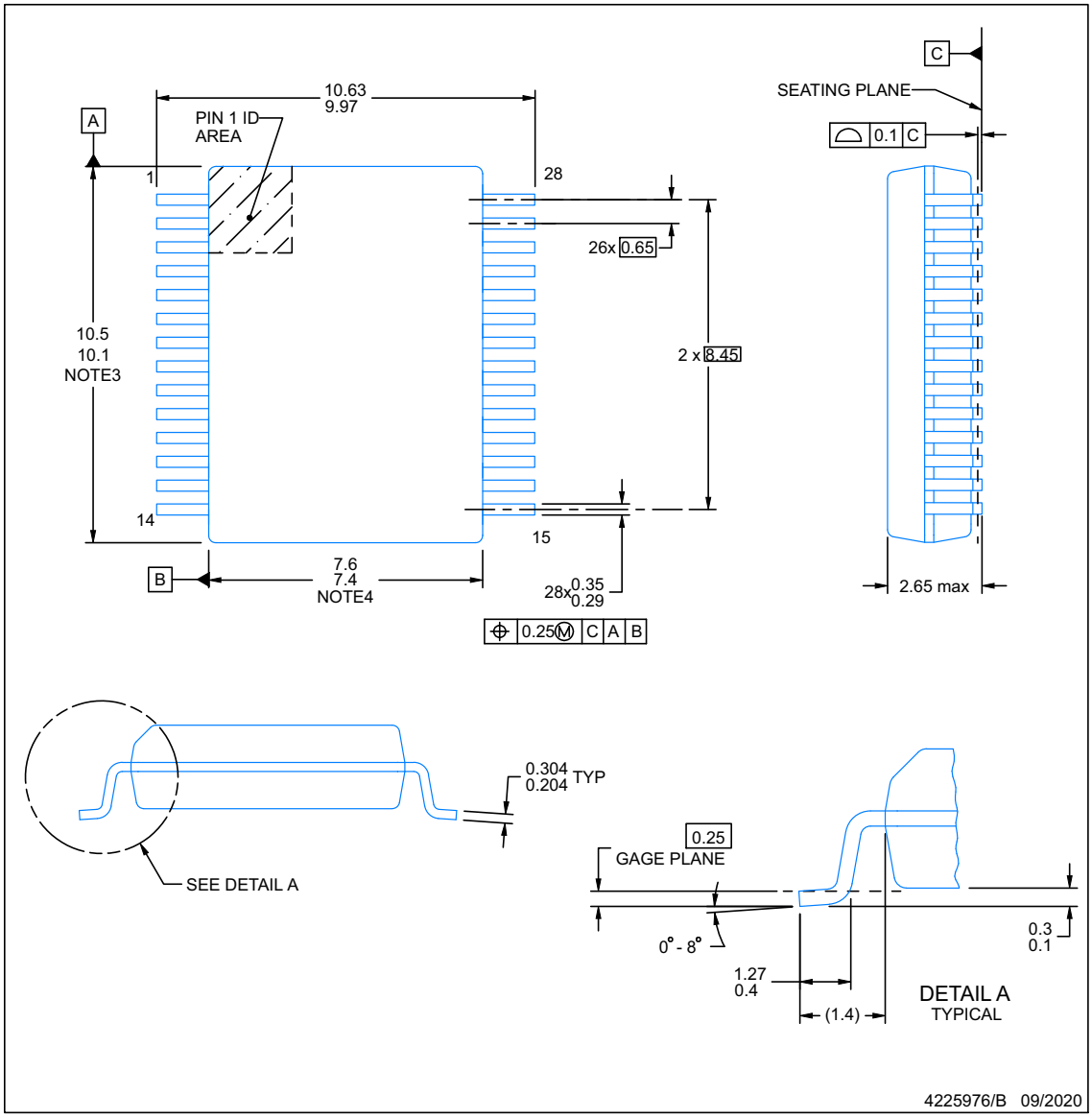
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DP0028A-C01

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

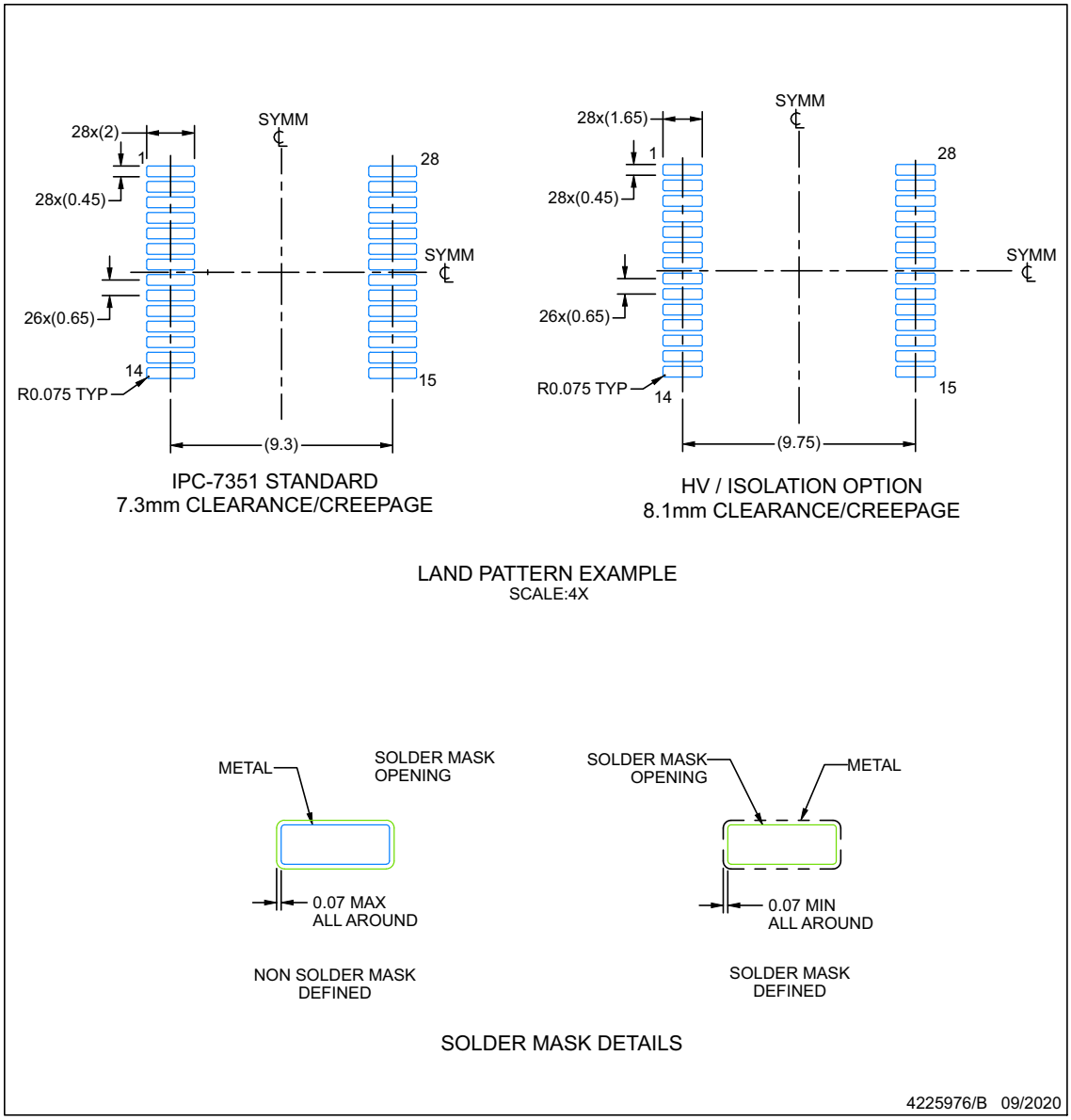
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DP0028A-C01

SSOP - 2.65 mm max height

SSOP



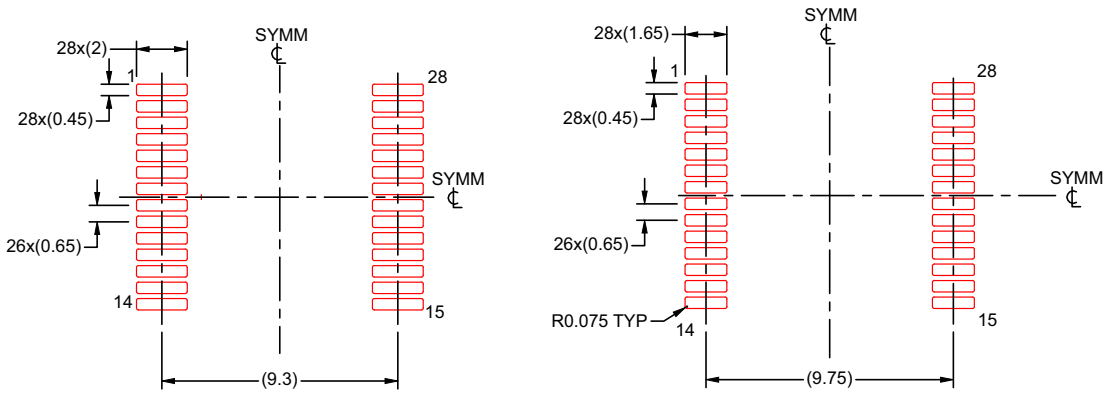
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DP0028A-C01 SSOP - 2.65 mm max height

SSOP



IPC-7351 STANDARD
7.3mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

SCALE:4X

4225976/B 09/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XISOUSB211DPRQ1	Active	Preproduction	SSOP (DP) | 28	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISOUSB211DPRQ1.A	Active	Preproduction	SSOP (DP) | 28	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF ISOUSB211-Q1 :

- Catalog : ISOUSB211

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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Last updated 10/2025