LM34917A Ultra Small 33V, 1.25A Constant On-Time Buck Switching Regulator with Intelligent Current Limit

Check for Samples: LM34917A

FEATURES

- **Functional Input Voltage Range: 8V to 33V**
- **DSBGA package**
- **Input Over-Voltage Shutdown at ≅35V**
- **Transient Capability to 50V**
- **Integrated N-Channel buck switch**
- **Valley current limit varies with V_{IN} and V_{OUT} to reduce excessive inductor current**
- **On-time is reduced when in current limit**
- **Integrated start-up regulator**
- **No loop compensation required**
- **Ultra-Fast transient response**
- **Maximum switching frequency: 2 MHz**
- **Operating frequency remains nearly constant with load current and input voltage variations**
- **Programmable soft-start**
- **Precision internal reference**
- **Adjustable output voltage**
- **Thermal shutdown**

TYPICAL APPLICATIONS

- **High Efficiency Point-Of-Load (POL) Regulator**
- **Non-Isolated Buck Regulator**
- **Secondary High Voltage Post Regulator**

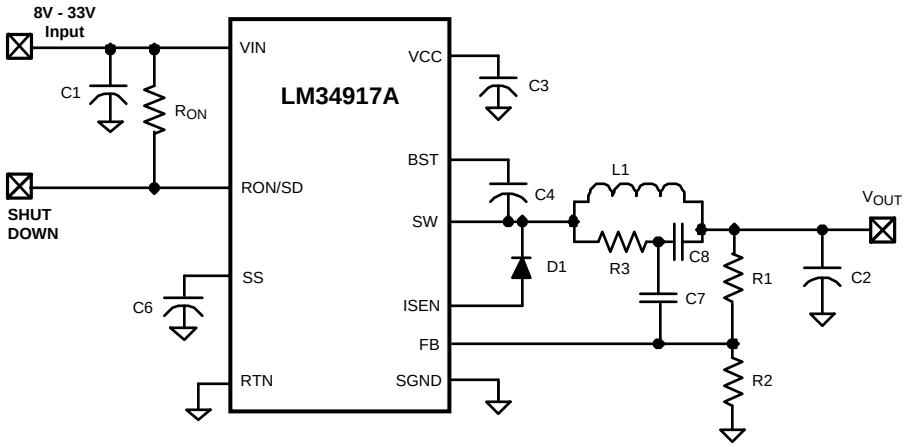
PACKAGE

- **12-Bump DSBGA Package**

DESCRIPTION

The LM34917A Step-Down Switching Regulator features all the functions needed to implement a low cost, efficient, buck bias regulator capable of supplying at least 1.25A to the load. To reduce excessive switch current due to the possibility of a saturating inductor the valley current limit threshold changes with input and output voltages, and the on-time is reduced when current limit is detected. This buck regulator contains an N-Channel Buck Switch, and is available in the 12 pin DSBGA package. The constant on-time feedback regulation scheme requires no loop compensation, results in fast load transient response, and simplifies circuit implementation. The operating frequency remains constant with line and load variations due to the inverse relationship between the input voltage and the on-time. The valley current limit results in a smooth transition from constant voltage to constant current mode when current limit is detected, reducing the frequency and output voltage, without the use of foldback. Additional features include: V_{CC} under-voltage lock-out, input over-voltage shutdown, thermal shutdown, gate drive under-voltage lock-out, and maximum duty cycle limit.

Basic Step Down Regulator



Connection Diagram

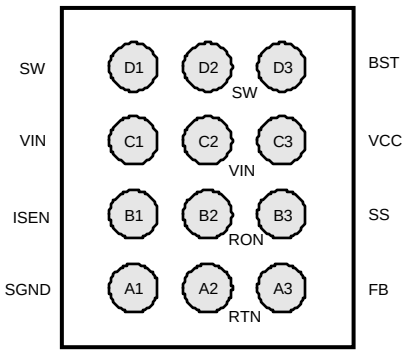


Figure 1. Bump Side
Package Number YZR0012UNA

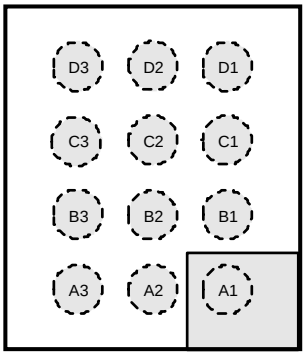


Figure 2. Top View
Package Number YZR0012UNA

PIN DESCRIPTIONS

Pin Number	Name	Description	Application Information
A1	SGND	Sense Ground	Re-circulating current flows into this pin to the current sense resistor.
A2	RTN	Circuit Ground	Ground for all internal circuitry other than the current limit detection.
A3	FB	Feedback input from the regulated output	Internally connected to the regulation and over-voltage comparators. The regulation level is 2.5V.
B1	ISEN	Current sense	The re-circulating current flows out of this pin to the free-wheeling diode.
B2	RON/SD	On-time control and shutdown	An external resistor from VIN to this pin sets the buck switch on-time. Grounding this pin shuts down the regulator.
B3	SS	Softstart	An internal current source charges an external capacitor to 2.5V, providing the softstart function.
C1,C2	VIN	Input supply voltage	Operating input range is 8.0V to 33V, with over-voltage shutdown internally set at ≅35V. Transient capability is 50V.
C3	VCC	Output from the startup regulator	Nominally regulated at 7.0V. Connect a 0.1 µF capacitor from this pin to RTN. An external voltage (8V to 14V) can be applied to this pin to reduce internal dissipation. An internal diode connects VCC to VIN.
D1,D2	SW	Switching Node	Internally connected to the buck switch source. Connect to the inductor, diode, and bootstrap capacitor.
D3	BST	Boost pin for bootstrap capacitor	Connect a 0.022 µF capacitor from SW to this pin. The capacitor is charged each off-time via an internal diode.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

VIN to RTN	50V
BST to RTN	64V
SW to RTN (Steady State)	-1.5V
BST to VCC	50V
VIN to SW	50V
BST to SW	14V
VCC to RTN	14V
SGND to RTN	-0.3V to +0.3V
Current out of ISEN	See text
SS to RTN	-0.3V to 4V
All Other Inputs to RTN	-0.3 to 7V
ESD Rating [3]	
Human Body Model	2kV
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Operating Ratings [1]

V_{IN} Voltage	8.0V to 33V
Junction Temperature	−40°C to + 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface** type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V, R_{ON} = 200kΩ. See [1] and [2].

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Start-Up Regulator, V_{CC}						
V_{CC}Reg	V_{CC} regulated output	Vin > 9V	**6.6**	7.0	**7.4**	V
	V_{IN}-V_{CC} dropout voltage	I_{CC} = 0 mA, V_{CC} = $UVLO_{VCC}$ + 250 mV		1.3		V
	V_{CC} output impedance (0 mA ≤ I_{CC} ≤ 5 mA)	V_{IN} = 8V		150		Ω
		V_{IN} = 12V		0.75		
	V_{CC} current limit [3]	V_{CC} = 0V		11		mA
$UVLO_{VCC}$	V_{CC} under-voltage lockout threshold	V_{CC} increasing		5.45		V
	$UVLO_{VCC}$ hysteresis	V_{CC} decreasing		145		mV
	$UVLO_{VCC}$ filter delay	100 mV overdrive		3		µs
	I_{IN} operating current	Non-switching, FB = 3V		0.68	**0.95**	mA
	I_{IN} shutdown current	RON/SD = 0V		85	**160**	µA
Switch Characteristics						
Rds(on)	Buck Switch Rds(on)	I_{TEST} = 200 mA		0.33	**0.7**	Ω
$UVLO_{GD}$	Gate Drive UVLO	V_{BST} - V_{SW} Increasing	**2.65**	4	**4.62**	V

(1) For detailed information on soldering DSBGA packages, refer to Application Note AN-1112 (SNVA009).
(2) Typical specifications represent the most likely parametric norm at 25°C operation.
(3) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface** type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V, R_{ON} = 200kΩ. See (1) and (2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	$UVLO_{GD}$ hysteresis			450		mV
Softstart Pin						
V_{SS}	Pull-up voltage			2.5		V
I_{SS}	Internal current source			11.6		µA
V_{RES}	Restart threshold after OVP shutdown			0.18		V
Current Limit						
I_{LIM}	Threshold	V_{IN} = 8V, V_{FB} = 2.4V	**1.15**	1.35	**1.55**	A
		V_{IN} = 30V, V_{FB} = 2.4V	**1.05**	1.2	**1.45**	
		V_{IN} = 30V, V_{FB} = 1.0V	**0.95**	1.15	**1.35**	
	Response time			150		ns
On Timer						
t_{ON} - 1	On-time (normal operation)	V_{IN} = 10V, R_{ON} = 200 kΩ	**2.1**	2.8	**3.5**	µs
t_{ON} - 2	On-time (normal operation)	V_{IN} = 32V, R_{ON} = 200 kΩ		860		ns
t_{ON} - 3	On-time (current limit)	V_{IN} = 10V, R_{ON} = 200 kΩ		1.13		µs
	Shutdown threshold at RON/SD	Voltage at RON/SD rising	**0.3**	0.65	**1.0**	V
	Shutdown Threshold hysteresis	Voltage at RON/SD falling		40		mV
Off Timer						
t_{OFF}	Minimum Off-time			90		ns
Regulation and Over-Voltage Comparators (FB Pin)						
V_{REF}	FB regulation threshold	SS pin = steady state	**2.445**	2.50	**2.550**	V
	FB over-voltage threshold			2.9		V
	FB bias current	FB = 3V		10		nA
Input Over-Voltage Shutdown						
$V_{IN(OV)}$	Shutdown voltage threshold at VIN	V_{IN} increasing	**33.0**	34.8	**36.9**	V
Thermal Shutdown						
T_{SD}	Thermal shutdown temperature	Junction temperature rising		175		°C
	Thermal shutdown hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient 0 LFPM Air Flow			58		°C/W

Typical Performance Characteristics

Unless otherwise specified the following conditions apply: T_J = 25°C

Efficiency at 1.5 MHz

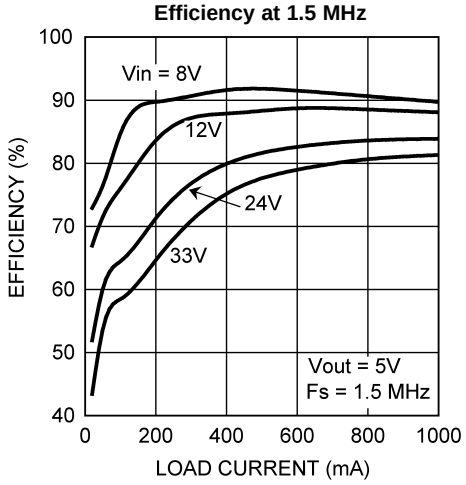


Figure 3.

Efficiency at 2 MHz

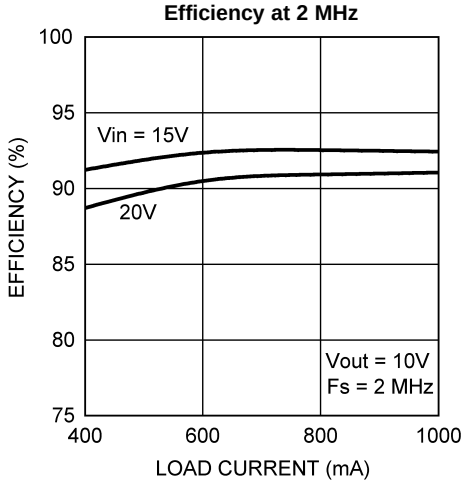


Figure 4.

V_{CC} vs. V_{IN}

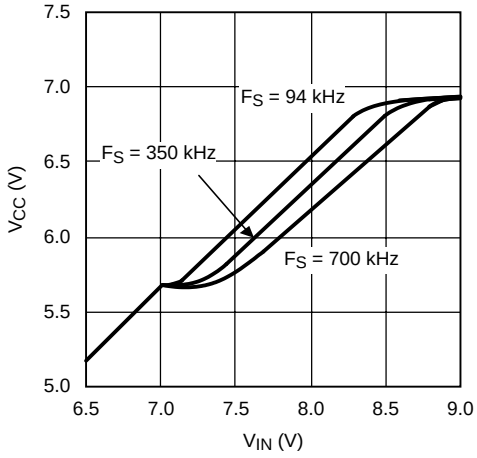


Figure 5.

ON-Time vs. V_{IN} and R_{ON}

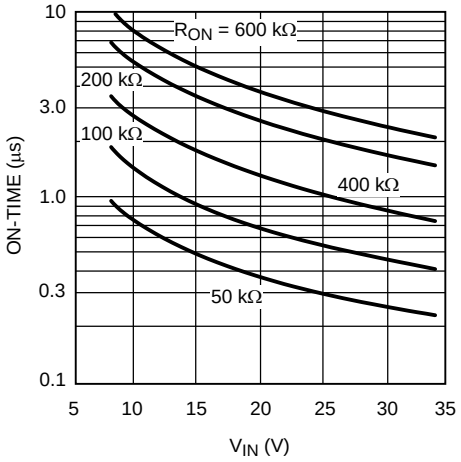


Figure 6.

Valley Current Limit Threshold vs. V_{FB} and V_{IN}

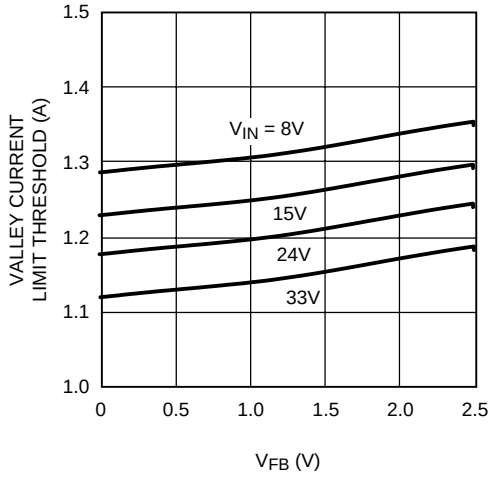


Figure 7.

Voltage at the R_{ON}/SD Pin

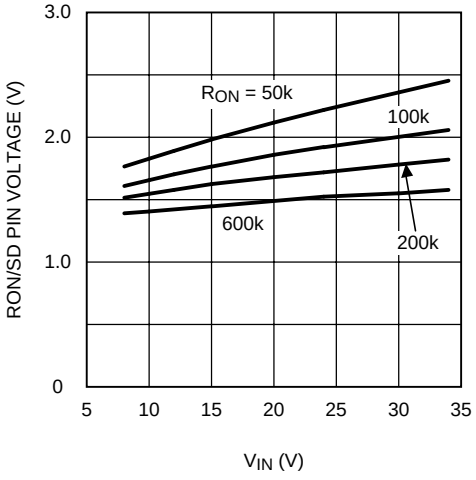


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C

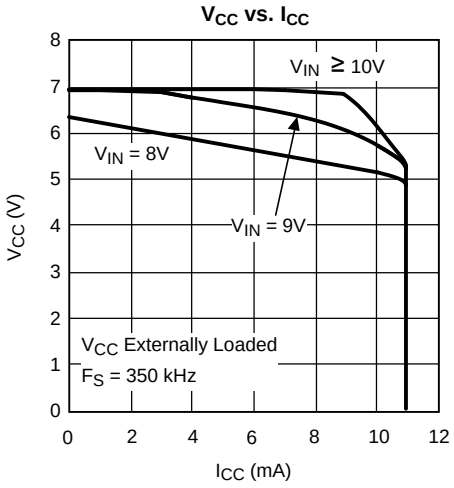


Figure 9.

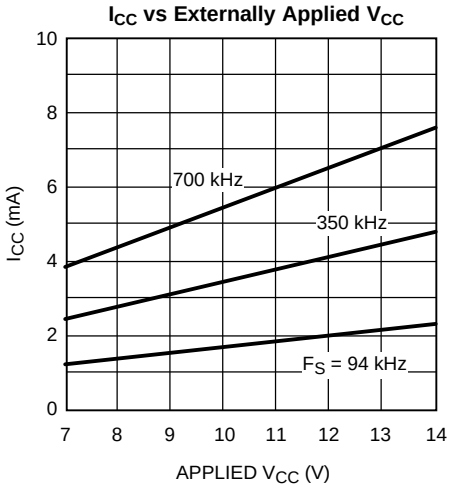


Figure 10.

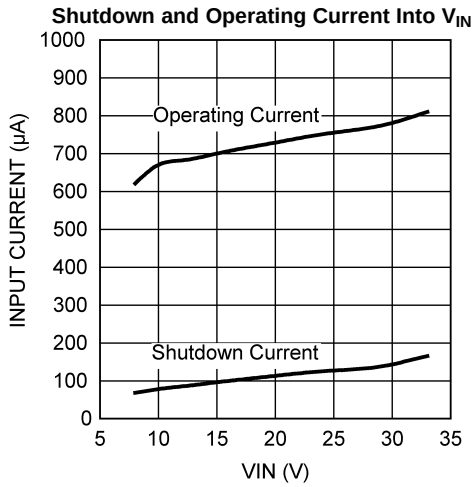
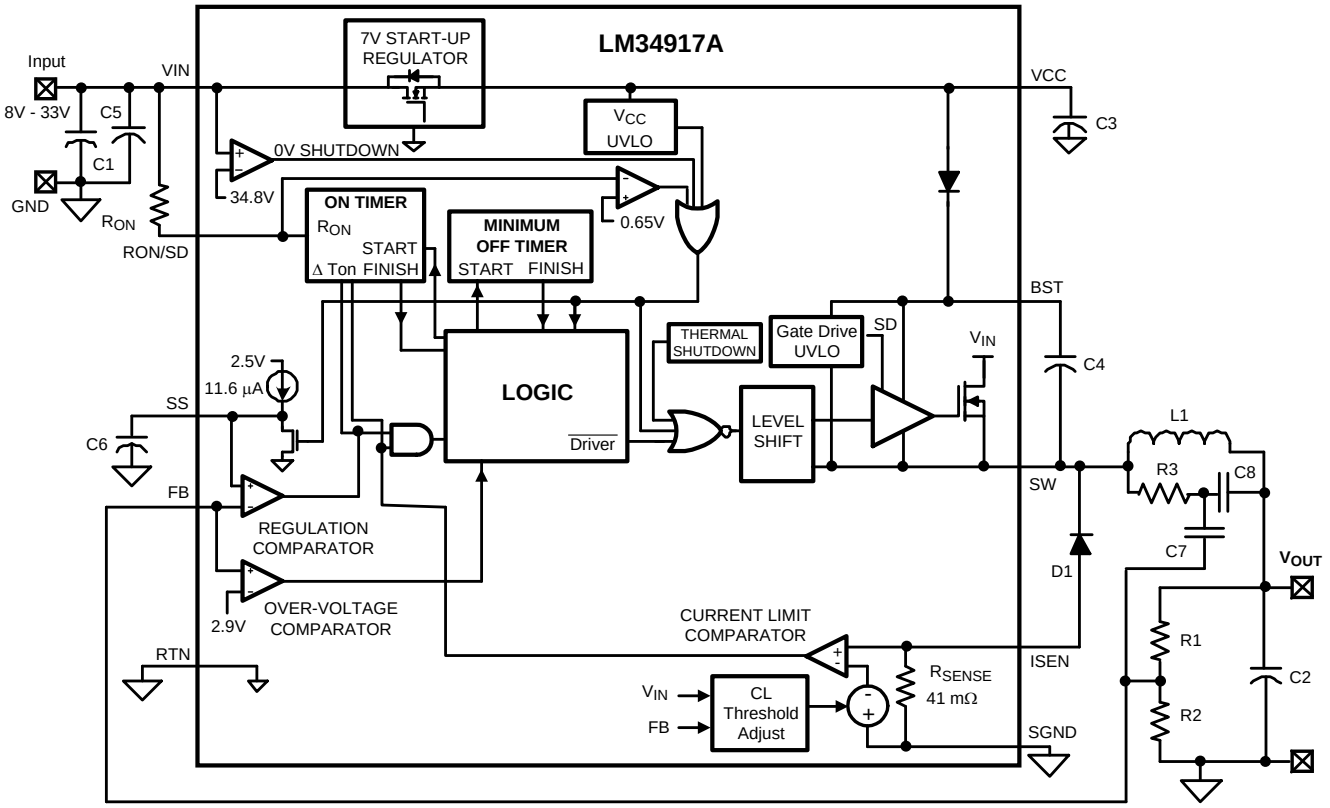


Figure 11.

Typical Application Circuit and Block Diagram



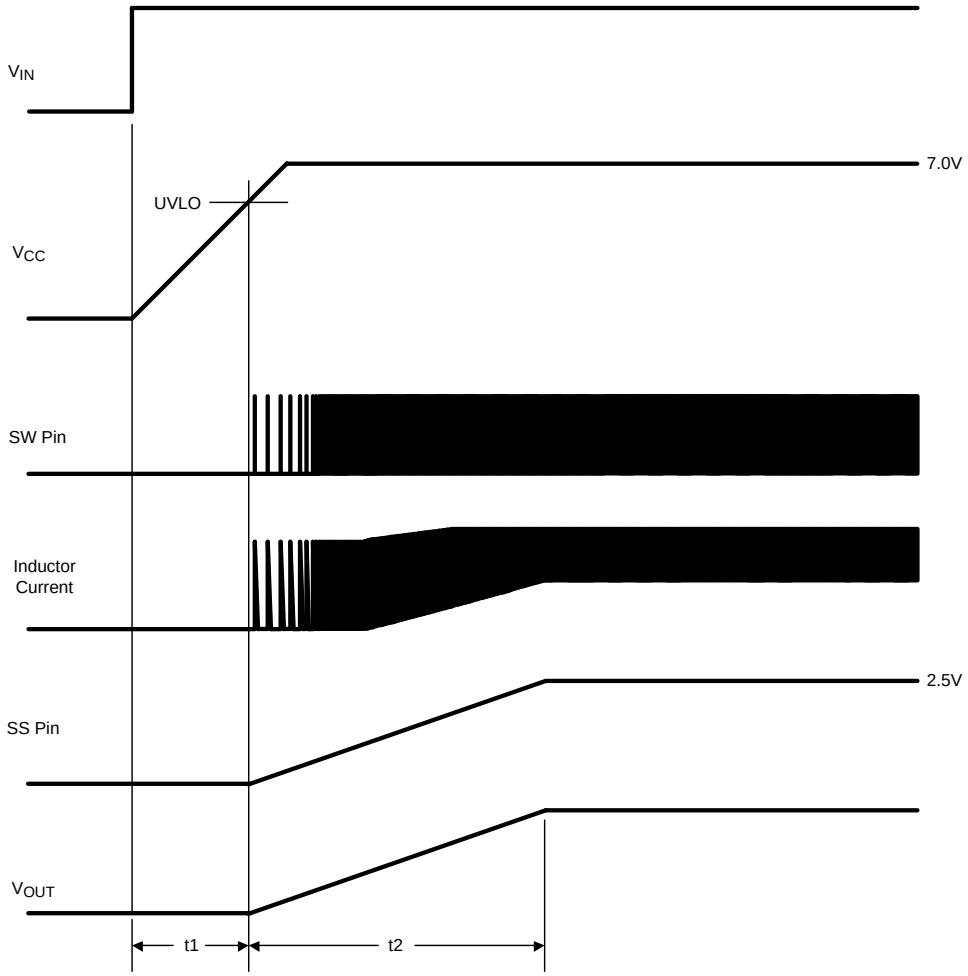


Figure 12. Startup Sequence

FUNCTIONAL DESCRIPTION

The LM34917A Step Down Switching Regulator features all the functions needed to implement a low cost, efficient buck bias power converter capable of supplying at least 1.25A to the load. This high voltage regulator contains an N-Channel buck switch, is easy to implement, and is available in the DSBGA package. The regulator's operation is based on a constant on-time control scheme where the on-time is inversely proportional to the input voltage. This feature results in the operating frequency remaining relatively constant with load and input voltage variations. The feedback control scheme requires no loop compensation resulting in very fast load transient response. The valley current limit scheme protects against excessively high currents if the output is short circuited when V_{IN} is high. To aid in controlling excessive switch current due to a possible saturating inductor the valley current limit threshold changes with input and output voltages, and the on-time is reduced by approximately 50% when current limit is detected. An over-voltage detection at V_{IN} stops the circuit's switching when the input voltage exceeds 34.8V. The LM34917A can be applied in numerous applications to efficiently regulate down higher voltages. Additional features include: Thermal shutdown, V_{CC} under-voltage lock-out, gate drive under-voltage lock-out, and maximum duty cycle limit.

Control Circuit Overview

The LM34917A buck DC-DC regulator employs a control scheme based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (2.5V). If the FB voltage is below the reference the buck switch is switched on for a time period determined by the input voltage and a programming resistor (R_{ON}). Following the on-time the switch remains off until the FB voltage falls below the reference, but for a time not less than the minimum off-time forced by the LM34917A. The buck switch is then switched on for another on-time period.

When in regulation, the LM34917A operates in continuous conduction mode at heavy load currents and discontinuous conduction mode at light load currents. In continuous conduction mode the inductor's current is always greater than zero, and the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The approximate operating frequency is calculated as follows:

$$f_{SW} = \frac{V_{OUT} \times (V_{IN} - 1.35V)}{V_{IN} \times 1.16 \times 10^{-10} \times (R_{ON} + 1.4k)} \quad (1)$$

The buck switch duty cycle is equal to:

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW} = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In discontinuous conduction mode, where the inductor's current reaches zero during the off-time forcing a longer-than-normal off-time, the operating frequency is lower than in continuous conduction mode, and varies with load current. Conversion efficiency is maintained at light loads since the switching losses reduce with the reduction in load and frequency. The approximate discontinuous operating frequency can be calculated as follows:

$$f_{SW} = \frac{V_{OUT}^2 \times L1 \times 1.48 \times 10^{20}}{R_L \times R_{ON}^2} \quad (3)$$

where R_L = the load resistance, and L1 is the circuit's inductor.

The output voltage is set by the two feedback resistors (R1, R2 in the Block Diagram). The regulated output voltage is calculated as follows:

$$V_{OUT} = 2.5 \times (R1 + R2) / R2 \quad (4)$$

Output voltage regulation is based on supplying ripple voltage to the feedback input (FB pin) in phase with the SW pin. The LM34917A requires a minimum of 25 mVp-p of ripple voltage at the FB pin. The ripple is generated as a triangle wavefrom at the junction of R3 and C8 as the SW pin switches high and low, and fed to the FB pin by C7.

If the voltage at FB rises above 2.9V, due to a transient at V_{OUT} or excessive inductor current which creates higher than normal ripple at V_{OUT}, the internal over-voltage comparator immediately shuts off the internal buck switch. The next on-time starts when the voltage at FB falls below 2.5V and the inductor current falls below the current limits threshold.

ON-Time Timer

The on-time for the LM34917A is determined by the R_{ON} resistor and the input voltage (V_{IN}), calculated from:

$$t_{ON} = \frac{1.16 \times 10^{-10} \times (R_{ON} + 1.4\ k\Omega)}{V_{IN} - 1.35V} + 100\ ns \quad (5)$$

The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. To set a specific continuous conduction mode switching frequency (f_{SW}), the R_{ON} resistor is determined from the following:

$$R_{ON} = \frac{V_{OUT} \times (V_{IN} - 1.35V)}{V_{IN} \times 1.16 \times 10^{-10} \times f_{SW}} - 1.4k\Omega \quad (6)$$

Equation 1, Equation 5 and Equation 6 are valid only during normal operation - i.e., the circuit is not in current limit. When the LM34917A operates in current limit, the on-time is reduced by approximately 50%. This feature reduces the peak inductor current which may be excessively high if the load current and the input voltage are simultaneously high. This feature operates on a cycle-by-cycle basis until the load current is reduced and the output voltage resumes its normal regulated value. Equation 1, Equation 5 and Equation 6 have a ±25% tolerance.

Remote Shutdown

The LM34917A can be remotely shut down by taking the RON/SD pin below 0.65V. See Figure 13. In this mode the SS pin is internally grounded, the on-timer is disabled, and bias currents are reduced. Releasing the RON/SD pin allows the circuit to resume operation after the SS pin voltage is below 0.18V. The voltage at the RON/SD pin is normally between 1.4V and 3.5V, depending on V_{IN} and the R_{ON} resistor.

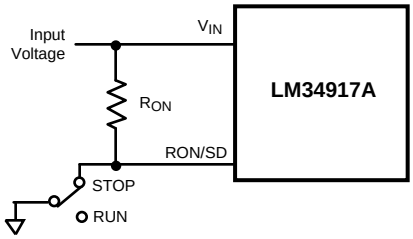


Figure 13. Remote Shutdown

Input Over-Voltage Shutdown

If the input voltage at VIN increases above 34.8V an internal comparator disables the buck switch and the on-timer, and grounds the soft-start pin. Normal operation resumes when the V_{IN} voltage reduces below 34.8V, and when the soft-start voltage (at the SS pin) has reduced below 0.18V.

Current Limit

Current limit detection occurs during the off-time by monitoring the recirculating current flowing out of the ISEN pin. Referring to the Block Diagram, during the off-time the inductor current flows through the load, into SGND, through the internal sense resistor, out of ISEN and through D1 to the inductor. If that current exceeds the current limit threshold the current limit comparator output delays the start of the next on-time period. The next on-time starts when the current out of ISEN is below the threshold **and** the voltage at FB falls below 2.5V. The operating frequency is typically lower due to longer-than-normal off-times.

The valley current limit threshold is a function of the input voltage (V_{IN}) and the output voltage sensed at FB, as shown in the graph "Valley Current Limit Threshold vs. V_{FB} and V_{IN}". This feature reduces the inductor current's peak value at high line and load. To further reduce the inductor's peak current, the next cycle's on-time is reduced by approximately 50% if the voltage at FB is below its threshold when the inductor current reduces to the current limit threshold (V_{OUT} is low due to current limiting).

Figure 14 illustrates the inductor current waveform during normal operation and in current limit. During the first "Normal Operation" the load current is I_{OUT1}, the average of the ripple waveform. As the load resistance is reduced, the inductor current increases until it exceeds the current limit threshold. During the "Current Limited" portion of Figure 14, the current limit threshold lowers since the high load current causes V_{OUT} (and the voltage at FB) to reduce. The on-time is reduced by approximately 50%, resulting in lower ripple amplitude for the inductor's current. During this time the LM34917A is in a constant current mode, with an average load current equal to the current limit threshold + ΔI/2 (I_{OUT2}). Normal operation resumes when the load current is reduced to I_{OUT3}, allowing V_{OUT}, the current limit threshold, and the on-time to return to their normal values. Note that in the second period of "Normal Operation", even though the inductor's peak current exceeds the current limit threshold during part of each cycle, the circuit is not in current limit since the current falls below the threshold before the feedback voltage reduces to its threshold to initiate the next on-time.

The peak current allowed through the buck switch, and the ISEN pin, is 2A, and the maximum allowed average current is 1.5A.

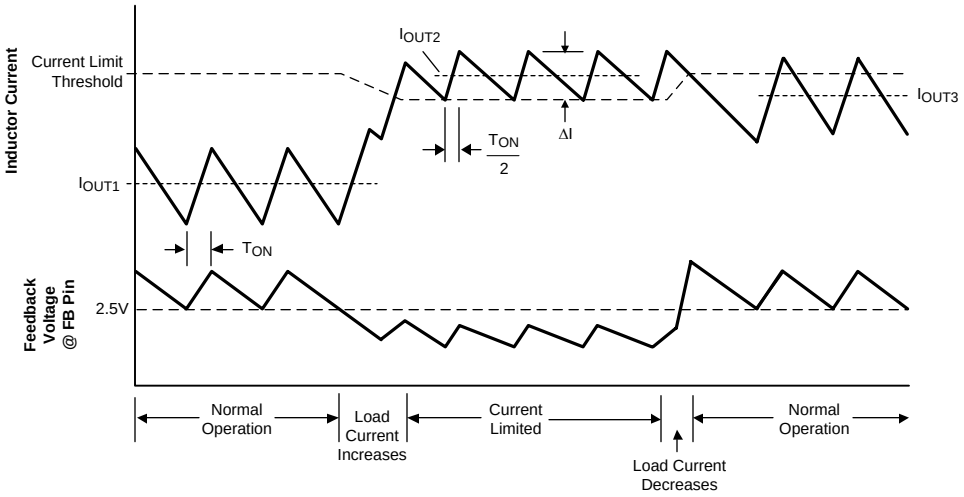


Figure 14. Inductor Current - Normal and Current Limit Operation

N - Channel Buck Switch and Driver

The LM34917A integrates an N-Channel buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.022 µF capacitor (C4) connected between BST and SW provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately -1V, and C4 is recharged for the next on-time from V_{CC} through the internal diode. The minimum off-time ensures a minimum time each cycle to recharge the bootstrap capacitor.

Softstart

The softstart feature allows the converter to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. Upon turn-on, after V_{CC} reaches the under-voltage threshold, an internal 11.6 µA current source charges up the external capacitor at the SS pin to 2.5V (t_2 in Figure 12). The ramping voltage at SS (and the non-inverting input of the regulation comparator) ramps up the output voltage in a controlled manner.

An internal switch grounds the SS pin if V_{CC} is below the under-voltage lockout threshold, if the RON/SD pin is grounded, or if V_{IN} exceeds the overvoltage threshold.

Thermal Shutdown

The LM34917A should be operated so the junction temperature does not exceed 125°C. If the junction temperature increases above that, an internal Thermal Shutdown circuit activates (typically) at 175°C, taking the controller to a low power reset state by disabling the buck switch. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature reduces below 155°C (typical hysteresis = 20°C), normal operation resumes.

Applications Information

EXTERNAL COMPONENTS

The procedure for calculating the external components is illustrated with the following design example. Referring to the Block Diagram, the circuit is to be configured for the following specifications:

- V_{OUT} = 5V
- V_{IN} = 8V to 33V
- Minimum load current = 200 mA
- Maximum load current = 1000 mA
- Switching Frequency = 1.5 MHz
- Soft-start time = 5 ms
- Output voltage ripple level: Minimum

R1 and R2: These resistors set the output voltage. The ratio of the feedback resistors is calculated from:

$$R1/R2 = (V_{OUT}/2.5V) - 1 \quad (7)$$

For this example, R1/R2 = 1. R1 and R2 should be chosen from standard value resistors in the range of 1.0 kΩ – 10 kΩ which satisfy the above ratio. For this example, 2.49 kΩ is chosen for R1 and R2.

R_{ON}: This resistor sets the on-time, and (by default) the switching frequency. Since the maximum frequency is limited by the minimum off-time forced by the LM34917A, first check that the desired frequency is less than:

$$f_{SW} < \frac{V_{IN} - V_{OUT}}{V_{IN} \times 105\ ns} = 3.57\ MHz \text{ at } V_{IN} = 8V \quad (8)$$

The R_{ON} resistor is calculated from Equation 6 using the minimum input voltage:

$$R_{ON} = \frac{V_{OUT} \times (V_{IN(min)} - 1.35V)}{V_{IN(min)} \times 1.16 \times 10^{-10} \times f_{SW}} - 1.4\ k\Omega = 22.49\ k\Omega \quad (9)$$

Equation 5 is used to verify that this value resistor does not set an on-time less than 120 ns at maximum input voltage. A standard value 22.1 kΩ resistor is used, resulting in a nominal frequency of 1.49 MHz. The minimum on-time is 188 ns at Vin = 33V, and the maximum on-time is 510 ns at Vin = 8V.

L1: The main parameter affected by the inductor is the inductor current ripple amplitude (I_{OR}). The minimum load current is used to determine the maximum allowable ripple in order to maintain continuous conduction mode, where the lower peak does not reach 0 mA. This is not a requirement of the LM34917A, but serves as a guideline for selecting L1. For this example, the maximum ripple current should be less than:

$$I_{OR(MAX)} = 2 \times I_{OUT(min)} = 400\ mAp\text{-}p \quad (10)$$

For other applications, if the minimum load current is zero, use 20% of $I_{OUT(max)}$ for $I_{OUT(min)}$ in Equation 10. The ripple amplitude calculated in Equation 10 is then used in the following equation:

$$L1_{(min)} = \frac{t_{on(min)} \times (V_{IN(max)} - V_{OUT})}{I_{OR(max)}} = 13.2\ \mu H \quad (11)$$

A standard value 15 µH inductor is selected. The maximum ripple amplitude, which occurs at maximum V_{IN}, calculates to 351 mA p-p, and the peak current is 1175 mA at maximum load current. Ensure the selected inductor is rated for this peak current.

C2: C2 should typically be no smaller than 3.3 µF, although that is dependent on the frequency and the desired output characteristics. C2 should be a low ESR good quality ceramic capacitor. Experimentation is usually necessary to determine the minimum value for C2, as the nature of the load may require a larger value. A load which creates significant transients requires a larger value for C2 than a non-varying load.

C1 and C5: C1's purpose is to supply most of the switch current during the on-time, and limit the voltage ripple at V_{IN}, since it is assumed the voltage source feeding VIN has some amount of source impedance.

At maximum load current, when the buck switch turns on, the current into V_{IN} suddenly increases to the lower peak of the inductor's ripple current, ramps up to the upper peak, then drops to zero at turn-off. The average current during the on-time is the load current. For a worst case calculation, C1 must supply this average load current during the maximum on-time, without letting the voltage at V_{IN} drop below ≅7.5V. The minimum value for C1 is calculated from:

$$C1 = \frac{I_{OUT\,(max)} \times t_{ON}}{\Delta V} = 1.02\ \mu F \tag{12}$$

where t_{ON} is the maximum on-time, and ΔV is the allowable ripple voltage at V_{IN} (0.5V at V_{IN} = 8V). C5's purpose is to minimize transients and ringing due to long lead inductance leading the VIN pin. A low ESR 0.1 µF ceramic chip capacitor must be located close to the VIN and RTN pins.

C3: The capacitor at the VCC pin provides noise filtering and stability for the VCC regulator. C3 should be no smaller than 0.1 µF, and should be a good quality, low ESR ceramic capacitor. C3's value, and the VCC current limit, determine a portion of the turn-on-time (t1 in Figure 12).

C4: The recommended value for C4 is 0.022 µF. A high quality ceramic capacitor with low ESR is recommended as C4 supplies a surge current to charge the buck switch gate at each turn-on. A low ESR also helps ensure a complete recharge during each off-time.

C6: The capacitor at the SS pin determines the soft-start time, i.e. the time for the output voltage to reach its final value (t_2 in Figure 12). The capacitor value is determined from:

$$C6 = \frac{t_2 \times 11.6\ \mu A}{2.5V} = 0.023\ \mu F \tag{13}$$

R3, C7, C8: The ripple amplitude at V_{OUT} is determined by C2's characteristics and the inductor's ripple current amplitude, and typically ranges from 5 mV to 30 mV over the Vin range. Since the LM34917A's regulation comparator requires a minimum of 25 mVp-p ripple at the FB pin, these three components are added to generate and provide the necessary ripple to FB in phase with the waveform at SW. R3 and C8 are chosen to generate a sawtooth waveform at their junction, and that voltage is AC coupled to the FB pin via C7. To determine the values for R3, C7 and C8, the following procedure is used:

$$\text{Calculate } V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN(min)})) \tag{14}$$

where V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 1V). V_A, the DC voltage at the R3/C8 junction, calculates to 4.63V, and is used in the next equation.

$$R3 \times C8 = \frac{(V_{IN\,(min)} - V_A) \times t_{ON}}{\Delta V} = 17.5 \times 10^{-6} \tag{15}$$

where t_{ON} is the maximum on-time (at minimum input voltage), and ΔV is the desired ripple amplitude at the R3/C8 junction, typically 100 mV. R3 and C8 are chosen from standard value components to satisfy the above product. For this example, 3300 pF is chosen for C8, and 5.23 kΩ is chosen for R3. C7 is chosen large compared to C8, typically 0.1 µF.

D1: A Schottky diode is recommended. Ultra-fast recovery diodes are not recommended as the high speed transitions at the SW pin may inadvertently affect the IC's operation through external or internal EMI. The diode must be rated for the maximum input voltage, the maximum load current, and the peak current which occurs when the current limit and maximum ripple current are reached simultaneously. The diode's average power dissipation is calculated from:

$$P_{D1} = V_F \times I_{OUT} \times (1\text{-}D) \tag{16}$$

where V_F is the diode's forward voltage drop, and D is the on-time duty cycle.

FINAL CIRCUIT

The final circuit is shown in Figure 15, and its performance is shown in Figure 16 and Figure 17. Current limit measured approximately 1.34A at Vin = 8V, and 1.27A at Vin = 33V. The output ripple amplitude measured 4 mVp-p at Vin = 8V, and 14 mVp-p at Vin = 33V.

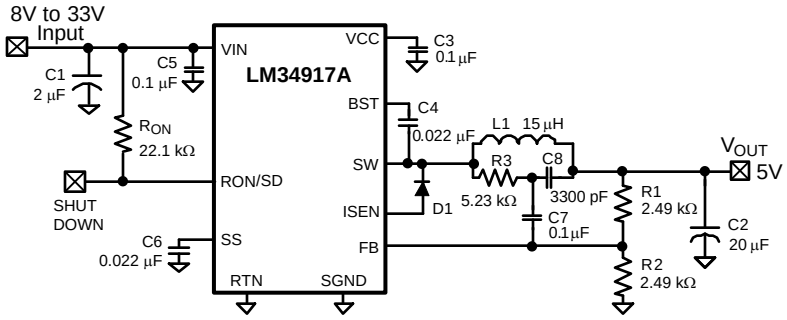


Figure 15. Example Circuit

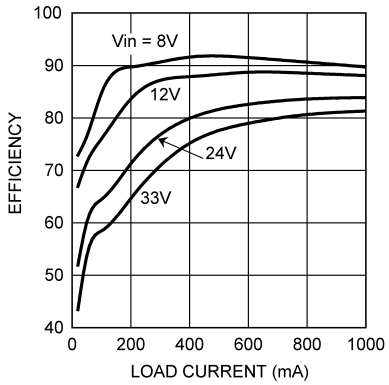


Figure 16. Efficiency vs. Load Current and V_{IN} (Circuit of Figure 15)

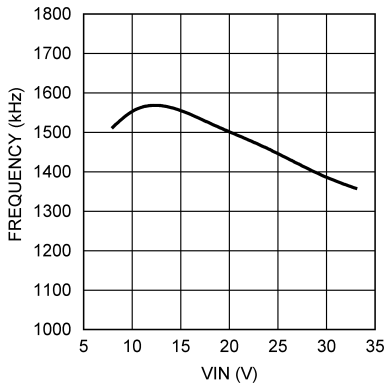


Figure 17. Frequency vs. V_{IN} (Circuit of Figure 15)

ALTERNATE OUTPUT RIPPLE CONFIGURATIONS

For applications which can accept higher levels of ripple at V_{OUT}, the following configurations are simpler and a bit more economical.

a) Alternate #1: In Figure 18, R3, C7 and C8 are removed, and Cff and R4 are installed, resulting in a higher ripple level than the circuit of Figure 15. Ripple is created at V_{OUT} by the inductor's ripple current passing through R4. That ripple voltage is AC coupled to the FB pin through Cff, allowing the minimum ripple at V_{OUT} to be set at 25 mVp-p. The minimum ripple current amplitude ($I_{OR(min)}$) is calculated by re-arranging Equation 11 using $t_{ON(max)}$ and $V_{IN(min)}$. The minimum value for R4 is calculated from:

$$R4 = \frac{25\ mV}{I_{OR\ (min)}} \quad (17)$$

The next larger standard value resistor should be selected for R4 to allow for tolerances. The minimum value for Cff is determined from:

$$Cff = \frac{t_{ON\ (max)}}{(R1//R2)} \tag{18}$$

The next larger standard value capacitor should be used for Cff.

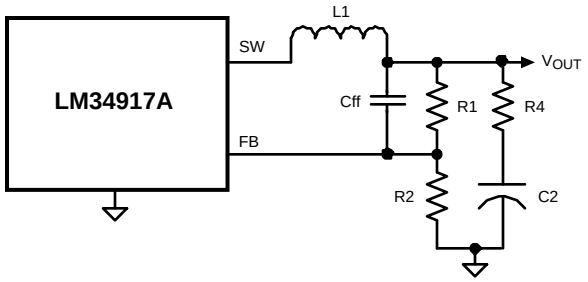


Figure 18. Reduced Ripple Configuration

b) Alternate #2: In Figure 19, R3, C7 and C8 are removed, and R4 is installed, resulting in a higher ripple level than the circuits of Figure 15 and Figure 18. Ripple is created at V_{OUT} by the inductor's ripple current passing through R4. That ripple voltage is coupled to the FB pin through the feedback resistors (R1, R2). Since the LM34917A requires a minimum of 25 mVp-p ripple at the FB pin, the ripple required at V_{OUT} is higher than 25 mVp-p by the gain of the feedback resistors. The minimum ripple current ($I_{OR(min)}$) is calculated by re-arranging Equation 11 using $t_{ON(max)}$ and $V_{IN(min)}$. The minimum value for R4 is calculated from:

$$R4_{(min)} = \frac{25\ mV \times (R1 + R2)}{R2 \times I_{OR\ (min)}} \tag{19}$$

The next larger standard value resistor should be used for R4.

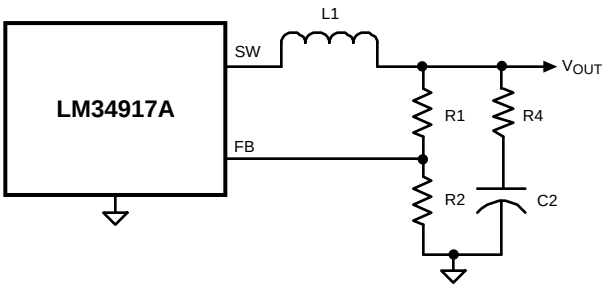


Figure 19. Maximum Ripple Configuration

c) Alternate minimum ripple configuration: The circuit in Figure 20 is the same as that in Figure 19, except the output voltage is taken from the junction of R4 and C2. The ripple at V_{OUT} is determined by the inductor's ripple current and C2's characteristics. However, R4 slightly degrades the load regulation. This circuit may be suitable if the load current is fairly constant. R4 is calculated as described in Alternate #2 above.

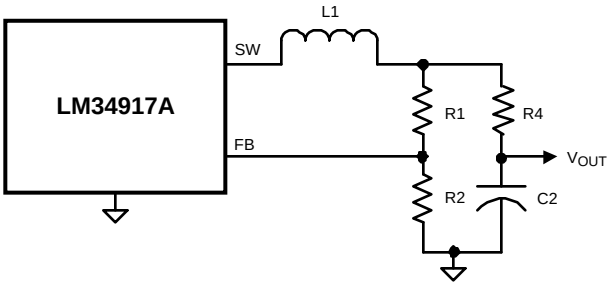


Figure 20. Alternate Minimum Output Ripple Configuration

Minimum Load Current

The LM34917A requires a minimum load current of 1 mA. If the load current falls below that level, the bootstrap capacitor (C4) may discharge during the long off-time, and the circuit will either shutdown, or cycle on and off at a low frequency. If the load current is expected to drop below 1 mA in the application, R1 and R2 should be chosen low enough in value so they provide the minimum required current at nominal V_{OUT}.

PC BOARD LAYOUT

Refer to application note AN-1112 for PC board guidelines for the DSBGA package.

The LM34917A regulation, over-voltage, and current limit comparators are very fast, and respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible, and all of the components must be as close as possible to their associated pins. The two major current loops have currents which switch very fast, and so the loops should be as small as possible to minimize conducted and radiated EMI. The first loop is that formed by C1, through the VIN to SW pins, L1, C2, and back to C1.The second current loop is formed by D1, L1, C2 and the SGND and ISEN pins.

The power dissipation within the LM34917A can be approximated by determining the total conversion loss (P_{IN} - P_{OUT}), and then subtracting the power losses in the free-wheeling diode and the inductor. The power loss in the diode is approximately:

$$P_{D1} = Iout \times V_F \times (1\text{-}D) \quad (20)$$

where Iout is the load current, V_F is the diode's forward voltage drop, and D is the on-time duty cycle. The power loss in the inductor is approximately:

$$P_{L1} = Iout^2 \times R_L \times 1.1 \quad (21)$$

where R_L is the inductor's DC resistance, and the 1.1 factor is an approximation for the AC losses. If it is expected that the internal dissipation of the LM34917A will produce excessive junction temperatures during normal operation, good use of the PC board's ground plane can help to dissipate heat. Additionally the use of wide PC board traces, where possible, can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM34917ATL/NOPB	Active	Production	DSBGA (YZR) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SRHA
LM34917ATL/NOPB.A	Active	Production	DSBGA (YZR) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SRHA
LM34917ATL/NOPB.B	Active	Production	DSBGA (YZR) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SRHA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

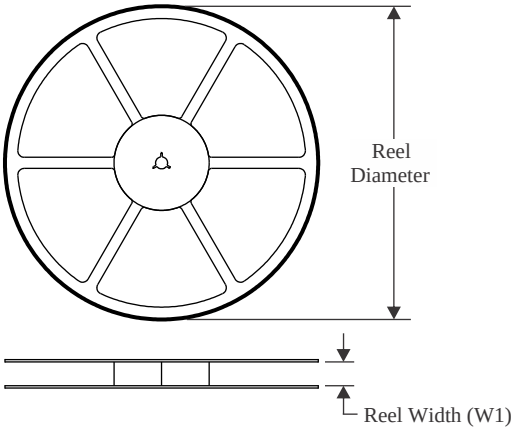
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

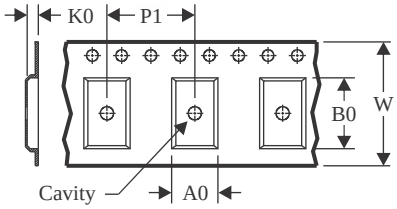
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

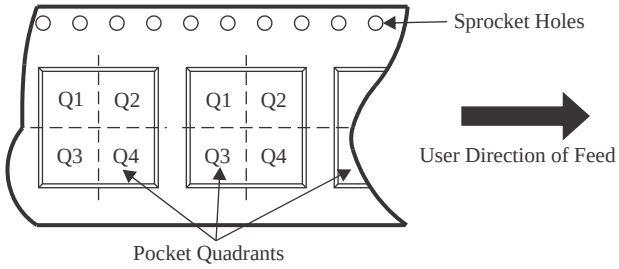


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

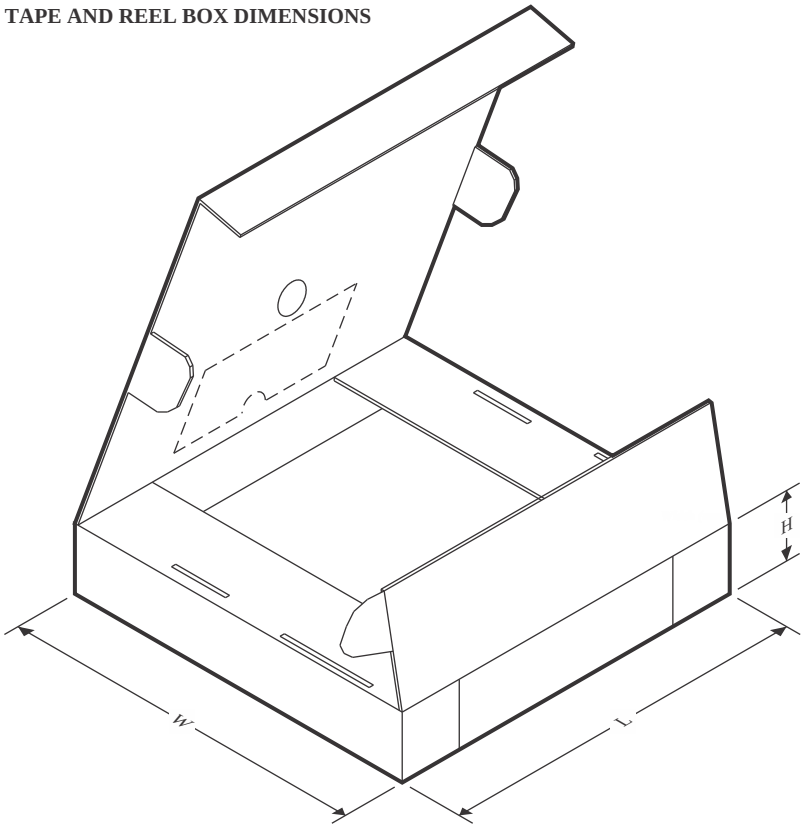
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM34917ATL/NOPB	DSBGA	YZR	12	250	178.0	8.4	2.01	2.57	0.76	4.0	8.0	Q1

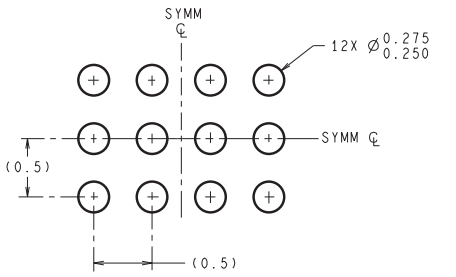
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

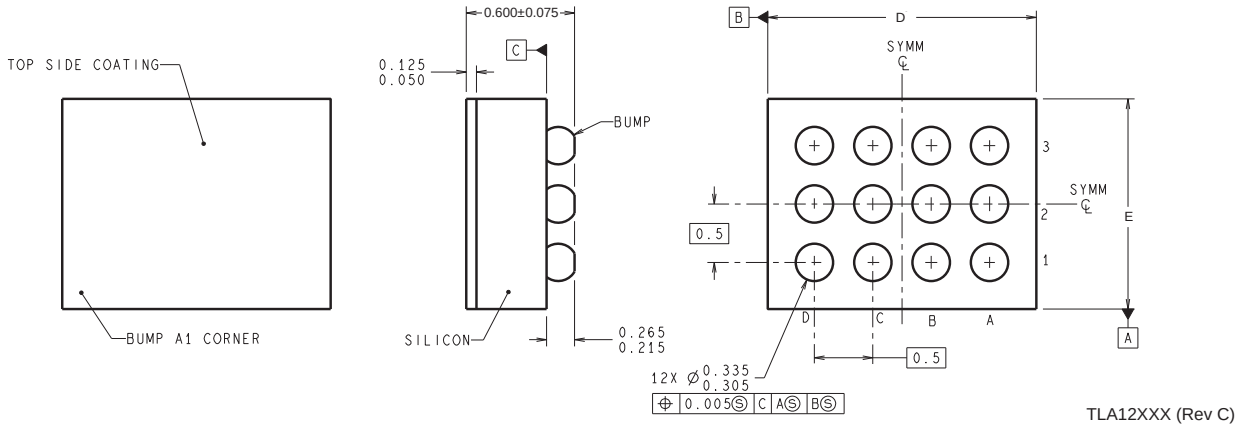
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM34917ATL/NOPB	DSBGA	YZR	12	250	208.0	191.0	35.0

YZR0012



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TLA12XXX (Rev C)

D: Max = 2.33 mm, Min = 2.269 mm

E: Max = 1.987 mm, Min =1.926 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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