LM5021-Q1 AC-DC Current-Mode PWM Controller

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM Classification Level 2: ±2 kV
  - Device CDM Classification Level C4B: 750 V
- Ultra-low Startup Current (25 µA Maximum)
- Current Mode Control
- Skip Cycle Mode for Low Standby Power
- Single Resistor Programmable Oscillator
- Synchronizable Oscillator
- Adjustable Soft-Start
- Integrated 0.7-A Peak Gate Driver
- Direct Opto-Coupler Interface
- Maximum Duty Cycle Limiting (80% for LM5021-1 or 50% for LM5021-2)
- Slope Compensation (LM5021-1 Only)
- Undervoltage Lockout (UVLO) with Hysteresis
- Cycle-by-Cycle Overcurrent Protection
- Hiccup Mode for Continuous Overload Protection
- Leading Edge Blanking of Current Sense Signal
- Package: VSSOP-8

2 Applications

- DCM/CCM Flyback Converters
- Industrial Power Conversion
- SMPS for Smart Meters and Audio Amplifiers
- Building Automation and White Goods SMPS
- Isolated Telecom Power Supplies

3 Description

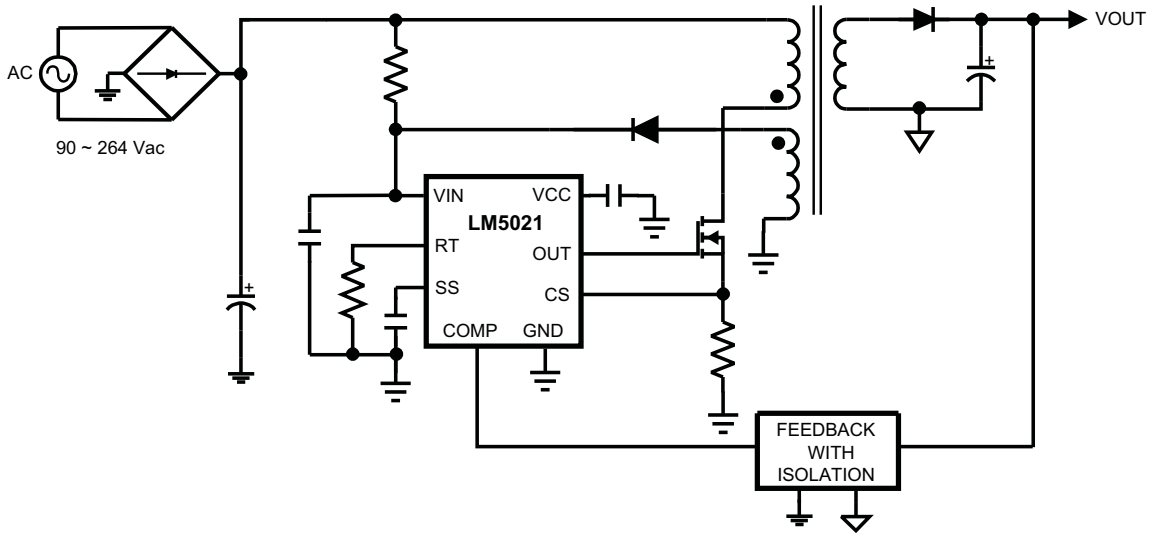
The LM5021 off-line pulse width modulation (PWM) controller contains all of the features needed to implement highly efficient off-line single-ended flyback and forward power converters using current-mode control. The LM5021 features include an ultra-low (25 µA) start-up current, which minimizes power losses in the high voltage start-up network. A skip cycle mode reduces power consumption with light loads for energy conserving applications (ENERGY STAR®, CECP, and so forth). Additional features include under-voltage lockout, cycle-by-cycle current limit, hiccup mode overload protection, slope compensation, soft-start and oscillator synchronization capability. This high performance 8-pin IC has total propagation delays less than 100 ns and a 1-MHz capable oscillator that is programmed with a single resistor.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5021-Q1	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Diagram



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4 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release.

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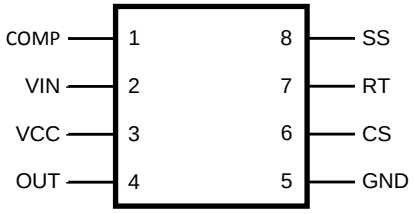
5 Pin Configuration and Functions

8-Pin VSSOP
Package DGK
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	COMP	I	Control input for the Pulse Width Modulator and Hiccup comparators.	COMP pull-up is provided by an internal 5K resistor which may be used to bias an opto-coupler transistor.
2	VIN	I	Input voltage.	Input to start-up regulator. The VIN pin is clamped at 36 V by an internal zener diode.
3	VCC	O	Output only of a linear bias supply regulator. Nominally 8.5 V.	VCC provides bias to controller and gate drive sections of the LM5021. An external capacitor must be connected from this pin to ground.
4	OUT	O	MOSFET gate driver output.	High current output to the external MOSFET gate input with source/sink current capability of 0.3 A and 0.7 A respectively.
5	GND	—	Ground return.	
6	CS	I	Current Sense input.	Current sense input for current mode control and over-current protection. Current limiting is accomplished using a dedicated current sense comparator. If the CS comparator input exceeds 0.5 V the OUT pin switches low for cycle-by-cycle current limit. CS is held low for 90ns after OUT switches high to blank the leading edge current spike.
7	RT / SYNC	O	Oscillator timing resistor pin and synchronization input.	An external resistor connected from RT to GND sets the oscillator frequency. This pin will also accept synchronization pulses from an external clock.
8	SS	O	Soft-start / Hiccup time	An external capacitor and an internal 22 µA current source set the soft-start ramp. The soft -start capacitor controls both the soft-start rate and the hiccup mode period.

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6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

	MIN	MAX	UNIT
VIN to GND	–0.3	30	V
VIN Clamp Continuous Current		5	mA
CS to GND	–0.3	1.25	V
RT to GND	–0.3	5.5	V
All other pins to GND	–0.3	7.0	V
Operating Junction Temperature		150	
Storage temperature range, T_{stg}	–65	150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. *Recommended Operation Conditions* are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics* .
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 — All pins	±750	
		Charged-device model (CDM), per AEC Q100-011 — Corner pins (1, 4, 5, and 8)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operation Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN Voltage (1)	8	30	V
Junction Temperature	–40	125	°C

(1) After initial turn-on at VIN = 20 V.

6.4 Thermal Information

THERMAL METRIC (1)		LM5021 DGK 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	83.2	
ψ_{JT}	Junction-to-top characterization parameter	5.9	
ψ_{JB}	Junction-to-board characterization parameter	81.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

MIN and MAX limits apply –40°C ≤ T_J ≤ 125°C. Unless otherwise specified: T_J= +25°C, V_{IN} = 15 V, R_T = 44.2 kΩ.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP CIRCUIT						
I_{ST}	Start up current	Before VCC Enable		18	25	µA
V_{VIN_EN}	VCC Regulator enable threshold		17	20	23	V
V_{VIN_DIS}	VCC Regulator disable threshold			7.25		V
V_{VIN_CMP}	VIN ESD clamp voltage	I = 5 mA	30	36	40	V
I_{VIN}	Operating supply current	COMP = 0 VDC		2.5	3.75	mA
VCC SUPPLY						
V_{VCC_EN}	Controller enable threshold		6.5	7	7.5	V
V_{VCC_DIS}	Controller disable threshold		5.3	5.8	6.3	V
V_{VCC}	VCC regulated output	No External Load	8	8.5	9	V
V_{VCC_DO}	VCC dropout voltage (VIN - VCC)	I = 5 mA		1.7		V
I_{VCC_LIM}	VCC regulator current limit	VCC = 7.5 V (2)	15	22		mA
SKIP CYCLE MODE COMPARATOR						
V_{SKP}	Skip cycle mode enable threshold	⅓ [COMP - 1.25 V]	75	125	175	mV
V_{SKP_HYS}	Skip cycle mode hysteresis			5		mV
CURRENT LIMIT						
t_{CS_DLY}	CS limit to OUT delay	CS stepped from 0 to 0.6 V, time to OUT transition low, C_{load} = 0		35		ns
V_{CS_MAX}	CS limit threshold		0.45	0.5	0.55	V
t_{LEB}	Leading edge blanking time			90		ns
R_{CS_BNK}	CS blanking sinking impedance			35	55	Ω
SOFT-START						
V_{SS_OCV}	SS pin open-circuit voltage		4.3	5.2	6.1	V
I_{SS}	Soft-start current source		15	22	30	µA
V_{SS_OFF}	Soft-start to COMP offset		0.35	0.55	0.75	V
R_{COMP}	COMP sinking impedance	During SS ramp		60		Ω
OSCILLATOR						
F_{OSC}	Frequency1 (RT = 44.2K)		135	150	165	kHz
F_{OSC}	Frequency2 (RT = 13.3K)		440	500	560	kHz
V_{SYNC}	Sync threshold		2.4	3.2	3.8	V
PWM COMPARATOR						
t_{PWM_DLY}	COMP to OUT delay	COMP set to 2 V CS stepped 0 to 0.4 V, time to OUT transition low, C_{load} = 0		20		ns
D_{MIN}	Min duty cycle	COMP = 0 V			0%	
D_{MAX}	Max duty cycle (-1 Device)		75%	80%	85%	
D_{MAX}	Max duty cycle (-2 Device)			50%		
K_{PWM}	COMP to PWM comparator gain			0.33		
V_{COMP_OC}	COMP open circuit voltage		4.2	5.1	6	V
V_{COMP_MAXD}	COMP at max duty cycle			2.75		V
I_{COMP}	COMP short circuit current	COMP = 0 V	0.6	1.1	1.5	mA

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Device thermal limitations may limit usable range.

Electrical Characteristics (continued)

MIN and MAX limits apply –40°C ≤ T_J ≤ 125°C. Unless otherwise specified: T_J= +25°C, V_{IN} = 15 V, R_T = 44.2 kΩ.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SLOPE COMPENSATION						
V_{SLP}	Slope comp amplitude (LM5021-1 only)	CS pin to PWM Comparator offset at maximum duty cycle	70	90	135	mV
OUTPUT SECTION						
V_{OUTH}	OUT high saturation	I_{OUT} = 50 mA, VCC - OUT		0.6	1.1	V
V_{OUTL}	OUT low saturation	I_{OUT} = 100 mA		0.3	1	V
I_{O_SRC}	Peak source current	OUT = VCC/2		0.3		A
I_{O_SNK}	Peak sink current	OUT = VCC/2		0.7		A
t_r	Rise time	C_{load} = 1nF		25		ns
t_f	Fall time	C_{load} = 1nF		10		ns
HICCUP MODE						
V_{OVLD}	Over load detection threshold	COMP pin	$V_{SS\text{-}OCV}$ – 0.8	$V_{SS\text{-}OCV}$ – 0.6	$V_{SS\text{-}OCV}$– 0.4	V
V_{HIC}	Hiccup mode threshold	SS pin	$V_{SS\text{-}OCV}$ – 0.8	$V_{SS\text{-}OCV}$ – 0.6	$V_{SS\text{-}OCV}$– 0.4	V
V_{RST}	Hiccup mode Restart threshold	SS pin	0.1	0.3	0.5	V
I_{DTCS}	Dead-time current source		0.1	0.25	0.4	µA
I_{OVCS}	Overload detection timer current source		6	10	14	µA

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6.6 Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C.

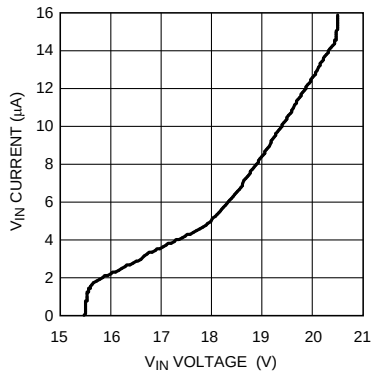

Figure 1. VIN Start-Up Current

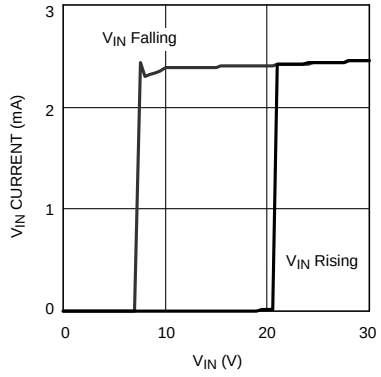

Figure 2. VIN UVLO

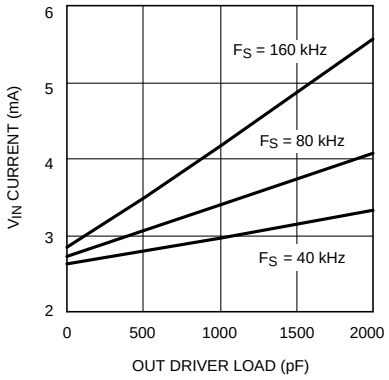

Figure 3. VIN Current vs OUT Load

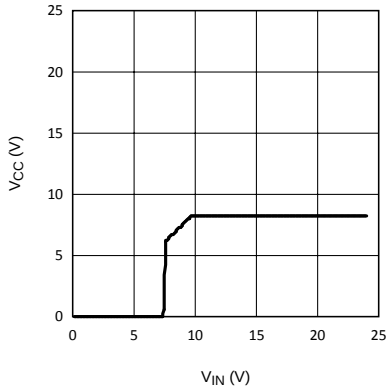

Figure 4. VIN Voltage Falling vs VCC Voltage

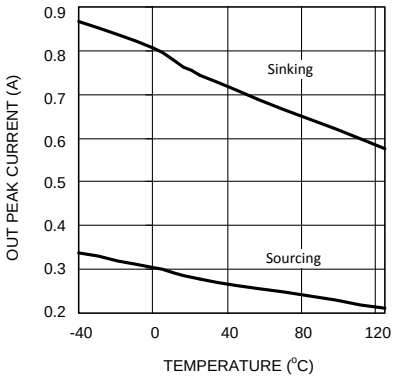

Figure 5. OUT Driver Current vs Temperature

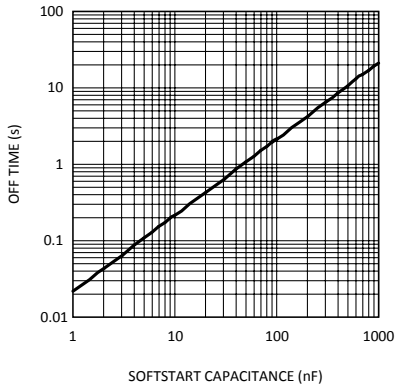

Figure 6. Hiccup Mode Deadtime vs Softstart Capacitance

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C.

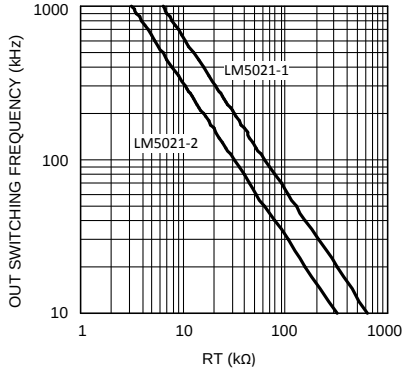

Figure 7. Output Switching Frequency vs RT

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7 Detailed Description

7.1 Overview

The LM5021 is a single ended current mode controller primarily intended for use in offline forward or flyback converters. It is also useful for boost converters. Low startup current and a wide UVLO hysteresis make low dissipation startup circuits simple to implement. An on board 7-V regulator supplies stable power for device operation and can supply external circuitry. A soft start function minimizes stresses during startup and allows the converter to come to steady state operating conditions gradually.

The device comes in two versions with different maximum duty cycles. The LM5021-1 has a maximum duty cycle of 80% while the LM5021-2 has a maximum duty cycle of 50%. For current mode control applications where the duty cycle can exceed 50%, slope compensation is implemented by simply adding a resistor between the LM5021-1 CS pin and the current sense filter capacitor.

Cycle-by-cycle overcurrent sensing provides robust protection. A 500-mV maximum current sense threshold minimizes power dissipation in supplies that sense the main switch current directly with a resistor. For a sustained overcurrent condition, the controller will enter a hiccup mode to reduce component stresses. The controller automatically restarts when the overload condition is removed.

The switching frequency is programmable using a single resistor connected from the RT pin to GND. For applications that require it, the switching frequency can be synchronized to an external clock source by capacitively coupling a pulse train into the RT pin.

Skip cycle operation is implemented to reduce input power and increase efficiency at light load conditions. For applications where this is not desirable, skip cycle operation may be disabled by adding an offset voltage to the CS pin.

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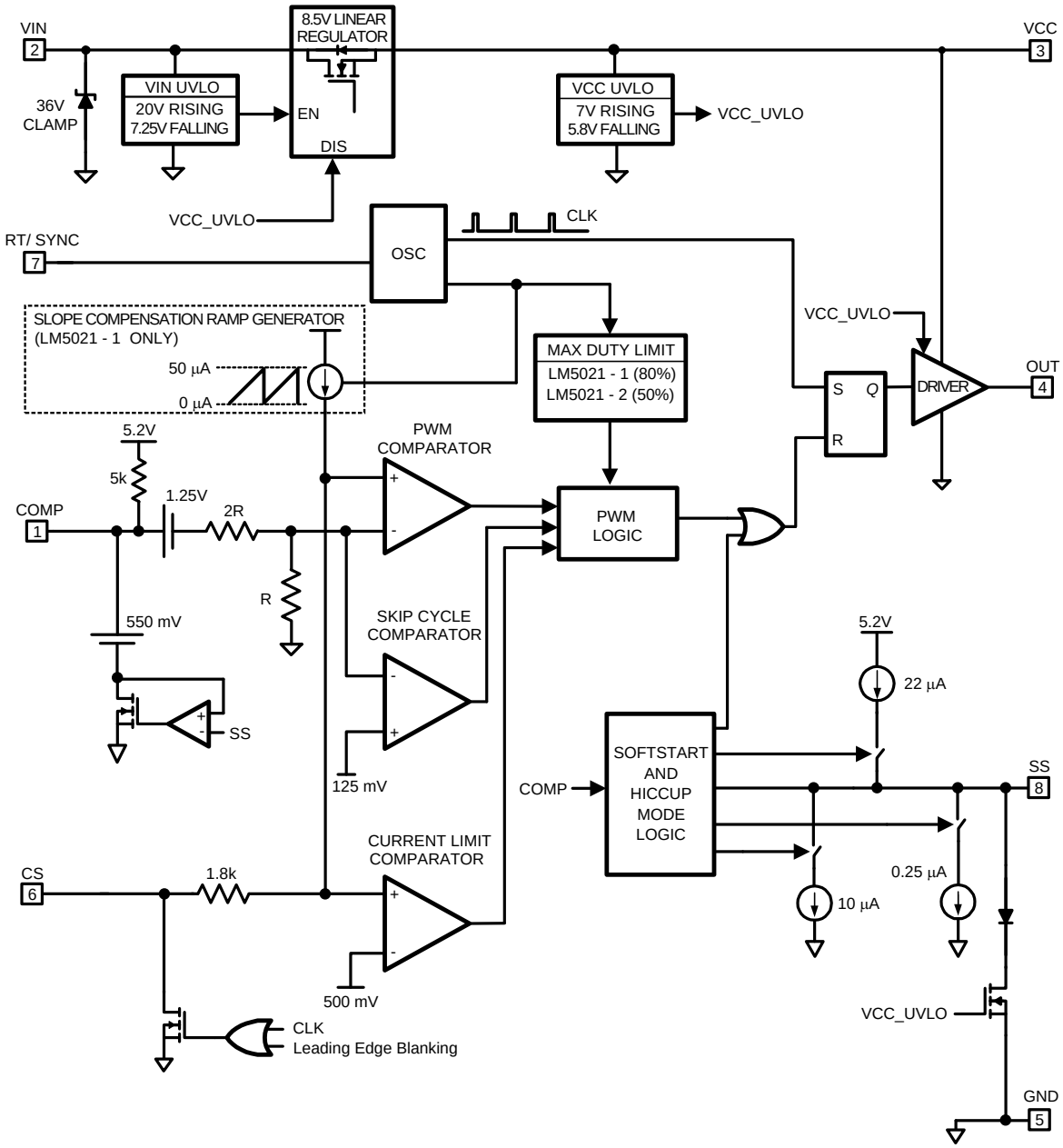
7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PWM Comparator and Slope Compensation

The PWM comparator compares the current sense signal with the loop error voltage from the COMP pin. The COMP pin voltage is reduced by 1.25 V then attenuated by a 3:1 resistor divider. The PWM comparator input offset voltage is designed such that less than 1.25 V at the COMP pin will result in a zero duty cycle at the controller output.

For duty cycles greater than 50 percent, current mode control circuits are subject to sub-harmonic oscillation. By adding an additional fixed slope voltage ramp signal (slope compensation) to the current sense signal, this oscillation can be avoided. The LM5021-1 integrates this slope compensation by summing a ramp signal generated by the oscillator with the current sense signal. The slope compensation is generated by a current ramp driven through an internal 1.8 kΩ resistor connected to the CS pin. Additional slope compensation may be added by increasing the resistance between the current sense filter capacitor and the CS pin, thereby increasing the voltage ramp created by the oscillator current ramp. Since the LM5021-2 is not capable of duty cycles greater than 50%, there is no slope compensation feature in this device.

7.3.2 Current Limit and Current Sense

The LM5021 provides a cycle-by-cycle over current protection feature. Current limit is triggered by an internal current sense comparator threshold which is set at 500 mV. If the CS pin voltage plus the slope compensation voltage exceeds 500 mV, the OUT pin output pulse will be immediately terminated.

An RC filter, located near the LM5021, is recommended for the CS pin to attenuate the noise coupled from the power FET's gate to source. The CS pin capacitance is discharged at the end of each PWM clock cycle by an internal switch. The discharge switch remains on for an additional 90ns leading edge blanking interval to attenuate the current sense transient that occurs when the external power FET is turned on. In addition to providing leading edge blanking, this circuit also improves dynamic performance by discharging the current sense filter capacitor at the conclusion of every cycle.

The LM5021 CS comparator is very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the IC (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor, which should also be located close to the IC. If a current sense resistor located in the power FET's source is used for current sense, a low inductance resistor is required. In this case, all of the noise sensitive low current grounds should be connected in common near the IC and then a single connection should be made to the power ground (sense resistor ground point).

7.3.3 Oscillator, Shutdown and Sync Capability

A single external resistor connected between RT and GND pins sets the LM5021 oscillator frequency. The LM5021-2 device, with 50% maximum duty cycle, includes an internal flip-flop that divides the oscillator frequency by two. This method produces a precise 50% maximum duty cycle limit. Because of this frequency divider, the oscillator frequency of the LM5021-2 is actually twice the frequency of the gate drive output (OUT). For the LM5021-1 device, the oscillator frequency and the operational output frequency are the same. To set a desired output switching frequency (Fsw), the RT resistor can be calculated from:

LM5021-1:

$$RT = \frac{6.63 \times 10^9}{F_{SW}} \tag{1}$$

LM5021-2:

$$RT = \frac{6.63 \times 10^9}{2 \times F_{SW}} \tag{2}$$

Feature Description (continued)

The LM5021 can also be synchronized to an external clock. The external clock must have a higher frequency than the free running oscillator frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin with a 100pF capacitor. A peak voltage level greater than 3.8 V at the RT pin is required for detection of the sync pulse. The dc voltage across the RT resistor is internally regulated at 2 V. Therefore, the ac pulse superimposed on the RT resistor must have 1.8-V or greater amplitude to successfully synchronize the oscillator. The sync pulse width should be set between 15 ns to 150 ns by the external components. The RT resistor is always required, whether the oscillator is free-running or externally synchronized. The RT resistor should be located very close to the device and connected directly to the pins of the LM5021 (RT and GND).

7.3.4 Gate Driver and Max Duty Cycle Limit

The LM5021 provides a gate driver (OUT), which can source peak current of 0.3A and sink 0.7A. The LM5021 is available in two duty-cycle limit options. The maximum output duty-cycle is typically 80% for the LM5021-1 option, and precisely equal to 50% for the LM5021-2 option. The maximum duty cycle function for the LM5021-2 is accomplished with an internal toggle flip-flop to ensure an accurate duty cycle limit. The internal oscillator frequency of the LM5021-2 is therefore twice the switching frequency of the PWM controller (OUT pin).

The 80% maximum duty-cycle function for the LM5021-1 is determined by the internal oscillator. For the LM5021-1 the internal oscillator frequency and the switching frequency of the PWM controller are the same.

7.3.5 Soft-Start

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and current surges. An internal 22 µA current source charges an external capacitor connected to the SS pin. The capacitor voltage will ramp up slowly, limiting the COMP pin voltage and the duty cycle of the output pulses. The soft-start capacitor is also used to generate the hiccup mode delay time when the output of the switching power supply is continuously overloaded.

7.3.6 Hiccup Mode Overload Current Limiting

Hiccup mode is a method of protecting the power supply from over-heating and damage during an extended overload condition. When the output fault is removed the power supply will automatically restart.

Figure 8, Figure 9, and Figure 10 illustrate the equivalent circuit of the hiccup mode for LM5021 and the relevant waveforms. During start-up and in normal operation, the external soft-start capacitor Css is pulled up by a current source that delivers 22 µA to the SS pin capacitor. In normal operation, the soft-start capacitor continues to charge and eventually reaches the saturation voltage of the current source (V_{SS_OCV}, nominally 5.2 V). During start-up the COMP pin voltage follows the SS capacitor voltage and gradually increases the peak current delivered by the power supply. When the output of the switching power supply reaches the desired voltage, the voltage feedback amplifier takes control of the COMP signal (via the opto-coupler). In normal operation the COMP level is held at an intermediate voltage between 1.25 V and 2.75 V controlled by the voltage regulation loop. When the COMP pin voltage is below 1.25 V, the duty-cycle is zero. When the COMP level is above 2.75 V, the duty cycle will be limited by the 0.5-V threshold of cycle-by-cycle current limit comparator.

If the output of the power supply is overloaded, the voltage regulation loop demands more current by increasing the COMP pin control voltage. When the COMP pin exceeds the over voltage detection threshold (V_{OVLD}, nominally 4.6 V), the SS capacitor Css will be discharged by a 10 µA overload detection timer current source, I_{OVCS}. If COMP remains above V_{OVLD} long enough for the SS capacitor to discharge to the Hiccup mode threshold (V_{HIC}, nominally 4.6 V), the controller enters the hiccup mode. The OUT pin is then latched low and the SS capacitor discharge current source is reduced from 10 µA to 0.25 µA, the dead-time current source, I_{DTCS}. The SS pin voltage is slowly reduced until it reaches the Restart threshold (V_{RST}, nominally 0.3 V). Then a new start-up sequence commences with 22 µA current source charging the capacitor C_{SS}. The slow discharge of the SS capacitor from the Hiccup threshold to the Restart threshold provides an extended off time that reduces the overheating of components including diodes and MOSFETs due to the continuous overload. The off time during the hiccup mode can be calculated from the following equation:

$$Toff = \frac{C_{SS} \times (V_{HC} - V_{RST})}{I_{DTCS}} = \frac{C_{SS} \times (4.6V - 0.3V)}{0.25\ \mu A} \quad (3)$$

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Feature Description (continued)

Example:

Toff = 808 ms, assuming the C_{SS} capacitor value is 0.047 µF

Short duration intermittent overloads will not trigger the hiccup mode. The overload duration required to trigger the hiccup response is set by the capacitor C_{SS}, the 10 µA discharge current source and voltage difference between the saturation level of the SS pin and the Hiccup mode threshold. Figure 10 shows the waveform of SS pin with a short duration overload condition. The overload time required to enter the hiccup mode can be calculated from the following equation:

$$\text{Toverload} = \frac{C_{SS} \times (V_{SS_OCV} - V_{HC})}{I_{OVCS}} = \frac{C_{SS} \times 0.6V}{10\ \mu A} \quad (4)$$

Example:

Toverload = 2.82 ms, assuming the C_{SS} capacitor value is 0.047 µF

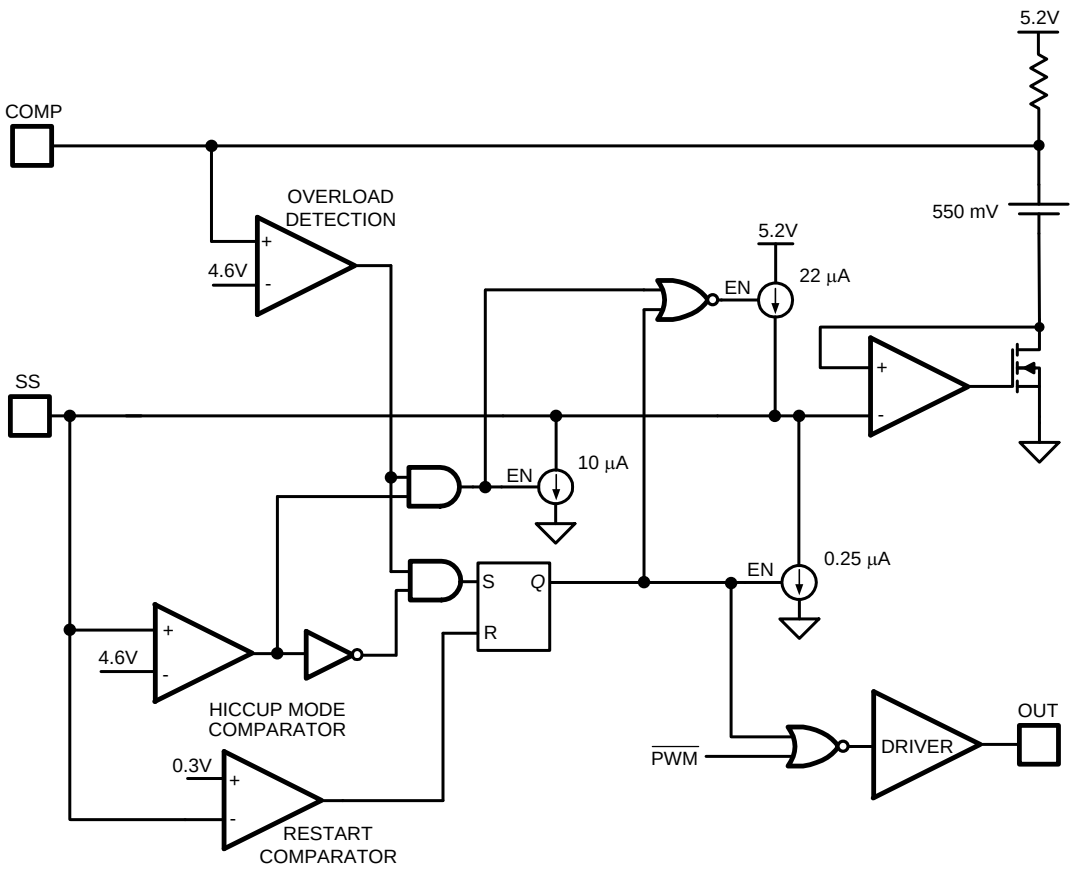

Figure 8. Hiccup Mode Control

Feature Description (continued)

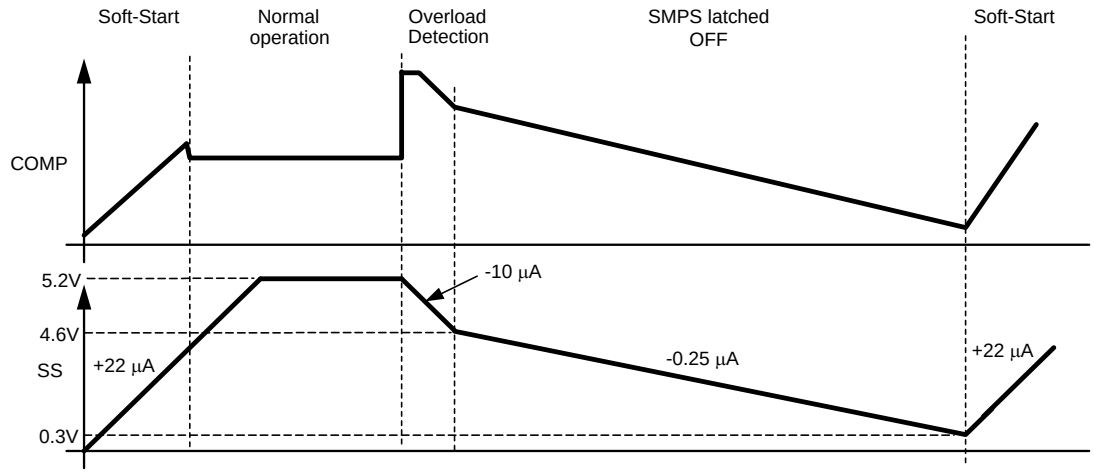

Figure 9. Waveform at SS and COMP Pin due to Continuous Overload

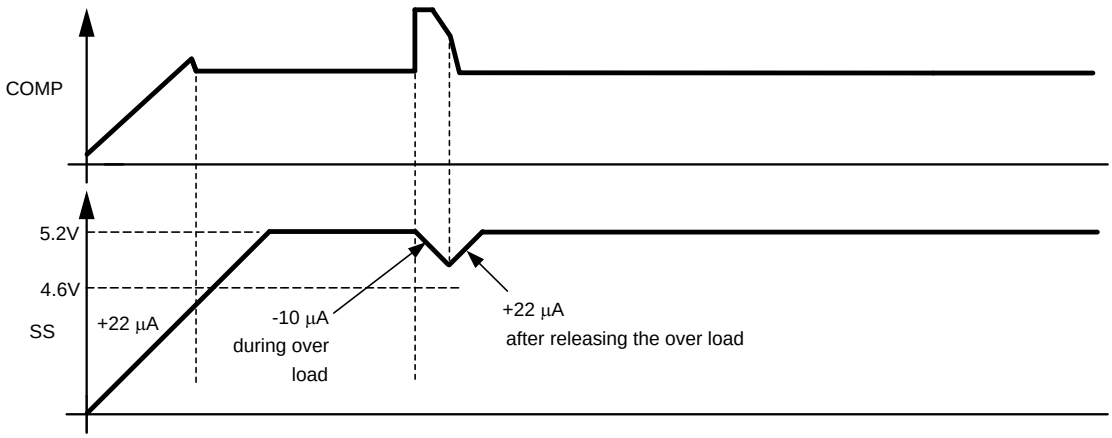

Figure 10. Waveform at SS and COMP Pin due to Brief Overload

7.3.7 Skip Cycle Operation

During light load conditions, the efficiency of the switching power supply typically drops as the losses associated with switching and operating bias currents of the converter become a significant percentage of the power delivered to the load. The largest component of the power loss is the switching loss associated with the gate driver and external MOSFET gate charge. Each PWM cycle consumes a finite amout of energy as the MOSFET is turned on and then turned off. These switching losses are proportional to the frequency of operation. The Skip Cycle function integrated within the LM5021 controller reduces the average switching frequency to reduce switching losses and improve efficiency during light load conditions.

When a light load condition occurs, the COMP pin voltage is reduced by the voltage feedback loop to reduce the peak current delivered by the controller. Referring to Figure 11, the PWM comparator input tracks the COMP pin voltage through a 1.25 V level shift circuit and a 3:1 resistor divider. As the COMP pin voltage falls, the input to the PWM comparator falls proportionately. When the PWM comparator input falls to 125 mV, the Skip Cycle comparator detects the light load condition and disables output pulses from the controller. The controller continues to skip switching cycles until the power supply output falls and the COMP pin voltage increases to demand more output current. The number of cycles skipped will depend on the load and the response time of the

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Feature Description (continued)

frequency compensation network. Eventually the COMP voltage will increase when the voltage loop requires more current to sustain the regulated output voltage. When the PWM comparator input exceeds 130 mV (5 mV hysteresis), normal fixed frequency switching resumes. Typical power supply designs will produce a short burst of output pulses followed by a long skip cycle interval. The average switching frequency in the Skip Cycle mode can be a small fraction of the normal operating frequency of the power supply.

The skip cycle mode of operation can be disabled by adding an offset voltage to the CS pin (refer to Figure 12). A resistive divider connected to a regulated source, injecting a 125 mV offset (minimum) on the CS pin, will force the voltage at the PWM Comparator to be greater than 125 mV, disabling the Skip Cycle Comparator.

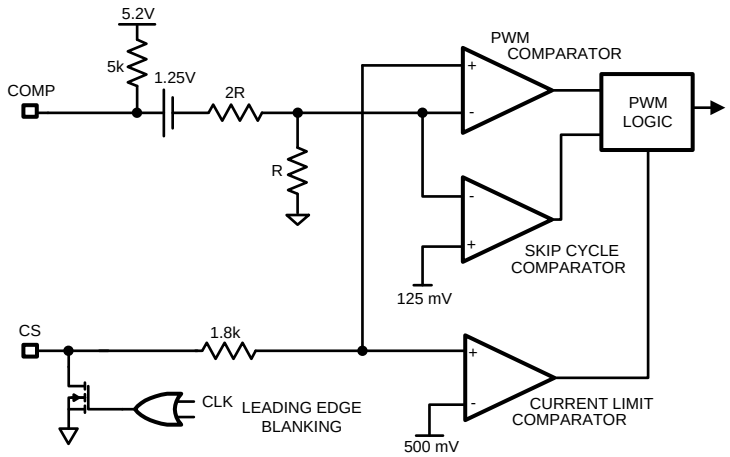

Figure 11. Skip Cycle Control

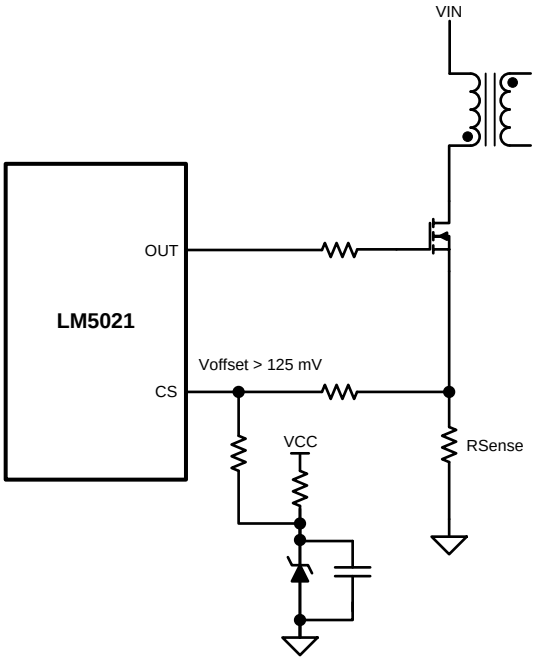

Figure 12. Disabling the Skip Cycle Mode

7.4 Device Functional Modes

7.4.1 Operation With VIN Below 20 V

When a converter is first powered up, there is typically no voltage present on the VIN pin of the controller and the controller is in a low current startup mode. In this mode, there is no activity at the OUT pin and the device is internally in a shutdown mode that consumes minimal current, typically 18 µA. The startup circuit must be capable of supplying the maximum startup current of 25 µA, plus additional current to charge the VIN capacitor to 20 V in any required startup time, at the minimum desired startup voltage for the converter. Once the VIN voltage reaches the startup voltage of 20 V, normal operation in soft start commences. The converter will continue to operate until the VIN voltage falls below the turn off threshold of 7.25 V

7.4.2 Operation in Soft Start

Soft-start mode occurs after the VIN pin reaches the startup voltage after being below 7.25 V or after a hiccup overcurrent cycle. In this mode the reference voltage applied to the PWM comparator from the COMP pin is clamped and allowed to rise at a rate determined by the charging of a capacitor connected to the SS pin. This ramped voltage controls the amount of peak current in the power stage and allows it to increase slowly to reduce stresses on system components. When the clamp level exceeds the level required by the voltage applied to the COMP pin externally, the external feedback circuitry supplying the voltage on COMP assumes control pf the power stage peak current.

7.4.3 Operation Under Normal Conditions

Once the converter has completed soft start, it operates at either a fixed switching frequency with the output pulse width determined by the voltage applied to the COMP pin and the ramp applied to the CS pin, or in a skip cycle mode when the converter load is light. For the normal fixed frequency mode of operation the output is set high when the oscillator starts a new clock cycle (or every other clock cycle in the LM5021-2). The CS pin is connected to the current sensing network for the converter and the voltage on that pin is compared to one-third of the voltage applied to the COMP pin less 1.25 V (see the *Functional Block Diagram* section) from the external error amplifier and compensation circuit. The CS pin signal should be a linearly increasing ramp proportional to the current in the power stage of the converter. The output pulse terminates when the voltage at the CS pin exceeds one-third of the voltage on COMP less 1.25 V.

7.4.4 Operation in Skip Cycle

During periods of minimal output power demand, the controller will operate in a skip cycle mode to reduce power consumption and increase efficiency at lighter loads. Skip cycle mode is entered when in normal operation the voltage on COMP is reduced by the external error amplifier to the point that the voltage on the PWM comparator falls below 125 mV. This will typically be about 1.625 V or lower at the COMP pin. When this mode is entered, the controller inhibits pulses on the output until the error amplifier and compensation circuit requires approximately 130 mV at the input of the PWM comparator. This is approximately 1.64 V at the COMP pin. The number and frequency of pulses in the skip cycle mode is dependent on the load and response time of the external error amplifier and compensation circuit. Skip cycle operation may be disabled by adding a 125-mV DC offset to the CS pin.

7.4.5 Operation at Overload

If the load on the converter increases beyond design limitations, the converter can fail due to component over stress. The LM5021 uses a fixed maximum CS pin voltage of 500 mV to limit the amount of current in the converter power stage. The output pulse will terminate when the CS pin voltage exceeds this threshold regardless of the current command voltage applied to the COMP pin. For short time duration overload events, the converter will operate normally with typically a small transient drop in output voltage that is corrected by the error amplifier when the overload is removed. If the overload is longer in duration, the error amplifier will apply higher and higher voltage to the COMP pin as the output voltage sags. If the COMP pin voltage exceeds the overload threshold of 4.6 V, the converter will enter hiccup mode.

7.4.6 Operation in Hiccup Mode

If during an overload, the COMP pin voltage rises above 4.6 V, hiccup mode operation is started. In this mode, the OUT pin is held low and the soft start capacitor is discharged using a 10-µA current source. When the soft start capacitor discharges to 0.3 V, a new startup sequence begins with the controller in the soft start mode.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Startup Circuit

Referring to Figure 13, the input capacitor C_{VIN} is trickle charged through the start-up resistor Rstart, when the rectified ac input voltage HV is applied. The VIN current consumed by the LM5021 is only 18 µA (nominal) while the capacitor C_{VIN} is initially charged to the start-up threshold. When the input voltage, VIN reaches the upper VIN UVLO threshold of 20 V, the internal VCC linear regulator is enabled. The VCC regulator will remain on until VIN falls to the lower UVLO threshold of 7.25 V (12.5 V hysteresis). When the VCC regulator is turned on, the external capacitor at the VCC pin begins to charge. The PWM controller, soft-start circuit and gate driver are enabled when the VCC voltage reaches the VCC UVLO upper threshold of 7 V. The VCC UVLO has 1.2 V hysteresis between the upper and lower thresholds to avoid chattering during transients on the VCC pin. When the VCC UVLO enables the switching power supply, energy is transferred from the primary to the secondary transformer winding(s). A bias winding, shown in Figure 13, delivers power to the VIN pin to sustain the VCC regulator. The voltage supplied should be from 11 V (VCC regulated voltage maximum plus VCC regulator dropout voltage) to 30 V (maximum operating VIN voltage). The bias winding should always be connected to the VIN pin as shown in Figure 13. Do not connect the bias winding to the VCC pin. The start-up sequence is completed and normal operation begins when the voltage from the bias winding is sufficient to maintain VCC level greater than the VCC UVLO threshold (5.8 V typical).

The LM5021 is designed for ultra-low start-up current into the VIN pin. To achieve this very low start-up current, the VCC regulator of the LM5021 is unique as compared to the VCC regulator used in other controllers of the LM5xxx family. The LM5021 is designed specifically for applications with the bias winding connected to the VIN pin as shown in Figure 13.

NOTE

It is not recommended that the bias winding be connected to the VCC pin of the LM5021. Doing so can cause the device to operate incorrectly or not at all.

The size of the start-up resistor Rstart not only affects power supply start-up time, but also power supply efficiency since the resistor dissipates power in normal operation. The ultra low start-up current of the LM5021 allows a large value Rstart resistor (up to 3 MΩ) for improved efficiency with reasonable start-up time.

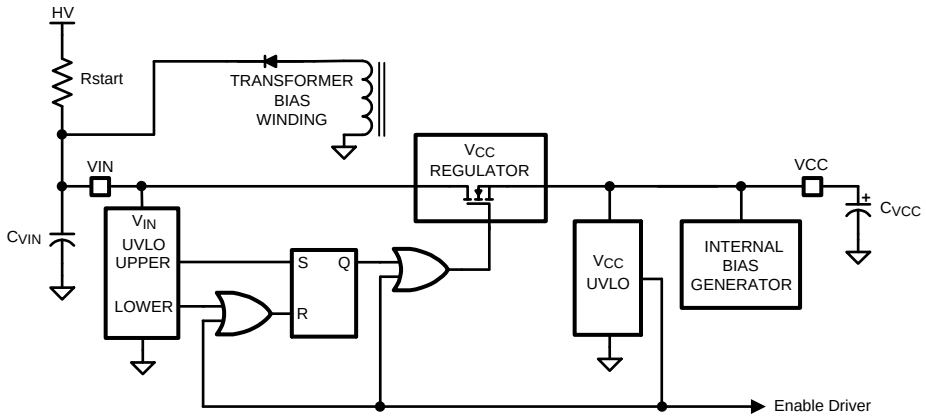

Figure 13. Start-Up Circuit Block Diagram

Application Information (continued)

8.1.2 Relationship Between Input Capacitor C_{IN} and V_{CC} Capacitor C_{VCC}

The internal VCC linear regulator is enabled when VIN reaches 20 V. The drop in VIN due to charge transfer from C_{VIN} to C_{VCC} after the regulator is enabled can be calculated from the following equations where VIN' is the voltage on C_{VIN} immediately after the VCC regulator charges C_{VCC}.

$$\Delta VIN \times C_{VIN} = \Delta VCC \times C_{VCC} \tag{5}$$

$$(20\ V - V_{IN'})\ C_{VIN} = 8.5V\ C_{VCC} \tag{6}$$

$$VIN = 20V - \left(8.5V \times \frac{C_{VCC}}{C_{VIN}}\right) \tag{7}$$

Assuming C_{VIN} value as 10 µF, and C_{VCC} of 1µF, then the drop in VIN will be 0.85 V, or the VIN value drops to 19.15 V. The value of the VCC capacitor can be small (less than 1 uF) as it supplies only transient gate drive current of a short duration. The C_{VIN} capacitor must be sized to supply the gate drive current and the quiescent current of LM5021, until the transformer bias winding delivers sufficient voltage to VIN to sustain the VCC voltage.

The C_{VIN} capacitor value can be calculated from the operating VCC load current after its output voltage reaches the VCC UVLO threshold. For example, if the LM5021 is driving an external MOSFET with total gate charge (Qg) of 25nC, the average gate drive current is Qg x Fsw, where Fsw is the switching frequency. Assuming a switching frequency of 150KHz, the average gate drive current is 3.75 mA. Since the IC consumes approximately 2.5 mA operating current in addition to the gate current, the total current drawn from C_{VIN} capacitor is the operating current plus the gate charge current, or 6.25 mA. The C_{VIN} capacitor must supply this current for a brief time until the transformer bias winding takes over. The C_{VIN} voltage must not fall below 8.5 V during the start-up sequence or the cycle will be restarted. The maximum allowable start-up time can be calculated using the value of C_{VIN}, the change in voltage allow at VIN (19.15 V – 8.5 V) and the VCC regulator current (6.25 mA). Tmax, the maximum time allowed to energize the bias winding is:

$$Tmax = \frac{C_{VIN} \times (19.15V - 8.5V)}{6.25\ mA} = 17\ ms \tag{8}$$

If the calculated value of Tmax is too small, the value of Cin should be increased further to allow more time before the transformer bias winding takes over and delivers the operating current to the VCC regulator. Increasing C_{VIN} will increase the time from the application of the rectified ac (HV in Figure 13) to the time when VIN reaches the 20 V start threshold. The initial charging time of C_{VIN} is:

$$T_{VIN_THRESHOLD} = R_{START} \times C_{VIN} \times \ln\left[\left(1 - \frac{20V}{HV}\right)^{-1}\right] \tag{9}$$

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8.2 Typical Application

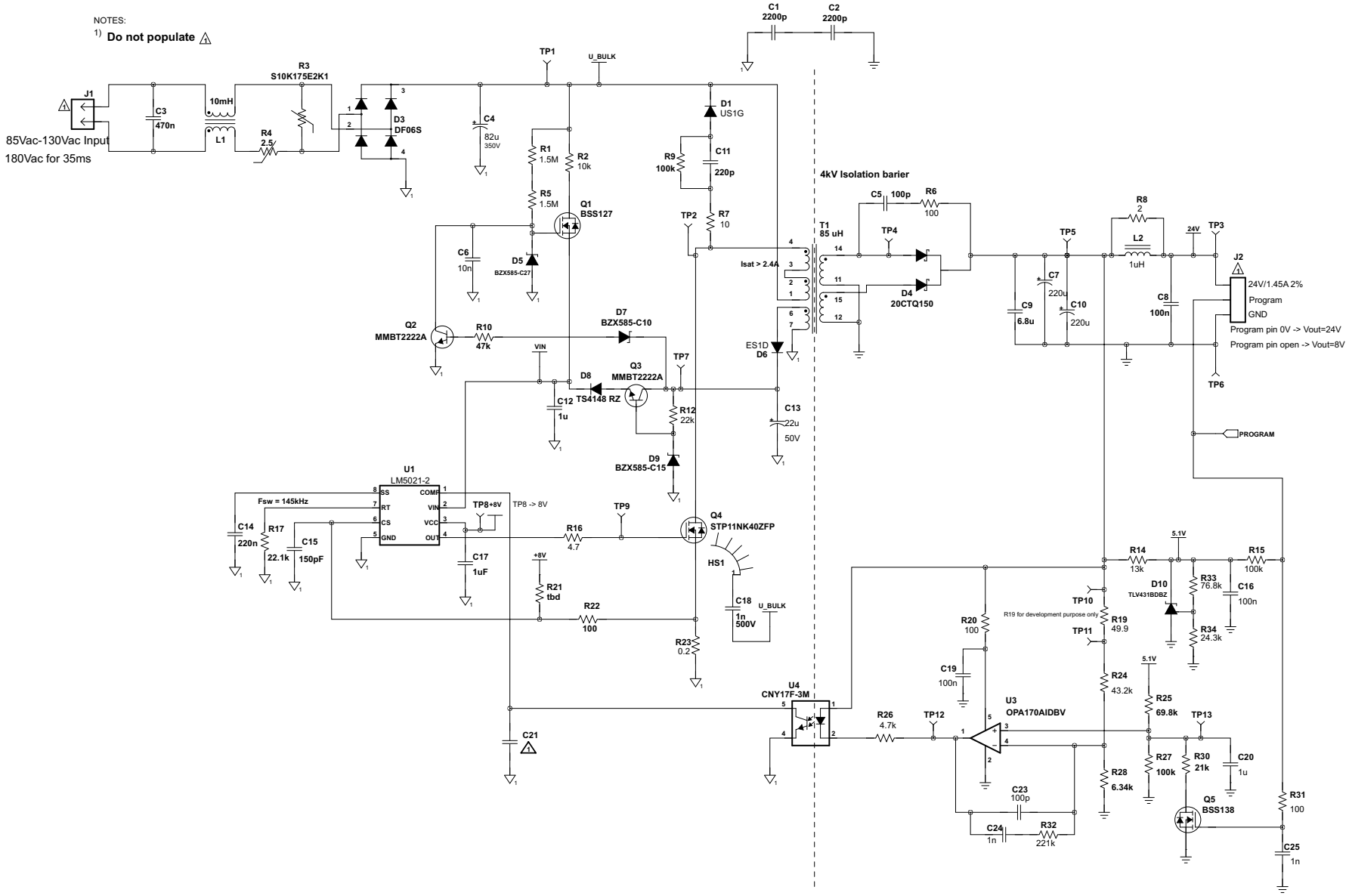

Figure 14. Typical Application Circuit

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8.2.1 Design Requirements

DESIGN PARAMETER	VALUE
Input voltage range	85 Vac - 130 Vac
Output voltage	24 Vdc or 8 Vdc (programmable)
Output current	1.45 Adc at 24 Vdc
Switching frequency	145 kHz
Maximum duty cycle	50%
Isolation level	4 kV
Footprint	68 mm × 34 mm

8.2.2 Detailed Design Procedure

8.2.2.1 Primary Bulk Capacitance

The primary side bulk cap, C4, is selected based on the power level and the desired minimum bulk voltage level. The bulk capacitor value can be calculated as:

$$C_4 = \frac{2P_{IN} \times \left[0.25 + \frac{1}{\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right]}{(2V_{IN(min)}^2 - V_{BULK(min)}^2) \times f_{LINE}}$$

where

- P_{IN} is the maximum input power. Input power is the maximum output power divided target efficiency.
- $V_{IN(min)}$ is the minimum AC input voltage RMS value.
- $V_{BULK(min)}$ is the target minimum bulk voltage.
- f_{LINE} is the line frequency. (10)

Based on the equation, to achieve 70-V minimum bulk voltage, the bulk capacitor should be larger than 72 µF and 82 µF was chosen in the design.

8.2.2.2 Transformer

The transformer design starts with selecting a suitable switching frequency. Generally, the switching frequency selection is based on the tradeoff between the converter size and efficiency. Higher switching frequency results in smaller transformer size, but the switching losses will increase, potentially impacting efficiency. Sometimes, the switching frequency is selected to avoid certain frequencies or harmonics that could interfere with those used for communication. The frequency selection is beyond the scope of this datasheet.

EMI regulations place limits on EMI noise at 150 kHz and higher. For this design, 145 kHz is selected for the switching frequency to minimize transformer size while keeping the switching frequency below the EMI regulation band.

The transformer turns ratio can be selected based on the desired MOSFET voltage rating and diode voltage rating. Since the maximum input voltage is 130 V AC, the peak bulk voltage can be calculated as:

$$V_{BULK(max)} = \sqrt{2} \times V_{IN(max)} = 184\ V \quad (11)$$

To take advantage of the low Rdson of lower voltage MOSFETs, a target device rating of 400 V is selected. Considering the design margin and extra voltage ringing on the MOSFET drain, the reflected output voltage should be less than 50 V. The transformer primary to secondary (n_{PS}) turns ratio can be selected as:

$$n_{PS} = \frac{50}{24} = 2.083 \quad (12)$$

The output rectifier diode (D4) voltage stress is also affected by the turns ratio. The stress applied to the diode is the output voltage plus the reflected input voltage. The voltage stress on the diode can be calculated as:

$$V_{D4} = \frac{V_{BULK(max)}}{n_{ps}} + V_{OUT} = \frac{184\,V}{2.083} + 24\,V = 112\,V \quad (13)$$

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Considering the ringing voltage spikes always present in a switching power supply and allowing for voltage derating (normally 80% derating is used), the diode voltage rating should be higher than 150 V.

The transformer inductance selection is based on the requirement for this converter to remain in discontinuous conduction (DCM). Selecting a larger inductance would allow the converter operate in continuous conduction (CCM). CCM operation tends to increase the transformer size. The primary inductance (L_m) can be calculated as:

$$L_m = \frac{1}{2} \frac{V_{BULK(min)}^2 \times \left(\frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}} \right)^2}{50\% \times P_{IN} \times f_{SW}} \tag{14}$$

In this equation, f_{SW} is the 145-kHz switching frequency. Therefore, the transformer inductance should be selected as 85 µH.

The auxiliary winding provides the power for LM5021 during normal operation. The auxiliary winding voltage is the output voltage reflected to the primary side. A higher reflected voltage allows the IC to quickly get energy from the transformer during startup and makes starting a heavy or highly capacitive load easier. However, a high auxiliary reflected voltage makes the IC consume more power, reducing efficiency and increasing standby power consumption. Therefore, a tradeoff is required. In this design, the auxiliary winding voltage is selected to ensure that there is enough voltage available to ensure the controller will operate when the output voltage is programmed to the lower 8-V setting. Therefore, the auxiliary winding to the output winding turns ratio is selected as:

$$n_{AS} = \frac{12V}{8V} = 1.5 \tag{15}$$

8.2.2.3 Main Switch FET and Output Rectifier

Based on calculated inductor value and the switching frequency, the current stress of the MOSFET (Q4) and diode (D4) can be calculated.

The peak current of Q4 can be calculated as:

$$I_{PK_Q4} = \frac{PIN}{V_{BULK(min)} \times \frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}}} + \frac{1}{2} \frac{V_{BULK(min)}}{L_m} \times \frac{\frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}}}{f_{SW}} \tag{16}$$

The peak current is 2.55 A.

The peak current in D4 is the peak current in Q4 reflected to the secondary side:

$$I_{D4} = N_{PS} \times I_{Q4} = 5.3\ A \tag{17}$$

The RMS current in Q4 can be calculated as:

$$I_{Q4_RMS} = \sqrt{\frac{1}{3} D^3 \times \left(\frac{V_{BULK(min)}}{L_m \times f_{SW}} \right)^2 - \frac{D^2 I_{PK_Q4} V_{BULK(min)}}{L_m \times f_{SW}} + D \times I_{PK_Q4}^2} \tag{18}$$

Here D is the Q4 on time duty cycle at minimum bulk voltage and it can be calculated as:

$$D = \frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}} \tag{19}$$

The RMS current in Q4 is 0.97 A. Therefore, STP11NK40ZFP is selected.

The average current in D4 is the output current 1.45 A. With a 150-V reverse voltage rating and a 20-A average current rating, 20CTQ150 is selected.

The output capacitor is selected based on the output voltage ripple requirement. In this design, 0.1% voltage ripple is assumed. Based on the 0.1% ripple requirement, the capacitor value can be selected based on:

$$C_{OUT} \geq \frac{I_{OUT} \times \frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}}}{0.1\% \times V_{OUT} \times f_{SW}} = 180 \mu F \tag{20}$$

Considering the tolerance and temperature effect, together with the ripple current rating of the capacitors, the output capacitor is selected as two 220 uF units in parallel.

8.2.2.4 Timing Resistor

The switching frequency is set by R17. From Equation 2:

$$R17 = \frac{6.63 \times 10^9}{2 \times 145000} \tag{21}$$

Choose R17 as 22.1 k as a common resistor close to the computed value.

8.2.2.5 Soft-Start Time

The soft start time is set by C14. This determines the rate of increase of converter primary peak current at startup. Set a time that is long enough so that the feedback lop can compensate for the transition from open loop during soft start to being closed loop as it takes over from soft start. The value is best determined experimentally after the rest of the converter is complete. For this example, 220 nF was chosen as the best fit for startup time and startup transient overshoot.

8.2.2.6 Current Sensing Network

The current sensing network consists of C15, R23, R22 and optionally R21. R23 sets the maximum peak current in the transformer primary. Given a peak current of 2.5 A:

$$R23 = \frac{0.5V}{2.5A} \tag{22}$$

Select R23 to be 0.2 Ω.

R22 and C15 form a pulse filter that helps provide additional immunity beyond the internal blanking time to the sudden voltage spike produced on R23 by the parasitic capacitance of the transformer and snubber network for Q4. The time constant for this filter is best determined experimentally but as a guideline should be no more than 25% of the minimum pulse width of the converter in actual operating conditions. Keeping the impedance low also helps with preventing noise coupling problems. For this converter 100 Ω and 150 pF were selected to give a time constant of 67 ns.

R21 is used to disable pulse skip mode if that is needed. To disable pulse skip mode, R21 must produce a 125 mVdc level or slightly higher at the CS pin. To calculate the required value:

$$R21 = \frac{R22}{0.125} \times VCC - R22 \tag{23}$$

Since VCC is 8 V:

$$R21 = 63 \times R22 \tag{24}$$

Select R21 to be 6.49 k to disable skip mode operation.

8.2.2.6.1 Gate Drive Resistor

R16 limits the turn on and turn off speed of the power switch, Q4. The purpose for this is controlling the voltage spike at the drain of Q4 turn off. Selection of this resistor value should be done in conjunction with EMI compliance testing. Slowing the turn off time of Q4 will reduce EMI but also increase power dissipation in Q4. A general range of values to consider would be 0 Ω to 10 Ω for this converter. 4.7 Ω was chosen as the best overall solution for this converter.

8.2.2.6.2 VCC Capacitor

C17 provides filtering for the internal linear regulator. Selection is somewhat arbitrary and was picked as 1 µF per recommendations above.

8.2.2.6.3 Startup Circuit

The startup circuit for this converter illustrates a technique for starting the converter quickly without the need to wait for the larger VIN capacitance to be trickle charged through high impedance from the bulk voltage. It also allows the steady state impedance connected to the bulk voltage to be higher than otherwise possible, reducing power dissipation. The circuit consists of a series pass regulator (R1, R2, R5, Q1, D5 and C6) from the bulk voltage supply to VIN, a series pass regulator from the rectified AUX winding to VIN (C12, D8, Q3, R12 and D9) and a turn off circuit that turns off the bulk regulator once the converter is running (D7, R10 and Q2).

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Q1 is selected for small size and the ability to withstand the maximum bulk voltage. A BSS127 is selected for its high maximum drain voltage of 600 V.

R2 is selected as 10k simply to limit current through Q1 to less than 50 mA per the BSS127 data sheet, at the maximum possible bulk voltage.

$$R2 \geq \frac{255V}{50mA} = 5.1k \tag{25}$$

The voltage the bulk regulator supplies is equal to the zener voltage of D5 less the threshold voltage of Q1, typically 4 V. Since the controller requires a maximum of 23 V to start, the zener voltage must be at least 27 V. D5 is selected as a 27 V device, BZX585-C27.

The bulk series regulator is turned on by R1 and R5. These are only required to supply enough current to bias D5 and overcome any leakage in Q2, approximately 10 µA. To guarantee operation, bias the circuit with 25 µA minimum.

$$R1 + R2 \leq \frac{113V - 27V}{10\mu A} \tag{26}$$

The sum of R1 and R2 must be less than 8.6 MΩ. R1 and R2 are selected as 1.5 M each for common values.

C6 is simply a time delay to soften the startup of the bulk regulator and was arbitrarily chosen as 10 nF.

Turning to the AUX regulator, D8 protects the b-e junction of Q3 while the bulk regulator is active. It is a low current device that must withstand 27 V minimum. A TS4148 was chosen for this purpose.

Q3 is the pass element for the AUX regulator and is again low current. The only requirement is that the Vce rating be greater than the maximum rectified AUX voltage of 36 V. A common MMBT2222A was chose for this function.

The voltage supplied to the controller VIN pin by the AUX regulator is determined by voltage on C13 less 1.4 V for the drop across D8 and Q3 when the voltage on C13 is less than the zener voltage of D9 or the zener voltage of D9 less 1.4 V when the voltage on C13 is higher than the zener voltage of D9. The maximum voltage supplied to the controller is the zener voltage of D9 less 1.4 V. Picking a zener voltage of 15 V lets the controller run at approximately 13.6 V under normal conditions. A BZX585-C15 is selected.

R12 provides bias for D9 and base drive for Q3. Bias for D9 is small compared to the required base drive for Q3. The current required from the regulator is the sum of the controller operating current and the drive current for Q4. The drive current for Q4 depends on the operating frequency and the total gate charge of Q4 at 13.6 V.

$$I_{REG} > I_{VIN} + I_{DRV} \tag{27}$$

$$I_{VIN} = 3.5\ mA \tag{28}$$

$$I_{DRV} = 40\ nC \times 145\ kHz = 5.8\ mA \tag{29}$$

The regulator must supply a minimum of about 9.5 mA for the controller to function. From the MMBT2222A datasheet, the minimum current gain is 75 for 10-mA collector current. The worst case base drive occurs when the output is programmed for 8 V, giving 12 V available to the collector of Q3 and to the base drive resistor R12. To get a minimum of 10 mA from the regulator requires 133 µA of base drive current. The VIN voltage cannot fall below 7.25 V or the controller will shut down. R12 must satisfy the following relationship:

$$R12 < \frac{12V - 7.5V - 1.4V}{133\mu A} 23.3k \tag{30}$$

R12 was picked as 22 k for this application.

The bulk regulator turn off circuit simply turns Q1 off when the voltage on C13 exceeds the zener voltage of D7 plus the b-e voltage of Q2 (0.7 V) and whatever voltage is required to get sufficient base drive through R10. The required collector current is at the maximum bulk voltage of 255 V.

$$I_{CQ2} = \frac{255V}{3M\Omega} = 85\mu A \tag{31}$$

Current gain for the selected MMBT2222A is over 100 at this level so the base drive required is only 8.5 µA. Picking R10 as 47 k requires only an additional 400 mV on C13 to effect turn off of the bulk regulator. The bulk regulator should turn off before the voltage on C13 reaches 12 V. Picking a zener voltage of 10 V with the BZX585-C10 ensures that the bulk regulator will turn off at no more than 11.8 V.

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8.2.3 Application Curves

All test results use 115-Vac input and 2200-µF external load capacitance.

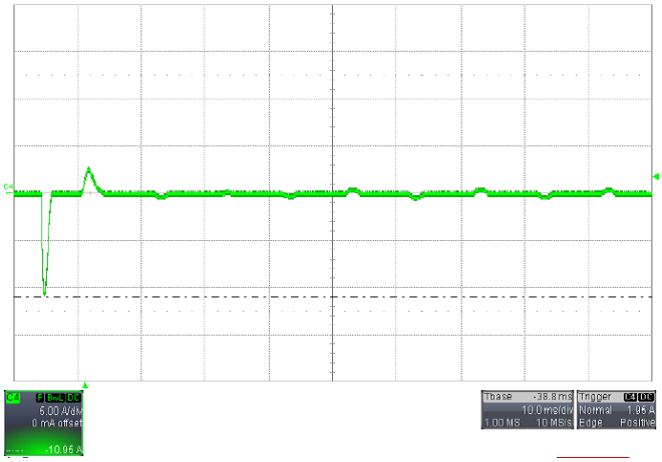

Figure 15. AC Inrush Current, No Load

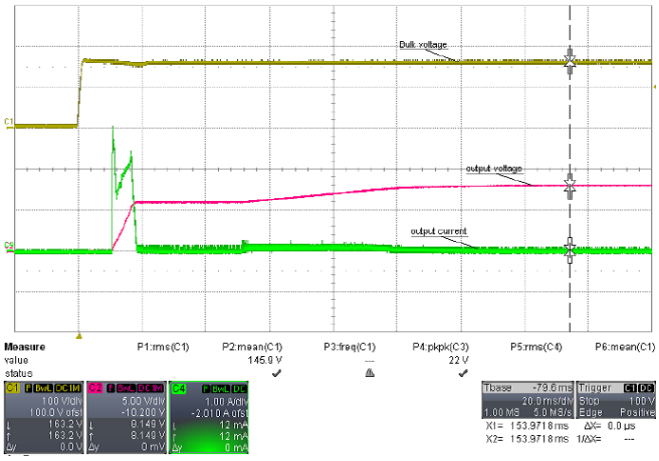

Figure 16. Bulk Voltage, Output Voltage and Output Current

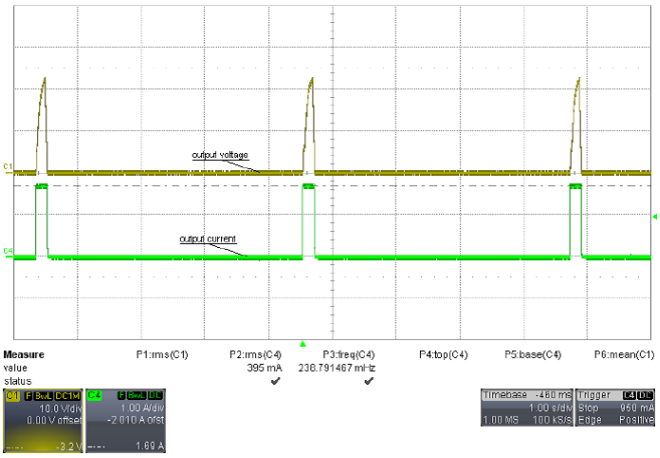

Figure 17. Output Overload Hiccup Protection

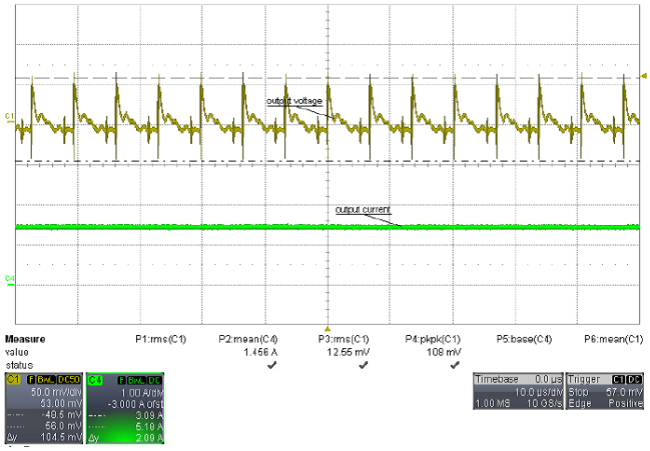

Figure 18. Output Ripple: 108 mVpp

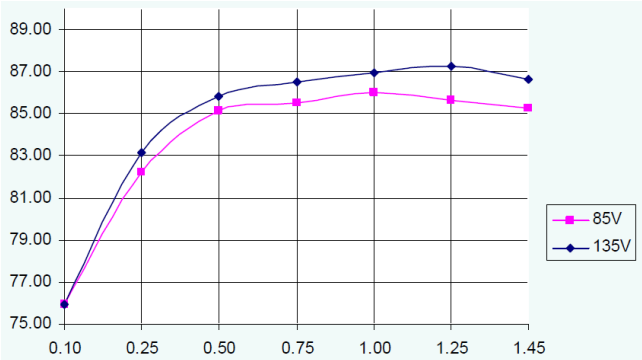

Figure 19. Converter Efficiency

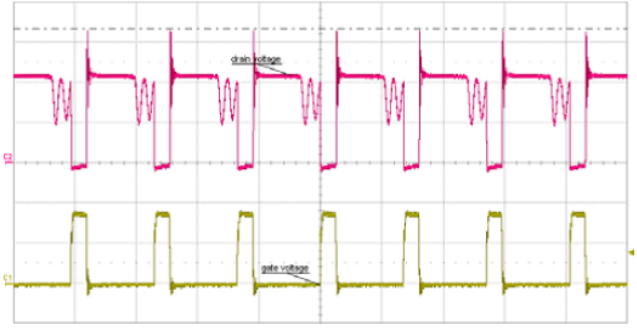

Figure 20. Typical Switching Waveforms
Red: Q4 Drain Voltage, Yellow: Q4 Gate Voltage

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All test results use 115-Vac input and 2200-µF external load capacitance.

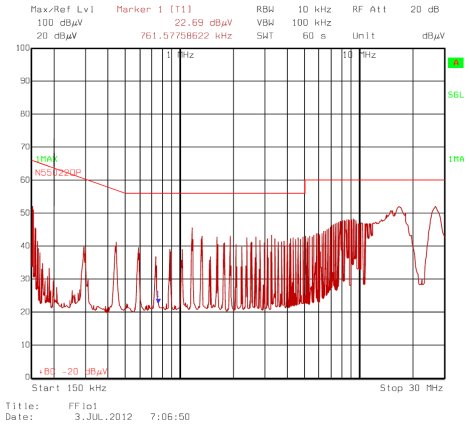

Figure 21. Quasi-Peak EMI Measurement, Not Done in Certified Lab

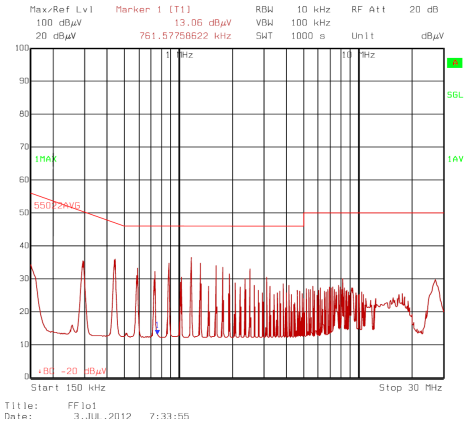

Figure 22. Average EMI measurement, Not Done in Certified Lab

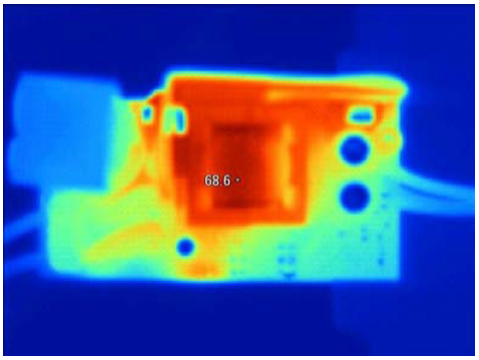

Figure 23. Thermal Image, Top Side

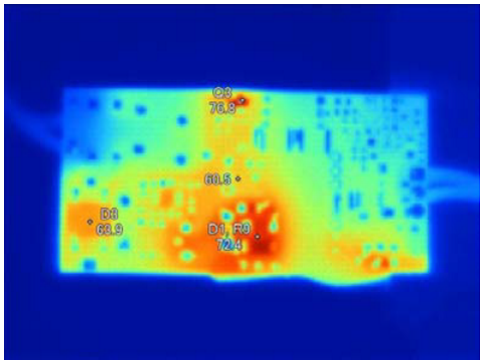

Figure 24. Thermal Image, Bottom Side

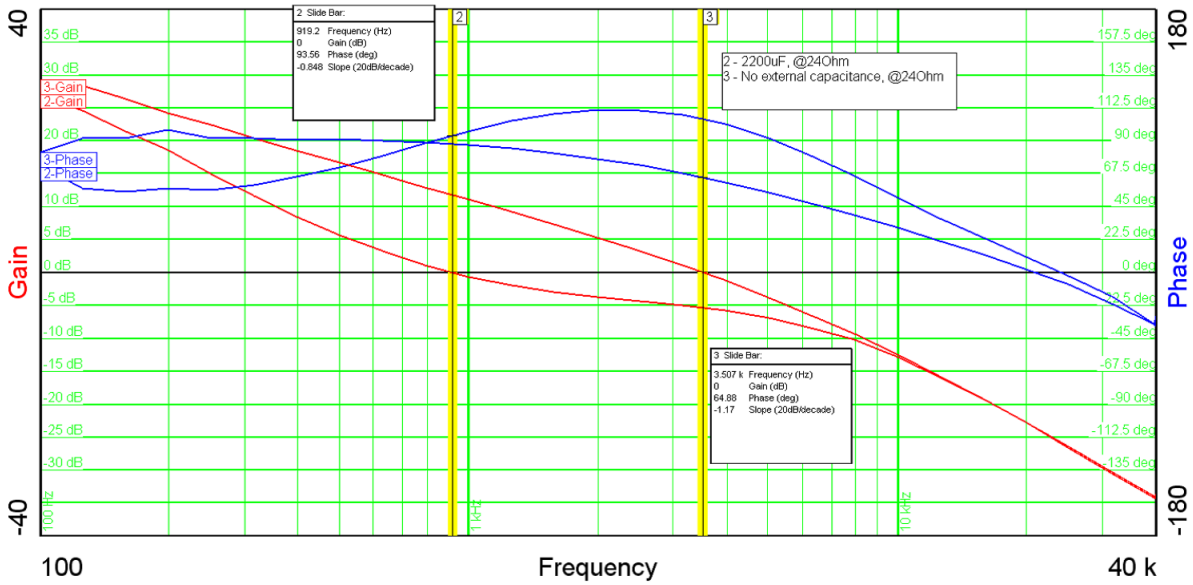

Figure 25. Loop Response

9 Power Supply Recommendations

The LM5021 is designed to run from a power supply in the range of 7.25 V to 30 V connected to VIN. A capacitor is required from VIN to GND to supply startup energy for the converter. Typical values are a few µF to a few tens of µF. Electrolytic capacitors are acceptable here.

The internal circuits of the controller operate from an internal 8-V regulator that is brought out on VCC. The VCC pin needs a small bypass capacitor, typically 100-nF to 1-µF ceramic, closely coupled to the GND pin for best operation. It is not recommended to directly drive the VCC pin from another power source.

NOTE

It is not recommended that the bias winding be connected to the VCC pin of the LM5021. Doing so can cause the device to operate incorrectly or not at all.

10 Layout

10.1 Layout Guidelines

In addition to following general power management IC layout guidelines (star grounding, minimal current loops, reasonable impedance levels, and so on) layout for the LM5021 should take into account the following:

- If possible, a ground plane should be used to minimize the voltage drop on the ground circuit and the noise introduced by parasitic inductances in individual traces.
- A decoupling capacitor is required for both the VIN pin and VCC pin and both should be returned to GND as close to the IC as possible. VIN is the more critical capacitor and should take first priority when connecting to GND as close as possible to the IC.
- The timing setting components such as the RT pin resistor, SS pin capacitor should be directly connected to the ground plane or returned directly to the GND pin on their own traces.
- The CS pin filter capacitor should be as close to the IC possible and grounded right at the IC ground pin. This ensures the best filtering effect and minimizes the chance of current sense pin malfunction.
- Gate driver loop area should be minimized to reduce the EMI noise because of the high di/dt current in the loop.

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10.2 Layout Example

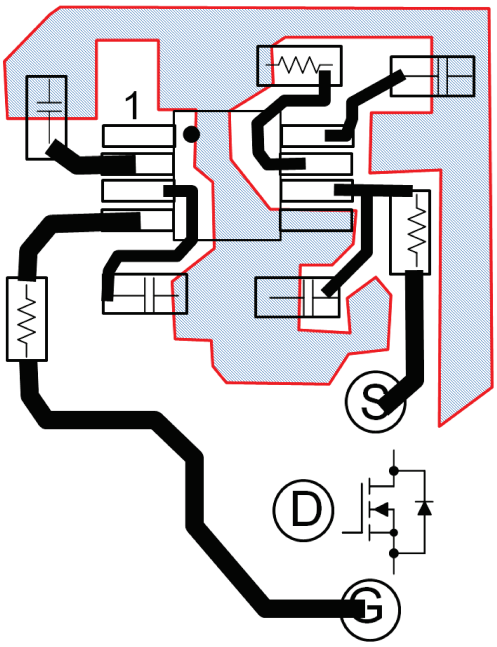

Figure 26. Layout Example

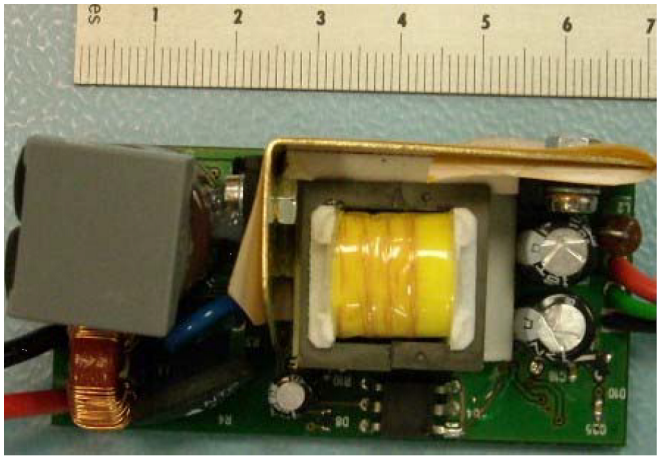

Figure 27. Top Side View

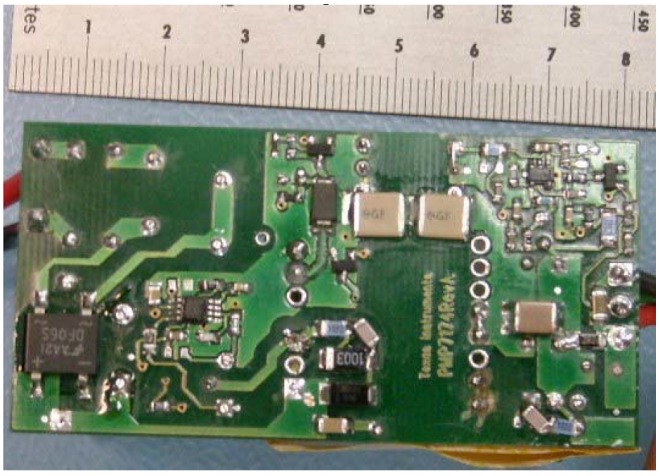

Figure 28. Bottom Side View

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5021-1QDGKRQ1	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	KAGQ
LM5021-1QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	KAGQ
LM5021-1QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	KAGQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM5021-Q1 :

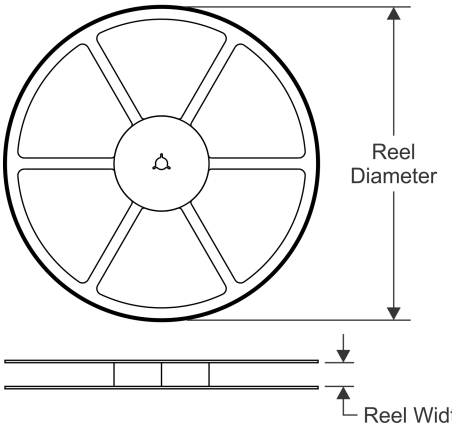
- Catalog : LM5021

NOTE: Qualified Version Definitions:

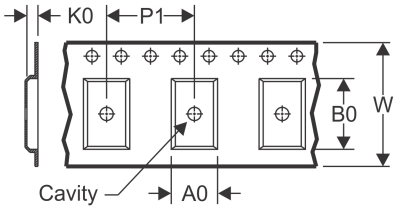
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

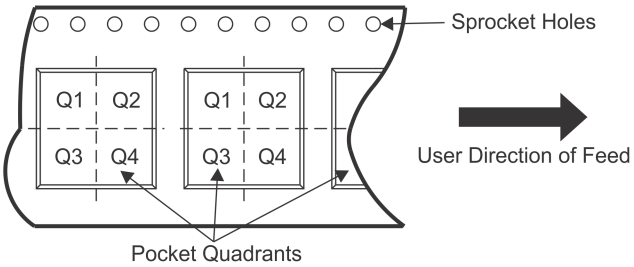


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

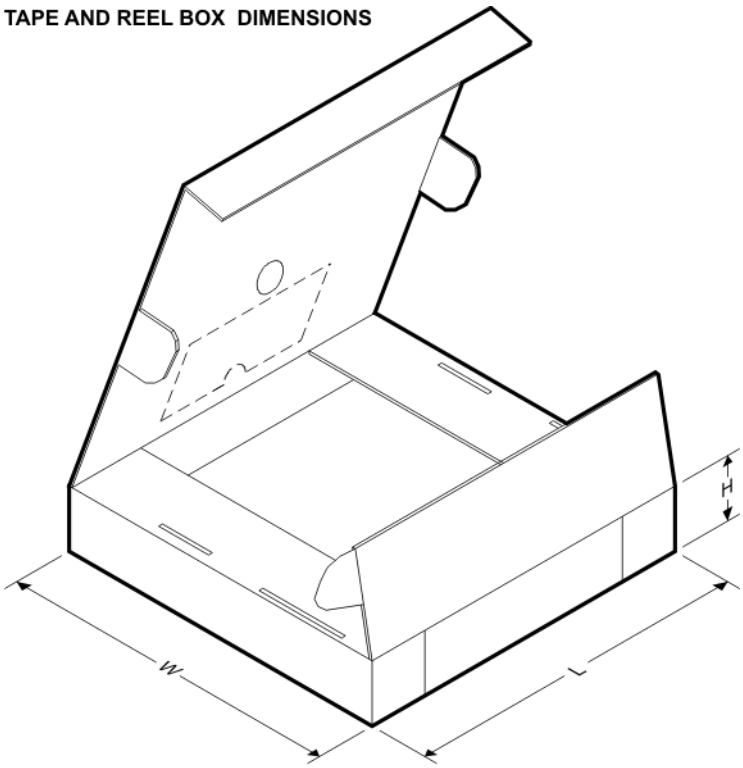
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5021-1QDGKRQ1	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

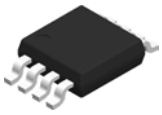


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5021-1QDGKRQ1	VSSOP	DGK	8	3500	367.0	367.0	35.0

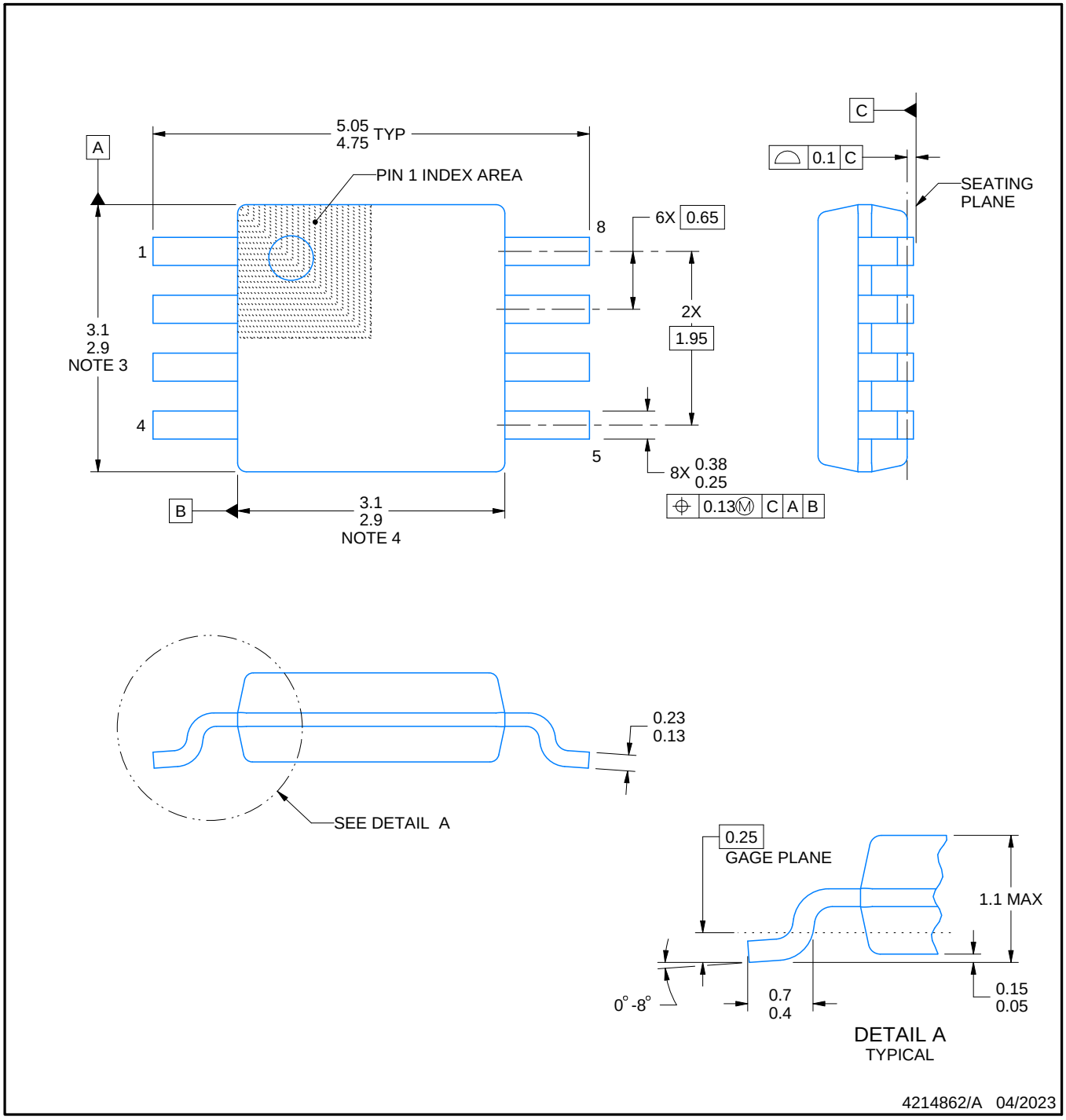
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

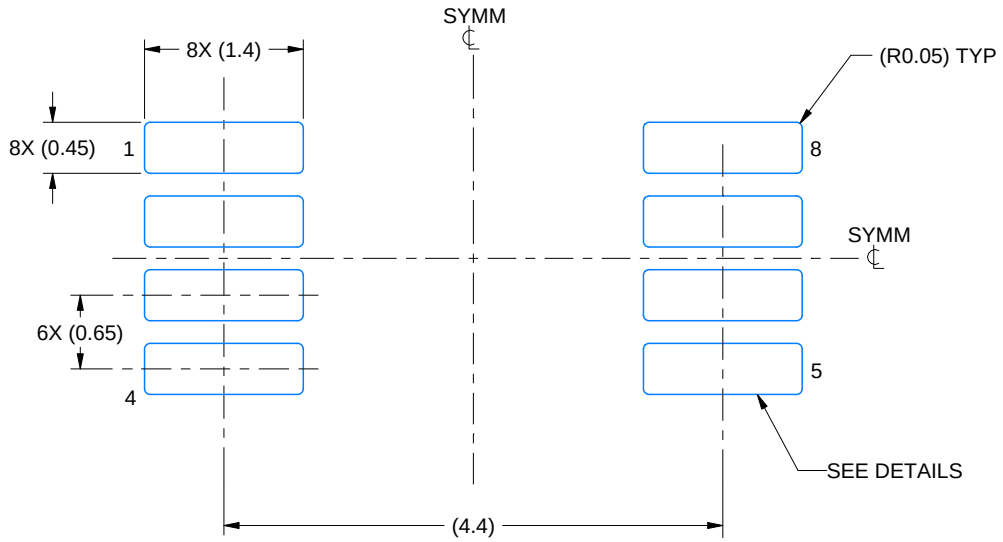
SMALL OUTLINE PACKAGE



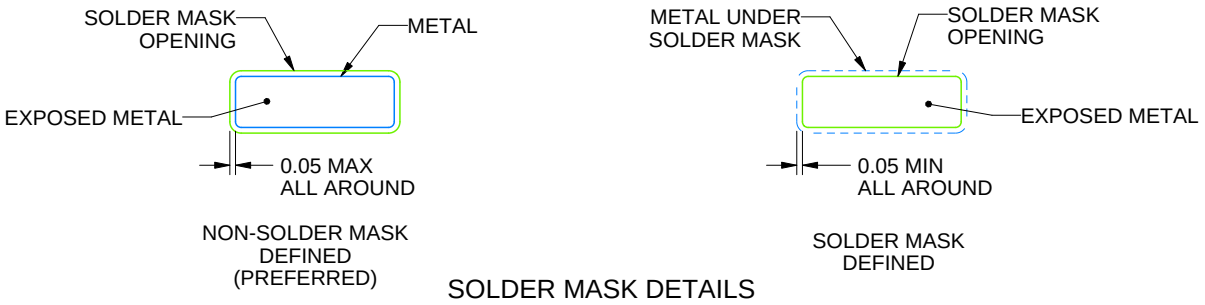
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

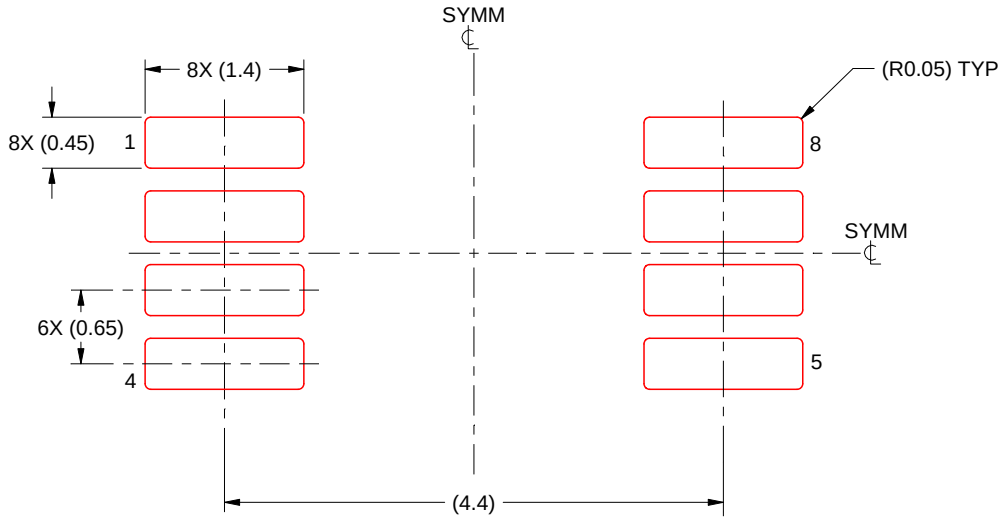


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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