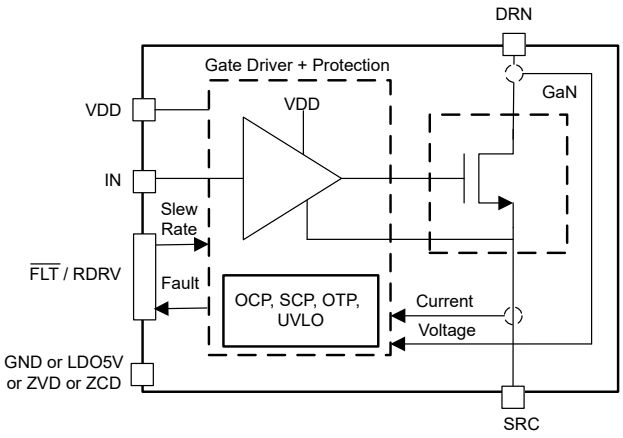
LMG365xR025 650V 25mΩ GaN FET With Integrated Driver and Protection

1 Features

- 650V 25mΩ GaN power FET with integrated gate driver
  - >200V/ns FET hold-off
  - Adjustable slew rates for optimization of switching performance and EMI mitigation
    - 10V/ns to 80V/ns turn-on slew rates
    - 10V/ns to full speed turn-off slew rates
  - Operates with supply pin and input logic pin voltage range from 9V to 26V
- Robust protection
  - Cycle-by-cycle overcurrent and latched short-circuit protection with <300ns response
  - Withstands 720V surge
  - Self-protection from internal overtemperature and UVLO monitoring
- Advanced power management
  - LMG3656R025 includes zero-voltage detection (ZVD) feature that facilitates soft-switching converters
  - LMG3657R025 includes zero-current detection (ZCD) feature that facilitates soft-switching converters
- 9.8mm × 11.6mm TOLL package with thermal pad

2 Applications

- Open rack server PSU
- Merchant telecom rectifiers
- Common redundant power supply
- Uninterruptible power supplies
- Solar inverters and industrial motor drives



Simplified Block Diagram

3 Description

The LMG365xR025 GaN FET with integrated driver and protection is targeted at switch-mode power converters and enables designers to achieve new levels of power density and efficiency.

Adjustable gate driver strength allows the control of turn-on and maximum turn-off slew rates independently, which can be used to actively control EMI and optimize switching performance. Turn on slew rate varies from 10V/ns to 80V/ns, while the turn off slew rate can be limited from 10V/ns to a maximum based on the magnitude of load current. Protection features include under-voltage lockout (UVLO), cycle-by-cycle overcurrent limit, and short-circuit and overtemperature protection. The LMG3651R025 provides a 5V LDO output on LDO5V pin that powers external digital isolators. The LMG3656R025 includes the zero-voltage detection (ZVD) feature which provides a pulse output from the ZVD pin when zero-voltage switching is realized. The LMG3657R025 includes the zero-current detection (ZCD) feature that sets the ZCD pin high when the drain-to-source current is negative and transitions to low upon detecting the zero-crossing point.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMG365xR025	KLA (TOLL, 9)	9.8mm × 11.6mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	LDO 5V OUTPUT	ZERO-VOLTAGE DETECTION FEATURE	ZERO-CURRENT DETECTION FEATURE
LMG3650R025	—	—	—
LMG3651R025 (1)	Yes	—	—
LMG3656R025 (1)	—	Yes	—
LMG3657R025 (1)	—	—	Yes

(1) Product Preview

Table of Contents

4 Pin Configuration and Functions

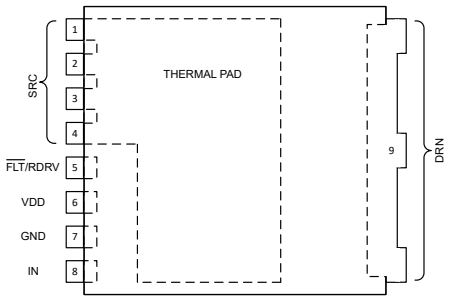


Figure 4-1. LMG3650R025, TOLL Package (Top View)

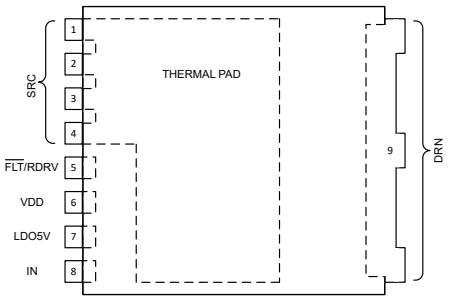


Figure 4-2. LMG3651R025, TOLL Package (Top View)

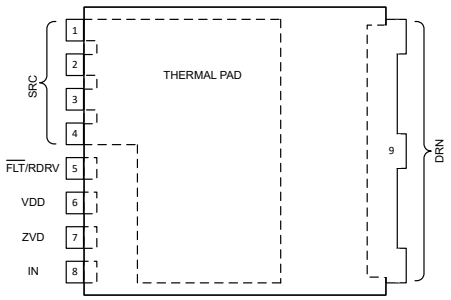


Figure 4-3. LMG3656R025, TOLL Package (Top View)

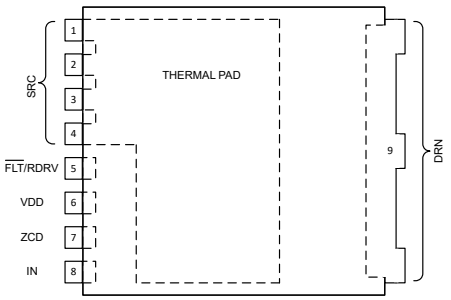


Figure 4-4. LMG3657R025, TOLL Package (Top View)

Table 4-1. Pin Functions

PIN					TYPE (1)	DESCRIPTION
NAME	LMG3650 R025	LMG3651 R025	LMG3656 R025	LMG3657 R025		
SRC	1 - 4	1 - 4	1 - 4	1 - 4	P	GaN FET source.
$\overline{\text{FLT}}$/RDRV	5	5	5	5	O, I	Fault monitoring and drive strength selection pin. Connect a resistor from this pin to GND to set the turn-on drive strength. Connect a resistor in series with capacitor from this pin to GND to set the turn-off drive strength. Slew rates are set one time at the time of power up, then the pin is used for fault monitoring.
VDD	6	6	6	6	P	Device input supply
GND	7	—	—	—	G	Signal ground. Internally connected to SRC, and THERMAL PAD.
LDO5V	—	7	—	—	P	5V LDO output for external digital isolator.
ZVD	—	—	7	—	O	Push-pull digital output that provides zero-voltage detection signal to indicate if device achieves zero-voltage switching in current switching cycle.
ZCD	—	—	—	7	O	Push-pull digital output that sets ZCD pin high when the drain-to-source current is negative and transitions to low upon detecting the zero-crossing point.
IN	8	8	8	8	I	CMOS compatible non inverting input used to turn the FET on and off
DRN	9	9	9	9	P	GaN FET drain
THERMAL PAD	—	—	—	—	—	Thermal pad.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to GND/SRC(1)

			MIN	MAX	UNIT
V_{DS}	Drain-source voltage, FET off			650	V
$V_{DS(surge)}$	Drain-source voltage, surge condition, FET off			720	V
$V_{DS(tr)(surge)}$	Drain-source transient ringing peak voltage, surge condition, FET off			800	V
	Pin voltage	VDD	-0.5	26	V
		IN	-5(2)	28	V
		$\overline{FLT}$/RDRV, ZVD (LMG3656 only), ZCD (LMG3657 only)	-0.5	5.5	V
		LDO5V (LMG3651 only)		5.5	V
$I_{D(cnts)}$	Drain (DRN to SRC) continuous current, FET on. Tj = 25°C(2)		-60	60	A
$I_{D(cnts)}$	Drain (DRN to SRC) continuous current, FET on. Tj = 150°C(2)		-48.5	48.5	A
$I_{D(pulse)}$	Pulse drain current, FET on, t_p < 10µs. Tj = 25°C(3)		-85	85	A
$I_{S(cnts)}$	Source (SRC to DRN) continuous current, FET off. Tj = 25°C			60	A
$I_{S(cnts)}$	Source (SRC to DRN) continuous current, FET off. Tj = 150°C			48.5	A
T_J	Operating junction temperature(4)		–40	175	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The IN pin voltage is limited to a minimum of -0.5V in steady state, with a transient tolerance of -5V for duration <1µs.
(3) Absolute maximum ratings are limited by device internal overcurrent protection feature. However, the FET drain intrinsic positive pulsed current rating for t_p < 10µs varies with junction temperature; 81A typ. at 150°C. The positive pulsed current must remain below the overcurrent threshold to avoid the FET being automatically shut off.
(4) Refer to the Electrical and Switching Characteristics Tables for junction temperature test conditions.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to GND/SRC

			MIN	NOM	MAX	UNIT
	Supply voltage	VDD	9		24	V
	Input voltage	IN	0		26	V
$I_{D(cnts)}$	Drain (DRN to SRC) continuous current, FET on. Tj = 25°C		-50		50	A
$I_{D(cnts)}$	Drain (DRN to SRC) continuous current, FET on. Tj = 150°C		-38		38	A
	Positive source current	LDO5V (LMG3651 only)			25	mA
$RDRV_{on}$	Resistance from external turn-on slew rate control resistor between $\overline{FLT}$/RDRV to GND		29.4		open	kΩ

Unless otherwise noted: voltages are respect to GND/SRC

		MIN	NOM	MAX	UNIT
$RDRV_{off}$	Resistance and capacitance from external turn-off slew rate control series resistor and capacitor configuration between $\overline{FLT}$/RDRV to GND	2		open	kΩ
$CDRV_{off}$		0		1800	pF

5.4 Thermal Information

THERMAL METRIC[1]		KLA (TOLL) 9 PINS	UNIT
$R_{\theta JC(bot,avg)}$	Junction-to-case (bottom) average thermal resistance	0.41	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/SRC; –40°C ≤ T_J ≤ 150°C; VDD = 12V; $\overline{FLT}$/RDRV resistances $RDRV_{on}$ & $RDRV_{off}$ are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FET						
$R_{DS(on)}$	Drain-source on resistance	T_J = 25°C, I_L = 16A		22	30	mΩ
		T_J = 150°C, I_L = 16A		44		mΩ
V_{SD}	Source-drain third-quadrant voltage	T_J = 25°C, I_{SD} = 0.1A		1.8		V
		T_J = 150°C, I_{SD} = 0.1A		1.6		V
		T_J = 25°C, I_{SD} = 20A		3.4		V
		T_J = 150°C, I_{SD} = 20A		4.8		V
I_{DSS}	Drain leakage current	T_J = 25°C, V_{DS} = 650V		7		µA
		T_J = 150°C, V_{DS} = 650V		10		µA
C_{OSS}	Output capacitance	V_{DS} = 400V		200		pF
Q_{OSS}	Output charge	V_{DS} = 0V to 400V		150		nC
E_{OSS}	Output capacitance stored energy			23		µJ
$C_{OSS(tr)}$	Time related effective output capacitance			400		pF
$C_{OSS(er)}$	Energy related effective output capacitance			280		pF
Q_{RR}	Reverse recovery charge			0		nC
OVERCURRENT AND SHORT-CIRCUIT PROTECTIONS						
$I_{T(OC)}$	Overcurrent fault - threshold current	T_J = -40°C	57	63	69	A
		T_J = 25°C	50	55	60	A
		T_J = 150°C	38	43	48.5	A
$V_{T(Idsat)}$	Saturation current detection - threshold voltage		8.5	9	9.6	V
OVERTEMPERATURE PROTECTION						
T_{T+}	Temperature fault - positive-going threshold temperature			190		°C
$T_{T(hyst)}$	Temperature fault - threshold temperature hysterisis			20		°C
IN						
$V_{IN,IT+}$	Positive-going input threshold voltage		1.6	2	2.45	V
$V_{IN,IT-}$	Negative-going input threshold voltage		0.6	0.9	1.3	V
$V_{IN,IT(hyst)}$	Input threshold voltage hysteresis			1		V
R_{PDN}	Pull-down input resistance		115	150	185	kΩ

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/SRC; –40°C ≤ T_J ≤ 150°C; VDD = 12V; $\overline{FLT}$/RDRV resistances $RDRV_{on}$ & $RDRV_{off}$ are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{FLT}$/RDRV						
V_{OL}	Low-level output voltage	Output sink 8mA		0.2	0.4	V
V_{OH}	High-level output voltage	Output source 8mA	4.5	4.8		V
VDD						
$I_{VDD(ON)}$	Quiescent current when FET is ON	IN=1		1.2	16	mA
$I_{VDD(OFF)}$	Quiescent current when FET is OFF	IN=0		0.8	1.1	mA
I_{CC_op}	Operation current at 140kHz	f_{sw} = 140kHz, V_{bus} = 0V, Soft-switched, 50% duty cycle.		4	5.6	mA
$V_{VDD, T+ (UVLO)}$	UVLO- positive-going threshold voltage		8.1	8.5	8.9	V
$V_{VDD, T- (UVLO)}$	UVLO- negative-going threshold voltage		7.6	8	8.4	V
$V_{VDD, T (hyst)}$	UVLO- threshold voltage hystresis			0.5		V

5.6 Switching Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/SRC; –40°C ≤ T_J ≤ 150°C; V_{DD} = 12V; $\overline{FLT}$/RDRV resistances $RDRV_{on}$ & $RDRV_{off}$ are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING TIMES						
$t_{d(on)}$	Turn-on delay time	From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320V, V_{BUS} = 400V, L_{HB} current = 0A, 80V/ns		45	55	ns
	Turn-on current rise time + delay time	From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320V, V_{BUS} = 400V, L_{HB} current = 10A, 80V/ns		45	60	ns
$t_{vf(on)}$	Turn-on voltage falling time	From V_{DS} < 320V to V_{DS} < 80V, V_{BUS} = 400V, L_{HB} current = 10A, 80V/ns	1	3.5	6	ns
	Turn-on slew rate	dv/dt when V_{DS} = 200V, V_{BUS} = 400V, L_{HB} current = 10A, 80V/ns	60	80	100	V/ns
	Pulse width distortion	slew-rate setting at 80V/ns, IDS = 31A, Measure difference between IN pulse width & VSW pulse width		9	20	ns
	Minimum input pulse changing the output L-H-L	slew-rate setting at 80V/ns such that SW crosses 200V			50	ns
$t_{d(off)}$	Turn-off delay time at full speed	From V_{IN} < $V_{IN,IT-}$ to V_{DS} > = 80V. V_{BUS} = 400V, I_L = 36A, fastest or full turn-off speed.	18	30	60	ns
$t_{vr(off)}$	Turn-off voltage rise time at full speed	From V_{DS} > = 80V to V_{DS} > = 320V. V_{BUS} = 400V, I_L = 36A, fastest or full turn-off speed.	3	5.5	7	ns
STARTUP TIMES						
T_{DRV_START}	Driver startup delay	From Driver supply crossing UVLO to switch turning on if IN is high.		56	70	µs
FAULT TIMES						
$t_{off(OC)}$	Overcurrent fault FET turn-off time, FET on before overcurrent	From I_D > = $I_{T(OC)}$ to V_{ds}> 10V, di/dt = 100A/µs, in the fastest turn-off speed		340	480	ns

5.6 Switching Characteristics (continued)

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/SRC; –40°C ≤ T_J ≤ 150°C; V_{DD} = 12V; $\overline{FLT}$/RDRV resistances $RDRV_{on}$ & $RDRV_{off}$ are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{off(OC\_ON)}$	Overcurrent total on time, turn-on into overcurrent.	From V_{ds} < = 10V to V_{ds} > = 10V, turning on at 110% of OC level, at 80V/ns turn-on slew rate and fastest turn-off speed.		420	580	ns
$t_{off\_cur(SC\_ON)}$	SC on time measured through drain current	LS V_{ds} > 10V, measured from LS I_{ds} > 50A to I_{ds} < 50A, at 80V/ns turn-on slew rate in a half-bridge configuration.	100	215	500	ns
$t_{off\_cur(SC)}$	SC response time with source current measurement	From LS Vds>9V to LS Ids<50A, at 80V/ns turn-on slew rate in a half-bridge configuration. .		155	350	ns
	Latched-Fault reset time	Time required to hold gate driver input low to clear latched-fault	300	380	450	µs
ZERO-VOLTAGE DETECTION AND ZERO-CURRENT DETECTION TIMES						
	ZCD delay	Current crossing zero (low to high) to ZCD output pulse di/dt = 0.03A/ns	15	40	75	ns
t_{DL_ZVD}	ZVD delay	IN rising to ZVD output pulse. 80V/ns turn-on speed.	35	50	58	ns
t_{WD_ZVD}	ZVD pulse width	V_{bus} = 10V, I_L = 5A, measure ZVD pulse width	90	120	170	ns
t_{3rd_zvd}	3rd quadrant conduction time when the ZVD pulse starts to appear	Vbus = 10V, IL = 5A, measure the 3rd quadrant conduction time when the ZVD pulse starts to appear, fet turn on (80V/ns).		20	30	ns

5.7 Typical Characteristics

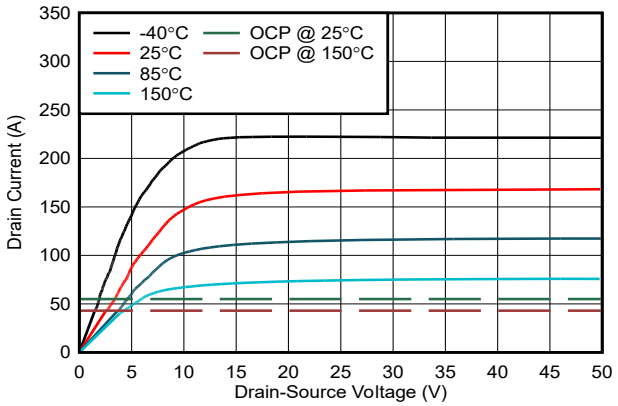


Figure 5-1. Drain Current vs Drain-Source Voltage

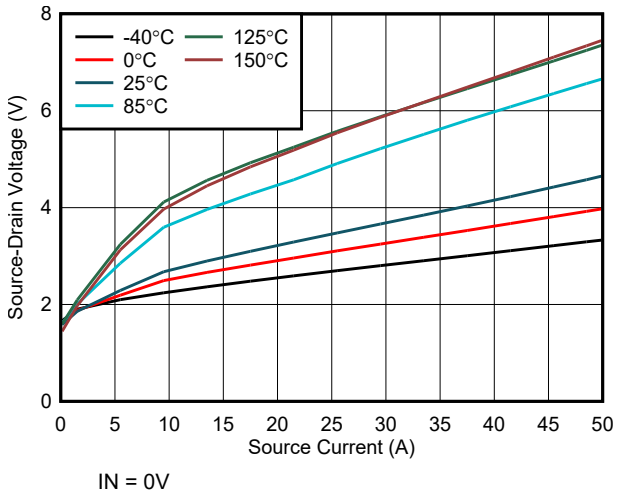


Figure 5-2. Off-State Source-Drain Voltage vs Source Current

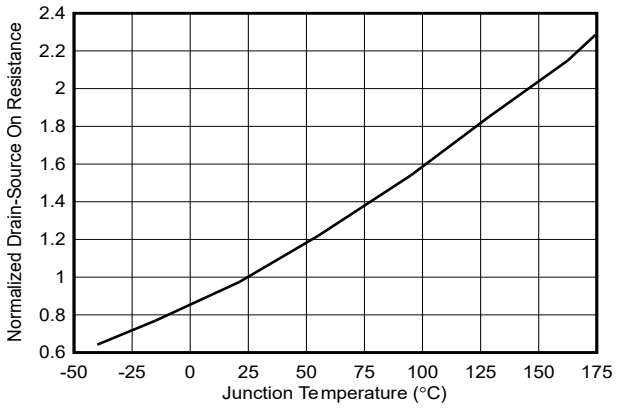


Figure 5-3. Normalized On-Resistance vs Junction Temperature

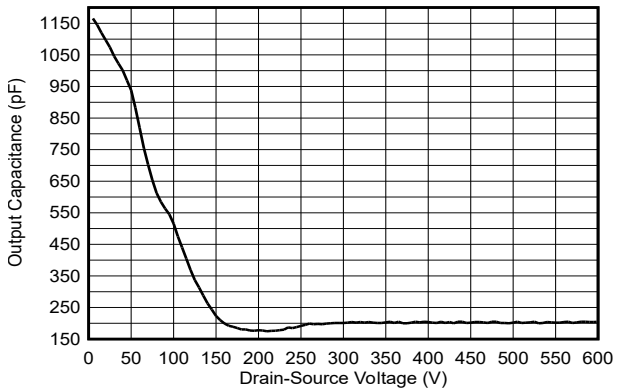


Figure 5-4. Output Capacitance vs Drain-Source Voltage

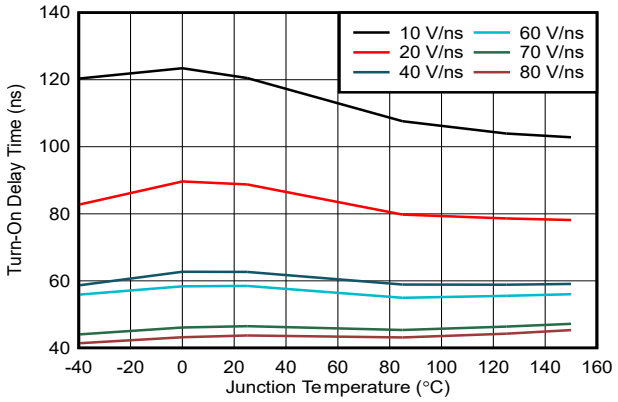


Figure 5-5. Turn-On Delay Time vs Junction Temperature

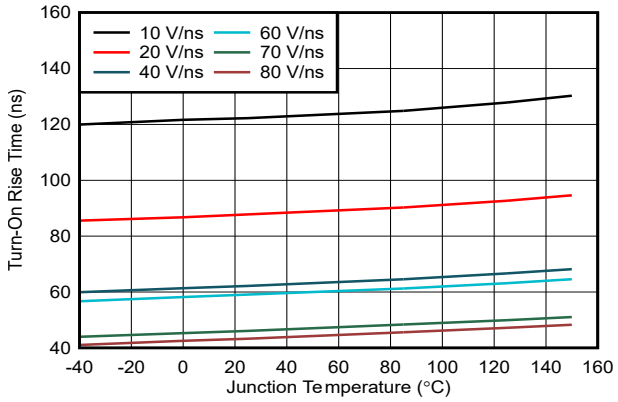


Figure 5-6. Turn-On Rise Time vs Junction Temperature

5.7 Typical Characteristics (continued)

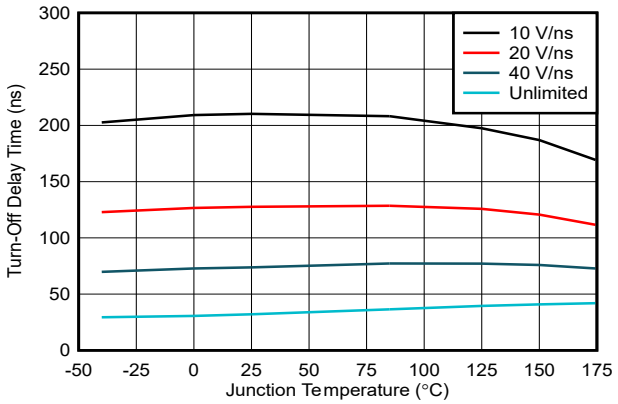


Figure 5-7. Turn-Off Delay Time vs Junction Temperature

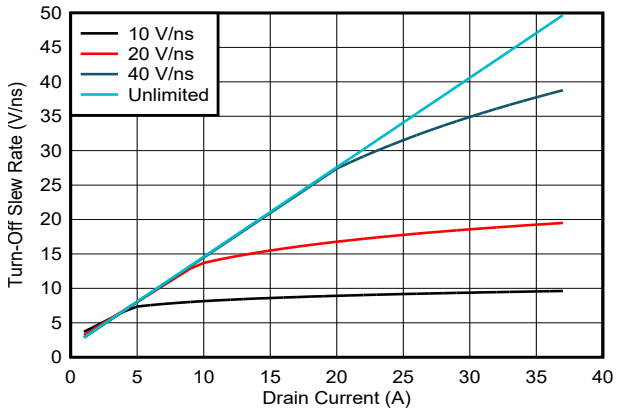


Figure 5-8. Turn-Off Slew Rate vs Drain Current

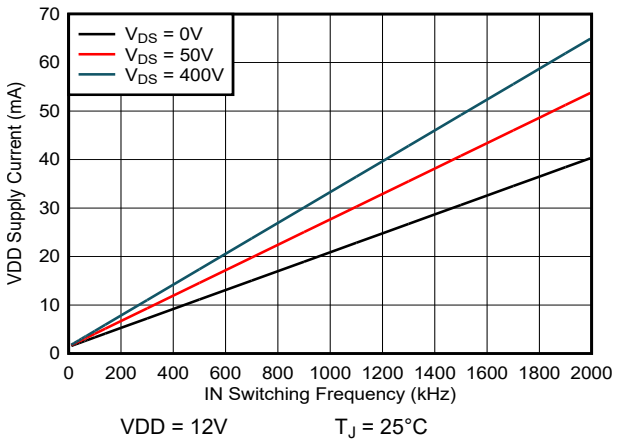


Figure 5-9. VDD Supply Current vs IN Switching Frequency

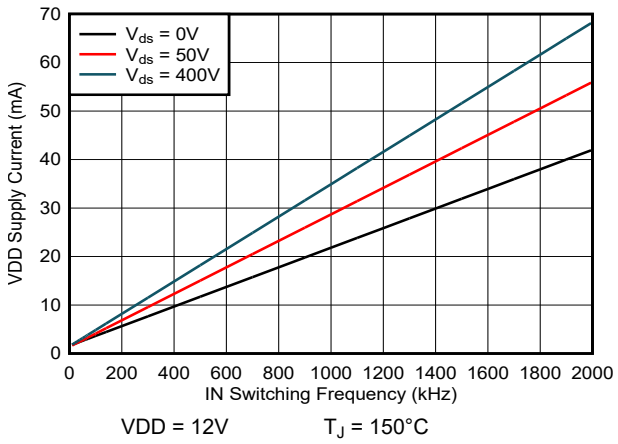


Figure 5-10. VDD Supply Current vs IN Switching Frequency

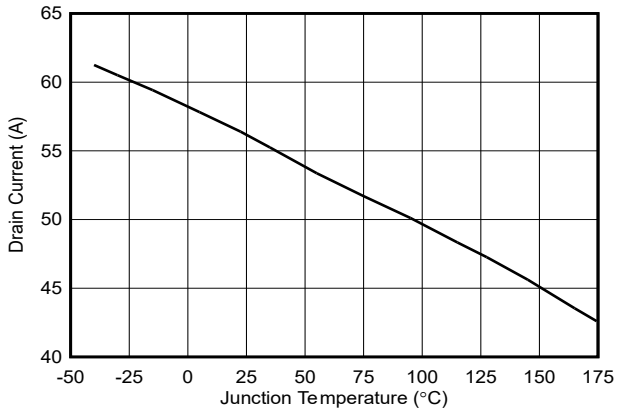


Figure 5-11. OCP vs Junction Temperature

6 Parameter Measurement Information

6.1 Switching Parameters

Circuit Used to Determine Switching Parameters shows the circuit used to measure most switching parameters. The top device in this circuit re-circulates the inductor current and functions in third-quadrant mode only. The bottom device is the active device that turns on to increase the inductor current to the desired test current. The bottom device turns off and on to create switching waveforms at a specific inductor current. Both the drain current (at the source) and the drain-source voltage are measured. Measurement to Determine Propagation Delays and Slew Rates shows the specific timing measurement. TI recommends using the half-bridge as a double pulse tester. Excessive third-quadrant operation can overheat the top device.

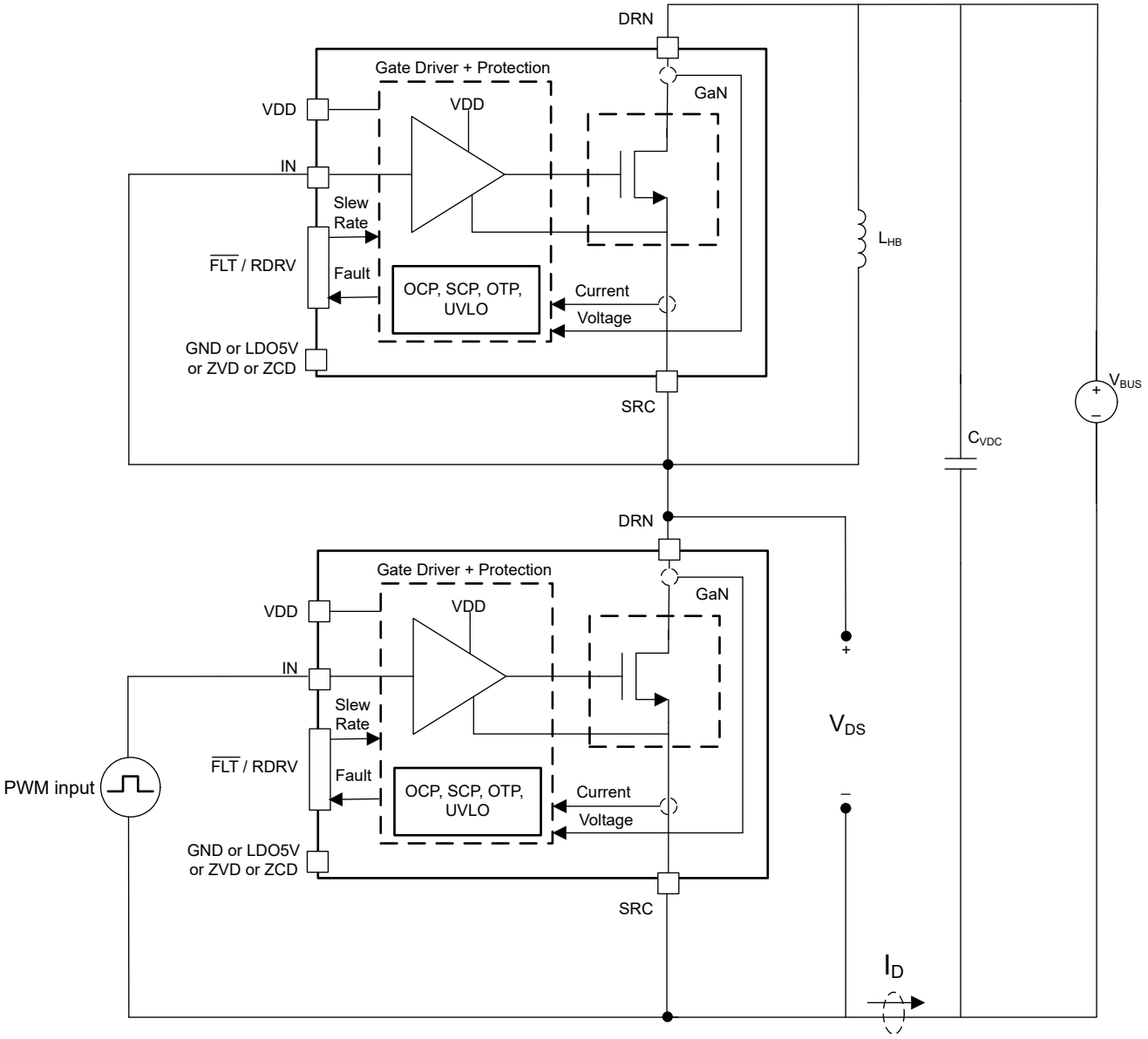


Figure 6-1. Circuit Used to Determine Switching Parameters

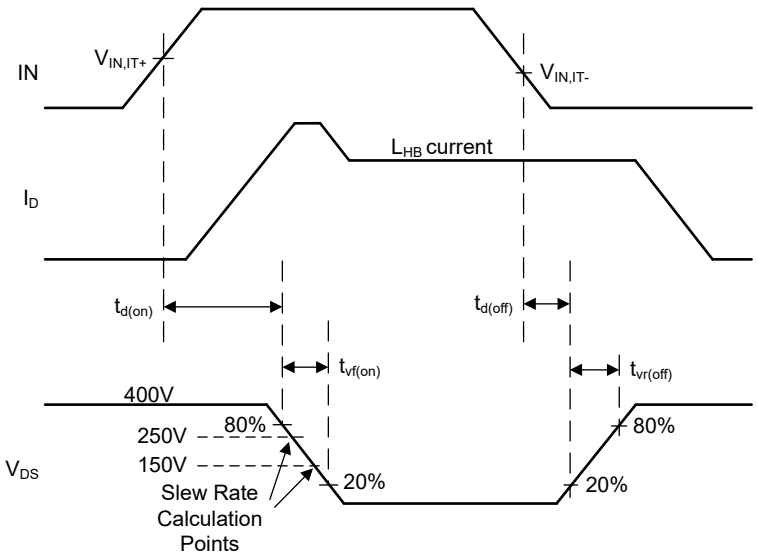


Figure 6-2. Measurement to Determine Propagation Delays and Slew Rates

6.1.1 Turn-On Times

The turn-on transition has two timing components: turn-on delay time and turn-on voltage fall time. The turn-on delay time is from when IN goes high to when the drain-source voltage falls 20% below the bus voltage. The turn-on voltage fall time is from when drain-source voltage falls 20% below the bus voltage to when the drain-source voltage falls 80% below the bus voltage. The turn-on timing components are a function of the turn-on drive strength resistance $RDRV_{on}$ connected to the $\overline{FLT}$/RDRV pin.

6.1.2 Turn-Off Times

The turn-off transition has two timing components: turn-off delay time and turn-off voltage rise time. The turn-off delay time is from when IN goes low to when the drain-source voltage rises to 20% of the bus voltage. The turn-off voltage rise time is from when the drain-source voltage rises from 20% of the bus voltage to when the drain-source voltage to 80% of the bus voltage. The turn-off timing components are dependent on the L_{HB} load current, however LMG365xR025 also includes the ability to limit turn-off drive strength. When the drain-to-source current is sufficiently high and the turn-off drive strength is limited, the timing components are dependent on the programming resistors $RDRV_{on}$, $RDRV_{off}$, and capacitance $CDRV_{off}$ connected to the $\overline{FLT}$/RDRV pin.

6.1.3 Drain-Source Turn-On and Turn-off Slew Rate

The drain-source turn-on and turn-off slew rate is measured on V_{DS} at approximately the midpoint of the bus voltage; the units are in volts per nanosecond. The resistors $RDRV_{on}$, $RDRV_{off}$, and capacitance $CDRV_{off}$ connect to the $\overline{FLT}$/RDRV pin and program the turn-on slew rate and limit the turn-off slew rate.

6.1.4 Zero-Voltage Detection Times (LMG3656R025 only)

ZVD Timing Specifications defines the switching timings related to the zero-voltage detection (ZVD) block, and shows the drain-to-source voltage, IN pin signal, and ZVD output signals of the device. When the device achieves zero-voltage switching (ZVS), the ZVD pin outputs a pulse-signal with width T_{WD_ZVD}, and the delay time in between IN pins rising edge and ZVD pulses rising edge is defined as T_{DL_ZVD}. A certain third quadrant conduction time is required to allow the device detecting a zero-voltage switching, and T_{3rd_ZVD} indicates this timing. See the Zero-Voltage Detection (ZVD) (LMG3656R070 Only) section for more information about the ZVD timing parameters.

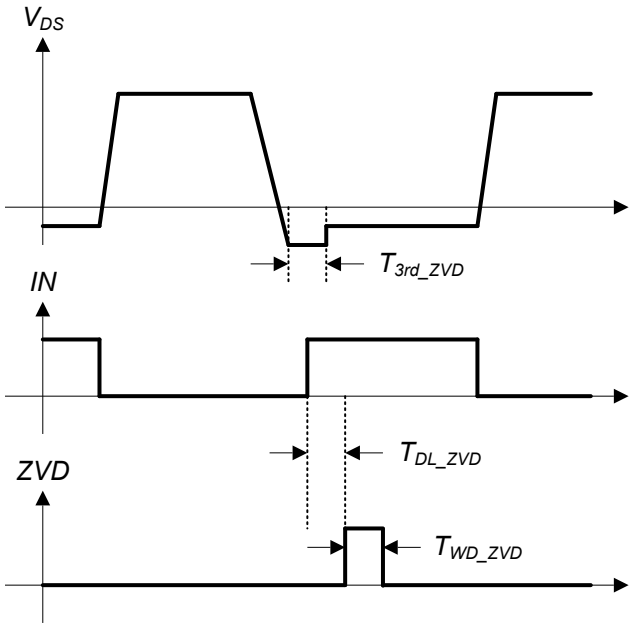


Figure 6-3. ZVD Timing Specifications

7 Detailed Description

7.1 Overview

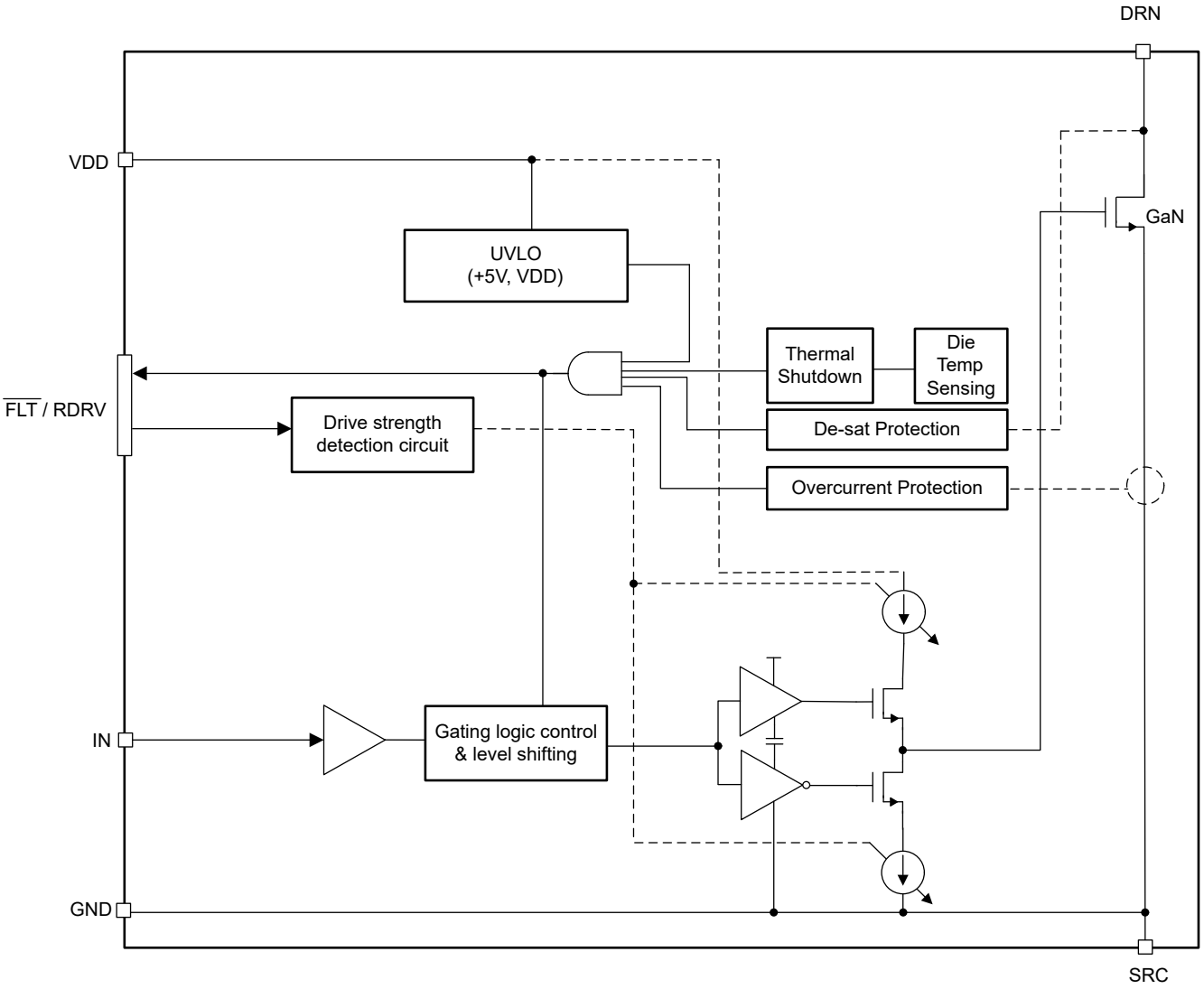
The LMG365xR025 is a high-performance power GaN device with an integrated gate driver. The GaN device offers zero reverse recovery and ultra-low output capacitance to enables high efficiency in bridge-based topologies.

The integrated driver establishes that the device remains off for high drain slew rates. The integrated driver protects the GaN device from overcurrent, short-circuit, overtemperature, and VDD undervoltage. The LMG3656R025 has a zero-voltage detection (ZVD) feature that outputs a pulse signal on the ZVD pin when zero-voltage switching (ZVS) is detected. The LMG3657R025 includes the zero-current detection (ZCD) feature which sets the ZCD pin high when the drain-to-source current is negative and transitions to low upon detecting the zero-crossing point.

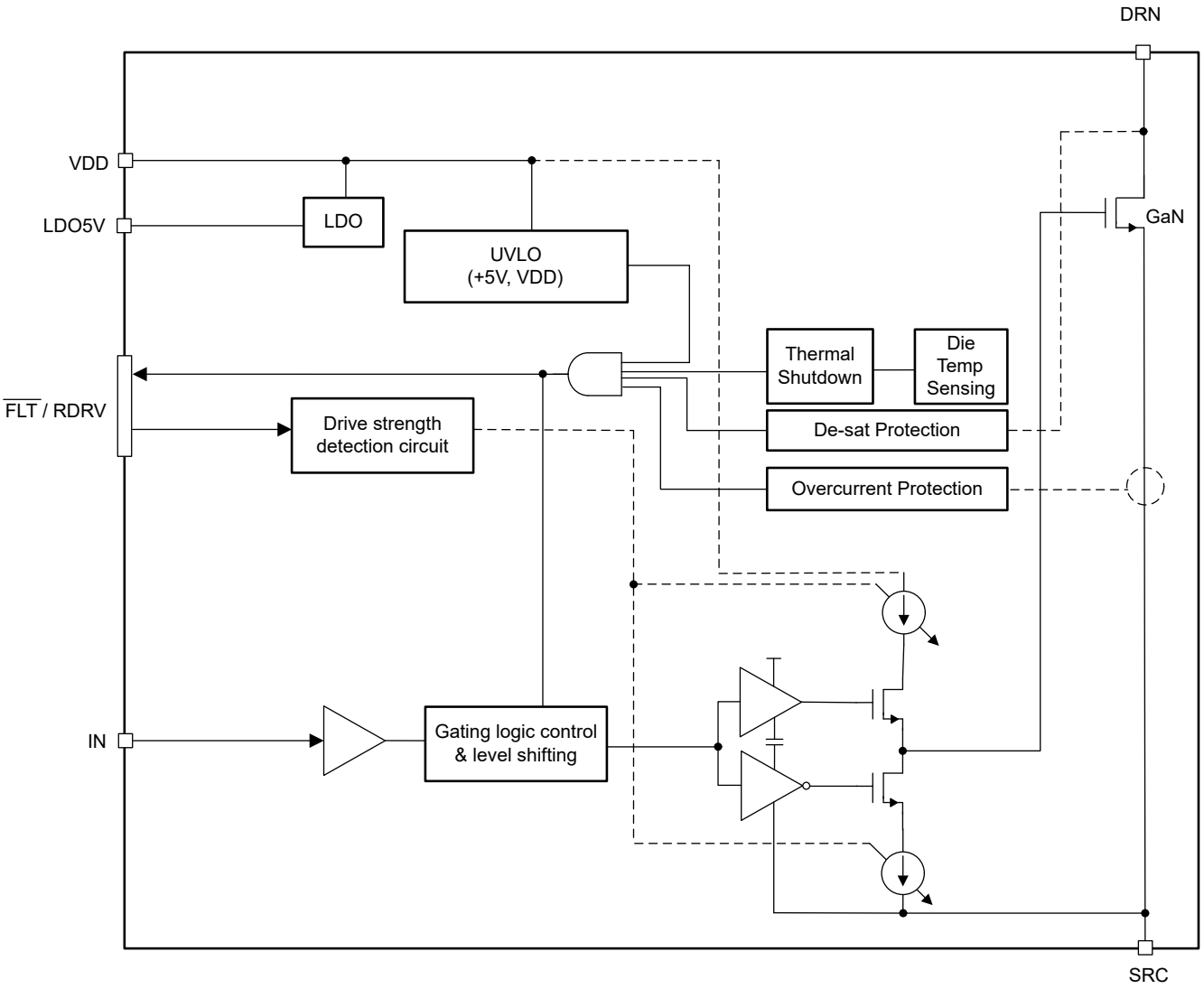
Unlike Si MOSFETs, GaN devices do not have a p-n junction from source to drain and thus have no reverse recovery charge. However, GaN devices still conduct from source to drain similar to a p-n junction body diode, but with higher voltage drop and higher conduction loss. Therefore, minimize source-to-drain conduction time while the LMG365xR025 GaN FET is turned off.

7.2 Functional Block Diagram

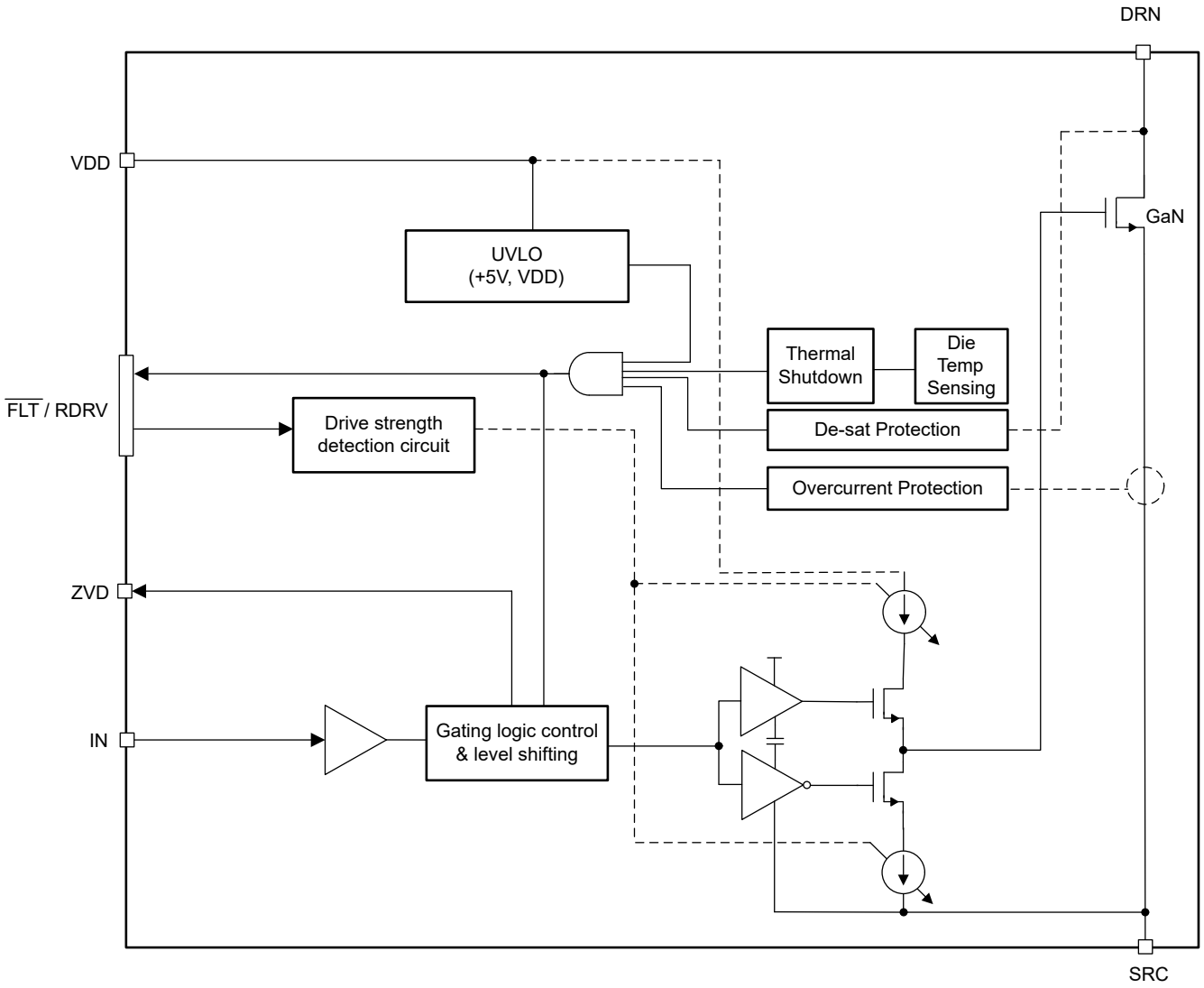
7.2.1 LMG3650R025 Functional Block Diagram



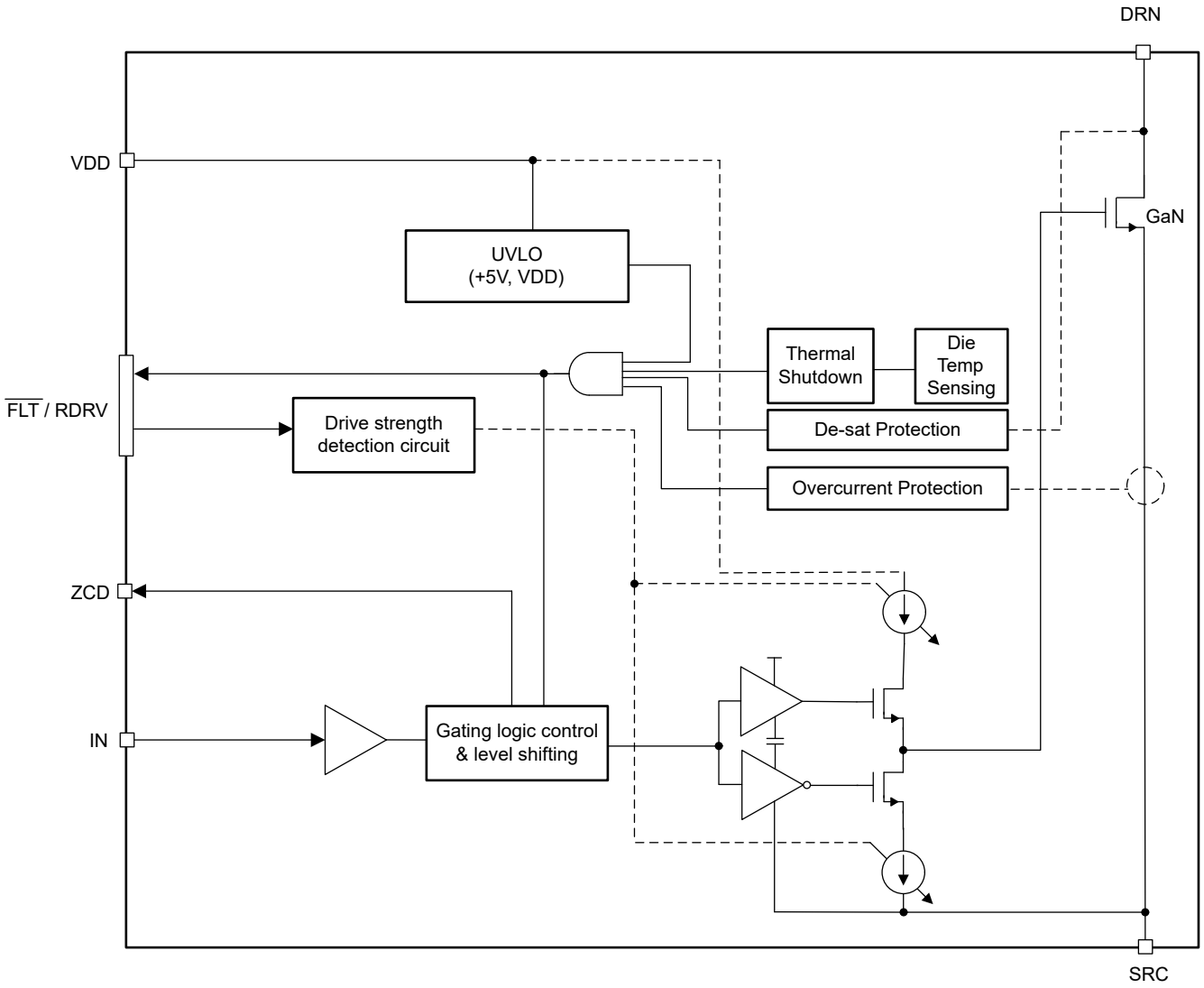
7.2.2 LMG3651R025 Functional Block Diagram



7.2.3 LMG3656R025 Functional Block Diagram



7.2.4 LMG3657R025 Functional Block Diagram



7.3 Feature Description

7.3.1 Drive Strength Adjustment

The LMG365xR025 allows users to adjust the drive strength of the device and obtain a desired slew rate, which provides flexibility when optimizing switching losses and minimizing EMI. Independently control the typical value of turn-on slew rate and the maximum value of turn-off slew rate by connecting the resistors and capacitor as shown in the Drive Strength Adjustment Circuit. The resistance and capacitance on $\overline{\text{FLT}}$/RDRV pin is sensed once at power-up. To do so, the device forces a step-function from 0V to 1.2V on the external $RDRV_{on}$-$RDRV_{off}$-$CDRV_{off}$ network and measures the resulting current waveform. The DC measurement (I_{up}) determines the turn-on slew rate setting, which is programmed by the resistance $RDRV_{on}$. The AC measurement dependent on $RDRV_{on}$-$RDRV_{off}$-$CDRV_{off}$ determines the turn-off slew rate setting, which is dependent on the magnitude of the drain-to-source current charging the output capacitance but can be limited to a maximum value programmed by the resistance $RDRV_{off}$ and capacitance $CDRV_{off}$, connected in parallel to $RDRV_{on}$.

$$I_{up} = \frac{1.2}{RDRV_{on}} A \quad (1)$$

Turn-On Slew Rate Control Table and Turn-Off Slew Rate Control Table show the recommended typical resistances and capacitance programming values at each slew rate setting. The $RDRV_{on}$ values listed in the table assume no parasitic resistance on the $\overline{FLT}$/RDRV pin. However, in real applications, this pin is often connected to an isolator input for fault monitoring. The internal configuration of the isolator can include either a pull-up or pull-down resistor, causing a mismatch between the measured and programmed slew rates—since both fault monitoring and drive strength adjustment share the same pin $\overline{FLT}$/RDRV. An internal pull-up is not preferred, as the voltage at the $\overline{FLT}$/RDRV pin is altered through a voltage divider with the supply of the isolator, Rpull-up, and $RDRV_{on}$, thus reducing control over I_{up}. Using an isolator with an internal pull-down resistor is recommended, as it forms a parallel path with $RDRV_{on}$, then I_{up} is determined by (Rpull-down || $RDRV_{on}$). To match the programmed turn-on slew rate settings, adjust $RDRV_{on}$ so that new I_{up} remains consistent with the programmed value.

$$I_{up} = \frac{1.2}{(Rpull-down \parallel RDRV_{on})} A \quad (2)$$

The slew rate settings are determined one time at power up, then the $\overline{FLT}$/RDRV pin is used as a push-pull 5V digital output for fault monitoring, as described in Fault Reporting. If $RDRV_{off}$ and $CDRV_{off}$ are not used, the device turns-off at full-speed and the turn-off slew rate is strictly determined by the Coss and the load current. If $RDRV_{on}$ is not used, the device defaults to the 80V/ns slew rate setting. Using slower turn-on settings results in higher Eon losses, and slower turn-off settings results in higher Eoff losses.

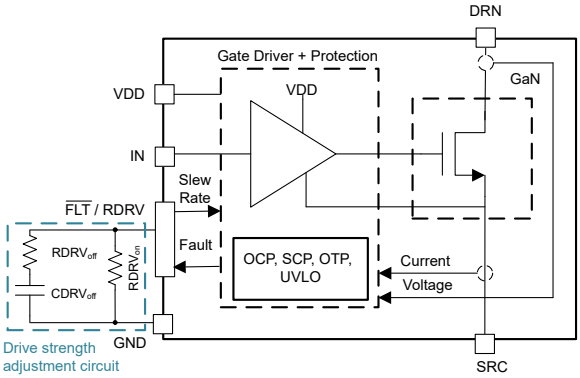


Figure 7-1. Drive Strength Adjustment Circuit

Table 7-1. Recommended Typical Programming Resistance (kΩ) for Adjusting Turn-on Slew Rates

TYPICAL TURN-ON SLEW RATE (V/ns)	$RDRV_{on}$(kΩ)(1)
10	29.4
20	35.7
40	43.2
60	53.6
70	69.8
80	> 400(2)

(1) Fully dependent on the magnitude of the drain-to-source current charging the output capacitance.
(2) Open-circuit connection for programming resistances is acceptable.

Table 7-2. Recommended Typical Programming Resistance (kΩ) and Capacitance (pF) for Adjusting Turn-off Slew Rate Limits

MAXIMUM TURN-OFF SLEW RATE (V/ns)	$RDRV_{off}$(kΩ)(1)	$CDRV_{off}$(pF)(2)
10	2	1800
20	3.57	1000
40	7.68	470

Table 7-2. Recommended Typical Programming Resistance (kΩ) and Capacitance (pF) for Adjusting Turn-off Slew Rate Limits (continued)

MAXIMUM TURN-OFF SLEW RATE (V/ns)	$RDRV_{off}$(kΩ)(1)	$CDRV_{off}$(pF)(2)
Unlimited (1)	High impedence	High impedence

(1) ±1% tolerance on resistance values.
(2) ±10% tolerance on capacitance values.

For example, setting $RDRV_{on}$ = 53.6kΩ, $RDRV_{off}$ = 3.57kΩ and $CDRV_{off}$ = 1000pF results in turn-on slew rate of 60V/ns and turn-off slew rate is limited to a maximum of 20V/ns.

Note

Parasitic power loop inductance can influence the voltage slew rate reading from the V_{DS} switching waveform. The inductance induces a drop on V_{DS} in the current rising phase before voltage falling phase, if this drop is more than 20% of the V_{DC}, the voltage slew rate reading can be influenced. Refer to Section 8.4.1.2 for the power loop design guideline and how to estimate the parasitic power loop inductance.

7.3.2 GaN Power FET Switching Capability

Due to the silicon FET's long reign as the dominant power-switch technology, many designers are unaware that the nameplate drain-source voltage cannot be used as an equivalent point to compare devices across technologies. The nameplate drain-source voltage of a silicon FET is set by the avalanche breakdown voltage. The nameplate drain-source voltage of a GaN FET is set by the long term compliance to data sheet specifications.

Exceeding the nameplate drain-source voltage of a silicon FET can lead to immediate and permanent damage. Meanwhile, the breakdown voltage of a GaN FET is much higher than the nameplate drain-source voltage. For example, the breakdown drain-source voltage of the LMG365xR025 GaN power FET is more than 800V which allows the LMG365xR025 to operate at conditions beyond an identically nameplate rated silicon FET.

The LMG365xR025 GaN power FET switching capability is explained with the assistance of GaN Power FET Switching Capability. The figure shows the drain-source voltage versus time for the LMG365xR025 GaN power FET for four distinct switch cycles in a switching application. No claim is made about the switching frequency or duty cycle. The first two cycles show normal operation and the second two cycles show operation during a rare input voltage surge. The LMG365xR025 GaN power FETs are intended to be turned on in either zero-voltage switching (ZVS) or discontinuous-conduction mode (DCM) switching conditions.

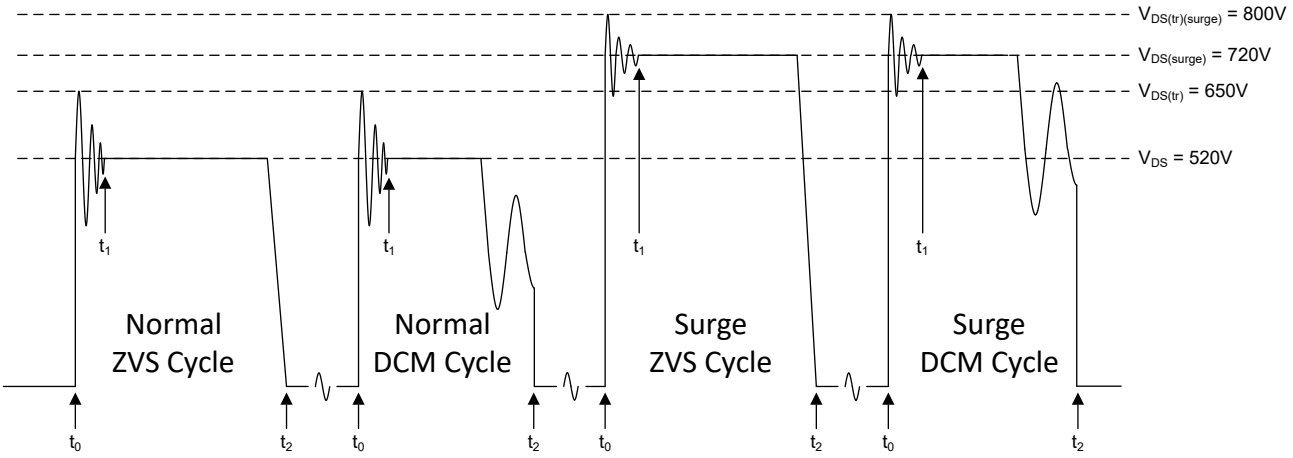


Figure 7-2. GaN Power FET Switching Capability

Each cycle starts before t_0 with the FET in the on state. At t_0 the GaN FET turns off and parasitic elements cause the drain-source voltage to ring at a high frequency. The high frequency ringing has damped out by t_1. Between

t_1 and t_2 the FET drain-source voltage is set by the characteristic response of the switching application. The characteristic is shown as a flat line (plateau), but other responses are possible. At t_2 the GaN FET is turned on. For normal operation, the transient ring voltage is limited to 650V and the plateau voltage is limited to 520V. For rare surge events, the transient ring voltage is limited to 800V and the plateau voltage is limited to 720V.

7.3.3 VDD Supply

VDD is the input supply for the internal circuits. Wide voltage ranges from 9V to 24V are supported on VDD pin.

7.3.4 Overcurrent and Short-Circuit Protection

The driver detects two types of current faults: overcurrent and short-circuit.

The overcurrent protection (OCP) circuit monitors drain current and compares that current signal with an internally set limit $I_{T(OC)}$. Upon detection of the overcurrent, the LMG365xR025 performs cycle-by-cycle protection as shown in Cycle-by-Cycle Overcurrent Protection Operation. In this mode, the GaN device is shut off when the drain current crosses the $I_{T(OC)}$ plus a delay $t_{off(OC)}$, but the overcurrent signal clears after the IN pin signal goes low.

In the next cycle, the GaN device turns on as normal. Use the cycle-by-cycle function in cases where steady-state operation current is below the OCP level but transient response still reach current limit, while the circuit operation cannot pause. The cycle-by-cycle function also prevents the GaN device from overheating by overcurrent induced conduction losses. Additionally, the OCP level dynamically adjusts with junction temperature, with the internally set limit $I_{T(OC)}$ being higher at lower temperatures and decreasing as temperature increases, as defined in the Specifications, based on Equation 3. Dynamic adjustment allows customer to operate the device at lower temperatures with higher currents.

$$\frac{I_{T(OC)150°C}}{I_{T(OC)25°C}} = 77\% \tag{3}$$

The short-circuit protection is based on detection of saturation (de-sat), which monitors the drain-source voltage V_{DS} and compares the voltage with an internally set limit $V_{T(Idsat)}$. Saturation can damage the GaN, causing failures if continued to operate in that condition. If saturation is detected, the GaN device is latched off. Turning off the device at high current causes significant voltage overshoot. Therefore, when turning off from saturation, the device is turned off with an intentionally slowed driver to achieve a lower overshoot voltage and ringing during the turn-off event. This fast response circuit helps protect the GaN device even under a hard short-circuit condition. In this protection, the GaN device is shut off and held off until the fault is reset by either holding the IN pin low for a period of time defined in the Specifications or removing power from VDD.

For safety considerations, OCP allows cycle-by-cycle operation while de-sat latches the device until reset. Both faults are reported on the $\overline{FLT}$/RDRV pin.

Figure Figure 7-4 shows the behavior of the OC and de-sat protection. In the first two cycles OC limit is triggered without de-sat being triggered, so cycle-by-cycle protection takes place. In the third cycle OC limit is triggered, but within the $t_{off(OC)}$ the de-sat protection is triggers when V_{DS} rises above $V_{T(Idsat)}$. Since de-sat protection triggers, this results in a slowed turn-off and latched protection.

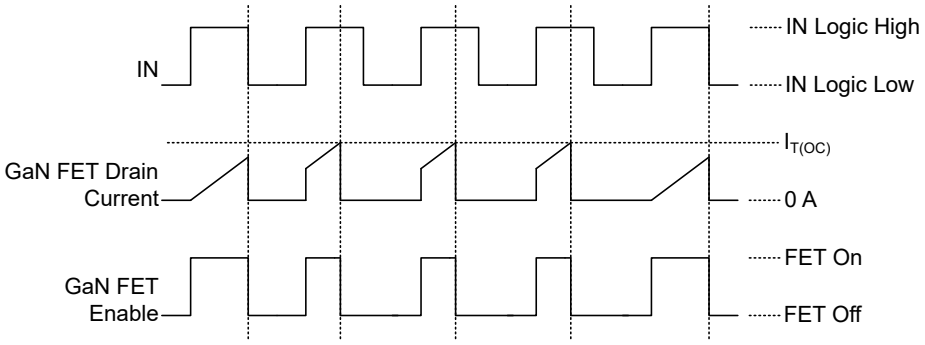


Figure 7-3. Cycle-by-Cycle Overcurrent Protection Operation

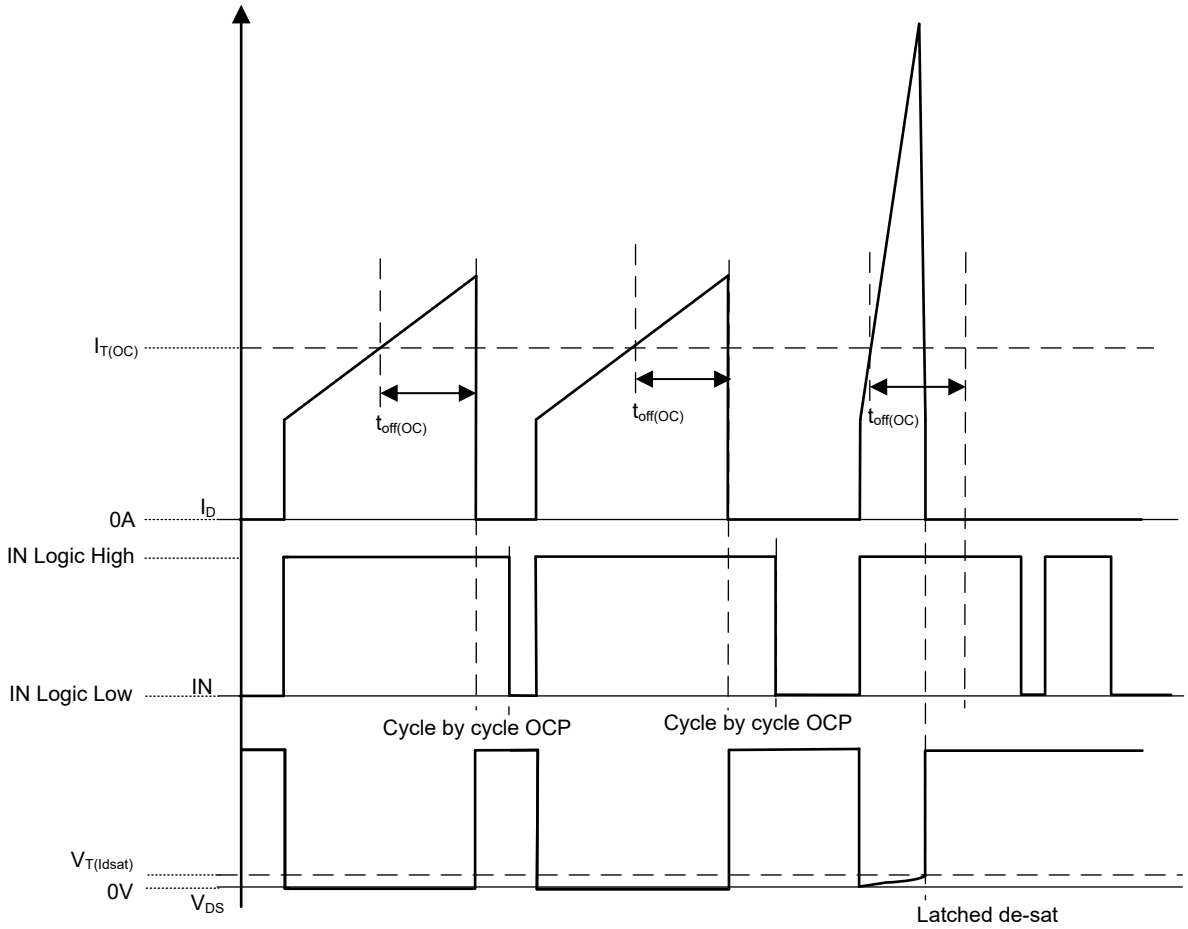


Figure 7-4. Overcurrent Detection vs Desaturation Detection

7.3.5 Overtemperature Protection

The overtemperature protection monitors the GaN FET temperature and holds off the GaN device when the temperature rises above the overtemperature protection threshold. The overtemperature protection hysteresis avoids erratic thermal cycling. An overtemperature fault is reported on the $\overline{FLT}$/RDRV pin when the overtemperature protection is asserted. $\overline{FLT}$/RDRV de-asserts and the device automatically returns to normal operation after the device temperature fall below the negative-going trip point.

7.3.6 UVLO Protection

The LMG365xR025 supports a wide range of V_{DD} voltages. However, when the V_{DD} voltage is below V_{DD} UVLO threshold, the GaN device stops switching and is held off. The V_{DD} UVLO voltage hysteresis prevents on-off chatter near the UVLO voltage trip point. The $\overline{FLT}$/RDRV pin is pulled low as an indication of UVLO.

7.3.7 Fault Reporting

All faults are reported on the $\overline{FLT}$/RDRV pin, which serves as both an input and output pin.

The $\overline{FLT}$/RDRV is configured as an input only at the time of power-up to adjust the drive-strength, as described in Drive Strength Adjustment.

The $\overline{FLT}$/RDRV is used as an active low digital output, indicating the fault status thereafter. The pin is a push-pull 5V digital output which goes high when all faults have cleared, which means that there is additional quiescent current through R1 when the pin is forced high.

Depending on the input threshold levels for the external digital receiver connected to the fault pin, the 1.2V step function which is forced on this pin at power-up can be interpreted as either high or low. For this reason,

TI recommends that the receiver has higher thresholds such as those common for CMOS-compatible inputs and not use TTL compatible inputs. If the minimum input threshold of the external digital receiver connected to the fault pin is at or below 1.2V, the 1.2V step function at power-up can be interpreted as a *high*, before the LMG365xR025 is ready to begin switching.

7.3.8 Auxiliary LDO (LMG3651R025 Only)

A 5V voltage regulator inside LMG365xR025 is used to supply external loads, such as digital isolators for the high-side drive signal. The digital outputs of LMG365xR025 use this 5V rail as a voltage supply. A capacitor is not required for stability, but transient response is poor if no external capacitor is provided. If the application uses the LDO5V pin to supply external circuits, TI recommends using a capacitor of at least 0.1µF for improved transient response. Use a larger capacitor for further transient response improvement. Verify that the decoupling capacitor is a low-ESR ceramic type. Capacitances above 0.47µF slow down the start-up time of the LMG365xR025, due to the ramp-up time of the 5V rail.

7.3.9 Zero-Voltage Detection (ZVD) (LMG3656R025 Only)

The zero-voltage switching (ZVS) converters are widely used to improve the power converter's efficiency. However, in those soft-switching topologies like LLC and triangular current mode (TCM) totem pole PFC, the device can lose ZVS depending on the load condition, inductor, magnetic parameters and control techniques, which affects the system efficiency. To insure ZVS, certain design margins or additional circuits are needed which sacrifices the converter performance and adds components.

To simplify the system design for soft-switching converters, the LMG3656R025 part integrates a zero-voltage detection (ZVD) circuit that provides a digital feedback signal to indicate if the device has achieved ZVS in the current switching cycle. The circuit diagram is shown in Circuit Diagram for Zero-Voltage Detection Circuit Block Diagram. When the IN pin signal goes high, the logic circuit checks if the device V_{DS} has reached below -1V to determine whether the device achieves zero voltage switching in the switching cycle. Once a ZVS is identified, a pulse-output with a width of T_{WD_ZVD} is sent out from the ZVD pin, after a delay time of T_{DL_ZVD} as indicated in ZVD Timing Specifications. Note that a certain third quadrant conduction time is required to allow the device detecting a zero-voltage switching, and T_{3rd_ZVD} is a function of the gate driver strength.

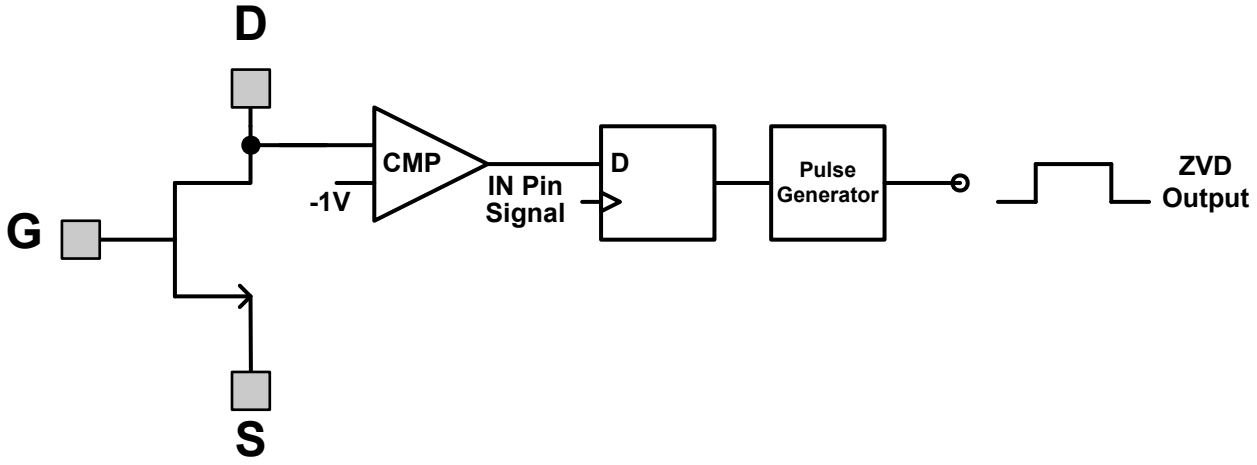


Figure 7-5. Circuit Diagram for Zero-Voltage Detection Circuit Block Diagram

ZVD Function in a CCM Buck Converter shows the waveforms of the ZVD pin corresponding to a continuous conduction mode buck converter. These waveforms demonstrate how ZVD function works in both hard-switching and soft-switching conditions. For I_L in the waveforms in ZVD Function in a CCM Buck Converter load current going out of the switch node is positive. In CCM buck operation, the high-side device is the hard-switching device while the low-side device can achieve zero-voltage switching with a proper dead-time settings. In the first switching cycle when low-side device IN pin rises, the switch-node voltage V_{DS} drops below zero and stays in third quadrant conduction for a period of T_1. Since this third quadrant conduction time T_1 is larger than the detection time T_{3rd_ZVD} specified in Electrical Characteristics, a zero-voltage transition is identified and the ZVD

pin outputs a pulse signal. The pulse width of the ZVD pulse is also defined in the electrical characteristic table as T_{WD}. In the second switching cycle, the device is turned on earlier, and the third quadrant conduction time T_2 is less than T_{3rd_ZVD}. Since T_2 is less than T_{3rd_ZVD}, the ZVD signal stays low, even though the device achieves ZVS. In the third switching cycle, the IN pin signal is advanced even earlier, and the device is in partial hard-switching. Accordingly, the ZVD output stays low when a ZVS transition is not acheived. Note the high side ZVD output stays low in this CCM buck operation as the high side device is always hard-switching turn-on.

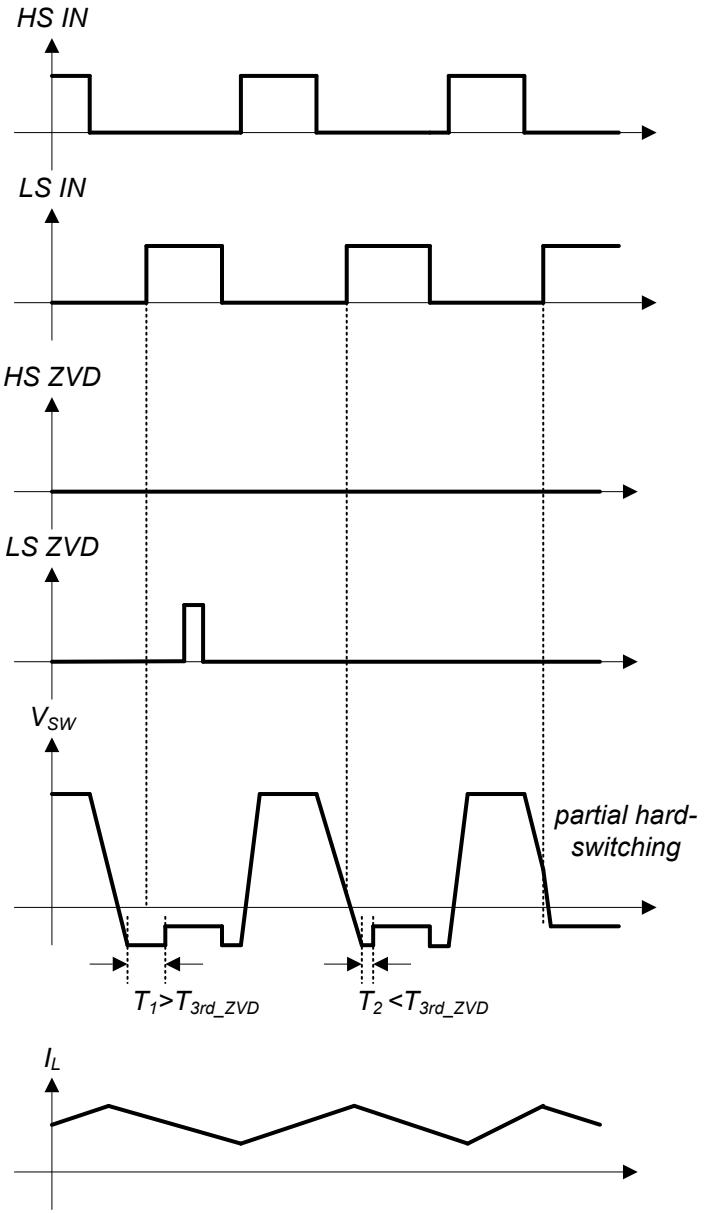


Figure 7-6. ZVD Function in a CCM Buck Converter

The ZVD function facilitates the control in soft-switching topology. ZVD Function in a TCM TP PFC Converter illustrate the facilitation with the ZVD waveforms in a TCM totem pole PFC. This diagram shows the positive half line-cycle with V_{IN} greater than half of V_{OUT}. For I_L in the waveforms in ZVD Function in a TCM TP PFC Converter load current going into the switch node is defined as positive. In the first switching cycle, the load current builds enough negative current, and the low-side device achieves ZVS with a clear third quadrant conduction time beyond T_{3rd_DET}. Therefore, the ZVD pin outputs a pulse signal. The ZVD pulses are missing

in the next two switching cycles because the third quadrant conduction time shortens in second cycle and the device loses ZVS in the third cycle.

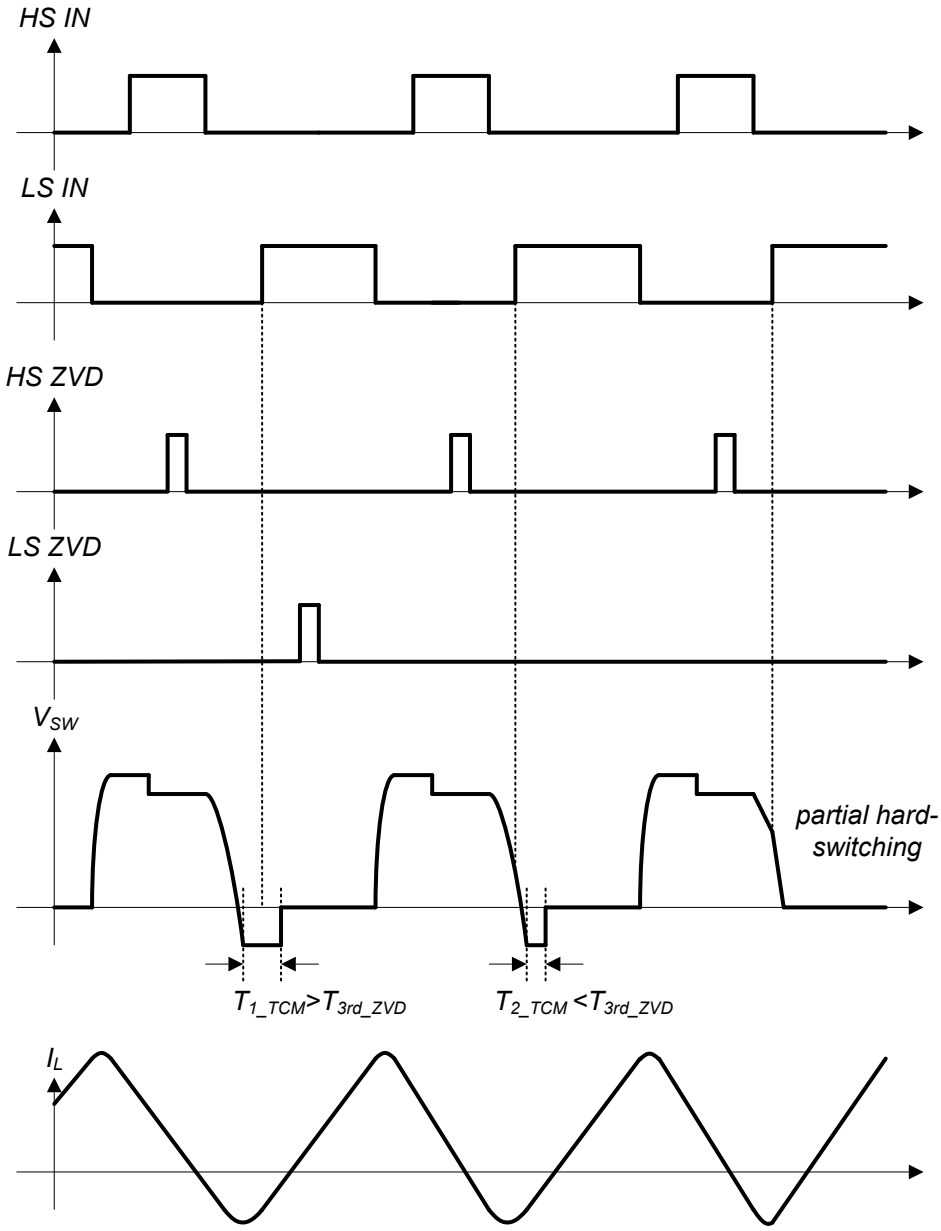


Figure 7-7. ZVD Function in a TCM TP PFC Converter

7.4 Device Functional Modes

The device has one applicable mode of operation when operating within the Recommended Operating Conditions.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMG365xR025 is a power IC targeting soft-switching applications operating up to 520V bus voltages. GaN devices offer zero reverse-recovery charge . Low Q_{OSS} of GaN devices also benefits soft-switching converters, such as the LLC and phase-shifted full-bridge configurations. As half-bridge configurations are the foundation of the two mentioned applications and many others, this section describes how to use the LMG365xR025 in a half-bridge configuration.

8.2 Typical Application

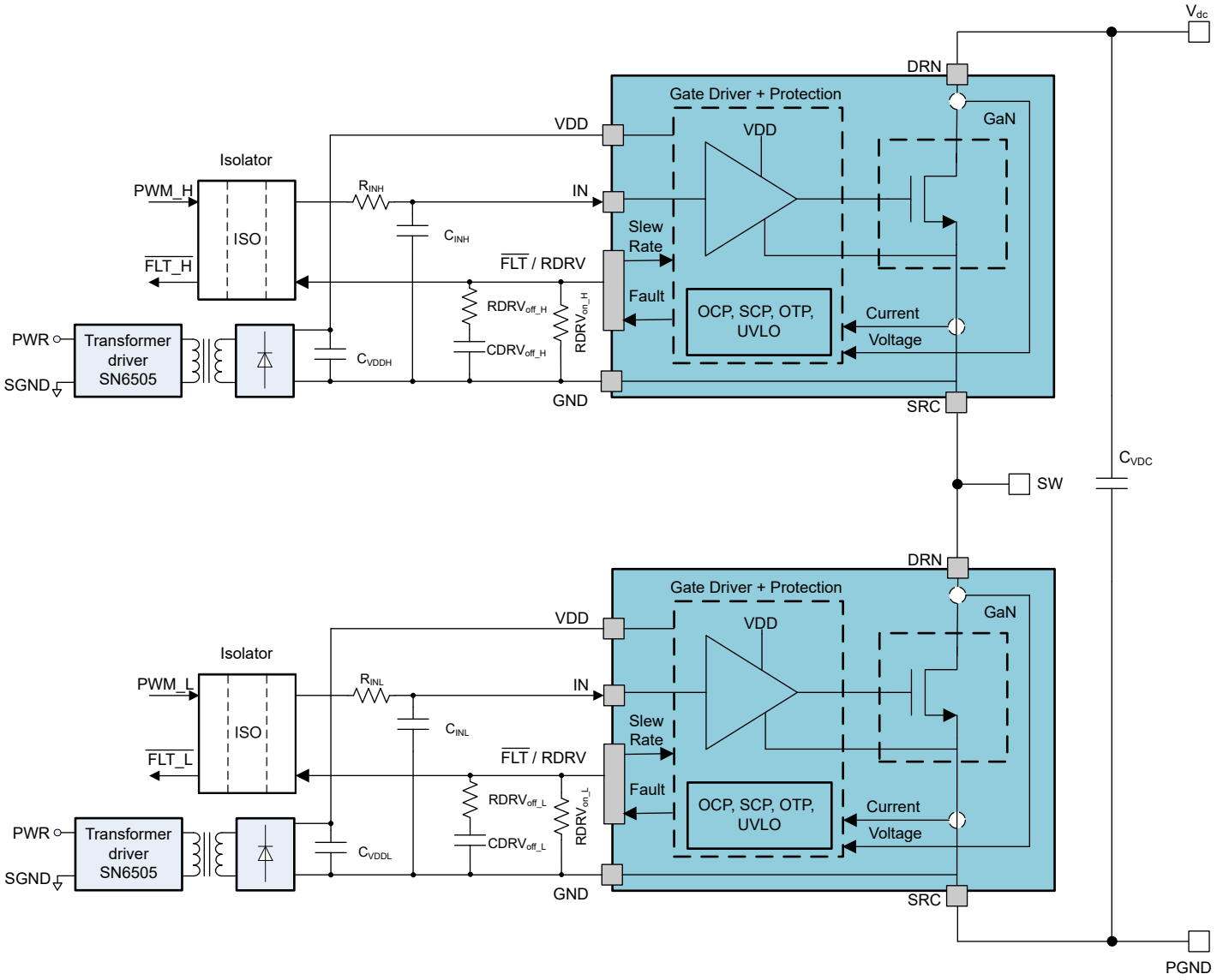


Figure 8-1. LMG3650R025 Typical Half-Bridge Application With Isolated Power Supply

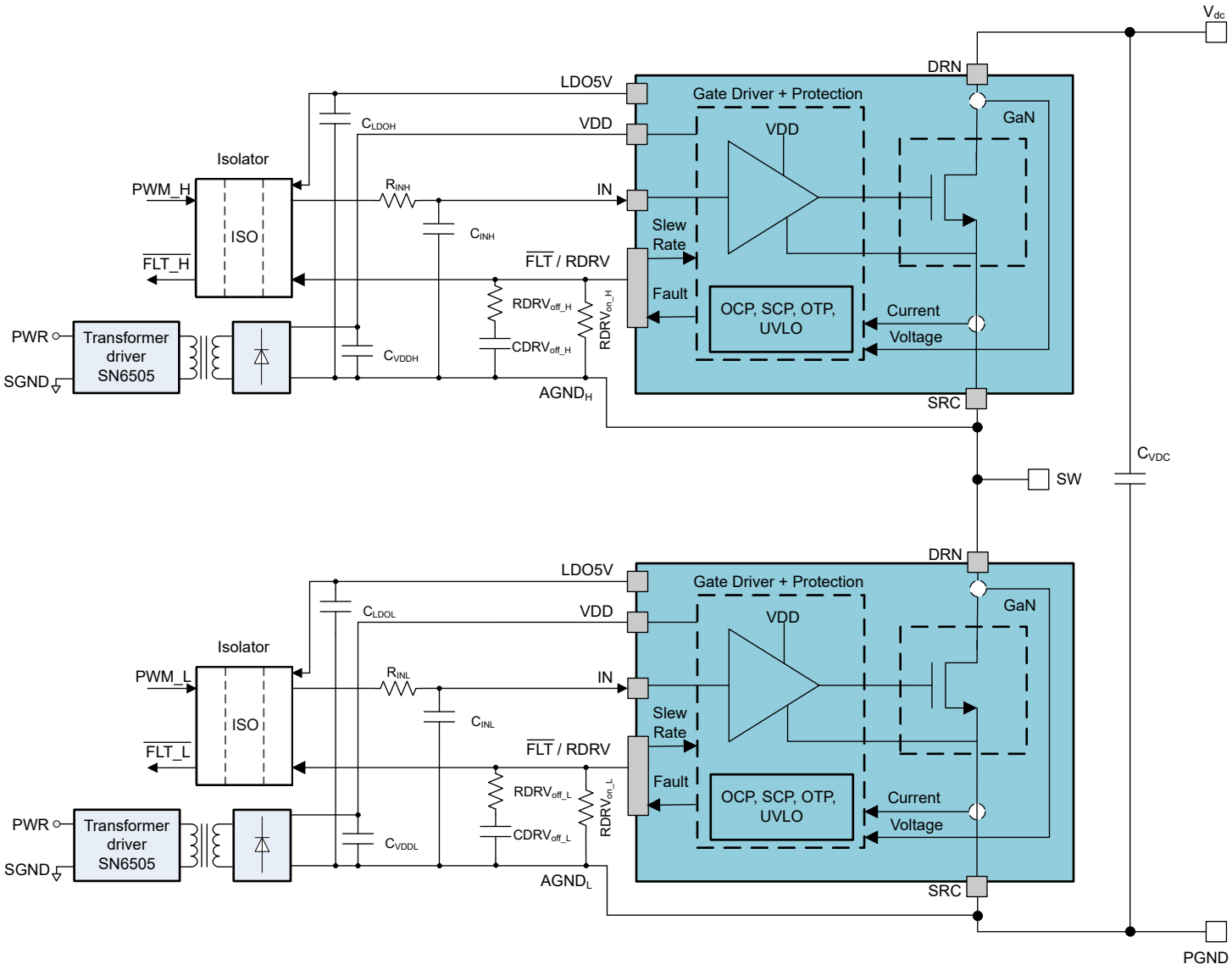


Figure 8-2. LMG3651R025 Typical Half-Bridge Application With Isolated Power Supply

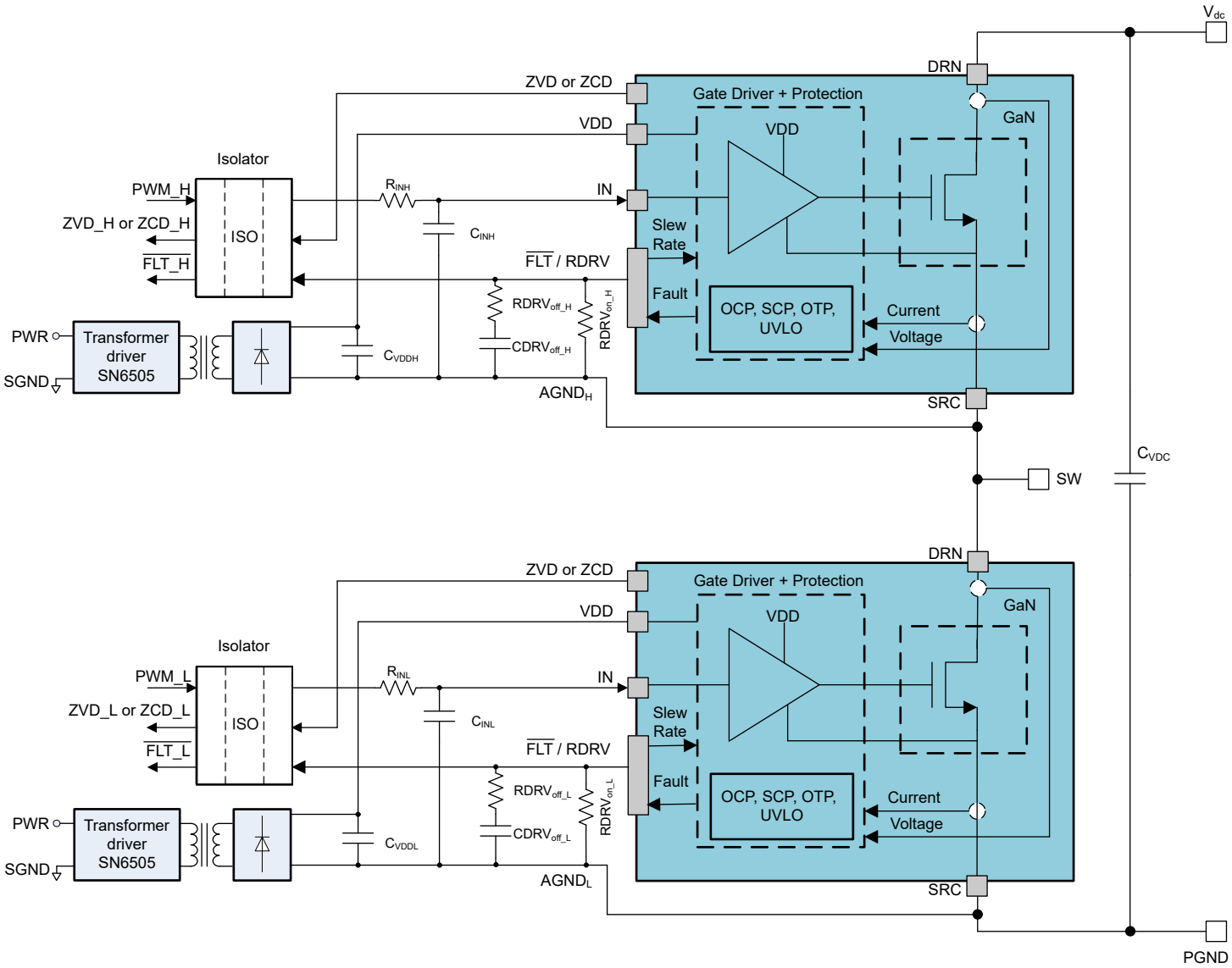


Figure 8-3. LMG3656R025 or LMG3657R025 Typical Half-Bridge Application With Isolated Power Supply

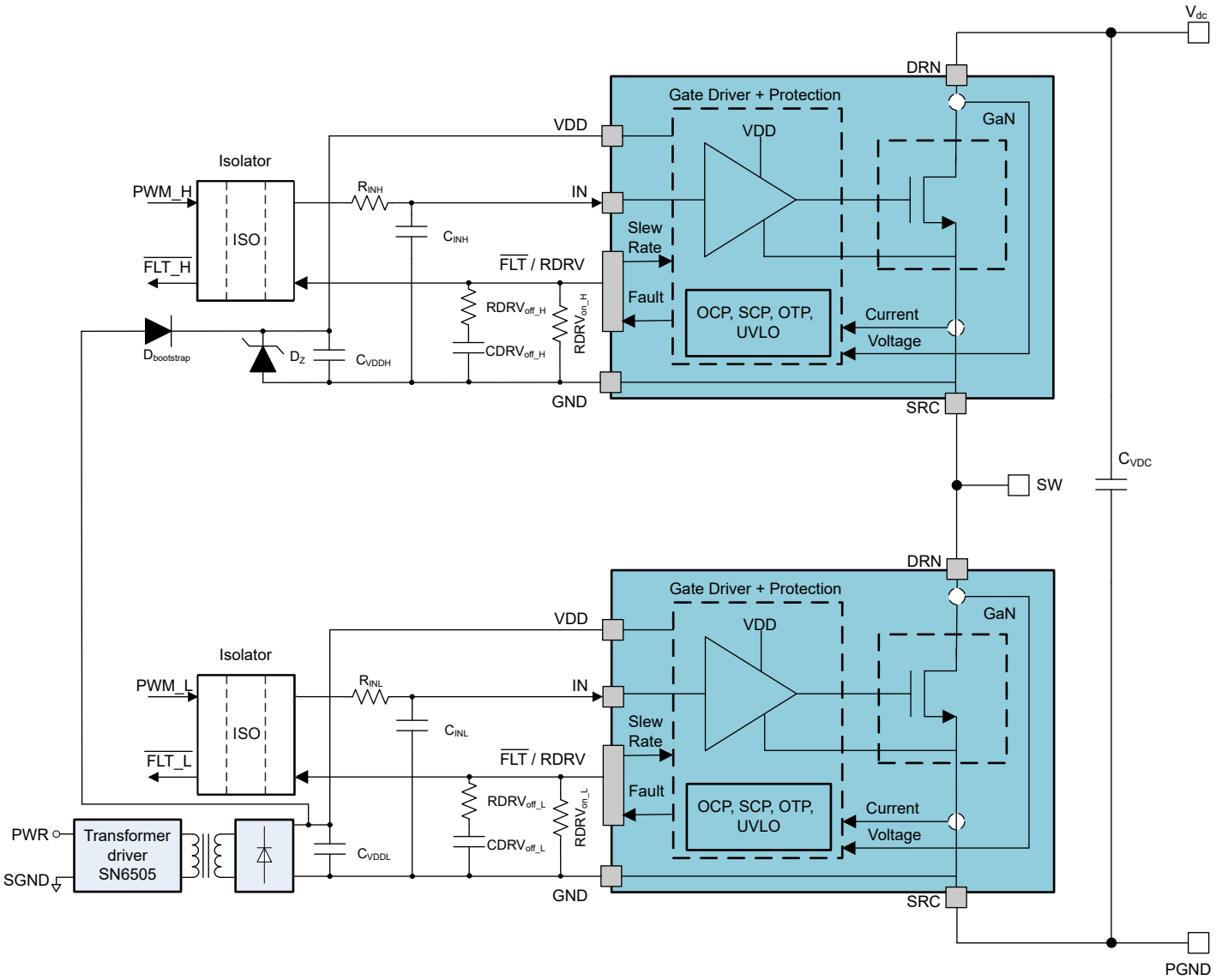


Figure 8-4. LMG3650R025 Typical Half-Bridge Application With Bootstrap

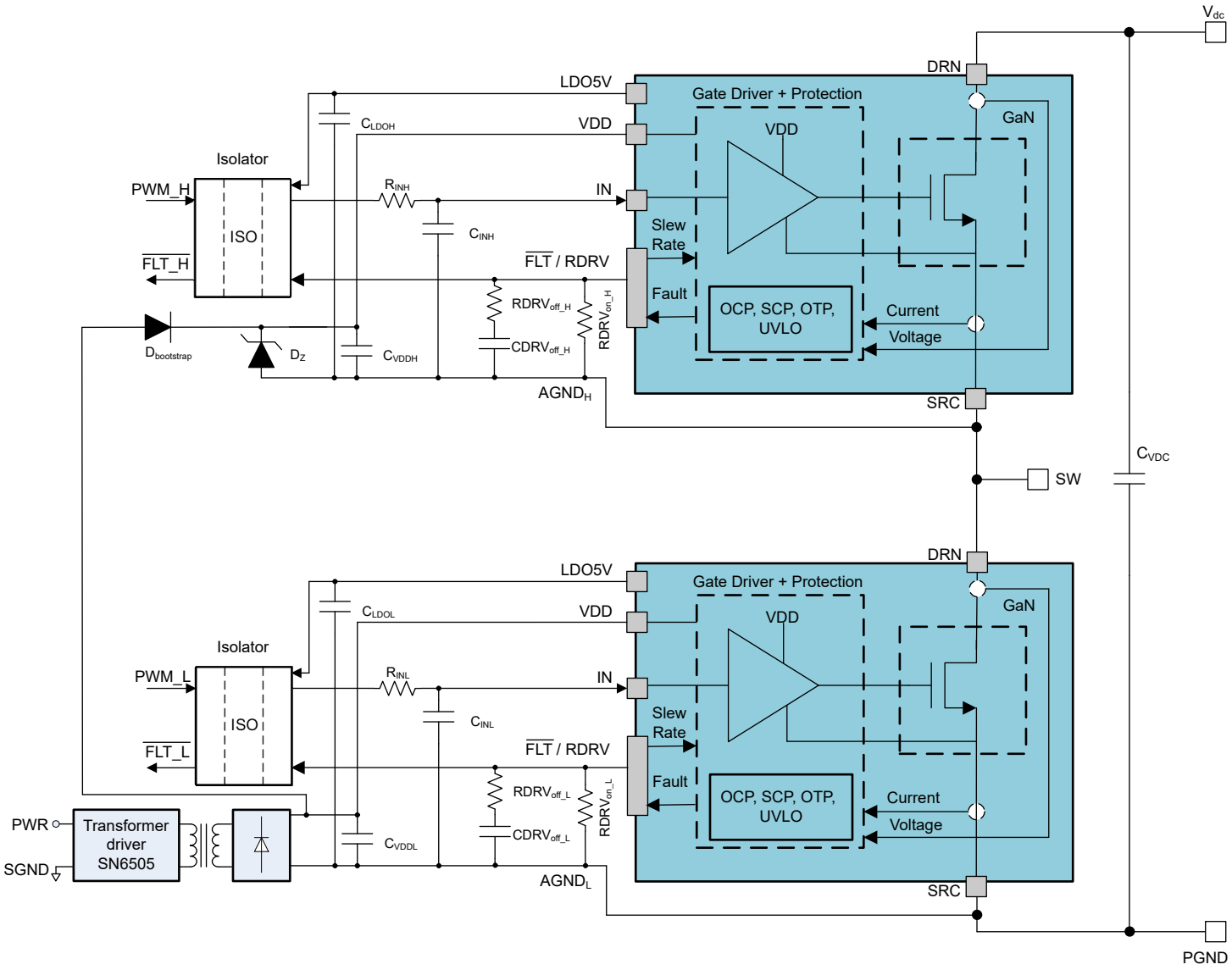


Figure 8-5. LMG3651R025 Typical Half-Bridge Application With Bootstrap

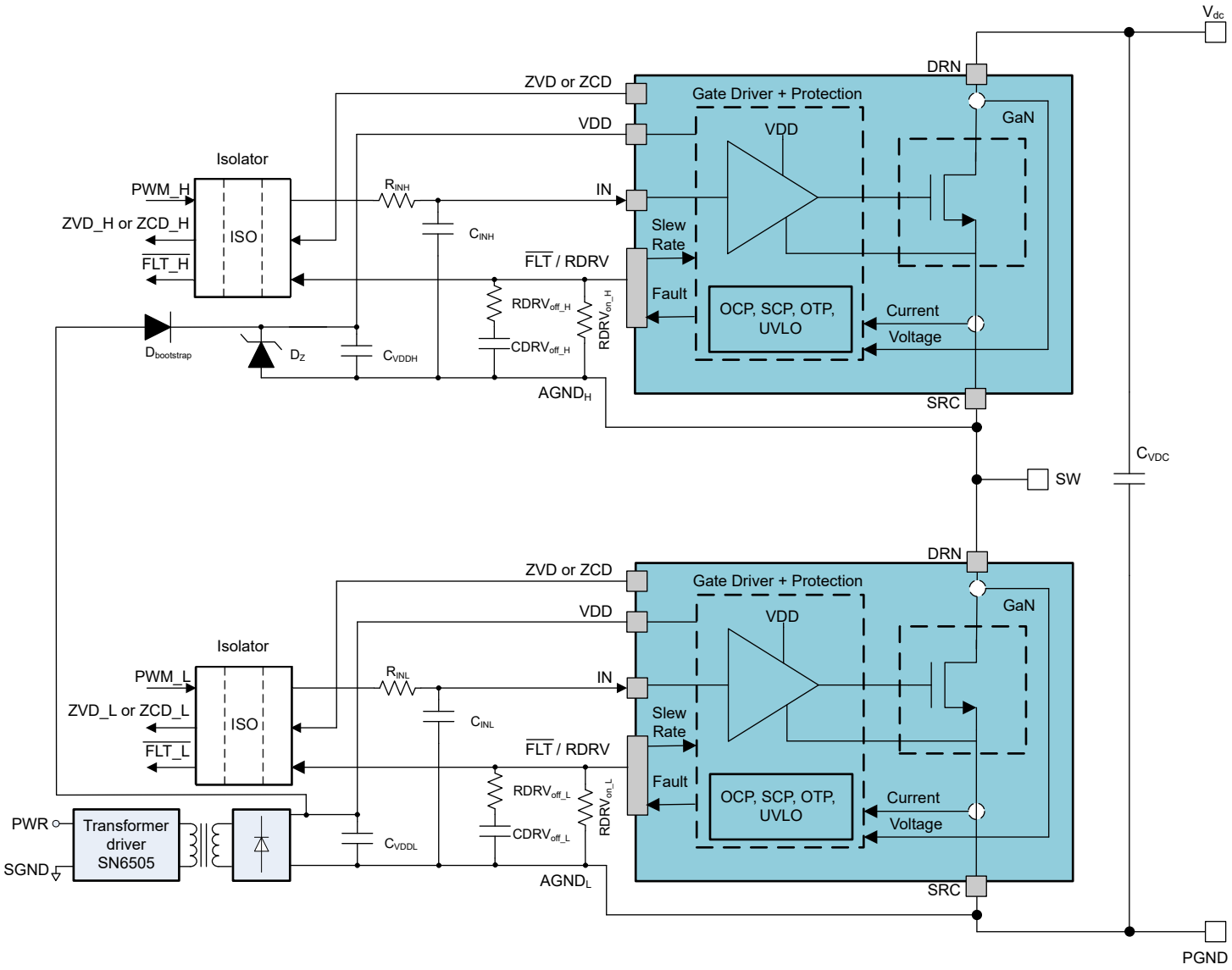


Figure 8-6. LMG3656R025 or LMG3657R025 Typical Half-Bridge Application With Bootstrap

8.2.1 Detailed Design Procedure

In high-voltage power converters, circuit design and PCB layout are essential for high-performance power converters. This data sheet describes design considerations for half-bridges using the LMG365xR025.

8.2.1.1 Slew Rate Selection

Adjust the turn-on slew rate of LMG365xR025 from approximately 10 V/ns to 80V/ns and adjust the maximum turn-off slew rate limit from 10V/ns to unlimited (controlled only by I_{ds}). Refer to Drive Strength Adjustment for the details.

The slew rate affects GaN device performance in terms of:

- Switching loss
- Voltage overshoot
- Noise coupling
- EMI emission

Generally, high slew rates provide low switching loss, but high slew rates can also create higher voltage overshoot, noise coupling, and EMI emissions. Follow the design recommendations in this data sheet to mitigate the challenges caused by a high slew rate. The LMG365xR025 offers circuit designers the flexibility to select the proper slew rate for the best performance of applications.

8.2.1.2 Signal Level-Shifting

In half-bridges, use high-voltage level shifters or digital isolators to provide isolation for signal paths between the high-side device and control circuit. Using an isolator is optional for the low-side device. However, using and isolator equalizes the propagation delays between the high-side and low-side signal paths, and provides the ability to use different grounds for the GaN device and the controller. If an isolator is not used on the low-side device, connect the control ground and power ground at the device and nowhere else on the board. For more information, see Layout Guidelines. With fast-switching devices, common ground inductance can easily cause noise issues without the use of an isolator.

Choosing a digital isolator for level-shifting is important for improvement of noise immunity. As GaN device can easily create high dv/dt, > 50V/ns, TI highly recommends using isolators with high common-mode transient immunity (CMTI) and low barrier capacitance. Isolators with low CMTI can easily generate false signals, which can cause shoot-through. The barrier capacitance is part of the isolation capacitance between the signal ground and power ground, which is directionally proportional to the common mode current and EMI emission generated during the switching. Additionally, TI strongly encourages selecting non-edge-triggered isolators. In an edge-triggered isolator, a high dv/dt event can cause the isolator to flip states and cause circuit malfunction.

Generally, the preference is ON/OFF keyed isolators with a low default output. Default low state establishes that the system does not shoot-through when starting up or recovering from fault events. A high CMTI event causes a very short (a few nanoseconds) false pulse, TI recommends placing a low pass filter (such as 50Ω and 150pF R-C) at the driver input to filter out the false pulses.

8.3 Power Supply Recommendations

The LMG365xR025 only requires an unregulated VDD power supply from 9V to 24V. Obtain the low-side supply from the local controller supply. Verify that the supply of the high-side device comes from an isolated or bootstrap supply.

8.3.1 Using an Isolated Power Supply

The advantage of using an isolated power supply to power the high-side device is that it works regardless of continued power-stage switching or duty cycle. Using an isolated power supply can also power the high-side device before power-stage switching begins for a smooth start-up

Obtain the isolated supply with a push-pull converter, a flyback converter, a FlyBuck™ converter, or an isolated power module. When using an unregulated supply, verify that the input of LMG365xR025 do not exceed the maximum supply voltage. Use a 24V TVS diode to clamp the VDD voltage of LMG365xR025 for additional protection.

8.3.2 Using a Bootstrap Diode

In half-bridge configuration, a floating supply is necessary for the high-side device. To obtain the best performance of LMG365xR025, TI recommends Using an isolated power supply. Use a bootstrap supply can be used with the recommendations of Using a Bootstrap Diode.

8.3.2.1 Diode Selection

The LMG365xR025 offers no reverse-recovery charge and very limited output charge. Circuits using the LMG365xR025 can exhibit high voltage slew rates. Verify that a compatible bootstrap diode do not introduce high output or reverse-recovery charge.

Use a silicon carbide diode, such as the GB01SLT06-214, to avoid reverse-recovery effects. The output charge of the SiC diode is 3nC. Although there is additional loss from its output charge, it does not dominate the losses of the switching stage.

8.3.2.2 Managing the Bootstrap Voltage

In a synchronous buck or other converter where the low-side switch occasionally operates in third-quadrant, the bootstrap supply charges through a path that includes the third-quadrant voltage drop of the low-side LMG365xR025 during the dead time as shown in Charging Path for Bootstrap Diode. This third-quadrant drop can be large, which can overcharge the bootstrap supply in certain conditions. Verify that the V_{DD} supply of LMG365xR025 remains below 26V.

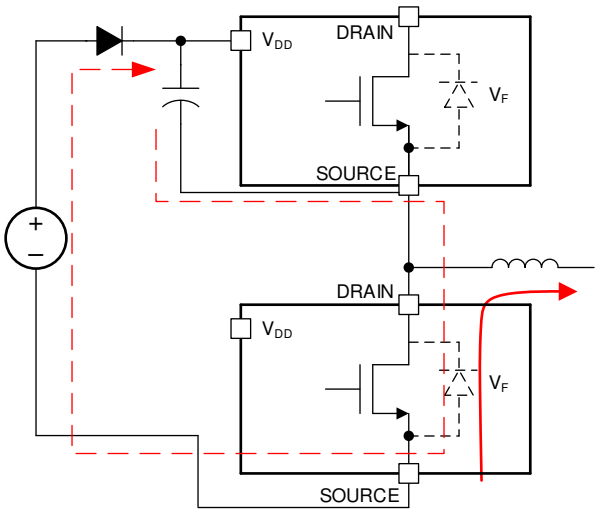


Figure 8-7. Charging Path for Bootstrap Diode

As Suggested Bootstrap Regulation Circuit shows, the recommended bootstrap supply includes a bootstrap diode, series resistor, and 24V TVS or Zener diode in parallel with the V_{DD} bypass capacitor. The parallel location prevents damage to the high-side LMG365xR025. The series resistor limits the charging current at start-up and when the low-side device operates in third-quadrant mode. Select the resistor to allow sufficient current to power the LMG365xR025 at the desired operating frequency. At 100kHz operation, TI recommends a value of approximately 2Ω. At higher frequencies, reduce or omit the resistor value to establish sufficient supply current.

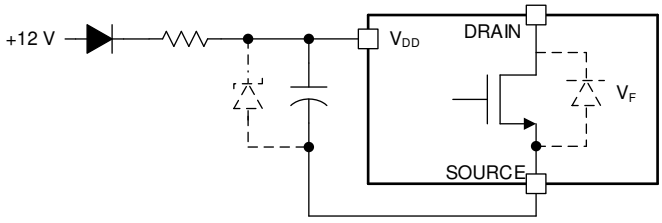


Figure 8-8. Suggested Bootstrap Regulation Circuit

8.4 Layout

8.4.1 Layout Guidelines

The layout of the LMG365xR025 is critical to device performance and functionality. Because the half-bridge configuration is typically used with GaN devices, layout recommendations are considered with this configuration. A four-layer or higher layer count board is recommended to reduce the parasitic inductances of the layout. The following figures summarize critical layout guidelines, and more details are further elaborated in the following sections.

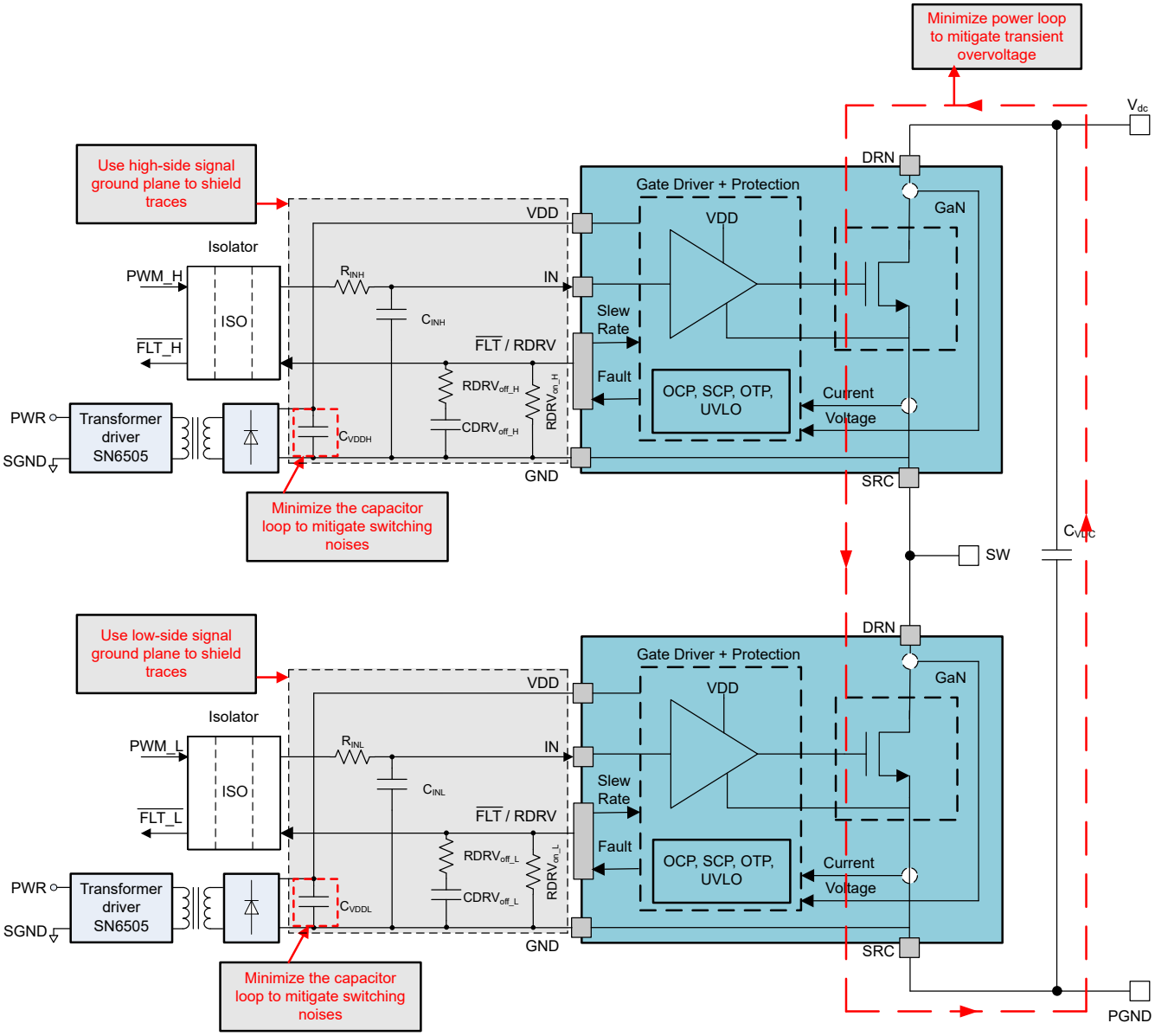


Figure 8-9. LMG3650R025 Typical Schematic With Layout Considerations

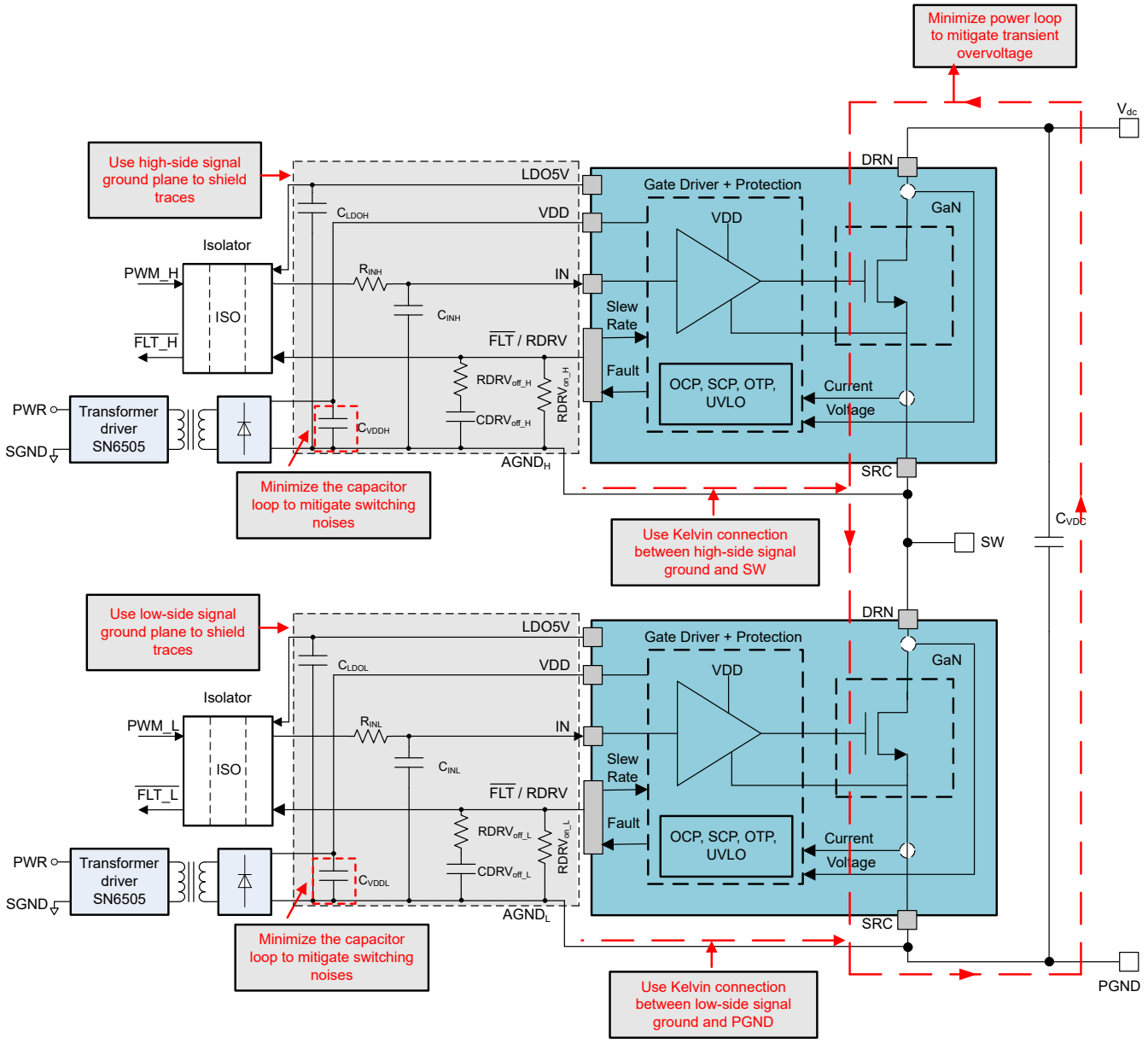


Figure 8-10. LMG3651R025 Typical Schematic With Layout Considerations

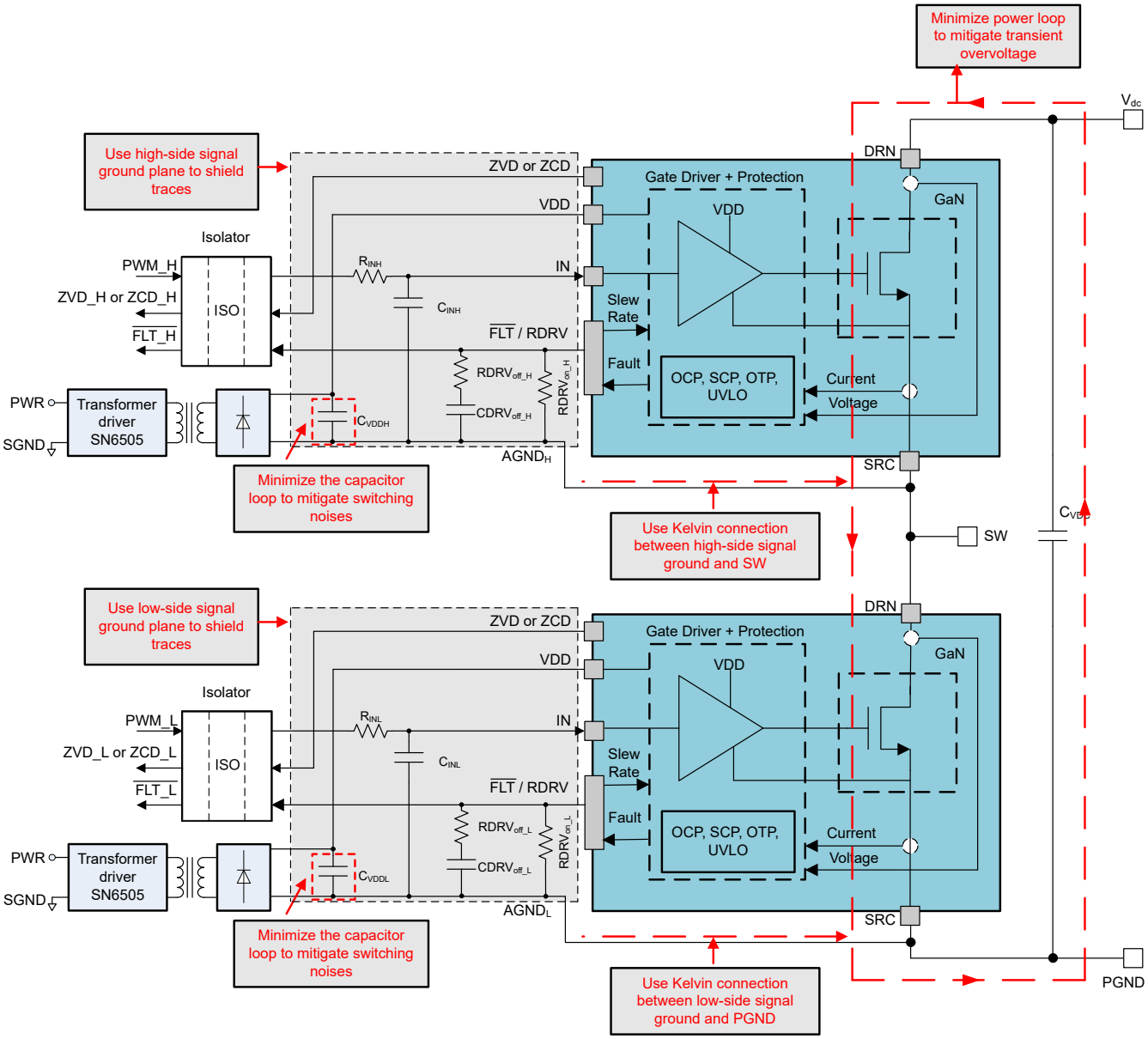


Figure 8-11. LMG3656R025 or LMG3657R025 Typical Schematic With Layout Considerations

8.4.1.1 Solder-Joint Reliability

Because TOLL packages are typically used in high-current applications, verify that the SRC and DRN pads are solder-mask defined (SMD). In practical layout, source and drain pads are often connected to the copper planes that make the largest possible contact area to the PCB to maximize conductivity. Establish that the other solder pads, which carry minimal current and are primarily used for signal connections, are non-solder-mask defined (NSMD), as shown in the land pattern example in Mechanical, Packaging, and Orderable Information. Finally, verify that any board trace in connection with an NSMD pad is less than 2/3 the width of the pad on the pad side where the board trace connects. The trace must maintain the 2/3 width limit for as long as the trace is not covered by solder mask. After the trace is under solder mask, there are no limits on the trace dimensions. All stated recommendations are followed in Layout Example.

8.4.1.2 Power-Loop Inductance

The power loop, comprising of the two devices in the half bridge and the high-voltage bus capacitance, undergoes high *di/dt* during switching events. By minimizing the inductance of the power loop, ringing and electromagnetic interference (EMI) can reduce, as well as a reduction in the voltage stress on the devices.

Place the power devices as close as possible to minimize the power-loop inductance. Position the decoupling capacitors in line with the two devices, close to either device. In Section 8.4.2, the decoupling capacitors are placed on the same layer as the devices. The return path (PGND in this case) is located on second layer in close proximity to the top layer. By using inner layer and not bottom layer, the vertical dimension of the loop reduces, thus minimizing inductance. A large number of vias near both the device terminal and bus capacitance carry the high-frequency switching current to the inner layer, while minimizing impedance.

Estimate the power loop inductance based on the ringing frequency f_{ring} of the drain-source voltage switching waveform based on the following equation:

$$L_{pl} = \frac{1}{4\pi^2 f_{ring}^2 C_{ring}} \quad (4)$$

In Equation 4, C_{ring} is equal to C_{OSS} at the bus voltage (refer to Output Capacitance vs Drain-Source Voltage for the typical value) plus the drain-source parasitic capacitance from the board and load inductor or transformer.

As the parasitic capacitance of load components is hard to characterize, TI recommends capturing the V_{DS} switching waveform without load components to estimate the power loop inductance. Typically, the power loop inductance of the Section 8.4.2 is approximately 2.5nH.

8.4.1.3 Signal-Ground Connection

The SRC pin of LMG365xR025 internally connects to the GND pin of the power IC, the signal-ground reference. Verify that the local signal-ground planes connect to the GND pin with low impedance star connection. In addition, verify that the return path for the passives associated to the driver (bypass capacitors) connect to the GND pin. In Section 8.4.2, local signal-ground planes are on second layer to act as the return path for the local circuitry. The local signal-ground planes do not connect to the high-current SRC pins, except the star connection at the GND pin.

8.4.1.4 Bypass Capacitors

Place the VDD pin bypass capacitors $C_{VDDL}$and C_{VDDH} close to the VDD pin with low impedance connections.

8.4.1.5 Switch-Node Capacitance

GaN devices have very low output capacitance and switch quickly with a high *dv/dt*, yielding very low switching losses. To preserve the low switching losses, minimize the number of additional capacitances added to the output node. Follow the below guidelines to minimize the PCB capacitance at the switch node:

- Minimize overlap between the switch-node plane and other power and ground planes.
- Make the GND return path under the high-side device thinner while still maintaining a low-inductance path.
- Choose high-side isolator ICs and bootstrap diodes with low capacitance.
- Place the power inductor as close to the GaN device as possible.
- Construct the power inductors with a single-layer winding to minimize intrawinding capacitance.
- If a single-layer inductor is not possible, consider placing a small inductor between the primary inductor and the GaN device to effectively shield the GaN device from the additional capacitance.
- If using a back-side heat-sink, use the least amount of area of the switch-node copper coverage on the bottom copper layer to improve the thermal dissipation.

8.4.1.6 Signal Integrity

Protect the control signals to the LMG365xR025 from the high *dv/dt* caused by fast switching. Coupling between the control signals and the drain can cause circuit instability and potential destruction. Route the control signals (IN, ZVD, ZCD, and $\overline{FLT}$/RDRV) over a ground plane placed on an adjacent layer. In Section 8.4.2, for example, all the signals route on layers close to the local signal ground plane.

Capacitive coupling between the traces for the high-side device and the static planes, such as PGND and HVBUS, can cause common mode current and ground bounce. Mitigate coupling by reducing overlap between the high-side traces and the static planes. For the high-side level shifter, ensure that no copper from either the input or output side extend beneath the isolator. Copper extending beneath the isolator can compromise the CMTI of the device.

8.4.1.7 High-Voltage Spacing

Circuits using the LMG365xR025 involve high voltage, potentially up to 650V. When laying out circuits using the LMG365xR025, understand the creepage and clearance requirements for the application and how the requirements apply to the GaN device. Functional (or working) isolation is required between the source and drain of each transistor, and between the high-voltage power supply and ground. Functional isolation or perhaps stronger isolation (such as reinforced isolation) can be required between the input circuitry to the LMG365xR025 and the power controller. Choose signal isolators and PCB spacing (creepage and clearance) distances which meet the user-specific isolation requirements.

If a heat sink is used to manage thermal dissipation of the LMG365xR025, establish that necessary electrical isolation and mechanical spacing is maintained between the heat sink and the PCB.

8.4.1.8 Thermal Recommendations

The LMG365xR025 is a lateral device grown on a Si substrate. The thermal pad connects to the source of device electrically and thermally. In applications with high power dissipation, cooling using just the PCB may not be sufficient to keep the part at a reasonable temperature. To improve the thermal dissipation of the part, TI recommends connecting a heat sink to the back of the PCB to extract additional heat. Using power planes, thicker copper layers, and numerous thermal vias, the heat dissipated in the LMG365xR025 can spread out in the PCB and effectively pass to the other side of the PCB. By connecting the top copper layer with the bottom layer, thermal vias allow heat flow to bypass the low-thermal-conducting FR4 layers. Therefore, the overall effective thermal conductivity of the PCB improves. Thermal vias are normally formed by mechanical drilling. Because air is a poor thermal conductor, a plated copper layer on the via inner surface is recommended to conduct heat vertically through the PCB. For better thermal performance, use higher via plating thickness. To further improve the effect of thermal vias, fill the air gap with high thermal conductive epoxy or copper. Also cap the vias located in the footprint of the device. Without capping, solder from the pad leak into the via causing solder voids under the device. Apply a heat sink to bare areas on the back of the PCB using an thermal interface material (TIM). Remove the solder mask from the back of the board underneath the heat sink for more effective heat removal.

8.4.2 Layout Example

Correct layout of the LMG365xR025 and surrounding components is essential for correct operation. The layouts shown here reflect the GaN device schematic in Figure 8-1. The layouts in Figure 8-1 produce good results and are intended as a guideline. However, obtaining acceptable performance with alternate layout schemes is possible. Additionally, please refer to the land pattern example in Section 11.2 for the latest recommended PCB footprint of the device.

The top-layer layout and mid-layer layout are shown. The layouts are zoomed in to the LMG3650R025 U2 and U4 component placements. The mid-layer layout includes the outlines of the top layer components to assist the user in lining up the top-layer and mid-layer layouts.

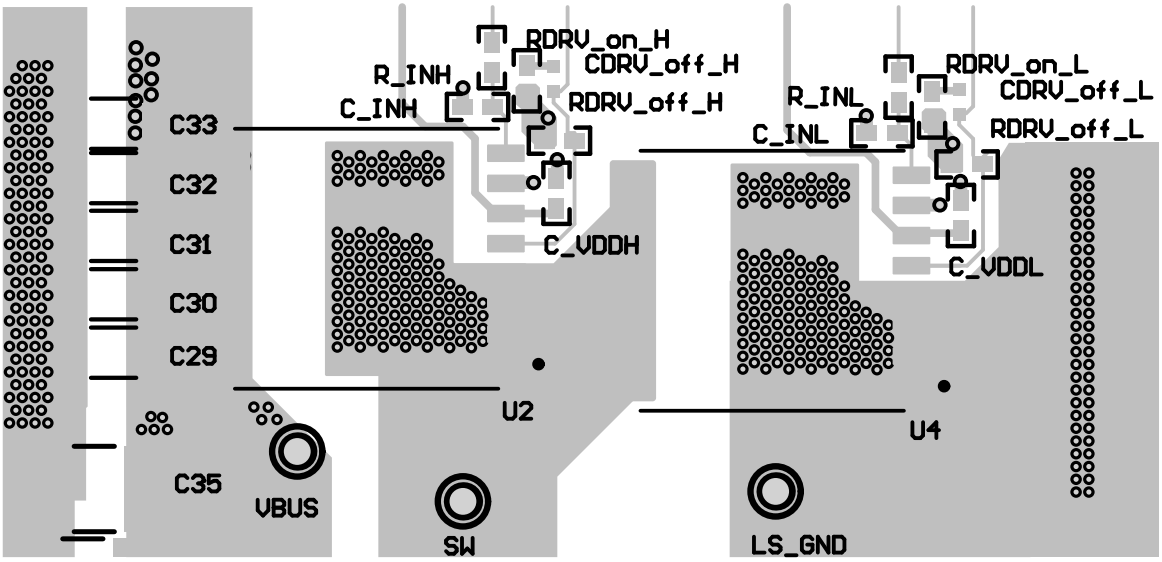


Figure 8-12. LMG3650R025 Half-Bridge Top-Layer Layout

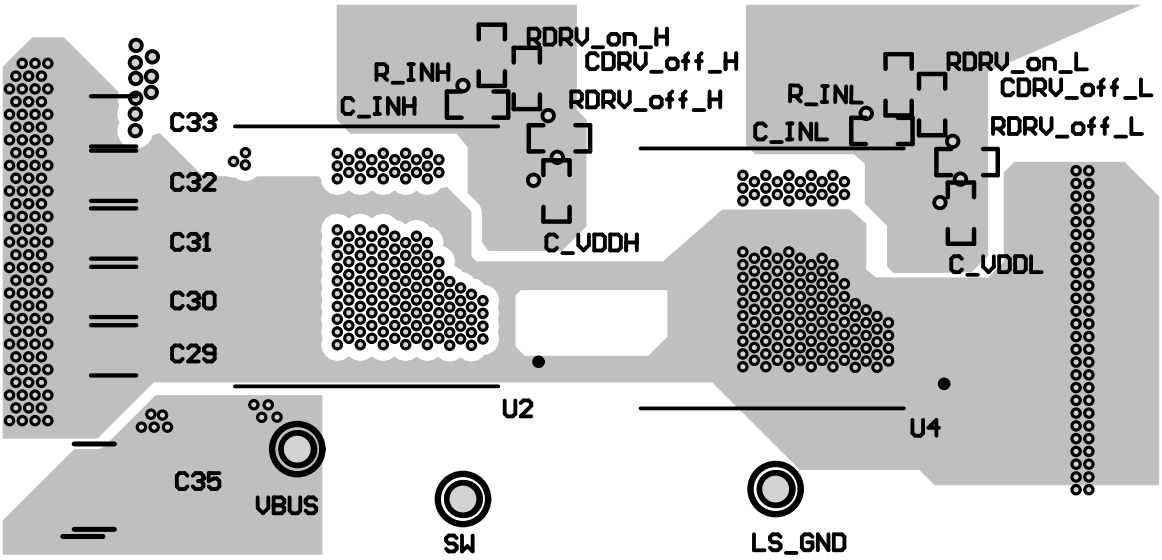


Figure 8-13. LMG3650R025 Half-Bridge Mid-Layer Layout

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

FlyBuck™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2025) to Revision A (December 2025)	Page
• Updated from Advance Information to Production Mix	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

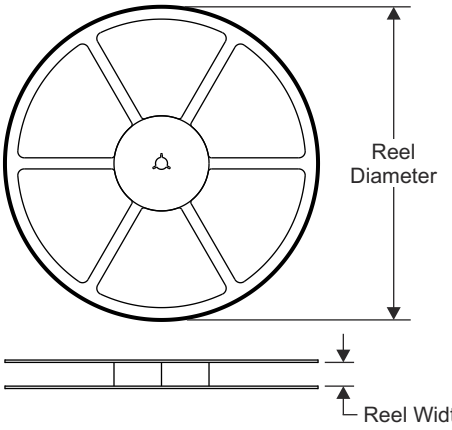
PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
LMG3650R025KLAR	Active	Production	KLA | 9	2000 | LARGE T&R	RoHS Exempt	Sn	Level-3-260C-168 HR	-40 to 175	LMG3650 R025

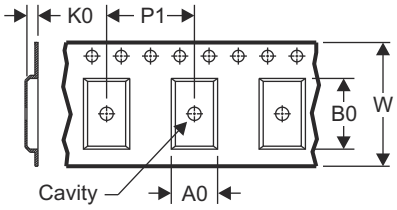
(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

11.1 Tape and Reel Information

REEL DIMENSIONS

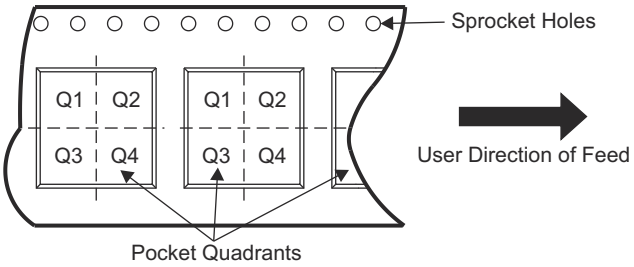


TAPE DIMENSIONS



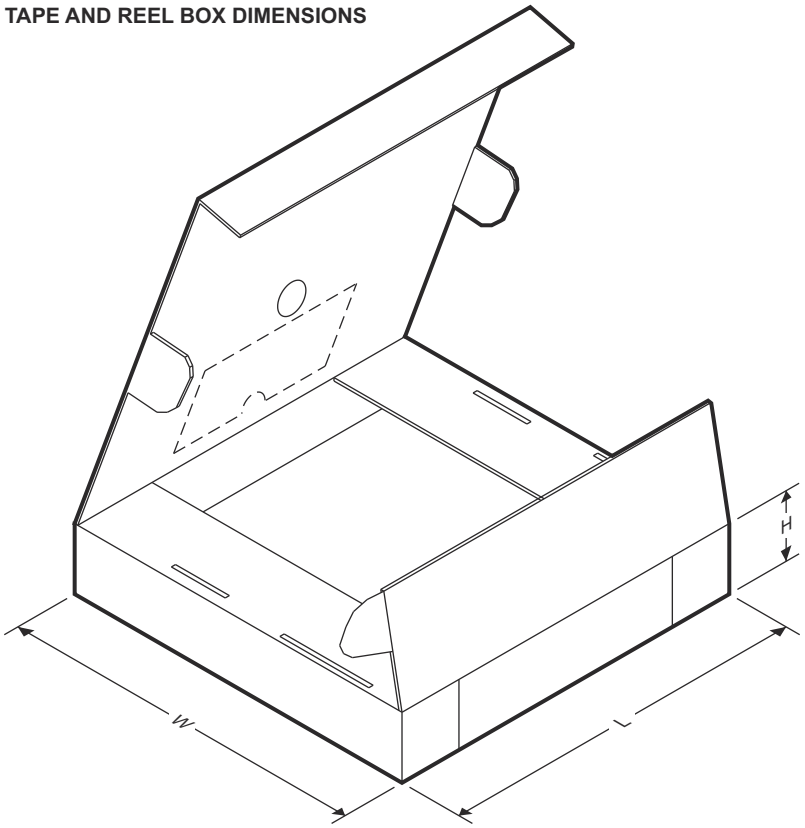
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

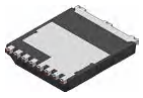


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG3650R025	TO	KLA	9	2000	330.0	24.4	10.20	11.98	2.6	12.0	21.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG3650R025	TO	KLA	9	2000	356.0	356.0	45.0

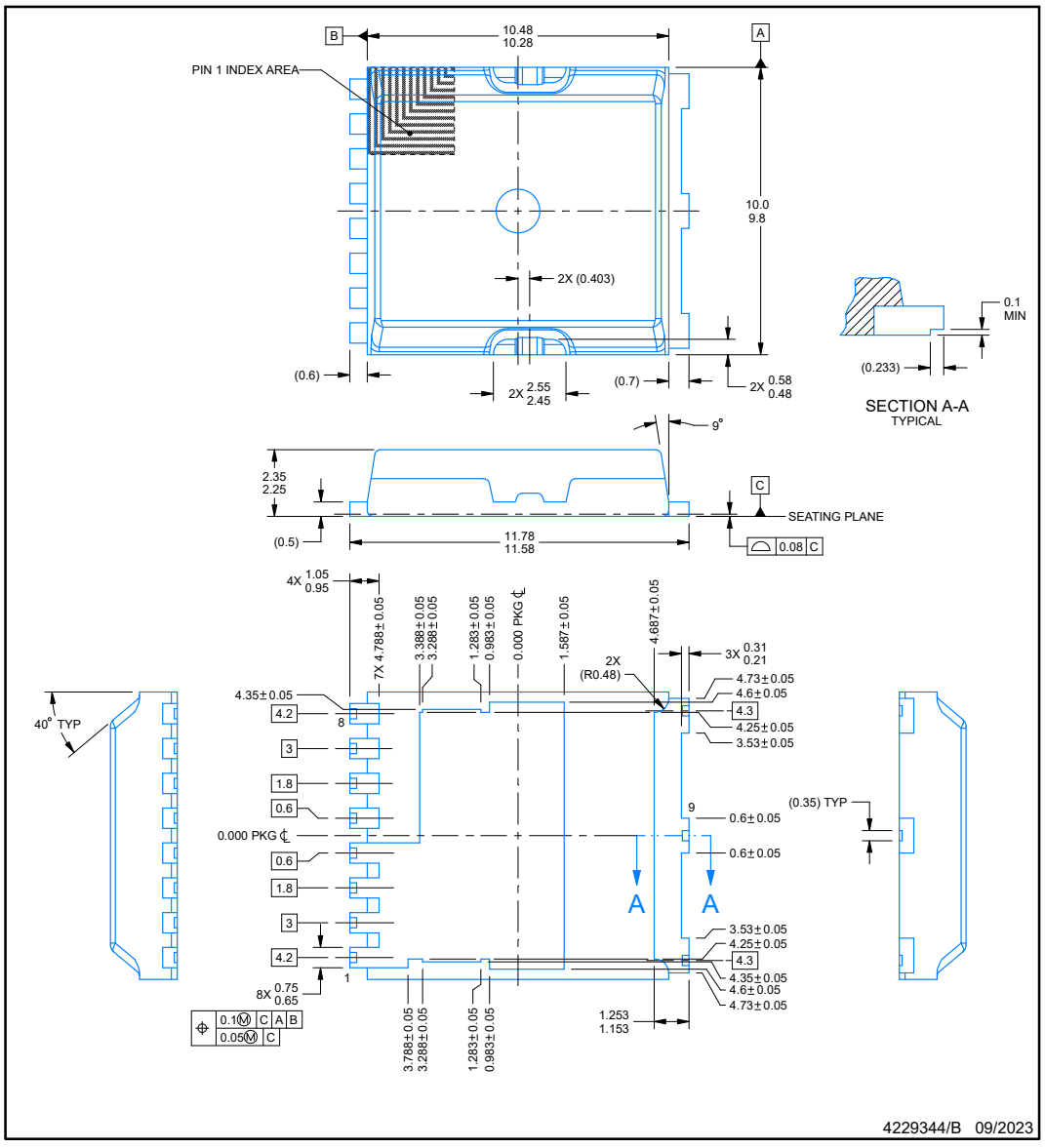


PACKAGE OUTLINE

KLA0009A

TOLL - 2.35 mm max height

TO LEADLESS



NOTES:

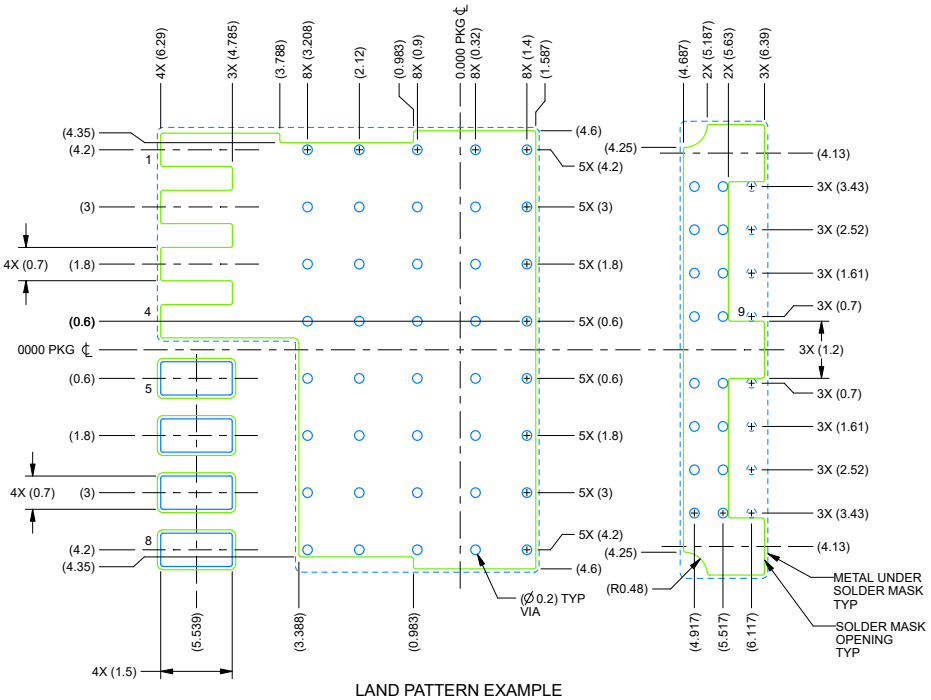
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

KLA0009A

TOLL - 2.35 mm max height

TO LEADLESS



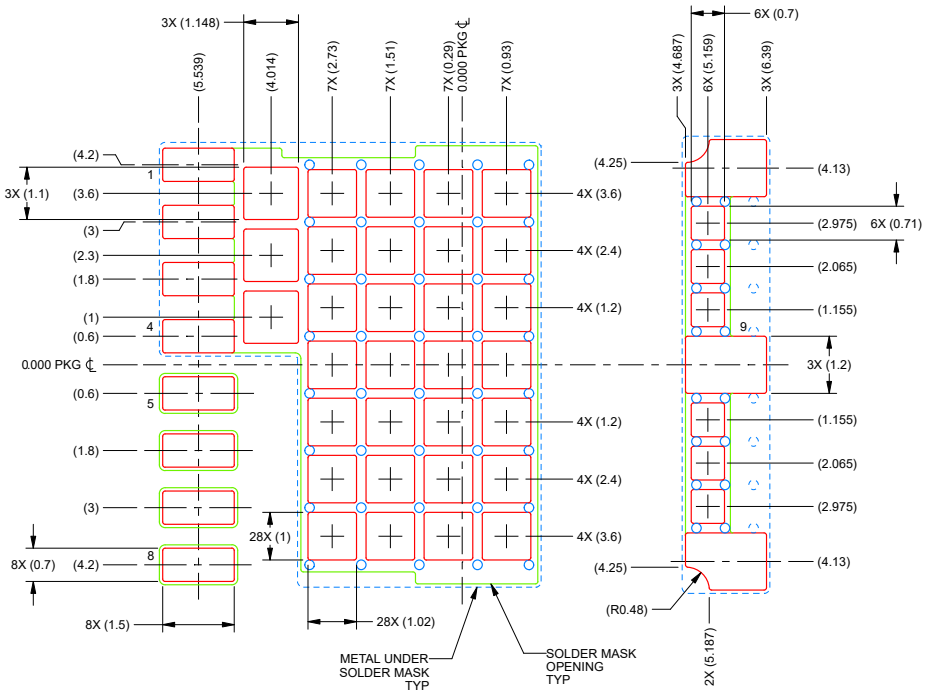
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KLA0009A **TOLL - 2.35 mm max height**

TO LEADLESS



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD CONNECTED TO PINS 1 - 4: 67%
PAD 9: 87%

4229344/B 09/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMG3650R025KLAR	Active	Production	TO (KLA) | 9	2000 | LARGE T&R	ROHS Exempt	SN	Level-3-260C-168 HR	-40 to 150	LMG3650 R025
XLMG3650R025KLAT	Active	Preproduction	TO (KLA) | 9	250 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
XLMG3650R025KLAT.B	Active	Preproduction	TO (KLA) | 9	250 | LARGE T&R	-	Call TI	Call TI	-40 to 175	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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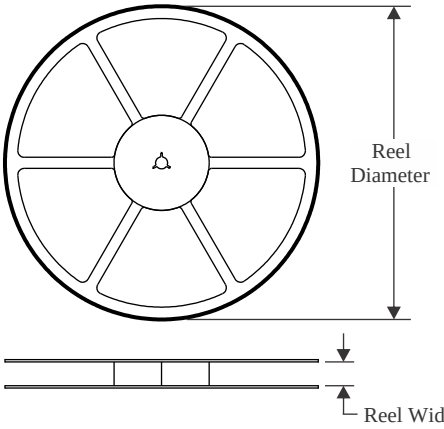
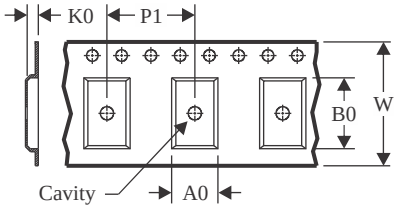
TAPE AND REEL INFORMATION

REEL DIMENSIONS

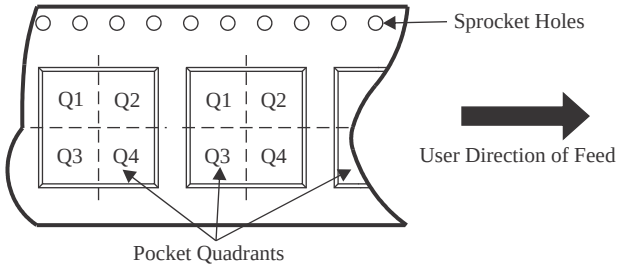


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

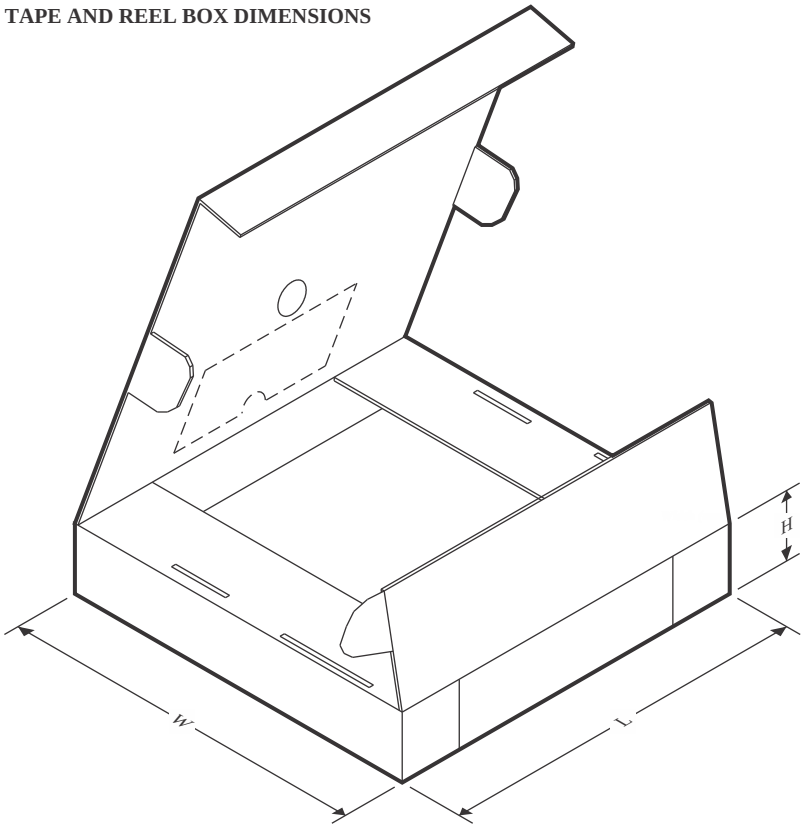
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG3650R025KLAR	TO	KLA	9	2000	330.0	24.4	10.2	11.98	2.6	12.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG3650R025KLAR	TO	KLA	9	2000	356.0	356.0	45.0

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