LMK5C33414AS1 3-DPLL 3-APLL 4-IN 14-OUT Network Synchronizer With IEEE-1588 PTP Stack Software

1 Features

- Ultra-low jitter BAW VCO based Wireless clocks
  - 40fs typical/ 57fs maximum RMS jitter at 491.52MHz
  - 50fs typical/ 62fs maximum RMS jitter at 245.76MHz
- Three high-performance Digital Phase Locked Loops (DPLLs) with paired Analog Phase Locked Loops (APLLs)
  - Programmable DPLL loop bandwidth from 1mHz to 4kHz
  - < 1ppt DCO frequency adjustment step size
- Four differential or single-ended DPLL inputs
  - 1Hz (1PPS) to 800MHz input frequency
  - Digital holdover and hitless switching
- 14 differential outputs with programmable HSDS, AC-LVPECL, LVDS, and HSCL formats
  - Up to 18 total frequency outputs when configured with 6 LVCMOS frequency outputs on OUT[1:0]_P/N, GPIO1, and GPIO2 and 12 differential outputs on OUT[13:2]_P/N
  - 1Hz (1PPS) to 1250MHz output frequency with programmable swing and common mode
  - PCIe Gen 1 to 6 compliant
- I^2C, 3-wire SPI, or 4-wire SPI
- –40°C to 85°C operating temperature

2 Applications

- 4G and 5G Wireless Networks
  - Active Antenna System (AAS), mMIMO
  - Macro Remote Radio Unit (RRU)
  - CPRI/eCPRI Baseband, Centralized, Distributed Units (BBU, CU, DU)
  - Small cell base station
- SyncE (G.8262), SONET/SDH (Stratum 3/3E, G.813, GR-1244, GR-253), IEEE-1588 PTP secondary clock
- Jitter cleaning, wander attenuation, and reference clock generation for 112G/224G PAM4 SerDes
- Optical Transport Networks (OTN G.709)
- Broadband fixed line access
- Industrial
  - Test and measurement

3 Description

The LMK5C33414AS1 is a high-performance network synchronizer and jitter cleaner designed to meet the stringent requirements of wireless communications and infrastructure applications.

The device is bundled with software support for IEEE-1588 PTP synchronization to a primary reference clock source. For more information, contact TI.

The device integrates three DPLLs and three APLLs to provide hitless switching and jitter attenuation with programmable loop bandwidth (LBW) and one external loop filter capacitor, maximizing flexibility and ease of use.

APLL3 features an ultra-high performance PLL with TI's proprietary Bulk Acoustic Wave (BAW) technology. The BAW APLL can generate 491.52MHz output clocks with 40fs typical / 60fs maximum RMS jitter (12kHz to 20MHz) irrespective of the DPLL reference input frequency and jitter characteristics. APLL2 and APLL1 (conventional LC VCOs) provide options for a second or third frequency and/or synchronization domain.

Reference validation circuitry monitors the DPLL reference inputs and automatically performs a hitless switch when the inputs are detected or lost. Zero-Delay Mode (ZDM) provides control over the phase relationship between inputs and outputs.

The device is fully programmable through I^2C or SPI. The integrated EEPROM can be used to customize system start-up clocks. The device also features factory default ROM profiles as fallback options.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
LMK5C33414AS1	RGC (VQFN, 64)	9.00mm × 9.00mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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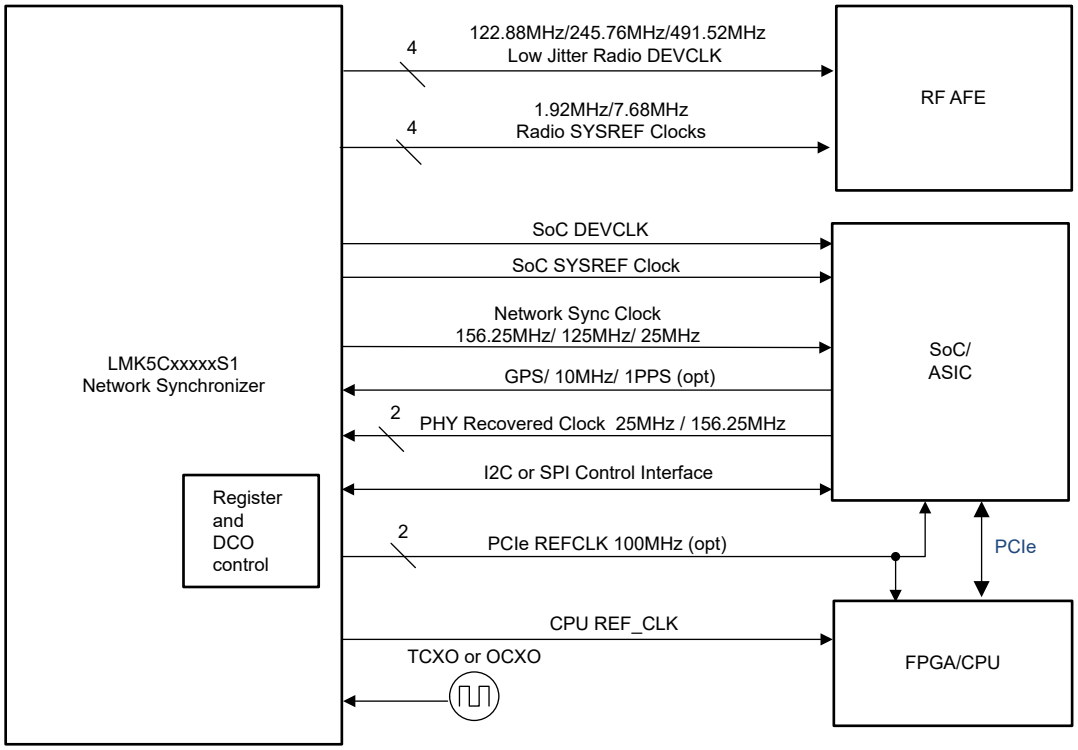

LMK5C33414AS1 Typical System Block Diagram

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4 Device Comparison

Table 4-1. Device Comparison Table

NEW PART NUMBER	IN	OUT	DPLL	APLL	VCBO FREQUENCY [MHz]	INCLUDED IEEE 1588 PTP STACK SOFTWARE
LMK5C33216A	2	16	3	3	2457.6	No
LMK5C33216AS1	2	16	3	3	2457.6	Yes
LMK5C33414A	4	14	3	3	2457.6	No
LMK5C33414AS1	4	14	3	3	2457.6	Yes
LMK5C22212A	2	12	2	2	2457.6	No
LMK5C22212AS1	2	12	2	2	2457.6	Yes
LMK5C23208A	2	8	2	3	2457.6	No
LMK5B33216	2	16	3	3	2500	No
LMK5B33414	4	14	3	3	2500	No
LMK5B12212	2	12	1	2	2500	No

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5 Pin Configuration and Functions

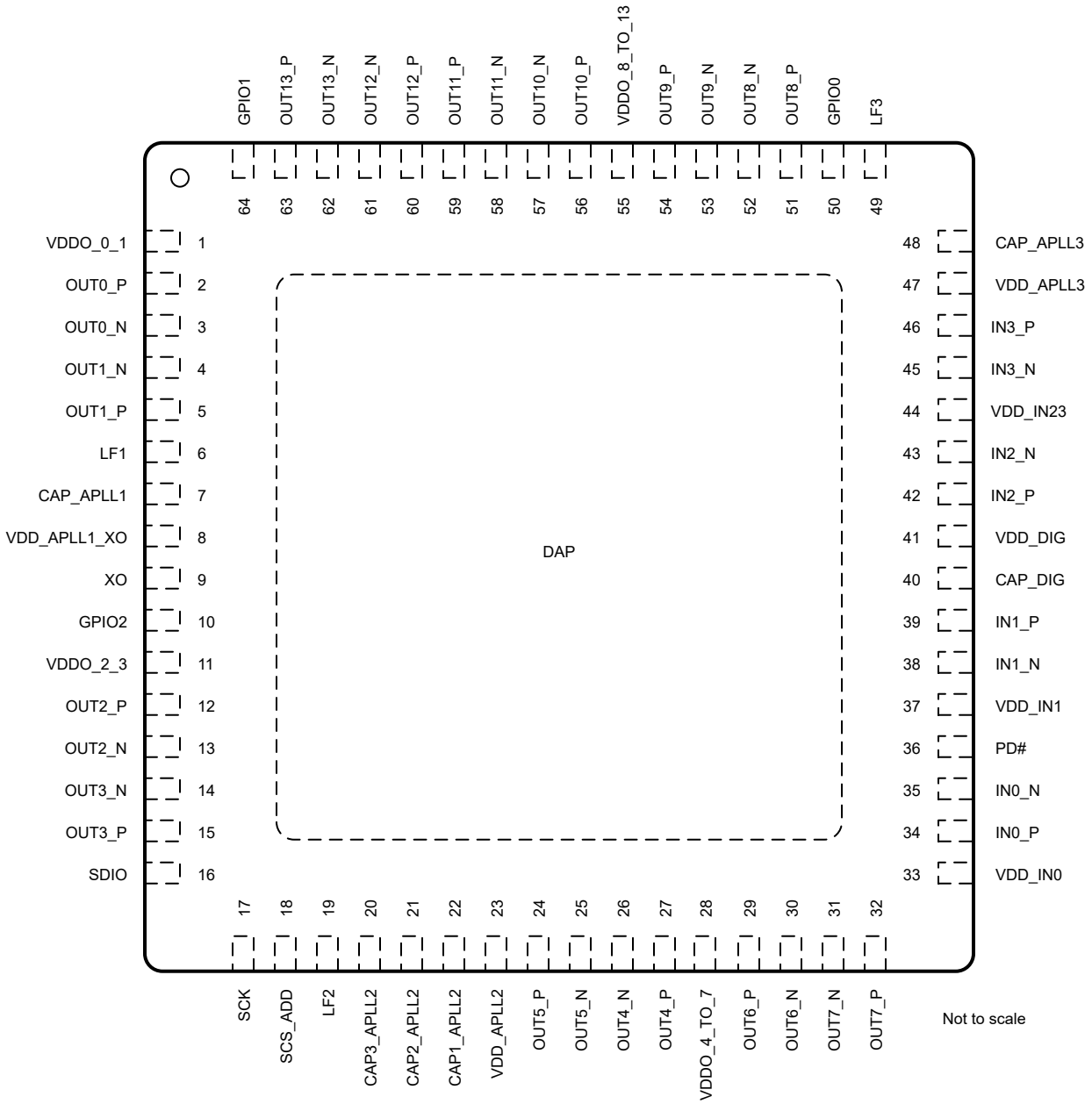

Figure 5-1. LMK5C33414AS1 RGC Package 64-Pin VQFN Top View

Table 5-1. LMK5C33414AS1 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
POWER			
VDDO_0_1	1	P	Power supply for OUT0 and OUT1. Connect to supply; do not leave floating or connect to GND.
VDD_APLL1_XO	8	P	Power supply for XO and APLL1. Connect to supply; do not leave floating or connect to GND.
VDDO_2_3	11	P	Power supply for OUT2 and OUT3. Connect to supply; do not leave floating or connect to GND.
VDD_APLL2	23	P	Power supply for APLL2

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Table 5-1. LMK5C33414AS1 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VDDO_4_TO_7	28	P	Power supply for OUT4 to OUT7
VDD_IN0	33	P	Power supply for IN0 DPLL reference input
VDD_IN1	37	P	Power supply for IN1 DPLL reference input
VDD_DIG	41	P	Power supply for digital. Connect to supply; do not leave floating or connect to GND.
VDD_IN23	44	P	Power supply for IN2 and IN3 DPLL reference inputs
VDD_APLL3	47	P	Power supply for APLL3 (BAW APLL). Connect to supply; do not leave floating or connect to GND.
VDDO_8_TO_13	55	P	Power supply for OUT8 to OUT13
DAP	N/A	G	Ground
CORE BLOCKS [2]			
LF1	6	A	External loop filter cap for APLL1. Recommended capacitor value is 100nF. Refer to APLL Loop Filters (LF1, LF2, LF3) for more details.
CAP_APLL1	7	A	LDO bypass capacitor for APLL1 VCO. Recommended capacitor value is 10µF.
LF2	19	A	External loop filter cap for APLL2. Recommended capacitor value is 100nF. Refer to APLL Loop Filters (LF1, LF2, LF3) for more details.
CAP3_APLL2	20	A	Internal bias bypass capacitor for APLL2 VCO. Recommended capacitor value is 10µF
CAP2_APLL2	21	A	Internal bias bypass capacitor for APLL2 VCO. Recommended capacitor value is 10µF.
CAP1_APLL2	22	A	LDO bypass capacitor for APLL2 VCO. Recommended capacitor value is 10µF.
CAP_DIG	40	A	LDO bypass capacitor for Digital Core Logic. Recommended capacitor value is 10µF.
CAP_APLL3	48	A	Internal bias bypass capacitor for the BAW APLL. Recommended capacitor value is 10µF.
LF3	49	A	External loop filter cap for the BAW APLL. Recommended capacitor value is 470nF. Refer to APLL Loop Filters (LF1, LF2, LF3) for more details.
INPUT BLOCKS			
XO	9	I	XO/TCXO/OCXO input pin, refer to Oscillator Input (XO) for configuring the internal XO input termination.
IN0_P	34	I	First reference input to DPLLx or buffered to OUT0 or OUT1. Refer to Reference Inputs for configuring the internal reference input termination.
IN0_N	35	I	
IN1_N	38	I	Second reference input to DPLLx or buffered to OUT0 or OUT1. Refer to Reference Inputs for configuring the internal reference input termination.
IN1_P	39	I	
IN2_P	42	I	Third reference input to DPLLx or buffered to OUT0 or OUT1. Refer to Reference Inputs for configuring the internal reference input termination.
IN2_N	43	I	
IN3_N	45	I	Fourth reference input to DPLLx or buffered to OUT0 or OUT1. Refer to Reference Inputs for configuring the internal reference input termination.
IN3_P	46	I	
OUTPUT BLOCKS			
OUT0_P	2	O	Clock Output 0. Sources from DPLL reference inputs, XO, the BAW APLL, APLL2, or APLL1. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, HCSL, 1.8V LVCMOS, or 2.65V LVCMOS. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT0_N	3	O	
OUT1_N	4	O	Clock Output 1. Sources from DPLL reference inputs, XO, the BAW APLL, APLL2, or APLL1. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, HCSL, 1.8V LVCMOS, or 2.65V LVCMOS. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT1_P	5	O	
OUT2_P	12	O	Clock Output 2. Sources from the BAW APLL and APLL2. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT2_N	13	O	

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Table 5-1. LMK5C33414AS1 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
OUT3_N	14	O	Clock Output 3. Sources from the BAW APLL and APLL2. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT3_P	15	O	
OUT5_P	24	O	Clock Output 5. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT5_N	25	O	
OUT4_N	26	O	Clock Output 4. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT4_P	27	O	
OUT6_P	29	O	Clock Output 6. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT6_N	30	O	
OUT7_N	31	O	Clock Output 7. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT7_P	32	O	
OUT8_P	51	O	Clock Output 8. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT8_N	52	O	
OUT9_N	53	O	Clock Output 9. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT9_P	54	O	
OUT10_P	56	O	Clock Output 10. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT10_N	57	O	
OUT11_N	58	O	Clock Output 11. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT11_P	59	O	
OUT12_P	60	O	Clock Output 12. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT12_N	61	O	
OUT13_N	62	O	Clock Output 13. Sources from the BAW APLL or APLL2. Supports SYSREF/1-PPS output. Programmable formats: AC-LVPECL, LVDS, HSDS, or HCSL. Refer to Clock Outputs for details on configuring and terminating the outputs.
OUT13_P	63	O	
LOGIC CONTROL/STATUS			
GPIO2[3]	10	I/O, S	POR: See ROM Detailed Description Normal Operation: GPIO input or output
SDIO[4]	16	I/O	SPI or I^2C Data (SDA)
SCK[4]	17	I	SPI or I^2C Clock (SCL)
SCS_ADD[3]	18	I, S	POR: I^2C address select (see GPIO1 and SCS_ADD Functionalities and I^2C Serial Interface) Normal Operation: SPI Chip Select (2-state)
PD#	36	I	Device power down (active low), internal 200kΩ pullup to V_{CC}
GPIO0[3]	50	I/O, S	POR: See ROM Detailed Description Normal Operation: GPIO input or output
GPIO1[3]	64	I/O, S	POR: See GPIO1 and SCS_ADD Functionalities Normal Operation: GPIO input or output

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input or Output, A = Analog, S = Configuration.
(2) Do not apply external stimulus to core pins. These performance critical pins are not designed to meet normal latch up testing compliance levels. For best filtering performance, capacitors must be placed close to the IC.
(3) When 3-level mode is enabled during power supply ramp or when PD# is LOW: internal voltage divider of 555kΩ to V_{CC} and 201kΩ to GND. When 2-level input mode is enabled: internal 408kΩ pulldown to GND.
(4) 670kΩ pullup to internal 2.6V LDO.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD(2)	Core supply voltages	–0.3	3.6	V
VDDO(3)	Output supply voltages	–0.3	3.6	V
V_{IN}	Input voltage range for clock and logic inputs	–0.3	VDD+0.3	V
V_{OUT_LOGIC}	Output voltage range for logic outputs	–0.3	VDD+0.3	V
V_{OUT}	Output voltage range for clock outputs	–0.3	VDDO+0.3	V
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) VDD refers to all core supply pins or voltages. All VDD core supplies must be powered-on before the PD# is pulled high to trigger the internal power-on reset (POR).
(3) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD(1)	Core supply voltages	3.135	3.3	3.465	V
VDDO_x(2)	Output supply voltages(3)	3.135	3.3	3.465	V
VDD_{OD}	Output voltage range for open drain outputs	1.71		3.465	V
T_A	Operating ambient temperature range	-40		85	°C
T_J	Junction temperature			135	°C
$T_{CONT-LOCK}$	Continuous lock over temperature - no VCO recalibration needed			125	°C
t_{VDD}	Power supply ramp time(4)	0.01		100	ms

(1) VDD refers to all core supply pins or voltages. All VDD core supplies must be powered-on before internal power-on reset (POR).
(2) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.
(3) CMOS output voltage levels are determined by internal programming of the CMOS output LDO to support either 1.8V or 2.65V.
(4) Time for VDD to ramp monotonically above 2.7V for proper internal power-on reset. For slower or non-monotonic VDD ramp, hold PD# low until after VDD voltages are valid.

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6.4 Thermal Information

THERMAL METRIC[1] [2] [3]		LMK5C33414AS1 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the application note, *Semiconductor and IC Package Thermal Metrics*.
(2) The thermal information is based on a 10-layer 200mm x 250mm board with 49 thermal vias (7mm x 7mm pattern, 0.3mm holes).
(3) Ψ_{JB} can allow the system designer to measure the board temperature (T_{PCB}) with a fine-gauge thermocouple and back-calculate the device junction temperature, $T_J = T_{PCB} + (\Psi_{JB} \times \text{Power})$. Measurement of Ψ_{JB} is defined by JESD51-6.

6.5 Electrical Characteristics

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Consumption Characteristics						
I_{DD_TOT}	Total current consumption with specified configuration	245.76MHz from OUT0 to OUT13, LVDS/HSDS 400mV, BAW APLL post-divider = 5, channel divider = 2. DPLL1, DPLL2, APLL1, APLL2 disabled.		850	940	mA
		245.76MHz from OUT0 to OUT13, HSDS 800mV, BAW APLL post-divider = 5, channel divider = 2. DPLL1, DPLL2, APLL1, APLL2 disabled.		965	1075	mA
		100MHz from OUT0 to OUT3 (APLL1), 312.5MHz from OUT4 to OUT7 (APLL2), 491.52MHz from OUT8 to OUT13 (BAW APLL), HSDS 800mV. DPLL1, DPLL2, and DPLL3 disabled.		1085	1195	mA
$I_{DD\text{-}XO}$	XO input current consumption	XO		3.5		mA
$I_{DD\text{-}XO2X}$	Current consumption per XO doubler	XO doubler[1]		0.3		mA
$I_{DD\text{-}INX}$	Core current consumption per DPLL reference input block	IN0		3.6		mA
		IN1		3.1		mA
		IN2 and IN3		5		mA
$I_{DD\text{-}DPLL}$	Current consumption per DPLL	DPLL[2]		55		mA
$I_{DD\text{-}APLL1}$	APLL1 current consumption	APLL1		90		mA
$I_{DD\text{-}APLL2}$	APLL2 current consumption	APLL2		160		mA
$I_{DD\text{-}APLL3}$	BAW APLL current consumption	APLL3, BAW APLL		120		mA
$I_{DD\text{-}ANA}$	Analog bias current consumption	Analog circuitry from VDD_APLL1_XO supply pin. Always on when device is enabled.		42		mA
$I_{DD\text{-}DIG}$	Digital control current consumption	Digital control circuitry from VDD_DIG supply pin always on when device is enabled.		34		mA
$I_{DDO\text{-}CHDIV}$	Current consumption per channel divider block	12-bit channel divider		20		mA
$I_{DDO\text{-}1PPSDIV}$	Current consumption per 1PPS/ SYSREF divider block	20-bit 1PPS/SYSREF divider		12		mA

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Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DDO-DELAY}$	Current consumption per 1PPS/ SYSREF analog delay block	Analog delay function enabled		10		mA
$I_{DDO-HSDS}$	HSDS current consumption per output driver	HSDS buffer (VCM level = s1, I_{out} = 4mA, 100Ω termination)		19		mA
		HSDS buffer (VCM level = s1, I_{out} = 7mA, 100Ω termination)		22		mA
		HSDS buffer (VCM level = s1, I_{out} = 10mA, 100Ω termination)		25		mA
$I_{DDO-HCSL}$	HCSL current consumption per output driver	HCSL output (50Ω termination per side)		30.5		mA
I_{DD_PD}	Power-down current consumption	Device powered-down, PD# = LOW		90	110	mA
Reference Input Characteristics (INx)						
f_{IN}	INx frequency range	Single-ended input	0.5E–6		200	MHz
		Differential input	5		800	
V_{IH}	Single-ended input high voltage	DC-coupled input mode (3)	1.2		VDD + 0.3	V
V_{IL}	Single-ended input low voltage				0.5	V
$V_{IN-SE-PP}$	Single-ended input voltage swing	AC-coupled input mode (4)	0.4		2	V_{pp}
$V_{IN-DIFF-PP}$	Differential input voltage swing	AC- or DC- coupled input (5)	0.4		2	V_{pp}
V_{ICM}	Input Common Mode	DC- coupled differential input (6)	0.1		2	V
dV/dt	Input slew rate	Single-ended input	0.2	0.5		V/ns
		Differential input	0.2	0.5		V/ns
IDC	Input Clock Duty Cycle	Non 1PPS signal	40		60	%
$t_{PULSE-1PPS}$	1PPS pulse width for input	1PPS or pulsed signal	100			ns
I_{IN-DC}	DC input leakage current	Single pin INx_P or INx_N, 50Ω and 100Ω internal terminations disabled, AC coupled mode enabled or disabled	–350		350	µA
C_{IN}	Input capacitance	Single-ended, each pin		2		pF
XO/TCXO Input Characteristics (XO)						
f_{CLK}	XO input frequency range (7)		10		156.25	MHz
V_{IH}	LVCMOS Input high voltage	DC-coupled input mode (8)	1.4		VDD + 0.3	V
V_{IL}	LVCMOS Input low voltage				0.8	V
V_{IN-SE}	Single-ended input voltage swing	AC-coupled input mode (9)	0.4		VDD + 0.3	V_{pp}
dV/dt	Input slew rate		0.2	0.5		V/ns
IDC	Input duty cycle		40		60	%
I_{IN-DC}	DC Input leakage current	Single pin XO_P, 50Ω and 100Ω internal terminations disabled	–350		350	µA
C_{IN}	Input capacitance on each pin			1		pF
C_{EXT}	External AC coupling capacitor			10		nF
APLL/VCO Characteristics						
f_{PFD}	PFD frequency range	BAW APLL Fractional feedback divider			110	MHz
		APLL1, APLL2 Fractional feedback divider			125	MHz
f_{VCO1}	VCO1 Frequency range	APLL1	4800		5350	MHz
f_{VCO2}	VCO2 Frequency range	APLL2	5595		5950	MHz
f_{VCBO}	VCBO Frequency range	APLL3, BAW APLL	2457.35	2457.6	2457.85	MHz
$t_{APLL1-LOCK}$	APLL1 lock time	Time between soft or hard reset and stable APLL1 output.		20	35	ms
$t_{APLL2-LOCK}$	APLL2 lock time	Time between soft or hard reset and stable APLL2 output.		350	460	ms

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Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BAW\ APLL-LOCK}$	BAW APLL lock time	Time between soft or hard reset and stable BAW APLL output.		12.5	13	ms
HSDS Output Characteristics (OUTx)						
f_{OUT}	Output frequency range		1E–6		1250	MHz
$V_{OUT-DIFF}$	Differential output swing			$2\times V_{OD-HSDS}$		mVpp
$V_{OD-HSDS}$	HSDS output voltage swing	f_{out} < 100MHz, I_{out} = 4mA	350	400	440	mV
		f_{out} < 100MHz, I_{out} = 7mA	625	700	750	mV
		f_{out} < 100MHz, I_{out} = 10mA	900	975	1050	mV
		100MHz ≤ f_{out} ≤ 325MHz, I_{out} = 4mA	335	400	445	mV
		100MHz ≤ f_{out} ≤ 325MHz, I_{out} = 5mA	425	500	575	mV
		100MHz ≤ f_{out} ≤ 325MHz, I_{out} = 6mA	510	600	690	mV
		100MHz ≤ f_{out} ≤ 325MHz, I_{out} = 7mA	595	700	805	mV
		100MHz ≤ f_{out} ≤ 325MHz, I_{out} = 8mA	680	800	920	mV
		100MHz ≤ f_{out} ≤ 325MHz, I_{out} = 9mA	765	900	1035	mV
		100MHz ≤ f_{out} ≤ 325MHz, I_{out} = 10mA	850	1000	1150	mV
		325MHz < f_{out} ≤ 800MHz, I_{out} = 4mA	300	350	400	mV
		325MHz < f_{out} ≤ 800MHz, I_{out} = 7mA	580	640	700	mV
		325MHz < f_{out} ≤ 800MHz, I_{out} = 10mA	800	865	940	mV
		800MHz < f_{out} ≤ 1250MHz, I_{out} = 4mA	235	320	400	mV
		800MHz < f_{out} ≤ 1250MHz, I_{out} = 7mA	480	625	740	mV
		800MHz < f_{out} ≤ 1250MHz, I_{out} = 10mA	600	800	1000	mV
V_{OH}	Output voltage high			V_{OL} + V_{OD}		mVpp
V_{OL}	Output voltage low	VCM level = s1	50	150	250	mV
		VCM level = s2+3	300	470	720	mV
V_{CM}	Output common mode voltage	VCM level = s1 or s2+3		V_{OL} + V_{OD}/2		V
		VCM level = s2, I_{out} = 4mA	0.6	0.7	0.8	V
		VCM level = s3, I_{out} = 4mA	1.125	1.25	1.375	V
t_{SKEW}	Output skew (12)	Same APLL, same post divider and channel divider values, same bank			50	ps
		Same APLL, same post divider and channel divider values, between banks			80	ps
t_R/t_F	Rise/Fall time	f_{OUT} < 100MHz, 20% to 80%, OUT_x_CAP_EN = 0, C_L = 2pF	200	250	350	ps
		100MHz ≤ f_{OUT} ≤ 325MHz, 20% to 80%, I_{out} ≥ 8mA, OUT_x_CAP_EN = 0, C_L = 2pF	165	225	260	ps
		100MHz ≤ f_{OUT} ≤ 325MHz, 20% to 80%, OUT_x_CAP_EN = 0, C_L = 2pF	175	230	300	ps
		325MHz < f_{OUT} ≤ 800MHz, 20% to 80%, OUT_x_CAP_EN = 0, C_L = 2pF	150	215	285	ps
		800MHz < f_{OUT} ≤ 1250MHz, 20% to 80%, OUT_x_CAP_EN = 0, C_L = 2pF	120	205	250	ps
ODC	Output duty cycle		48		52	%
HCSL Output Characteristics (OUTx)						
f_{OUT}	Output frequency range	HSCL output mode	25	100	650	MHz
V_{OL}	Output voltage low		–150	0	150	mV
V_{OH}	Output voltage high		600	750	900	mV

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VMIN	Output voltage minimum	Including undershoot	–300	0	150	mV
VMAX	Output voltage maximum	Including overshoot	600	750	1150	mV
dV/dt	Differential output slew rate	±150mV around center point, OUT_x_CAP_EN = 1, C_L= 2pF	2		4	V/ns
dV/dt	Differential output slew rate	±150mV around center point,OUT_x_CAP_EN = 0, C_L= 2pF	3		5	V/ns
t_{SKEW}	Output skew (12)	Same APLL, same post divider and channel divider values, same bank			50	ps
		Same APLL, same post divider and channel divider values, between banks			80	ps
V_{CROSS}	Absolute voltage crossing point	f_{OUT} = 100MHz	300		500	mV
ΔV_{CROSS}	Voltage crossing point variation	f_{OUT} = 100MHz			75	mV
ODC	Output duty cycle		45		55	%
1.8V LVCMOS Output Characteristics (OUT0, OUT1)						
f_{OUT}	Output frequency range		1E–6		200	MHz
V_{OH}	Output high voltage	I_{OH} = -2mA	1.5			V
V_{OL}	Output low voltage	I_{OL} = 2mA			0.2	V
t_R/t_F	Output rise/fall time	20% to 80%		150		ps
t_{SK}	Output-to-output skew	OUT0_P, OUT0_N, OUT1_P, OUT1_N with same polarity, same APLL post divider and output divider values. Same polarity and output type (LVCMOS)			60	ps
		Same APLL, same post divider and output divider values. Skew between LVCMOS and differential outputs	0.7	1	1.3	ns
ODC	Output duty cycle		45		55	%
R_{OUT}	Output impedance		54	64	75	Ω
2.65V LVCMOS Output Characteristics (OUT0, OUT1)						
f_{OUT}	Output frequency range		1E–6		200	MHz
V_{OH}	Output high voltage	I_{OH} = -2mA	2.3			V
V_{OL}	Output low voltage	I_{OL} = 2mA			0.2	V
t_R/t_F	Output rise/fall time	20% to 80%		150		ps
t_{SK}	Output-to-output skew	OUT_P, OUT0_N, OUT1_P, OUT1_N with same polarity, same APLL post divider and output divider values. Same polarity and output type (LVCMOS)			60	ps
		Same APLL, same post divider and output divider values. Skew between LVCMOS and differential outputs	0.7	1.0	1.3	ns
PN_{FLOOR}	Output phase noise floor (f_{OFFSET} > 10MHz)	25MHz		–155		dBc/Hz
ODC	Output duty cycle		45		55	%
R_{OUT}	Output impedance		40	50	65	Ω
3.3V LVCMOS GPIO Clock Output Characteristics (GPIO0, GPIO1, GPIO2)						
f_{OUT}	Maximum output frequency	GPIO1, GPIO2			25	MHz
V_{OH}	Output high voltage	I_{OH}= 2mA	2.4			V
V_{OL}	Output low voltage	I_{OL}= 2mA			0.4	V
I_{IH}	Input high current	V_{IN} = V_{DD}			100	µA
I_{IL}	Output low current	V_{IN} = 0V	-100			µA
t_R/t_F	Output rise/fall time	20% to 80%, 1kΩ to GND	0.5	1.3	2.6	ns

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SK}	Output-to-output skew	GPIO1, GPIO2 output skew compared to OUT0_P, OUT0_N, OUT1_P, OUT1_N CMOS outputs. GPIOx_SEL = 115 fout = 100kHz		7.5	11	ns
ODC	Output duty cycle		45		55	%
R_{OUT}	Output impedance		35	42	50	Ω
PLL Output Clock Noise Characteristics						
$RJ_{BAW\ APLL}$	12kHz to 20MHz integrated RMS jitter for BAW APLL outputs	XO = 48MHz, fout = 1222.8MHz, post divider $P1_{APLL3}$ = 2, HSDS output VOD ≥ 800mV			45	fs
		XO = 48MHz, fout = 614.4MHz, post divider $P1_{APLL3}$ = 4, HSDS output VOD ≥ 800mV		35	50	fs
		XO = 48MHz, fout = 491.52MHz, post divider $P1_{APLL3}$ = 5, HSDS output VOD ≥ 800mV		40	57	fs
		XO = 48MHz, fout = 245.76MHz, post divider $P1_{APLL3}$ = 10, HSDS output VOD ≥ 800mV		45	64	fs
		XO = 48MHz, fout = 245.76MHz, bypass post divider $P1_{APLL3}$ = 1, HSDS output VOD ≥ 800mV (10)		50	62	fs
		XO = 48MHz, fout = 122.88MHz, bypass post divider $P1_{APLL3}$ = 1, HSDS output VOD ≥ 800mV (10)		55	86	fs
		XO = 48MHz, f_{out} = 245.76MHz, HSDS output, all VOD levels		50	80	fs
		XO = 48MHz, f_{out} = 122.88MHz, HSDS output, all VOD levels		60	90	fs
RJ_{APLL2}	12kHz to 20MHz integrated RMS jitter for APLL2 outputs	XO = 48MHz, f_{out} = 153.6MHz (VCO2 = 5836.8MHz), 155.52MHz (VCO2 = 5598.72MHz), 174.703084MHz (VCO2 = 5765.2 MHz) or 184.32MHz (VCO2 = 5898.24MHz) from APLL2. HSDS output , VOD ≥ 800mV from OUT4, OUT5, OUT6 and OUT7 or OUT2 and OUT3. 156.25MHz from BAW APLL output in all other output banks.		110	150	fs
		XO = 48MHz, f_{out} = 161.1328125MHz or 322.265625MHz (VCO2 = 5800.78125MHz), or 212.5MHz (VCO2 = 5950MHz) from APLL2. HSDS output , VOD ≥ 800mV from OUT4, OUT5, OUT6 and OUT7. 156.25MHz from BAW APLL output in all other output banks.		110	150	fs
		XO = 48MHz, f_{out} = 156.25MHz or 125MHz (VCO2 = 5625MHz), or 100MHz (VCO2 = 5600MHz) from APLL2. HSDS output , VOD ≥ 800mV from OUT4, OUT5, OUT6 and OUT7 or OUT2 and OUT3. 156.25MHz from BAW APLL output in all other output banks.		110	150	fs

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ_{APLL1}	12kHz to 20MHz integrated RMS jitter for APLL1 outputs	XO = 48MHz, fout ≥ 100MHz, HSDS output buffer VOD ≥ 800mV		200	300	fs
$PSNR_{VDDO_0_1}$	Power supply noise rejection VDDO_0_1	Vcc = 3.3V, V_N = 50mVpp, HSDS, LVDS or AC-LVPECL outputs. (11)		-105		dBc
$PSNR_{VDDO_2_3}$	Power supply noise rejection VDDO_2_3	Vcc = 3.3V, V_N = 50mVpp, HSDS, LVDS or AC-LVPECL outputs. (11)		-105		dBc
$PSNR_{VDDO_4_TO_7}$	Power supply noise rejection VDDO_4_TO_7	Vcc = 3.3V, V_N = 50mVpp, HSDS, LVDS or AC-LVPECL outputs. (11)		-110		dBc
$PSNR_{VDDO_8_TO_13}$	Power supply noise rejection VDDO_8_TO_13	Vcc = 3.3V, V_N = 50mVpp, HSDS, LVDS or AC-LVPECL outputs. (11)		-110		dBc
$PSNR_{VDD_APLL1_XO}$	Power supply noise rejection VDD_APLL1_XO	Vcc = 3.3V, V_N = 50mVpp, HSDS, LVDS or AC-LVPECL outputs. (11)		-100		dBc
$PSNR_{VDD_APLL2}$	Power supply noise rejection VDD_APLL2	Vcc = 3.3V, V_N = 50mVpp, HSDS, LVDS or AC-LVPECL outputs. (11)		-105		dBc
$PSNR_{VDD_APLL3}$	Power supply noise rejection VDD_APLL3	Vcc = 3.3V, V_N = 50mVpp, HSDS, LVDS or AC-LVPECL outputs. (11)		-105		dBc
$PSNR_{VDD_DIG}$	Power supply noise rejection VDD_DIG	Vcc = 3.3V, V_N = 50mVpp, HSDS, LVDS or AC-LVPECL outputs. (11)		-120		dBc
PCIe Jitter Characteristics						
$J_{PCIE-Gen1-CC}$	PCIe Gen 1 (2.5 GT/s) Common Clock jitter	APLLx output, 3x noise folding		0.8	5	ps p-p
$J_{PCIE-Gen2-CC}$	PCIe Gen 2 (5.0 GT/s) Common Clock jitter	APLLx output, 3x noise folding		85	250	fs RMS
$J_{PCIe-Gen3-CC}$	PCIe Gen 3 (8 GT/s) Common Clock jitter	APLLx output, 3x noise folding		25	100	fs RMS
$J_{PCIe-Gen4-CC}$	PCIe Gen 4 (16 GT/s) Common Clock jitter	APLLx output, 3x noise folding		25	100	fs RMS
$J_{PCIe-Gen5-CC}$	PCIe Gen 5 (64 GT/s) Common Clock jitter	APLLx output, 3x noise folding		9	50	fs RMS
$J_{PCIe-Gen6-CC}$	PCIe Gen 6 (32 GT/s) Common Clock jitter	APLLx output, 3x noise folding		6	40	fs RMS
DPLL Characteristics						
f_{TDC}	TDC rate range for DPLLx		1E–6		26	MHz
dφ/dt	Phase slew during switchover	Programmable range		695		ns/s
DPLL-BW	DPLL loop bandwidth	Programmable loop bandwidth(16)	1E–3		4000	Hz
J_{PK}	DPLL closed-loop jitter peaking			0.1		dB
J_{TOL}	Jitter tolerance	Compliant with G.8262 Options 1 and 2. Jitter modulation = 10Hz, 25.78152Gbps line rate		6455		UI p-p
DCO Characteristics						
$f_{DCO-DPLL}$	DPLL DCO frequency tuning range	DPLLx	-200		200	ppm
$f_{DCO-APLL}$	DCO frequency tuning range	BAW APLL in holdover or APLL only operation.	-200		200	ppm
		APLL2, APLL1 in holdover or APLL only operation.	-1000		1000	ppm
Zero-Delay Mode (ZDM) Characteristics						
$f_{OUT-ZDM}$	Output frequency range with ZDM enabled	DPLL3: OUT0 or OUT10	1E–6		1250	MHz
		DPLL2: OUT0 or OUT4	1E–6		700	MHz
		DPLL1: OUT0	1E–6		1250	MHz
$t_{DLY-ZDM}$	Input-to-output propagation delay with ZDM enabled	OUT0, $f_{IN} \le f_{TDC_MAX}$, $f_{OUT} \le f_{TDC_MAX}$, DPLLx_PH_OFFSET = 172500		150		ps

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DLY-VAR-ZDM}$	Input-to-output propagation delay variation with ZDM enabled	OUT0, $f_{IN} \le f_{TDC_MAX}$, $f_{OUT} \le f_{TDC_MAX}$, DPLLx_PH_OFFSET = 0			65	±ps
1PPS Reference Characteristics						
t_{DPLL_FL}	DPLL frequency lock time with 1PPS reference	XO = 48MHz, initial error = ±25ppb, -180° ≤ Θ ≤ 180°. DPLL LBW = 10mHz, frequency lock $\Delta f_{out} \le$ ±4.6ppm		5	6	s
t_{DPLL_PL}	DPLL phase lock time with 1PPS reference	XO = 48MHz, initial error = ±25ppb, -180° ≤ Θ ≤ 180°. DPLL LBW = 10mHz, DPLL LBW = 10mHz, phase lock ≤ ±100ns		34	38	s
Hitless Switching Characteristics						
t_{HIT}	Phase transient during switchover	INx = 1Hz, INy = 1Hz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 10mHz.		4		± ps
		INx = 8kHz, INy = 8kHz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 1Hz		19		± ps
		Nx = 25MHz, INy = 25MHz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 1Hz		1.8		± ps
f_{HIT}	Frequency transient during switchover	INx = 1Hz, INy = 1Hz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 10mHz		0.85		± ppb
		INx = 8kHz, INy = 8kHz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 1Hz		0.45		± ppb
		INx = 25MHz, INy = 25MHz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 1Hz		0.63		± ppb
Programmable Output Delay Characteristics						
$t_{ANA-DLY}$	Analog delay step size (13)	BAW APLL = 2457.6MHz, VCO post-divider = 2, 0.5x range scale, 1Hz ≤ OUTx ≤ 122.88MHz, ANA_DELAY_LINEARITY_CODE = 2		13.13		ps
		BAW APLL = 2457.6MHz, VCO post-divider= 1, 2x range scale, 1Hz ≤ OUTx ≤ 122.88MHz, ANA_DELAY_LINEARITY_CODE = 5		26.25		ps
		APLL2 = 5625.0MHz, VCO post-divider = 3, 1x range scale, 1Hz ≤ OUTx ≤ 156.25MHz, ANA_DELAY_LINEARITY_CODE = 3		17.2		ps
		APLL2= 5625.0MHz, VCO post-divider = 4; 1x range scale, 1Hz ≤ OUTx ≤ 156.25MHz, ANA_DELAY_LINEARITY_CODE = 4		22.9		ps

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ANA-DLY-ERR}$	Analog delay step size error	BAW APLL = 2457.6MHz, VCO post-divider = 2, 0.5x range scale, 1Hz ≤ OUTx ≤ 122.88MHz, ANA_DELAY_LINEARITY_CODE = 2	-6.56		6.56	ps
		BAW APLL = 2457.6MHz, VCO post-divider= 1, 2x range scale, 1Hz ≤ OUTx ≤ 122.88MHz, ANA_DELAY_LINEARITY_CODE = 5	-13.13		13.13	ps
		APLL2 = 5625.0MHz, VCO post-divider = 3, 1x range scale, 1Hz ≤ OUTx ≤ 156.25MHz, ANA_DELAY_LINEARITY_CODE = 3	-8.6		8.6	ps
		APLL2 = 5625.0MHz, VCO post-divider = 4; 1x range scale, 1Hz ≤ OUTx ≤ 156.25MHz, ANA_DELAY_LINEARITY_CODE = 4	-11.45		11.45	ps
$t_{ANA-DLY-RANGE}$	Analog delay range			31 × $t_{ANA-DLY}$		ps
$t_{ANA-DLY-ACC}$	Analog delay accuracy	Analog delay absolute accuracy for any setting N = 0 to 31 across analog delay range. Worst case error of actual value relative to expected value N × $t_{ANA-DLY-STEP}$ for ANA_DELAY_LINEARITY_CODE = 3, 4, 5	-25		25	ps
$t_{ANA-DLY-LIN}$	Analog delay linearity (14)	ANA_DELAY_LINEARITY_CODE = 2	333		450	ps
		ANA_DELAY_LINEARITY_CODE = 3	450		600	ps
		ANA_DELAY_LINEARITY_CODE = 4	600		750	ps
		ANA_DELAY_LINEARITY_CODE = 5	750		1050	ps
$t_{DIG-DLY}$	Digital delay step size	VCO post-divider frequency output = 2457.6MHz, half step setting		196.6		ps
		VCO post-divider frequency output = 2457.6MHz, full step setting		786.4		ps
3-Level Logic Input Characteristics (GPIO0, GPIO1, GPIO2, SCS_ADD)						
V_{IH}	Input high voltage		1.4			V
V_{IM}	Input mid voltage		0.6		0.95	V
V_{IM}	Input mid voltage self-bias	Input floating with internal bias and PD# pulled low	0.7		0.9	V
R_{IM-PD}	Internal pulldown resistor for mid level self-bias (15)		145	163	180	kΩ
R_{IM-PU}	Internal pullup for mid level self-bias (15)		470	526	580	kΩ
V_{IL}	Input low voltage				0.4	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF
2-Level Logic Input Characteristics (PD#, SCK, SDIO, SCS_ADD; GPIO0, GPIO1 and GPIO2 after power up)						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.4	V
I_{IH}	Input high current	V_{IH} = VDD, except PD#	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND, except PD#	–40		40	µA
I_{IH}	Input high current	V_{IH} = VDD, PD# with internal 200kΩ pull-up	–57		24	µA

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input low current	V_{IL} = GND, PD# with internal 200kΩ pull-up	–57		24	µA
t_{WIDTH}	Input pulse width for GPIO SYNC, SYSREF request, TEC trigger, DPLL input selection, FDEV trigger and FDEV_dir	Monotonic edges	200			ns
C_{IN}	Input capacitance			2		pF
Logic Output Characteristics (GPIO0, GPIO1, GPIO2, SDIO)						
V_{OH}	Output high voltage	I_{OH} = 1mA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 1mA			0.4	V
t_R/t_F	Output rise/fall time	20% to 80%, LVCMOS mode, 1kΩ to GND		500		ps
Open Drain Output (GPIO0, GPIO1, GPIO2, SDA)						
V_{OL}	Output Low Level	I_{OL} = 3mA			0.3	V
		I_{OL} = 6mA			0.6	V
I_{OH}	Output Leakage Current		-15		15	µA
SPI Timing Requirements (SDIO, SCK, SCS_ADD)						
f_{SCK}	SPI clock rate				20	MHz
	SPI clock rate; during SRAM read and write operations			5	10	MHz
t_1	SCS to SCK setup time (start communication cycle)		10			ns
t_2	SDI to SCK setup time		10			ns
t_3	SDI to SCK hold time		10			ns
t_4	SCK high time		25			ns
t_5	SCK low time		25			ns
t_6	SCK to SDO valid read-back data				20	ns
t_7	SCS pulse width		20			ns
t_8	SCK to SCS setup time (end communication cycle)		10			ns
I^2C Timing Requirements (SDA, SCL)						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.5	V
I_{IH}	Input leakage		–15		15	µA
C_{IN}	Input capacitance			2		pF
V_{OL}	Output low voltage	I_{OL} = 3mA			0.3	V
V_{OL}	Output low voltage	I_{OL} = 6mA			0.6	V
f_{SCL}	I^2C clock rate	Standard			100	kHz
		Fast mode			400	
$t_{SU(START)}$	START condition setup time	SCL high before SDA low	0.6			µs
$t_{H(START)}$	START condition hold time	SCL low after SDA low	0.6			µs
$t_{W(SCLH)}$	SCL pulse width high		0.6			µs
$t_{W(SCLL)}$	SCL pulse width low		1.3			µs
$t_{SU(SDA)}$	SDA setup time		100			ns
$t_{H(SDA)}$	SDA hold time	SDA valid after SCL low	0		0.9	µs
$t_{R(IN)}$	SDA/SCL input rise time				300	ns
$t_{F(IN)}$	SDA/SCL input fall time				300	ns
$t_{F(OUT)}$	SDA output fall time	C_{BUS} ≤ 400pF			300	ns

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU(STOP)}$	STOP condition setup time		0.6			µs
t_{BUS}	Bus free time between STOP and START		1.3			µs
t_{VD-DAT}	Data valid time				0.9	µs
t_{VD-ACK}	Data valid acknowledge time				0.9	µs
EEPROM Characteristics						
n_{EE-CYC}	EEPROM programming cycles				100	cycle
$t_{SRAM-R/W}$	EEPROM SRAM read/write time delay between bytes		0			ms

(1) This is the current consumption of one XO doubler. All XO doublers consume the same current.
(2) This is the current consumption of one DPLL. Each DPLL consumes the same current.
(3) REFx_ITYPE = 8 or 12.
(4) REFx_ITYPE = 1, 3 or 5, non-driven input directly tied to GND, capacitor to GND or 50Ω to GND.
(5) REFx_ITYPE = 1, 3 or 5.
(6) Combination of common mode voltage and DC coupled different input voltage must not exceed Absolute Maximum Ratings.
(7) When XO input frequency is greater than the APLL phase detector maximum supported comparison frequency, the APLL R divider must be set to minimum of divide by 2.
(8) Register XO_ITYPE = 8 or 12.
(9) Register XO_ITYPE = 1, 3 or 5
(10) The BAW APLL post divider is bypassed by setting $P1_{BAW\ APLL}$ = 1. All OUTx are sourced from channel dividers.
(11) PSNR is the single-sideband spur level measured in dBc when sinusoidal noise with amplitude V_N and frequency between 100kHz and 10MHz is injected onto VDD and VDDO pins with 1.0µF decoupling capacitance.
(12) Output dividers are synchronized. SYNC status achieved from power up or SYNC_SW.
(13) Typical analog delay step size based on APLL post-divider output period divided by 31, times the analog delay range scale value 0.5, 1 or 2.
(14) Analog delay linearity typically selected based on the period of the analog delay range, $t_{ANA-DLY-RANGE}$.
(15) Variation of internal pullup resistor tracks variation of pulldown resistor to maintain a consistent mid voltage self-bias ratio.
(16) DPLL loop bandwidth must be less than 1/100 of TDC frequency and less than 1/10 of APLL loop bandwidth.

6.6 Timing Diagrams

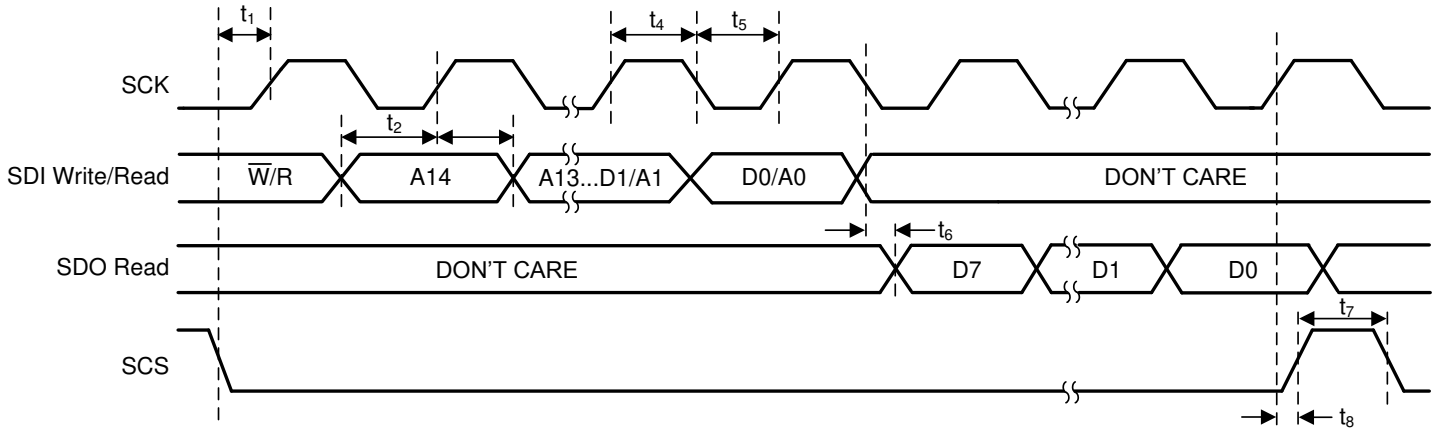

Figure 6-1. SPI Write Timing Diagram

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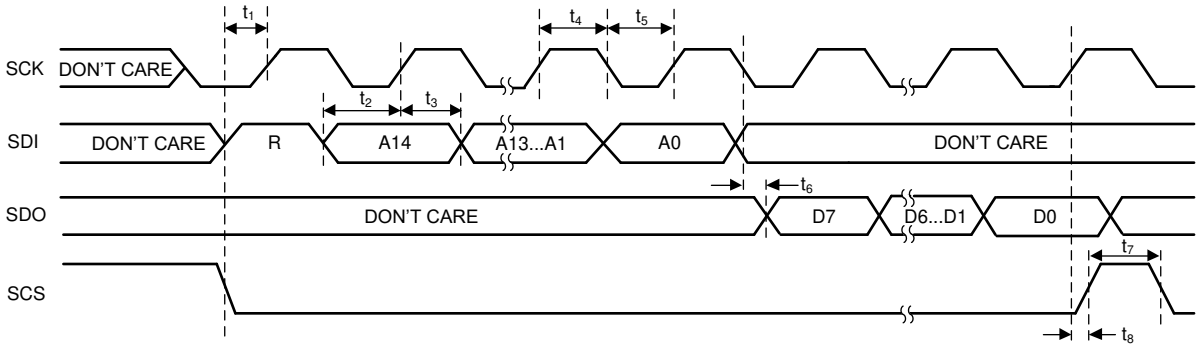

Figure 6-2. SPI 4-Wire Read Timing Diagram

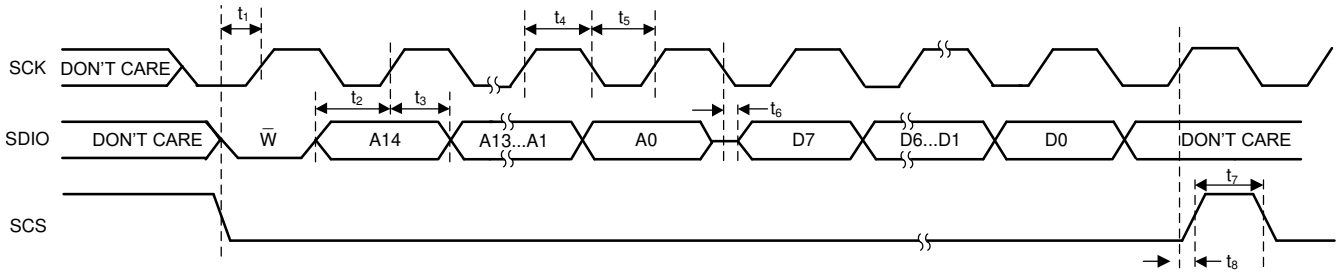

Figure 6-3. SPI 3-Wire Read Timing Diagram

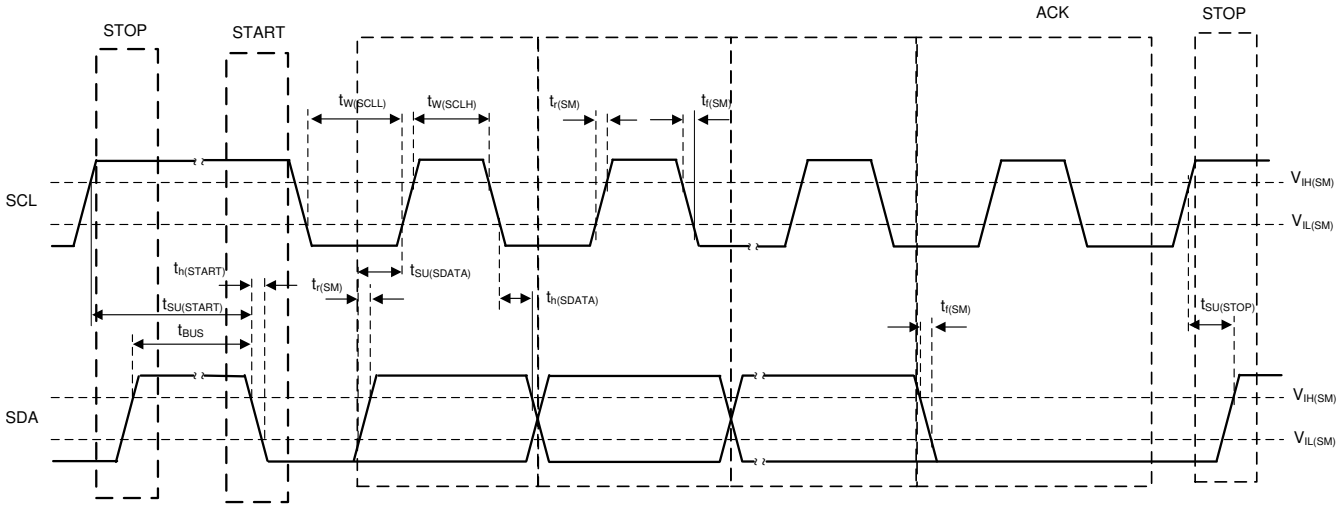

Figure 6-4. I²C Timing Diagram

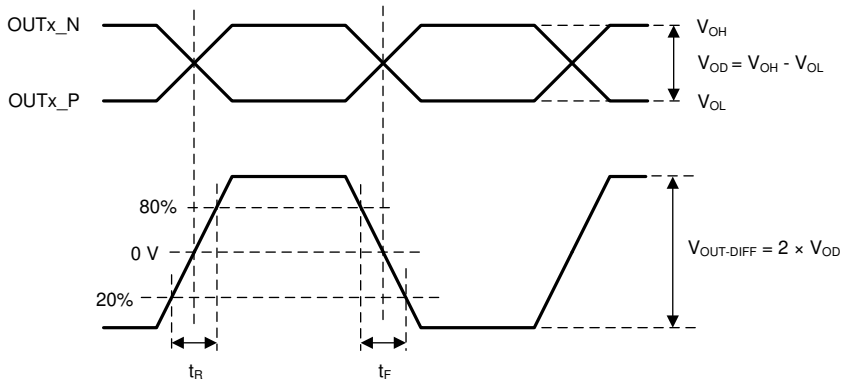

Figure 6-5. Differential Output Voltage and Rise/Fall Time

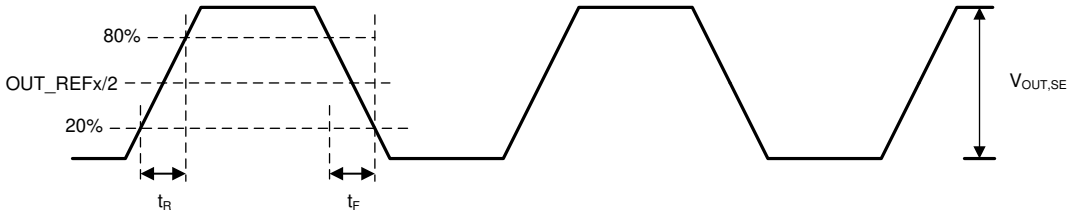

Figure 6-6. Single-Ended Output Voltage and Rise/Fall Time

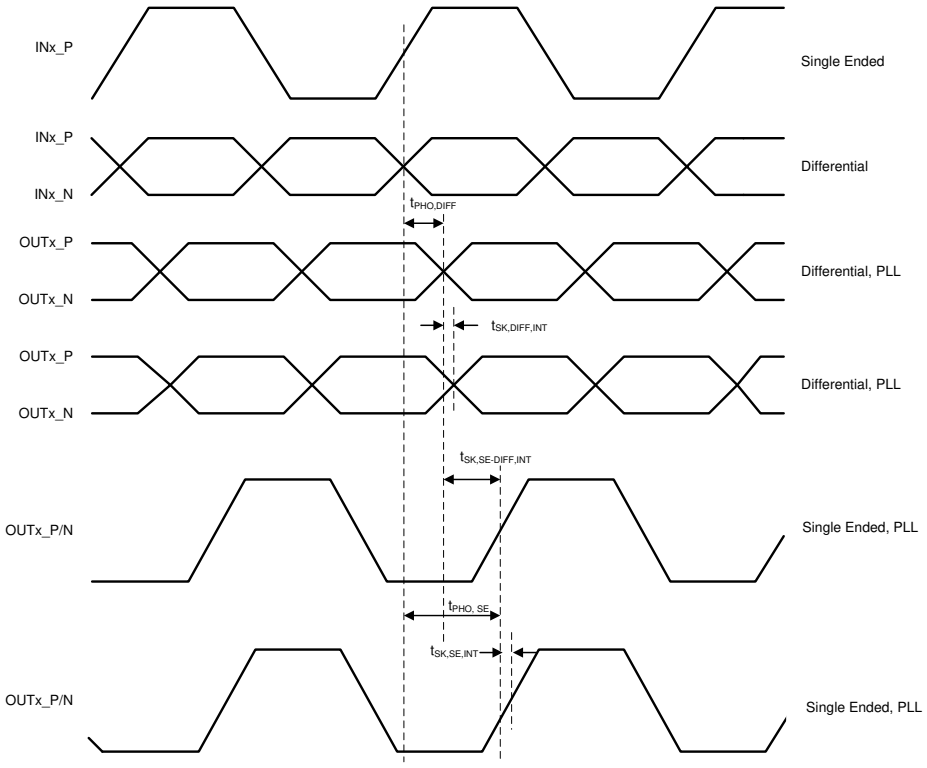

Figure 6-7. Differential and Single-Ended Output Skew and Phase Offset

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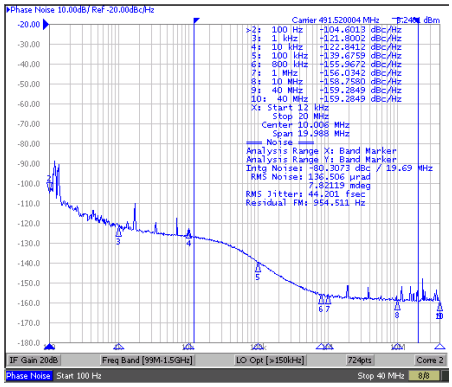
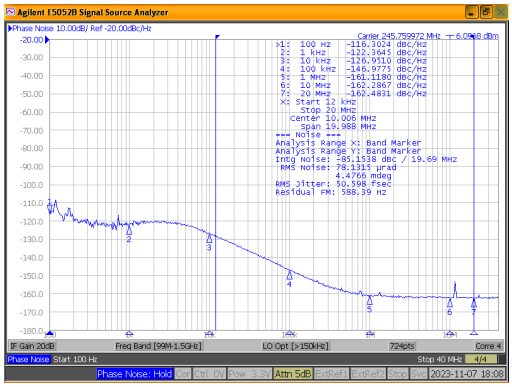
6.7 Typical Characteristics



Jitter = 44fs RMS (12kHz to 20MHz)

$f_{BAW\ APLL}$ = 2457.6MHz

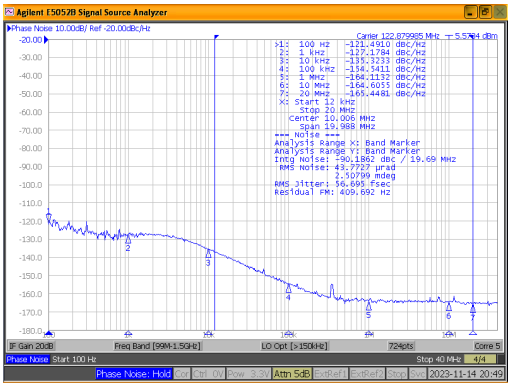
Figure 6-8. 491.52MHz HSDS Output From BAW APLL



Jitter = 51fs RMS (12kHz to 20MHz)

$f_{BAW\ APLL}$ = 2457.6MHz

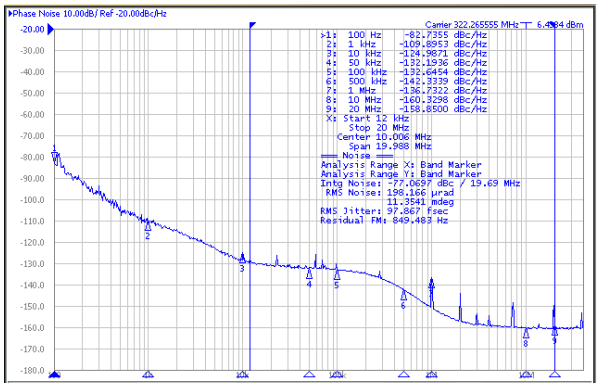
Figure 6-9. 245.76MHz HSDS Output From BAW APLL



Jitter = 57fs RMS (12kHz to 20MHz)

$f_{BAW\ APLL}$ = 2457.6MHz

Figure 6-10. 122.88MHz HSDS Output From BAW APLL



Jitter = 98fs RMS (12kHz to 20MHz)

f_{APLL2} = 5800.78125MHz

Figure 6-11. 322.265625MHz HSDS Output From APLL2

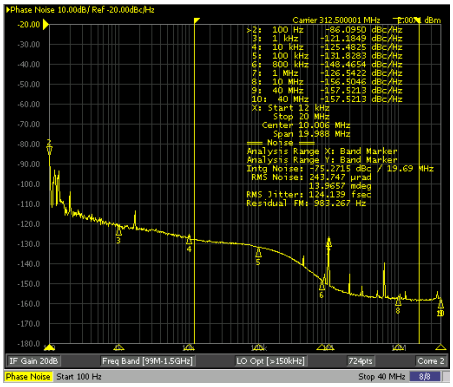
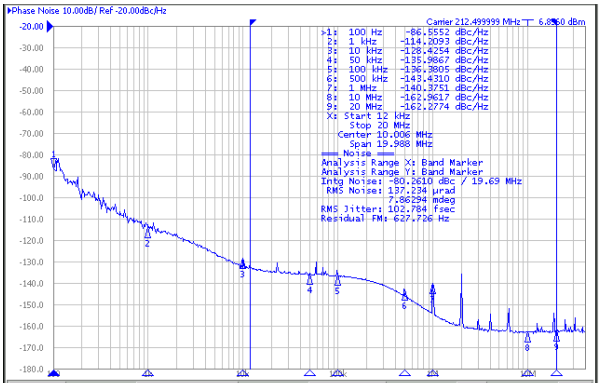


Figure 6-12. 312.5MHz HSDS Output From APLL2



Jitter = 103fs RMS (12kHz to 20MHz)

f_{APLL2} = 5950MHz

Figure 6-13. 212.5MHz HSDS Output From APLL2

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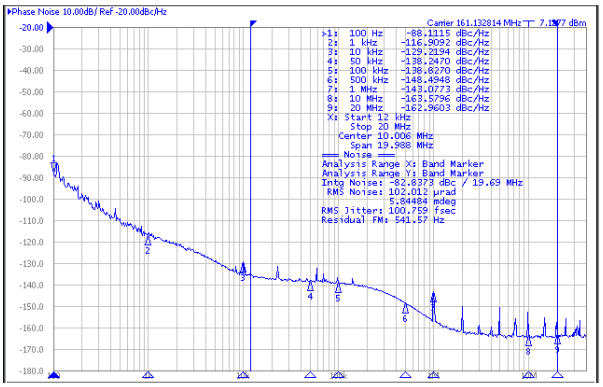
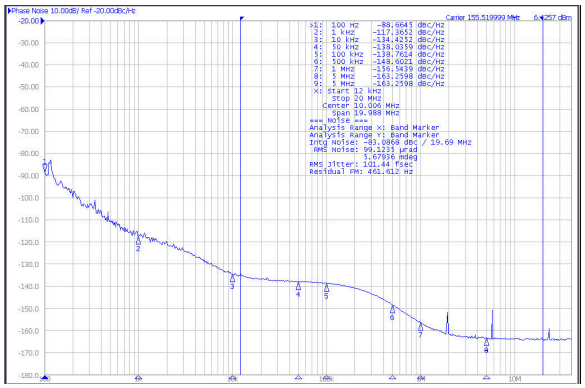


Jitter = 101fs RMS (12kHz to 20MHz)

f_{APLL2} = 5800.78125MHz

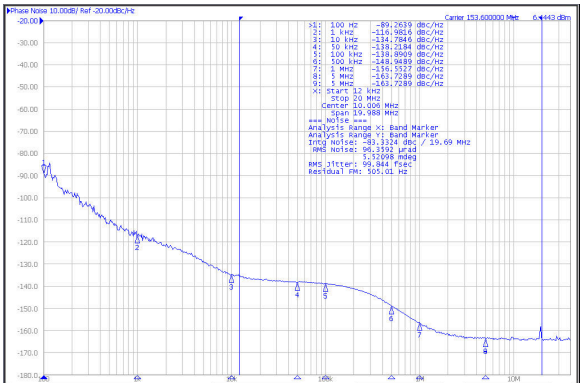
Figure 6-14. 161.1328125MHz HSDS Output From APLL2



Jitter = 101fs RMS (12kHz to 20MHz)

f_{APLL2} = 5598.72MHz

Figure 6-15. 155.52MHz HSDS Output From APLL2



Jitter = 100fs RMS (12kHz to 20MHz)

f_{APLL2} = 5836.8MHz

Figure 6-16. 153.6MHz HSDS Output From APLL2

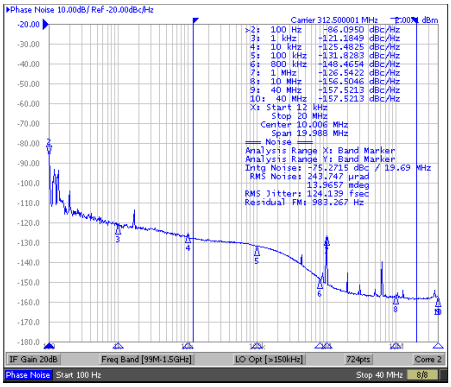
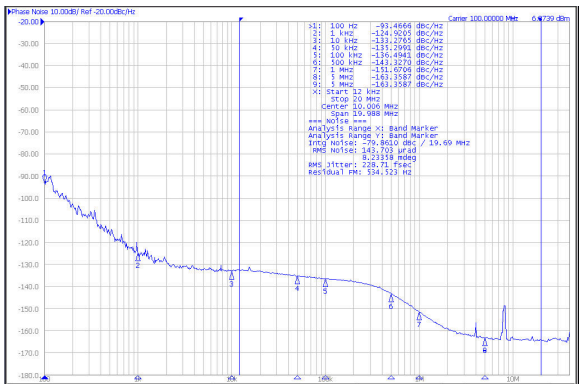


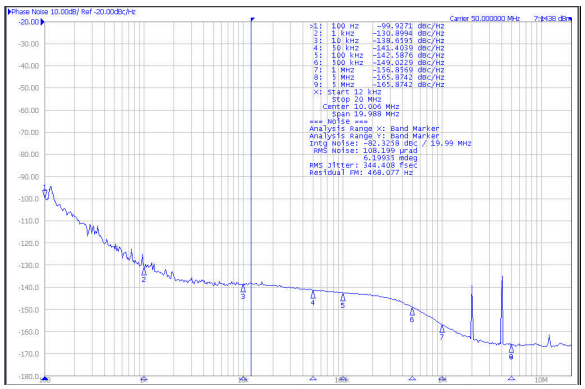
Figure 6-17. 312.5MHz HSDS Output From APLL1



Jitter = 230fs RMS (12kHz to 20MHz)

f_{APLL1} = 5200MHz

Figure 6-18. 100MHz HSDS Output From APLL1



Jitter = 345fs RMS (12kHz to 20MHz)

f_{APLL1} = 5200MHz

Figure 6-19. 50MHz HSDS Output From APLL1

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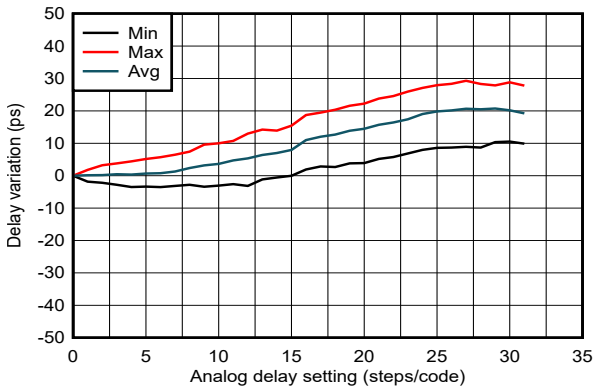

Figure 6-20. SYSREF/1PPS Delay Linearity vs. Analog Delay Code 2

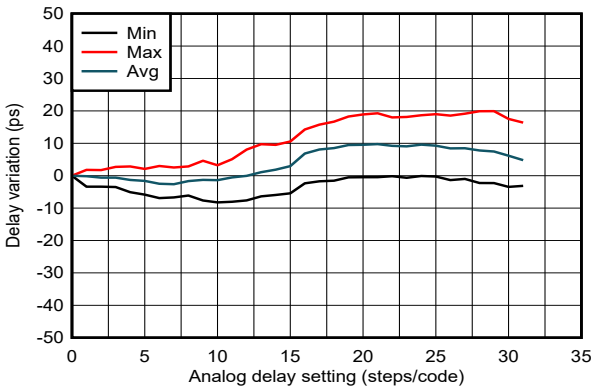

Figure 6-21. SYSREF/1PPS Delay Linearity vs. Analog Delay Code 3

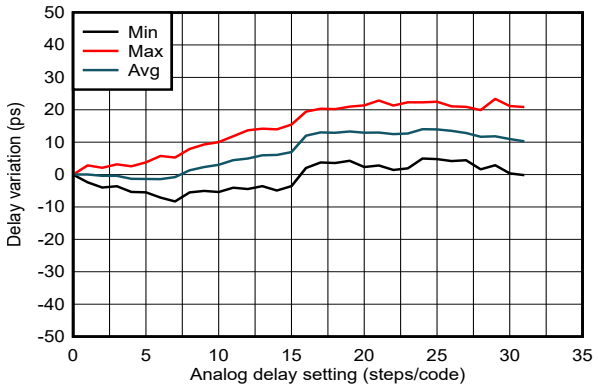

Figure 6-22. SYSREF/1PPS Delay Linearity vs. Analog Delay Code 4

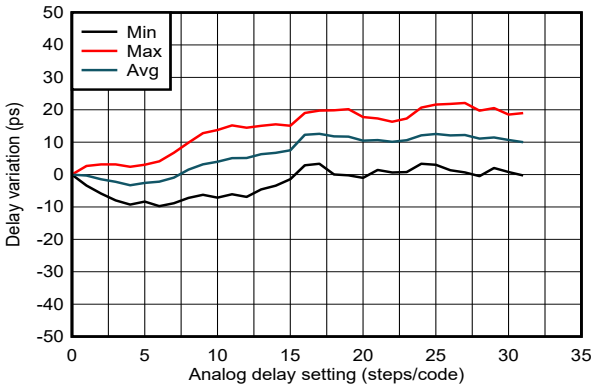

Figure 6-23. SYSREF/1PPS Delay Linearity vs. Analog Delay Code 5

7 Parameter Measurement Information

7.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions, causing confusion when reading data sheets or communicating with other engineers. This section addresses the measurement and description of a differential signal so that the reader is able to understand and distinguish between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, the signal only exists in reference to the differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 7-1 shows the two different definitions side-by-side for inputs and Figure 7-2 shows the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the noninverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

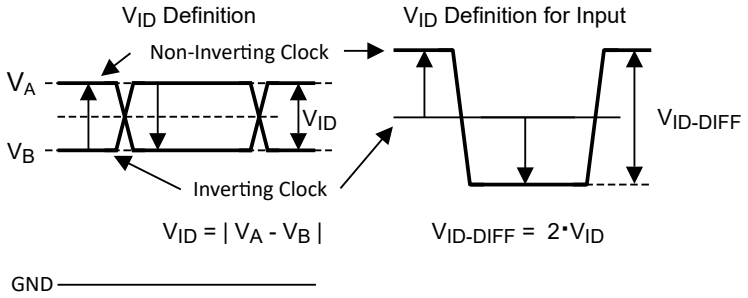

Figure 7-1. Two Different Definitions for Differential Input Signals

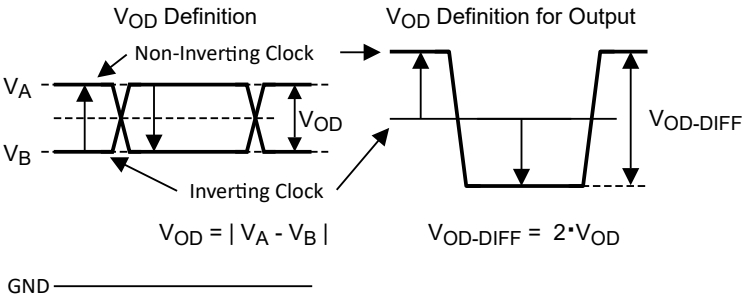

Figure 7-2. Two Different Definitions for Differential Output Signals

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7.2 Output Clock Test Configurations

This section describes the characterization test setup for different output formats.

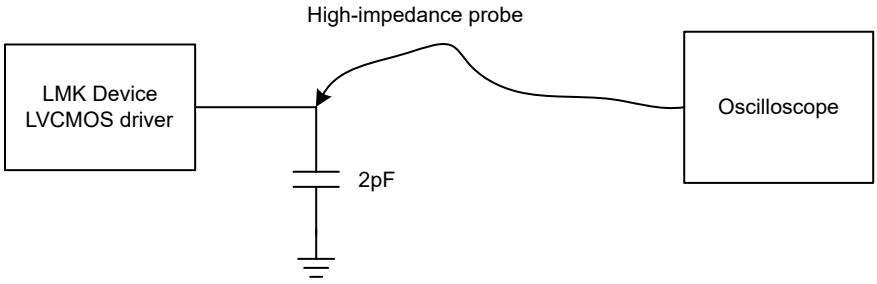


Figure 7-3. LVCMOS Output Time Domain Test Configuration

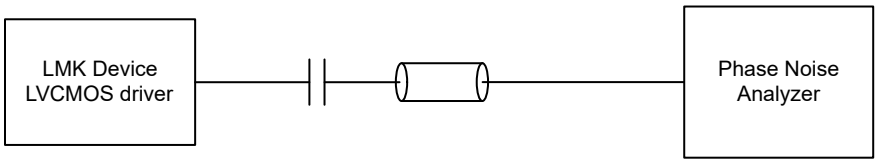


Figure 7-4. LVCMOS Output Phase Domain Test Configuration

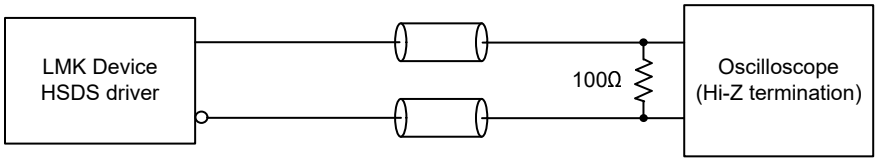


Figure 7-5. HSDS Output Time Domain Test Configuration

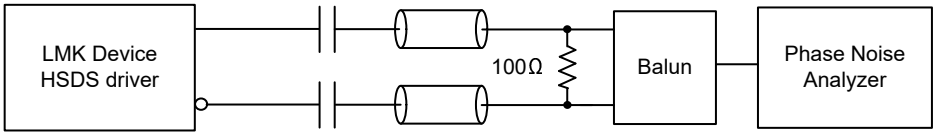


Figure 7-6. HSDS Output Phase Domain Test Configuration

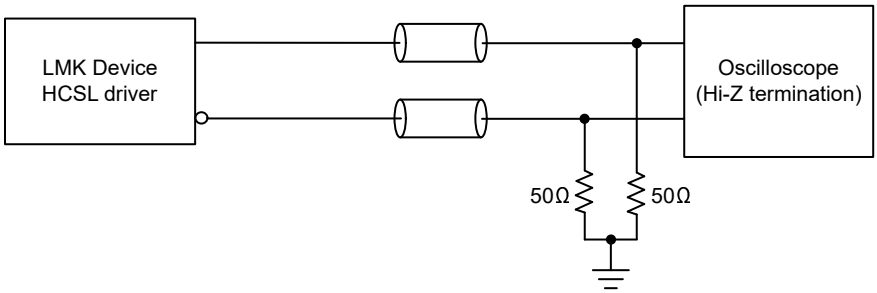


Figure 7-7. HCSL Output Time Domain Test Configuration

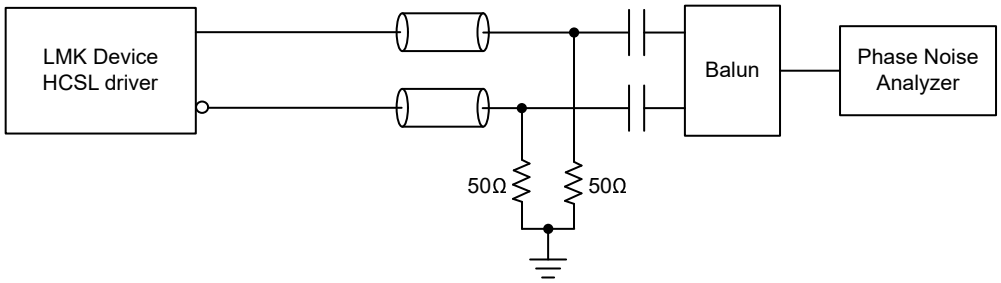
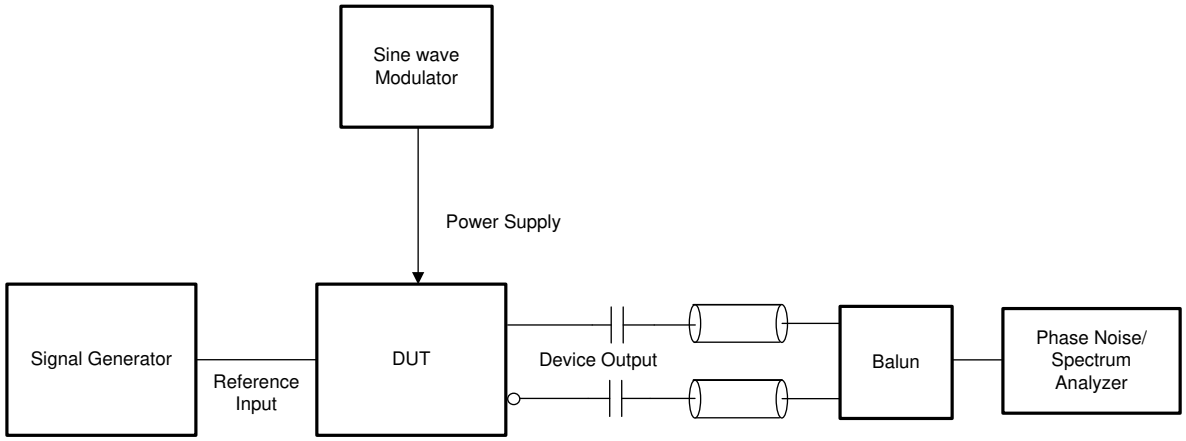


Figure 7-8. HCSL Output Phase Domain Test Configuration



Single-side band spur level measured in dBc with a known noise amplitude and frequency injected onto the device power supply.

Figure 7-9. Power Supply Noise Rejection (PSNR) Test Configuration

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8 Detailed Description

8.1 Overview

The LMK5C33414AS1 has four reference inputs, three digital PLLs (DPLL), three analog PLLs (APLLs) with integrated VCOs, and 14 output clocks. The BAW APLL (APLL3) uses an ultra-high performance BAW VCO (VCBO) with a very high quality factor, and thus minimizes dependency on the phase noise or frequency of the external oscillator (XO) input clock. TI's VCBO technology reduces the overall design cost to meet the free-run and holdover frequency stability requirements. An XO, TCXO, or OCXO input is required and must be selected based on system holdover stability requirements. Each APLL can be controlled by the corresponding DPLL, allowing the APLL domain to be locked to the DPLL reference input for synchronous clock generation. Each APLL can select a reference from XO port or another APLL divided clock. Each DPLL can select a synchronization input reference from reference inputs INx or align to another APLL domain by selecting feedback from one of the cascade dividers.

The DPLL reference input mux supports automatic input selection based on priority and reference signal monitoring criteria. Manual input selection is also possible through software or pin control. The device provides Hitless Switching between reference sources with proprietary phase cancellation and phase slew control for good phase buildout and transient performance. The Reference Input Monitoring block monitors the clock inputs and performs a hitless switchover or holdover when a loss of reference (LOR) is detected. A LOR condition is detected upon any violation of the threshold limits set for the input monitors, which include frequency, missing and early pulse, runt pulse, and 1PPS (pulse-per-second) detectors. The threshold limits for each input detector can be set and enabled per reference clock input. The Tuning Word History monitor feature determines the initial output frequency accuracy upon entry into holdover based on the historical average frequency when locked, thereby minimizing the frequency and phase disturbance during a LOR condition.

The LMK5C33414AS1 has 14 outputs with programmable output driver types, allowing up to 14 differential clocks, or a combination of differential and single-ended clocks. Up to four single-ended 1.8V or 2.65V LVCMOS clocks (each from _P and _N outputs from OUT0 and OUT1) can be configured with 12 differential output clocks..

Each output clock derives from one of the supported APLL/VCO domains through the output muxes. Output 0 (OUT0) and Output 1 (OUT1) are the most flexible and can select the source from the XO, reference input, or any APLL domain. A SYSREF or 1PPS output can be supported on Output 0 (OUT0) and Output 1 (OUT1) as well as any other differential output sourced from a Section 8.3.13 divider. The output dividers have a SYNC feature to allow multiple outputs to be phase-aligned. Zero-Delay Mode (ZDM) can also achieve a deterministic phase alignment between a clock from any DPLL presented to OUT0 and the selected reference input. ZDM feedback paths are also available on OUT10 for DPLL3 and OUT4 for DPLL2.

To support IEEE 1588 PTP secondary clock or other clock steering applications, the DPLL supports DCO mode with less than 1-ppt (part per trillion) frequency resolution for precise frequency and phase adjustment through software or pin control. The LMK5C33414AS1 includes the IEEE 1588 PTP stack synchronization software to form a complete network synchronizer and provide high accuracy, ultra-low jitter, reference clocks disciplined to a primary reference clock source.

The device is fully programmable through I^2C or SPI and supports start-up frequency configuration with factory preprogrammed internal ROM pages. A programmable EEPROM Overlay, which allows POR configuration of registers related to APLL and output configuration, provides flexible power up output clocks. The DPLL configuration is not set by EEPROM values, but initialized based on the ROM Detailed Description, and fully programmable using the serial control interface. Internal LDO regulators provide excellent PSNR to reduce the cost and complexity of the power delivery network. The clock input and PLL monitoring status are visible through the GPIO status pins and interrupt registers readback for full diagnostic capability.

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8.2 Functional Block Diagram

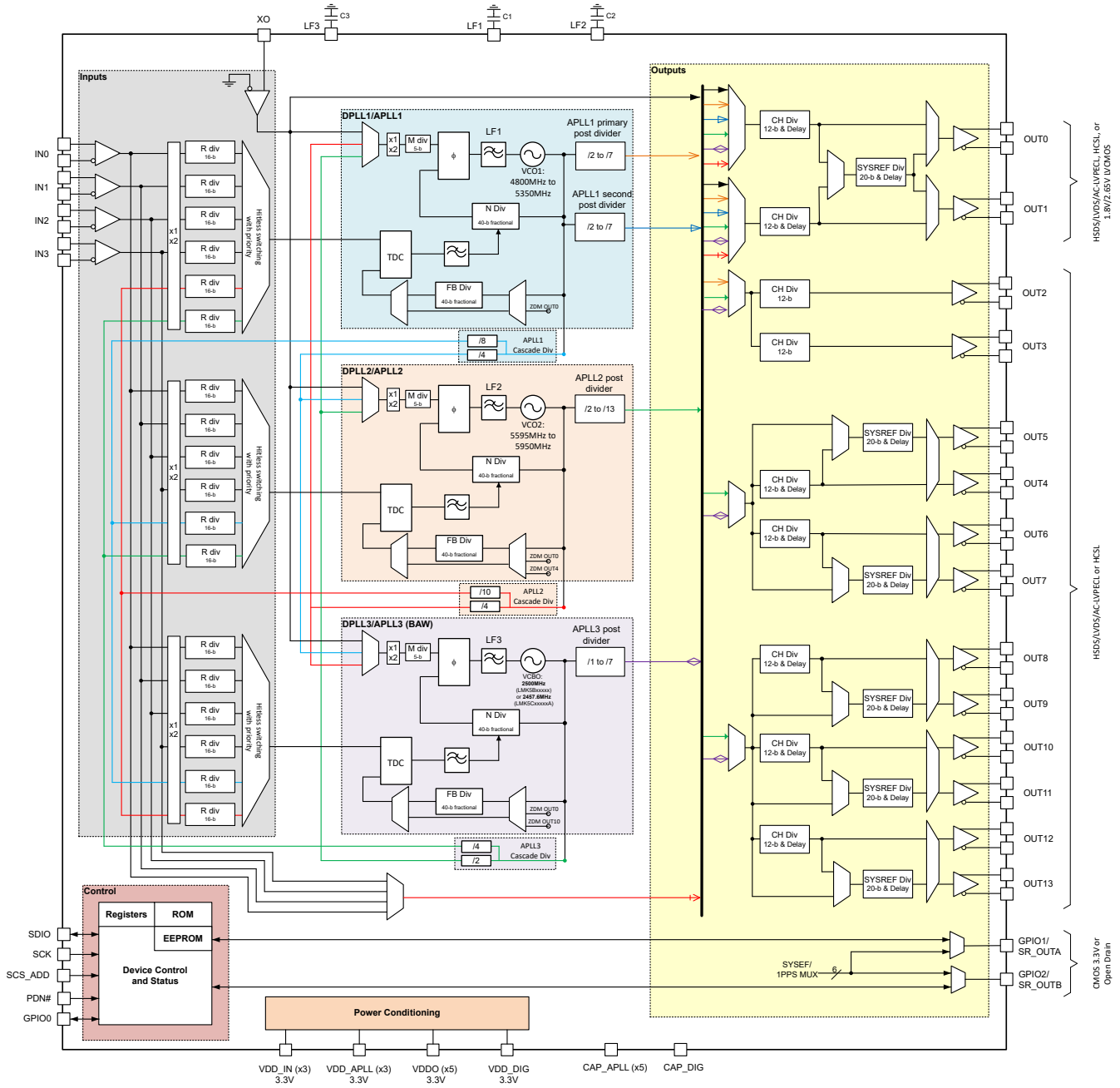

Figure 8-1. LMK5C33414AS1 Top-Level Block Diagram

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8.2.1 PLL Architecture Overview

Figure 8-2 shows the PLL architecture implemented in the LMK5C33414AS1. The ultra-low jitter channel consists of a digital PLL (DPLL3) and the BAW APLL (APLL3) with integrated VCBO (VCO3). APLL2 with integrated LC VCO (VCO2) can generate a second low jitter clock frequency domain. The APLL2 feedback N divider numerator can be controlled by DPLL2. APLL1 with integrated LC VCO (VCO1) can be used as a third clock generation domain. APLL1's feedback N divider numerator can be controlled by DPLL1.

The DPLL is comprised of a time-to-digital converter (TDC), digital loop filter (DLF), and programmable 40-bit fractional feedback (FB) divider with sigma-delta-modulator (SDM). The APLLs are comprised of a reference (R) divider, phase-frequency detector (PFD), loop filter (LF), fractional feedback (N) divider with SDM, and VCO.

Each DPLL has a reference selection mux that allows the DPLL to be either locked to another VCO domain (Cascaded DPLL Operation) of the APLL or locked to any reference input (Independent DPLL Operation) to provide unique flexibility in frequency and phase control across multiple clock domains. The cascading architecture provides unique flexibility for hybrid synchronization of frequency and phase control across multiple clock domains.

Each APLL has a reference selection mux that allows the APLL to be either locked to the XO input or to the cascaded divider output of another APLL (APLL Cascaded With DPLL).

Do not cascade one VCO output to both the DPLL reference and APLL reference of the same DPLL+APLL pair.

Each APLL has a fixed 40-bit denominator controllable by the DPLL when locked to an input reference. When one or more of the APLL are operating without DPLL control in APLL only mode, a programmable 24-bit denominator is also available for selection to synthesize exact frequency ratios. TI recommends the programmable 24-bit denominator when implementing hybrid synchronization or cascading between frequency domains to maintain 0ppm frequency error without DPLL control.

Any unused DPLL or APLL must be disabled (powered-down) to save power. Each VCO of the APLL drives the clock distribution blocks using the respective VCO post-dividers. If the post-divider setting is 1 for the VCBO, then the post-divider is bypassed and the VCBO feeds the output clock distribution blocks directly.

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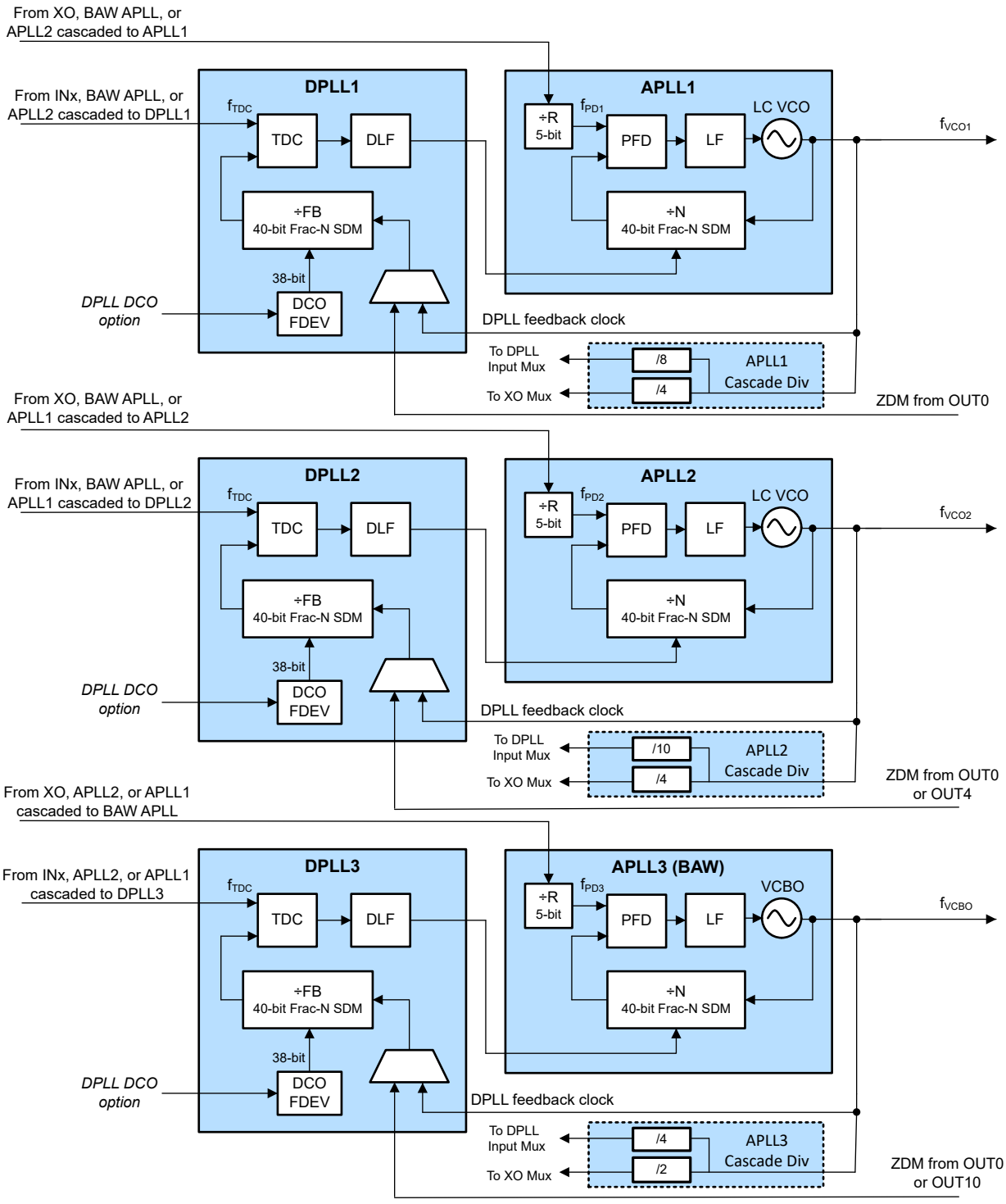

Figure 8-2. PLL Architecture

The following sections describe the basic principles of DPLL and APLL operation. See DPLL Operating States for more details on the PLL modes of operation including holdover.

8.2.2 DPLL

When DPLL operation is enabled and the DPLL is locked, the DPLL reference inputs (INx pins) determine the frequency stability and accuracy of the output clocks. The clock source on the XO pin determines the

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free-run and holdover frequency stability and accuracy of the output clocks. The VCBO determines the BAW APLL output clock phase noise and jitter performance over the 12kHz to 20MHz integration band, regardless of the frequency and jitter of the XO pin input. This increased immunity from reference noise degradation allows the BAW APLL to use a cost-effective, low-frequency TCXO or OCXO as the external XO input while still maintaining standards-compliant frequency stability and low loop bandwidth (≤10Hz) required for SyncE and PTP synchronization applications. The other APLLThe other APLLs contain a conventional LC-type VCO which can be optimized for best jitter performance over the DC to 100kHz integration band by using a wide loop bandwidth with a clean reference and a high phase detector frequency. When encountering system performance limitations arising from XO frequency or phase noise, there are unique cascading options to provide a clean high frequency reference for the LC APLL The LMK5C33414AS1 allows the user to select the divided output from the VCBO (BAW APLL Cascaded) which can significantly reduce the LC APLL output RMS jitter.

If DCO mode is enabled on a DPLL, a frequency deviation step value (FDEV) can be programmed and used to adjust (increment or decrement) the FB divider numerator of the DPLL. The DCO frequency adjustment effectively propagates through the APLL domain to the output clocks and any cascaded DPLL orAPLL domains.

The programmed DPLL loop bandwidth (BW_{DPLL}) must be lower than all of the following:

1. 1/100th of the DPLL TDC rate.
2. 1/10th the APLL loop bandwidth.
3. The maximum DPLL bandwidth setting of 4kHz.

8.2.2.1 Independent DPLL Operation

During independent DPLL operation, each DPLL can select a reference input (INx) as preferred. Each DPLLs can share the same reference or each can select a different reference. At start-up, each APLL locks to the XO input after initialization and operates in free-run mode. When a valid DPLL reference input is detected, each DPLL begins lock acquisition on based on the reference priority settings. The TDC in the DPLL compares the phase between the selected reference input clock and the FB divider clock from the respective VCO, generating a digital correction word corresponding to the phase error. The correction word is filtered by the digital loop filter (DLF), and the DLF output adjusts the APLL N divider numerator to pull the VCO frequency into lock with the reference input.

Since each DPLL can work independently in this mode, the DPLLs can lock or unlock without impacting other channels.

When selecting an XO input frequency, TI recommends to avoid ratios falling near integer or half integer boundaries to minimize spurious noise. The best practice is to select an XO input frequency that results in an APLL fractional N divider ratio (NUM/DEN) between the range of 0.125 to 0.45 and 0.55 to 0.875. Choosing a higher frequency XO is better for jitter performance, especially for the BAW APLL and APLL2 outputs. Cascade the BAW APLL output into APLL2 or APLL1 when the XO frequency or phase noise performance is poor.

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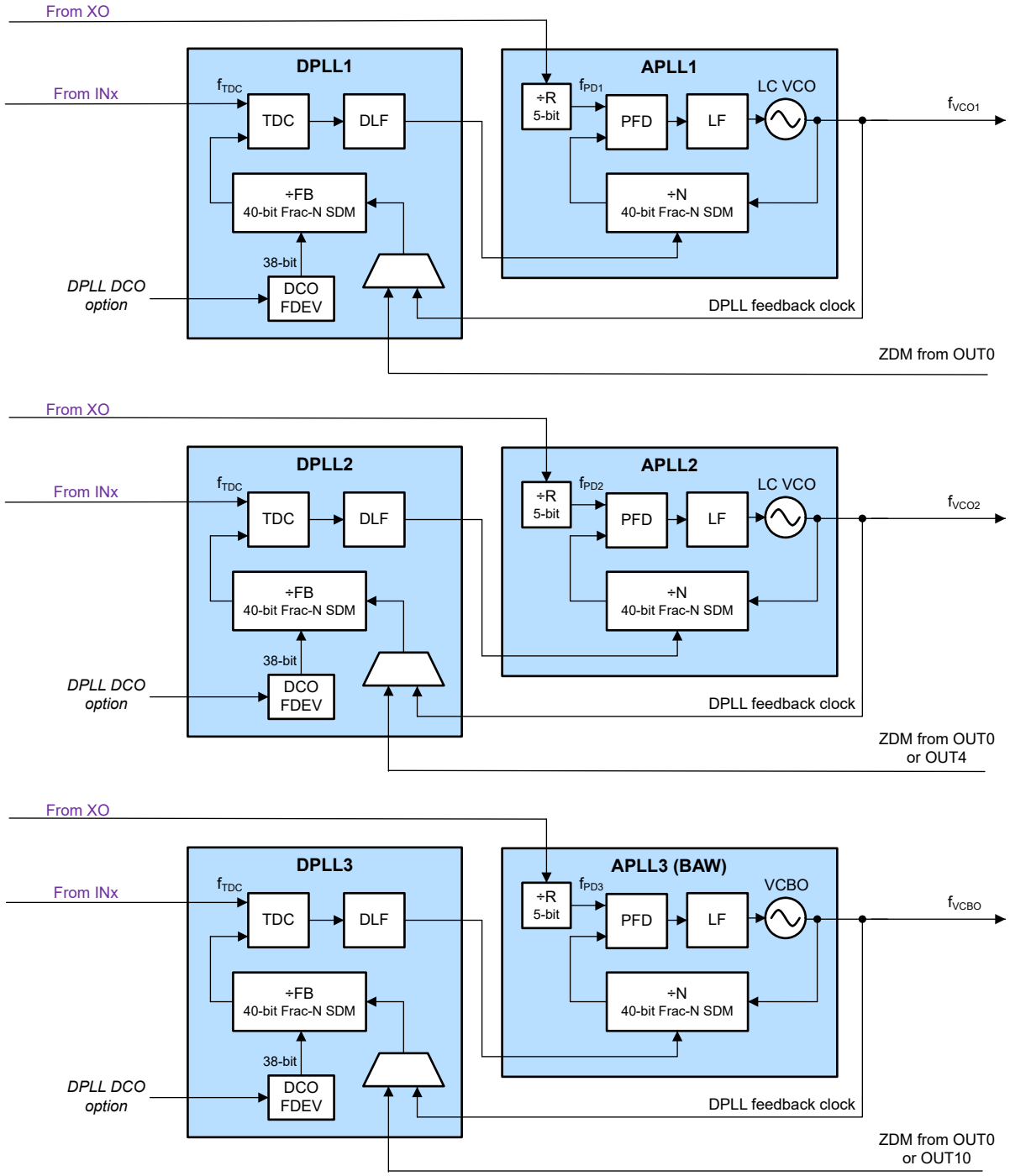

Figure 8-3. DPLL Independent Mode

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8.2.2.2 Cascaded DPLL Operation

Figure 8-4 shows an example where the other DPLLx is in cascaded mode from DPLL3 and the BAW APLL. In this example, DPLL3 is the main synchronization DPLL. The other DPLLx is the cascaded DPLL.

Cascading of DPLLs provides clean, low jitter, output clocks synchronized with DPLL3. When all enabled DPLLs and APLLs are locked, all enabled outputs are synchronized to the reference selected by the main synchronization DPLL.

When no valid reference input is present, each APLL locks the VCO frequency to the external XO input and operates in free-run mode.

When a valid DPLL reference input is detected, the main DPLL begins lock acquisition. The DPLL TDC compares the phase of the selected reference input clock with the FB divider clock from the respective VCO and generates a digital correction word corresponding to the phase error. The correction word is filtered by the DLF, and the DLF output adjusts the APLL N divider numerator to pull the VCO frequency into lock with the reference input.

DPLL3 lock status does not necessarily impact the other DPLLx lock status. If the BAW APLL is in free-run mode or holdover mode, and the VCBO frequency offset ppm value is still within the valid reference conditions for the other DPLLx, then the cascaded DPLLx and paired APLLx are able to maintain lock status while tracking the same frequency offset as the BAW APLL. Note in the cascaded DPLL mode, the best jitter performance and frequency stability is achieved after DPLL3 has locked.

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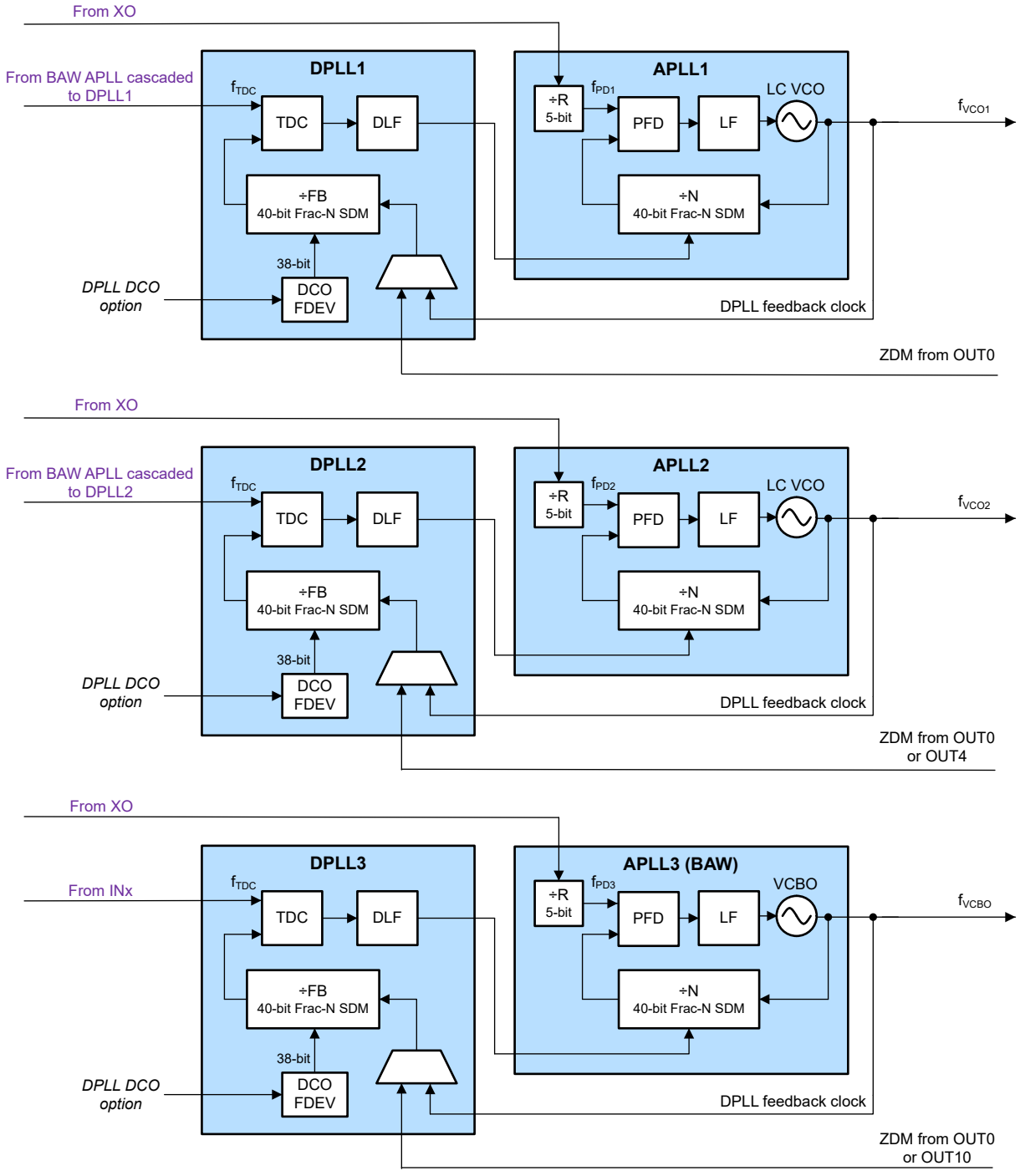

Figure 8-4. DPLL Cascaded Mode

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8.2.2.3 APLL Cascaded With DPLL

Figure 8-6 shows APLL1 and APLL2 cascaded from the BAW APLL. The VCBO is held around the nominal center frequency of 2457.6MHz while APLL1 and APLL2 acquire lock. Subsequently, the BAW APLL locks the VCBO frequency to the external XO input and operates in free-run mode until a valid reference input is detected.

Cascaded PLLs lock to a divided frequency from the source VCO. When a valid DPLL reference input is detected beyond a minimum valid time, the DPLLs begin lock acquisition to the reference input. Each DPLL TDC compares the phase of the selected reference input clock and the FB divider clock from the respective VCO and generates a digital correction word corresponding to the phase error. At the beginning, the DPLL TDC simply cancels out the phase error with the no filtering correction word. Then, the subsequent correction word is filtered by the DLF, and the DLF output controls the APLL N divider SDM to pull the VCO frequency into lock with the reference input.

Using the VCBO as a cascade source to APLL1 or APLL2 provides the APLL a high-frequency, ultra-low-jitter reference clock. This unique cascading feature can provide improved close in phase noise performance if the XO/TCXO/OCXO is a low frequency or has poor phase noise performance. Note that in cascaded DPLL operation the best jitter performance and frequency stability is achieved after DPLL3 locked.

DPLL3 lock status impacts the other DPLLx lock status when DPLL3 is cascaded to the other DPLLx or APLLx. If the BAW APLL is in free-run mode or holdover mode, the VCBO frequency offset ppm value can introduce a similar frequency offset to the APLLx outputs even though the cascaded DPLLx remains in a locked status. In this configuration example, the best practice is to monitor the lock status of both the BAW APLL and the other APLLx. Alternatively at start-up, verify that the DPLL3 and the BAW APLL are locked first; next, toggle the other APLLx enable (APLLx_EN bit = 0 → 1) to calibrate the VCOx; then, double check the APLLx lock status.

In the above example, the BAW APLL is the upstream APLL, while APLL1 and APLL2 are the downstream APLLs. If there are system start-up requirements on the clock sequencing, APLL1 or APLL2 can also be configured as the upstream APLL.

When cascading APLLs, the downstream APLL can use the DPLL or bypass and power down the DPLL depending on performance requirements. If the other DPLLx is disabled from the above APLL cascaded mode, then DPLL3-only cascade mode can be used. In this case, VCO1 or VCO2 can track the VCBO domain during DPLL3 lock acquisition and locked modes, which allows the user to synchronize the clock domain of the APLL1 or APLL2 to the DPLL3 reference input.

When a DPLL is disabled, the best practice is to use the 24-bit numerator and programmable 24-bit denominator instead of the fixed 40-bit denominator to eliminate frequency error from APLL reference to output.

Do not cascade one VCO output to both the DPLL reference and APLL reference of the same DPLL+APLL pair.

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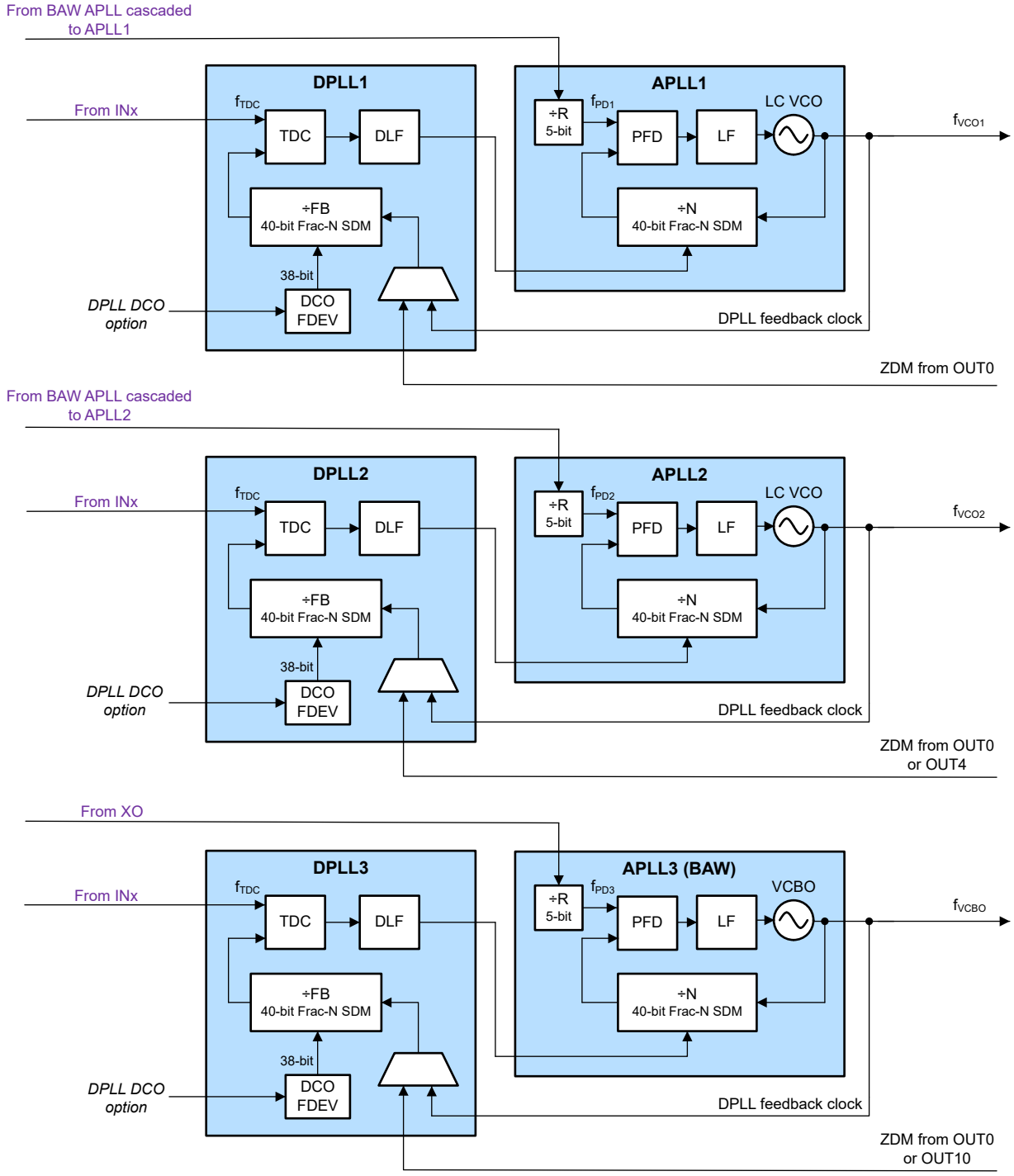

Figure 8-5. APLL Cascaded With DPLLs Enabled Example

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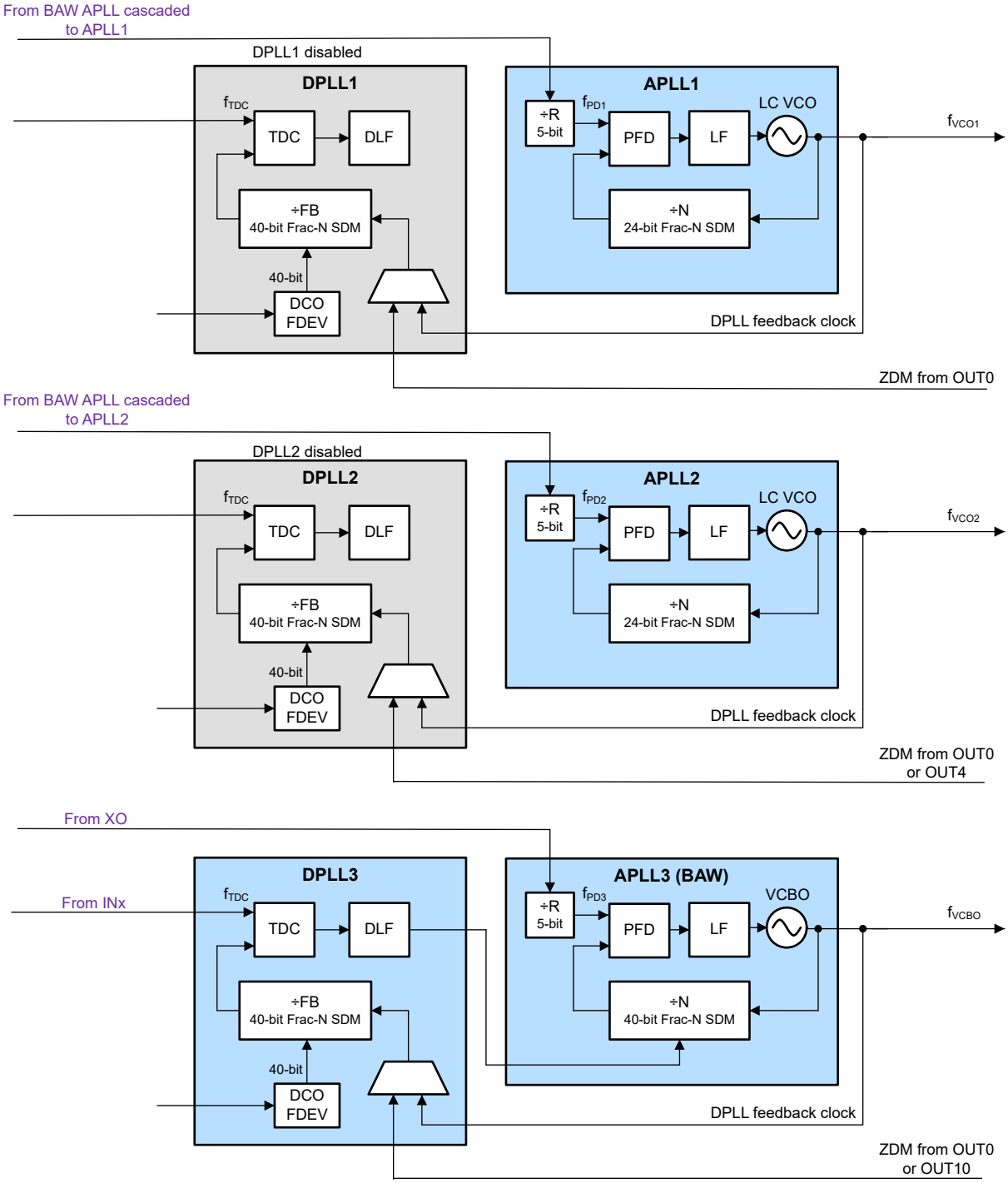

Figure 8-6. APLL Cascaded With DPLLs Disabled Example

8.2.3 APLL-Only Mode

In APLL-only mode, the external XO input source determines the free-run frequency stability and accuracy of the output clocks. The DPLL blocks are not used and do not affect the APLLs. The APLLs can operate in cascaded mode or independent mode. DCO for each APLL is available through control register writes.

The principle of operation for APLL-only mode after power-on reset and initialization is as follows. If APLL1 or APLL2 is in cascaded mode as shown in Figure 8-6 (DPLL3 also is not used), VCO1 or VCO2 tracks the VCBO domain. APLLs lock in APLL priority order using bits: APLLx_STRT_PRTY. Cascading APLL1 or APLL2 from VCBO provides a high-frequency, ultra-low-jitter reference clock to minimize the in-band phase noise/jitter degradation that can otherwise occur from a lower performance XO/TCXO/OCXO.

If APLL1 or APLL2 is not cascaded as shown in Figure 8-7, VCO1 or VCO2 locks to the XO input in APLLx_STRT_PRTY order after initialization and operate independent of the BAW APLL domain.

When operating in APLL-Only mode without DPLL control, select the programmable 24-bit denominator (PLLx_MODE = 0) instead of a fixed 40-bit denominator (PLLx_MODE = 1) to synthesize exact frequency ratios and maintain 0ppm frequency error.

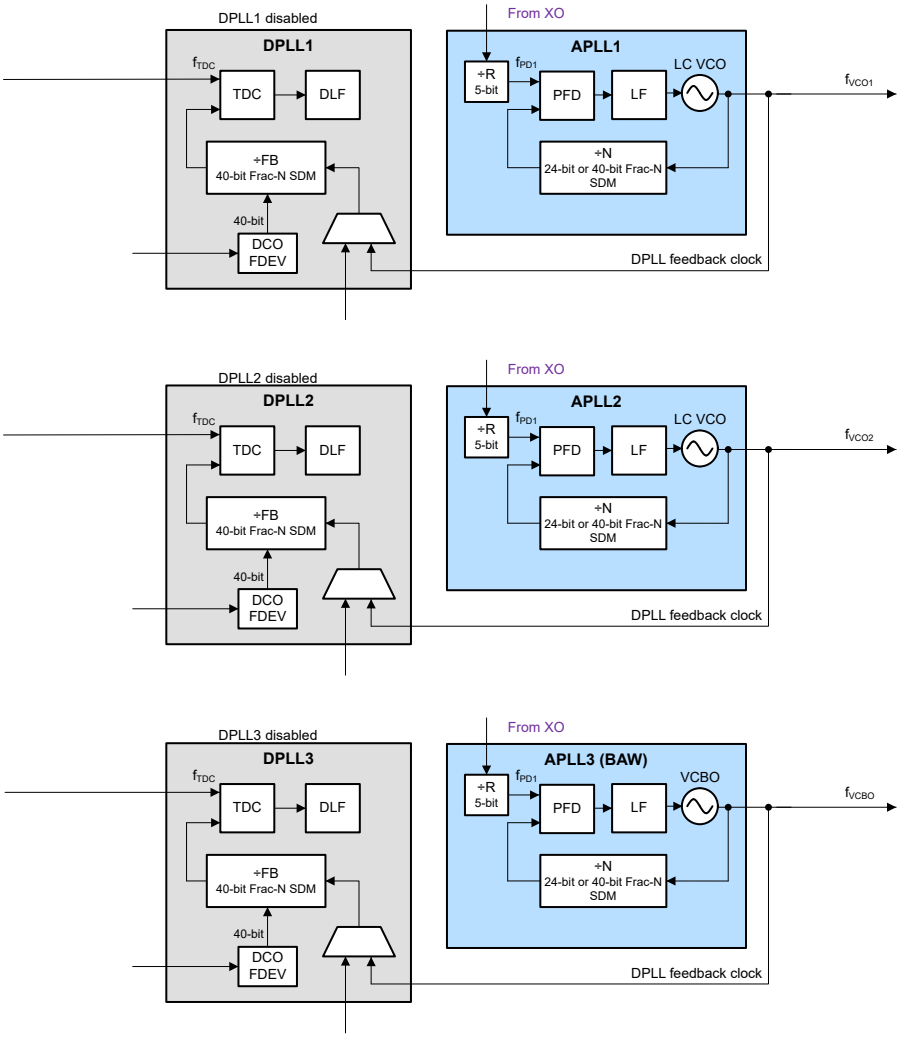

Figure 8-7. APLL-Only Independent Mode

8.3 Feature Description

The following sections describe the features and functional blocks of the LMK5C33414AS1.

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8.3.1 Oscillator Input (XO)

The XO input is the reference clock for the fractional-N APLLs when the APLLs are not used in cascade mode. The XO input determines the output frequency accuracy and stability in free-run or holdover modes.

For proper DPLL operation, the XO frequency must have a **non-integer relationship** with the VCO frequency so the respective APLL N divider has a fractional divider ratio. For APLL-only mode, the XO frequency can have an integer or fractional relationship with the VCOs frequencies.

For applications requiring DPLL functionality, such as SyncE and PTP/IEEE-1588 for eCPRI, the XO input can be driven by a TCXO, OCXO, or external traceable clock that conforms to the frequency accuracy and holdover stability required by the applicable synchronization standard. TCXO and OCXO frequencies of 13MHz, 14.4MHz, 19.44MHz, 24MHz, 25MHz, 27MHz, 38.88MHz, 48MHz, and 54MHz are commonly available and cost-effective options that allow the BAW APLL to operate in fractional mode for a VCBO frequency of 2457.6MHz.

An XO/TCXO/OCXO source with low frequency or high phase jitter/noise floor has no impact on the BAW APLL output jitter performance because the VCBO determines the jitter and phase noise over the 12kHz to 20MHz integration bandwidth. An XO doubler increasing the PFD frequency can be enabled for each APLL to further optimize close in phase noise performance.

The XO input buffer has programmable input on-chip termination and AC-coupled input biasing configurations as shown in Figure 8-8. The buffered XO path also drives the input monitoring blocks.

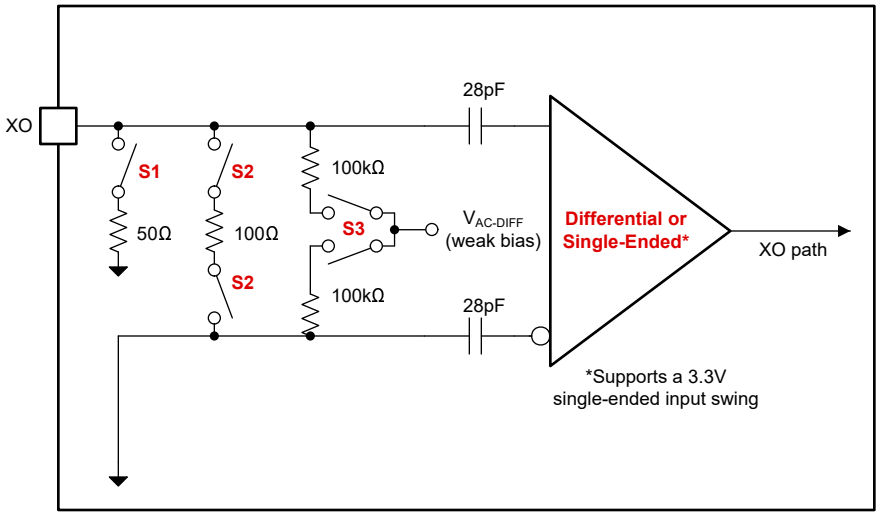

Figure 8-8. XO Input Buffer

Table 8-1 lists the typical XO input buffer configurations for common clock interface types.

Table 8-1. XO Input Buffer Modes

XO_TYPE	INPUT TYPES	INTERNAL SWITCH SETTINGS	
		INTERNAL TERM. (S1, S2)(1)	INTERNAL BIAS (S3)(2)
0x00	DC (external termination)	OFF	OFF
0x01	AC (external termination)	OFF	ON (1.3V)
0x03	AC (internal 100Ω to GND)	100Ω	ON (1.3V)
0x04	DC (internal 50Ω to GND)	50Ω	OFF
0x05	AC (internal 50Ω to GND)	50Ω	ON (1.3V)
0x08	LVCMOS	OFF	OFF
0x0C	LVCMOS (internal 50Ω to GND)	50Ω	OFF

(1) S1, S2: OFF = External termination is assumed.
(2) S3: OFF = External input bias or DC coupling is assumed.

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8.3.2 Reference Inputs

The reference inputs (IN0, IN1, IN2 and IN3) can accept differential or single-ended clocks. Each input has programmable input type, termination, and DC-coupled or AC-coupled input biasing configurations as shown in Figure 8-9. Each input buffer drives the reference input mux of the DPLL block. The DPLL input mux can select from any of the reference inputs. The DPLL can switch between inputs with different frequencies if the frequencies can be divided-down to a common frequency by DPLL R dividers. The reference input paths also drive the various detector blocks for reference input monitoring and validation. DC-path switch can bypass internal AC-coupling capacitors to make low frequency input work robustly.

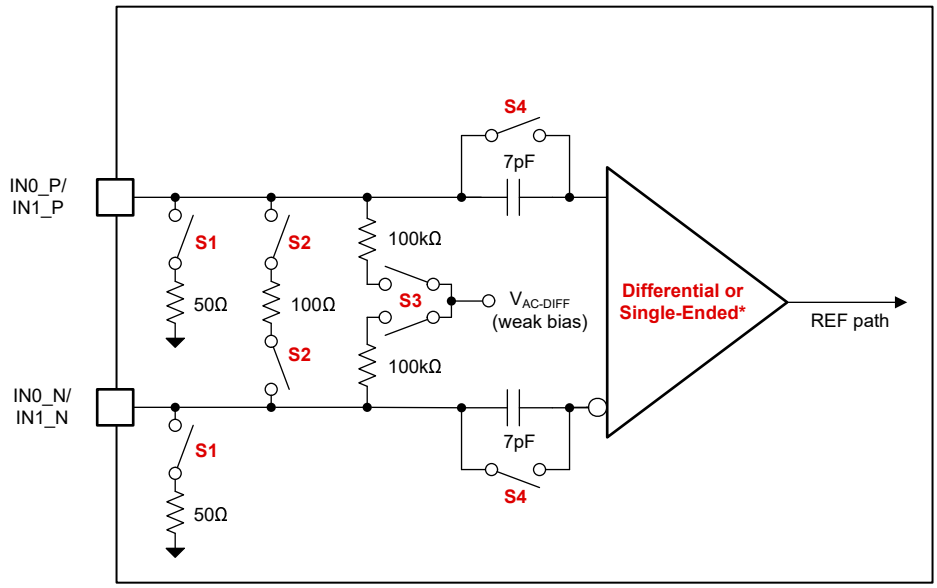

Figure 8-9. Reference Input Buffer

Table 8-2 lists the reference input buffer configurations for common clock interface types.

Table 8-2. Reference Input Buffer Modes

REFx_ITYPE, R68/R67/R66/R65	INPUT TYPE	INTERNAL REGISTER AND SWITCH SETTINGS					
		HYSTERESIS, R68[5]	AC CAPACITOR BYPASS, R68[4], S4(1)	SINGLE-ENDED SELECT, R68[3]	SINGLE-ENDED TERM., R68[2], S1(2)	DIFFERENTIAL TERM., R68[1], S2(2)	WEAK BIAS (1.3V) R68[0], S3(3)
0x00	Differential, ext. DC-coupled, ext. term.	0	0	0	0	0	0
0x01	Differential, ext. AC-coupled, ext. term.	0	0	0	0	0	1
0x02	Differential, ext. DC-coupled, int. 100Ω diff. term., LVDS/HSDS	0	0	0	0	1	0
0x03	Differential, ext. AC-coupled, int. 100Ω diff. term., LVDS/HSDS	0	0	0	0	1	1
0x04	Differential, ext. DC-coupled, int. 50Ω to GND HCSL	0	0	0	1	0	0
0x05	Differential, ext. AC-coupled, int. 50Ω to GND, HCSL	0	0	0	1	0	1

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Table 8-2. Reference Input Buffer Modes (continued)

REFx_ITYPE, R68/R67/R66/R65	INPUT TYPE	INTERNAL REGISTER AND SWITCH SETTINGS					
		HYSTERESIS, R68[5]	AC CAPACITOR BYPASS, R68[4], S4(1)	SINGLE-ENDED SELECT, R68[3]	SINGLE-ENDED TERM., R68[2], S1(2)	DIFFERENTIAL TERM., R68[1], S2(2)	WEAK BIAS (1.3V) R68[0], S3(3)
0x08	Single-ended, ext. DC-coupled, int. AC-coupled 70mV threshold, LVCMOS	0	0	1	0	0	0
0x0C	Single-ended, ext. DC-coupled, int. AC-coupled, int. 50Ω to GND, 70mV threshold	0	0	1	1	0	0
0x18	Single-ended, ext. DC-coupled, int. DC-coupled 150mV hysteresis, LVCMOS	0	1	1	0	0	0
0x28	Single-ended, ext. DC-coupled, int. AC-coupled 210mV hysteresis, LVCMOS	1	0	1	0	0	0
0x38	Single-ended, ext. DC-coupled, int. DC-coupled 0mV hysteresis, LVCMOS	1	1	1	0	0	0

(1) S4: 0 = Differential input amplitude detector can be used for all input types except LVCMOS or single-ended.
(2) S1, S2: 0 = External termination is assumed.
(3) S3: 0 = External input bias or DC-coupling is assumed.

8.3.3 Clock Input Interfacing and Termination

Figure 8-10 through Figure 8-14 show the recommended input interfacing and termination circuits. Unused clock inputs can be left floating or pulled down.

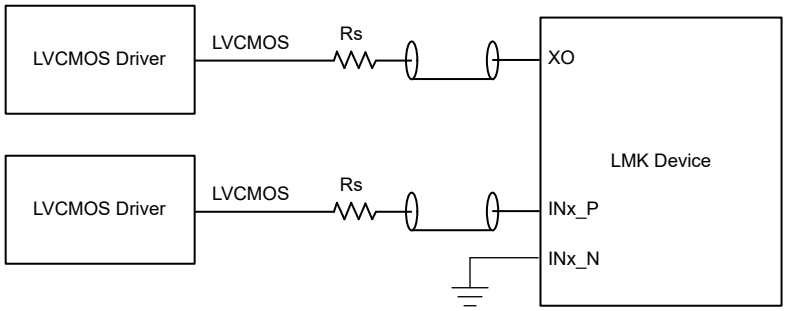

Figure 8-10. Single-Ended LVCMOS (1.8V, 2.5V, 3.3V) to Reference (INx_P) or XO Input (XO)

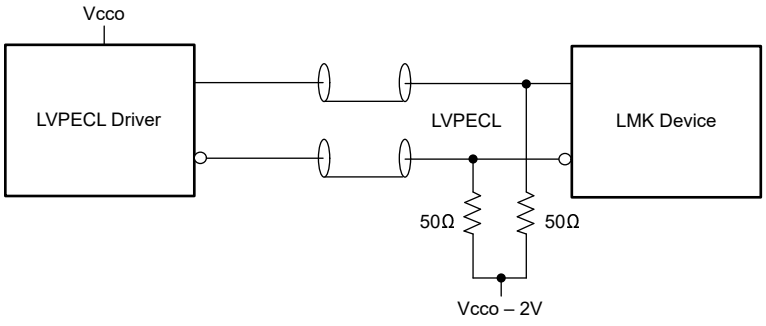

Figure 8-11. DC-Coupled LVPECL to Reference (INx)

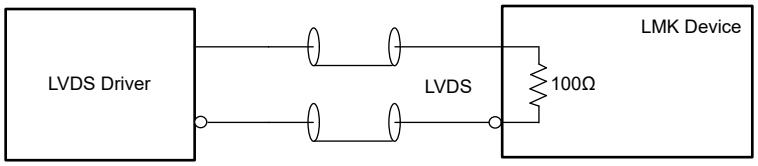

Figure 8-12. DC-Coupled HSDS/LVDS to Reference (INx)

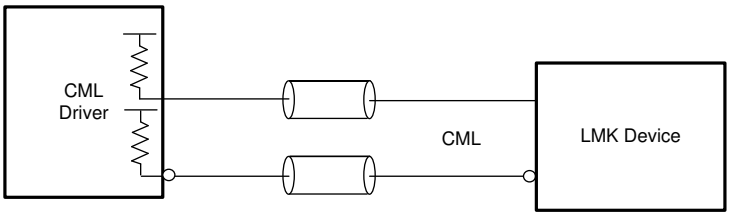

Figure 8-13. DC-Coupled CML (Source Terminated) to Reference (INx)

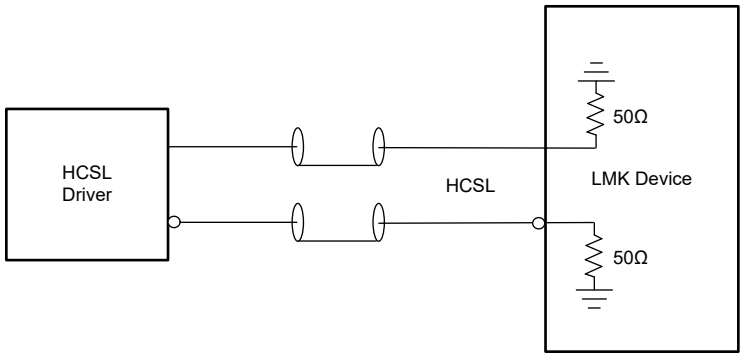

Figure 8-14. HCSL (Load Terminated) to Reference (INx)

Driver	R_B (Ω)
LVDS	open
CML*	open
LVPECL	120
HCSL	50

*CML driver requires 50Ω pull-ups

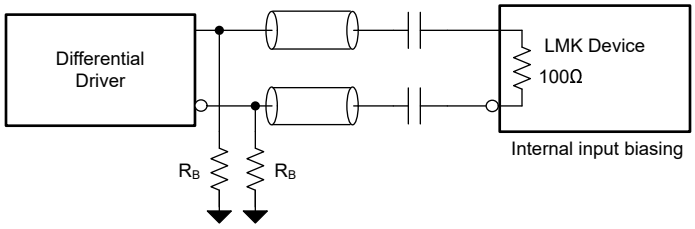

Figure 8-15. AC-Coupled Differential to Reference (INx)

8.3.4 Reference Input Mux Selection

For the DPLL block, the reference input mux selection can be done automatically using an internal state machine with a configurable input priority scheme, or manually through software register control or hardware pin control. The input mux can select IN0, IN1, IN2 or IN3 for LMK5C33414AS1. The priority for all inputs can be assigned through registers. The priority ranges from 0 to 7, where 0 = ignore (never select), 1 = first priority, 2 = second priority and 7 = 7th priority. When inputs are configured with the same priority setting, the lower enumeration INx is given first priority (with IN0 being the highest priority). The selected input can be monitored through the status pins or register.

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8.3.4.1 Automatic Input Selection

There are two automatic input selection modes that can be set by register: Auto Revertive and Auto Non-Revertive.

- *Auto Revertive:* In this mode, the DPLL automatically selects the valid input with the highest configured priority. If a clock with higher priority becomes valid, the DPLL automatically switches over to that clock immediately.
- *Auto Non-Revertive:* In this mode, the DPLL automatically selects the highest priority input that is valid. If a higher priority input because valid, the DPLL does not switch over until the currently selected input becomes invalid.

8.3.4.2 Manual Input Selection

There are two manual input selection modes that can be set by a register: Manual with Auto-Fallback and Manual with Auto-Holdover. In either manual mode, the input selection can be done through register control (using the DPLLx_MAN_REFSEL register) or hardware pin control (GPIOs).

- *Manual with Auto-Fallback:* In this mode, the manually selected reference is the active reference until the reference becomes invalid. If the reference becomes invalid, the DPLL automatically falls back to the highest priority input that is valid or qualified. If no prioritized inputs are valid, the DPLL enters holdover mode (if tuning word history is valid) or free-run mode. The DPLL exits holdover mode when the selected input becomes valid.
- *Manual with Auto-Holdover:* In this mode, the manually selected reference is the active reference until the reference becomes invalid. If the reference becomes invalid, the DPLL automatically enters holdover mode (if tuning word history is valid) or free-run mode. The DPLL exits holdover mode when the selected input becomes valid.

The reference input selection flowchart is shown in Figure 8-16.

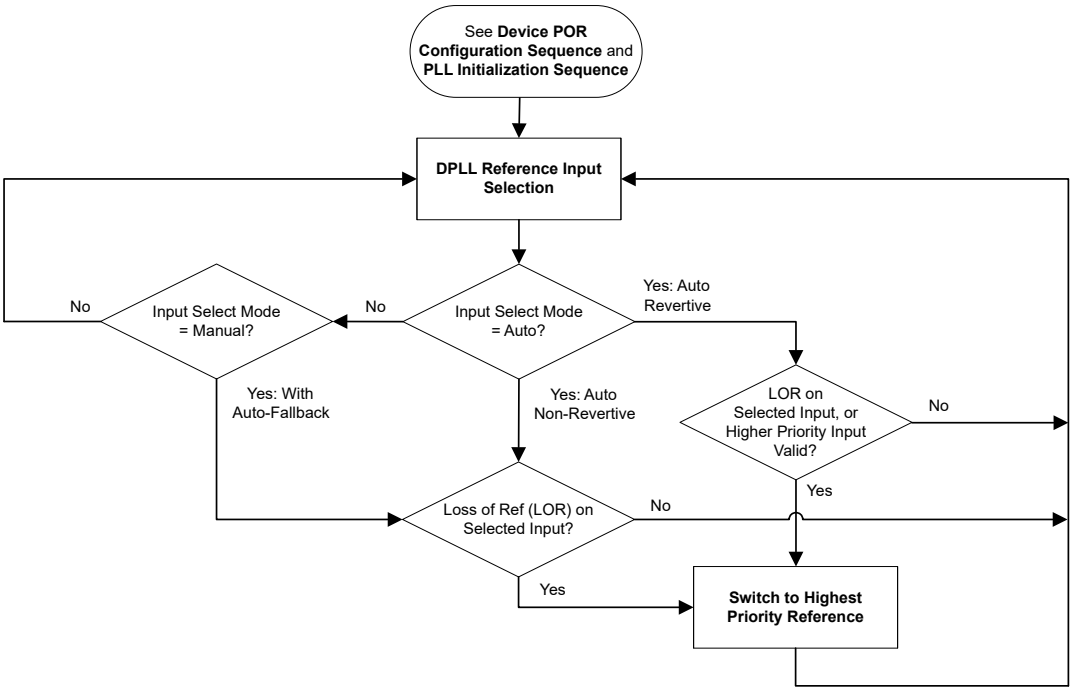

Figure 8-16. DPLL Reference Input Selection Flowchart

8.3.5 Hitless Switching

The DPLL supports hitless switching through TI's proprietary phase cancellation scheme with an optional phase slew control scheme. When hitless switching is disabled, a phase hit equal to the phase offset between the two inputs is propagated to the output at a rate determined by the filtering of the DPLL bandwidth.

8.3.5.1 Hitless Switching With Phase Cancellation

Typically phase cancellation is enabled during hitless switching to prevent a phase transient (phase hit) from immediately propagating to the outputs when switching between two frequency-locked reference inputs with a fixed phase offset. The phase cancellation persists indefinitely in the use case scenario when phase slew is not enabled commonly referred to as phase buildout. The inputs are frequency-locked when the inputs have the same exact frequency (0ppm offset), or have frequencies that are integer-related and can each be divided to a common frequency by integers. The hitless switching specifications ($t_{HITLESS}$ and $f_{HITLESS}$) are valid for reference inputs with no wander. In the case where two inputs are switched but are not frequency-locked, the output smoothly transitions to the new frequency with reduced transient.

8.3.5.2 Hitless Switching With Phase Slew Control

Enabling Phase Slew Control constrains the output phase transient or phase hit during hitless switching and holdover exit. Users can select DPLLx_PHS1_EN to enable Phase Slew Control to follow the step limits set in DPLLx_PHS1_THRESH and DPLLx_PHS1_TIMER. When transitioning slowly is desired while tracking the new input phase, enabling phase slew control removes the phase cancellation or phase build out based on the programmed timer value and step limits. Similarly when the DPLL switches from APLL-only mode or holdover mode to DPLL Lock Acquisition mode, or hitless switching with two inputs are not frequency-locked the phase slew limits are then applied. When both Phase Cancellation function and Phase Slew Control function are disabled, a phase hit equal to the phase offset between XO and selected input or between the two inputs at the moment of switching are then propagated to the output at a rate determined by the DPLL loop bandwidth. In the case where two inputs are switched but are not frequency-locked Phase Slew Control function can verify that the output smoothly transitions to the new frequency as the rate the defined by the step limits.

8.3.5.3 Hitless Switching With 1PPS Inputs

Hitless switching between 1PPS inputs is supported when ZDM synchronization is disabled, but the switchover event must only occur after the DPLL has acquired lock. If a switchover occurs before the DPLL has locked initially, the switchover is not hitless and the DPLL takes an indeterminate amount of time to lock. In this case, issue a soft-reset for the DPLL to lock to the selected input. In an application, the system host can monitor the DPLL lock status through a STATUS pin or bit to determine that the DPLL is locked before allowing a switchover between 1PPS inputs. The DPLL lock time is governed by the DPLL bandwidth (typically 10mHz for a 1PPS input).

8.3.6 Gapped Clock Support on Reference Inputs

The DPLL supports locking to an input clock that has missing periods and is referred to as a gapped clock. Gapping severely increases the jitter of a clock, so the DPLL provides the high input jitter tolerance and low loop bandwidth necessary to generate a low-jitter periodic output clock. The resulting output is a periodic non-gapped clock with an average frequency of the input with the missing cycles. The gapped clock width can not be longer than the reference clock period after the R divider (R_{INx} / f_{INx}). The reference input monitors must be configured to avoid any flags due to the worst-case clock gapping scenario to achieve and maintain lock. Reference switchover between two gapped clock inputs can violate the hitless switching specification if the switch occurs during a gap in either input clock.

8.3.7 Input Clock and PLL Monitoring, Status, and Interrupts

The following section describes the input clock and PLL monitoring, status, and interrupt features. The reference input frequency detector and phase valid detector can not be used at the same time on a single input.

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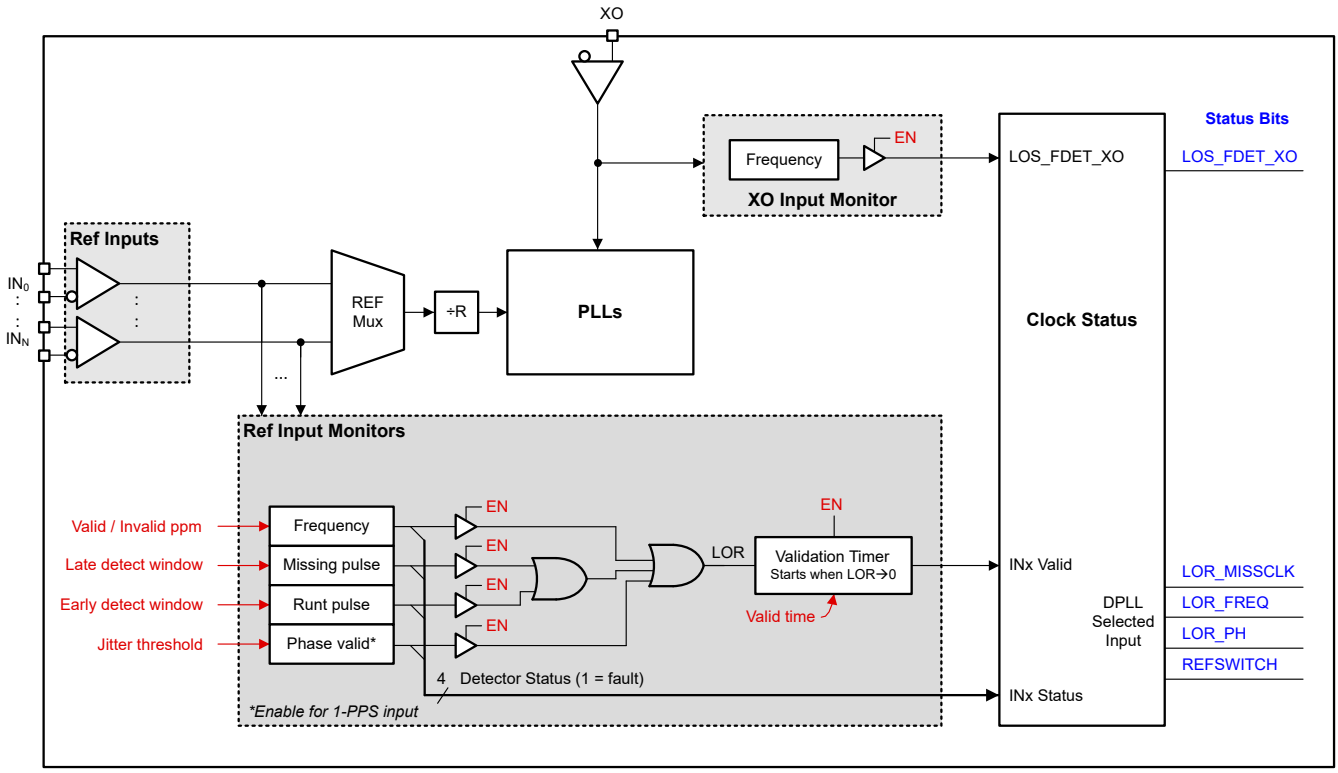

Figure 8-17. Clock Monitors for Reference and XO Inputs

8.3.7.1 XO Input Monitoring

The XO input has a coarse frequency monitor to help qualify the input before the monitor is used to lock the APLLs.

The XO frequency detector clears the LOS_FDET_XO flag when the XO input frequency is detected within the specified range listed in the Electrical Characteristics. The XO frequency monitor uses a RC-based detector and therefore can not precisely determine whether XO input clock has sufficient frequency stability. A stable XO input verifies successful VCO calibration of APLL2 or APLL1 during the APLL start-up. When the external XO clock has a slow or delayed start-up behavior, force a calibration on APLL2 and APLL1 once the XO input is stable. See Slow or Delayed XO Start-Up for more information.

The XO frequency detector can be bypassed by setting the XO_FDET_BYP bit (shown as **EN** in the XO input monitor block of Figure 8-17) so that the XO input is always considered valid by the PLL control state machine. The user can observe the LOS_FDET_XO status flag through the status pins and status bit. Setting XO_FDET_BYP bit bypasses the detect, but does not reflect any change to LOS_FDET_XO status flag.

8.3.7.2 Reference Input Monitoring

Each DPLL reference clock input is independently monitored for input validation before the clock is qualified and available for selection by the DPLL. The reference monitoring blocks include frequency, missing pulse, and runt pulse monitors. For a 1PPS input, the phase valid monitor is supported, while the frequency, missing pulse, and runt pulse monitors are not supported and must be disabled. A validation timer sets the minimum time for all enabled reference monitors to be clear of flags before an input is qualified.

The enablement and valid threshold for all reference monitors and validation timers are programmable per input. The reference monitors and validation timers are optional to enable, but are critical to achieve reliable DPLL lock and optimal transient performance during holdover or switchover events, and are also used to avoid selection of an unreliable or intermittent clock input. If a given detector is not enabled, the detector does not set a flag and is ignored. The status flag of any enabled detector can be observed through the status pins for any reference input

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(selected or not selected). The status flags of the enabled detectors can also be read through the status bits for the selected input of the DPLL.

8.3.7.2.1 Reference Validation Timer

The validation timer sets the amount of time required for each reference to be clear of flags from all enabled input monitors before the reference is qualified and valid for selection. The validation timer and enable settings are programmable.

8.3.7.2.2 Frequency Monitoring

The precision frequency detector measures the frequency offset or error (in ppm) of all input clocks relative to the XO input frequency, which is considered as the 0ppm reference clock for frequency comparison. The valid and invalid ppm frequency thresholds are configurable through the registers. The monitor clears the REFx_FDET_STATUS flag when the relative input frequency error is less than the valid ppm threshold. Otherwise, the monitor sets the REFx_FDET_STATUS flag when the relative input frequency error is greater than the invalid ppm threshold. The ppm delta between the valid and invalid thresholds provides hysteresis to prevent the REFx_FDET_STATUS flag from toggling when the input frequency offset is crossing these thresholds.

A measurement accuracy (ppm) and averaging factor are used in computing the frequency detector register settings. A higher measurement accuracy (smaller ppm) or higher averaging factor increases the measurement delay to set or clear the flag, which allows more time for the input frequency to settle, and can also provide better measurement resolution for an input with high drift or wander. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

8.3.7.2.3 Missing Pulse Monitor (Late Detect)

The missing pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period plus a programmable late window threshold (T_{LATE}). When an input pulse arrives before T_{LATE}, the pulse is considered valid and the missing pulse flag is cleared if set. When an input pulse does not arrive before T_{LATE} (due to a missing or late pulse), the missing pulse flag is set to disqualify the input.

Typically, T_{LATE} must be set higher than the longest clock period input (including cycle-to-cycle jitter), or higher than the gap width for a gapped clock. The missing pulse monitor can act as a coarse frequency detector with faster detection than the ppm frequency detector. The missing pulse monitor is supported for input frequencies between 2kHz and $f_{VCO}/12$ and must be disabled when outside this range.

The missing pulse and runt pulse monitors operate from the same window detector block for each reference input. The status flags for both these monitors are combined by logic-OR gate and can be observed through status pin. The window detector flag for a reference can also be observed through the corresponding REFx_MISSCLK_STATUS bit.

8.3.7.2.4 Runt Pulse Monitor (Early Detect)

The runt pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period minus a programmable early window threshold (T_{EARLY}). When an input pulse arrives after T_{EARLY}, the pulse is considered valid and the runt pulse flag is cleared. When an early or runt input pulse arrives before T_{EARLY}, the monitor sets the flag immediately to disqualify the input.

Typically, T_{EARLY} must be set lower than the shortest clock period of the input (including cycle-to-cycle jitter). The early pulse monitor can act as a coarse frequency detector with faster detection than the ppm frequency detector. The early pulse monitor is supported for input frequencies between 2kHz and $f_{VCO}/12$ and must be disabled when outside of this range.

Users must enable missing clock detect to use early clock detect. Early clock detect can not be enabled alone.

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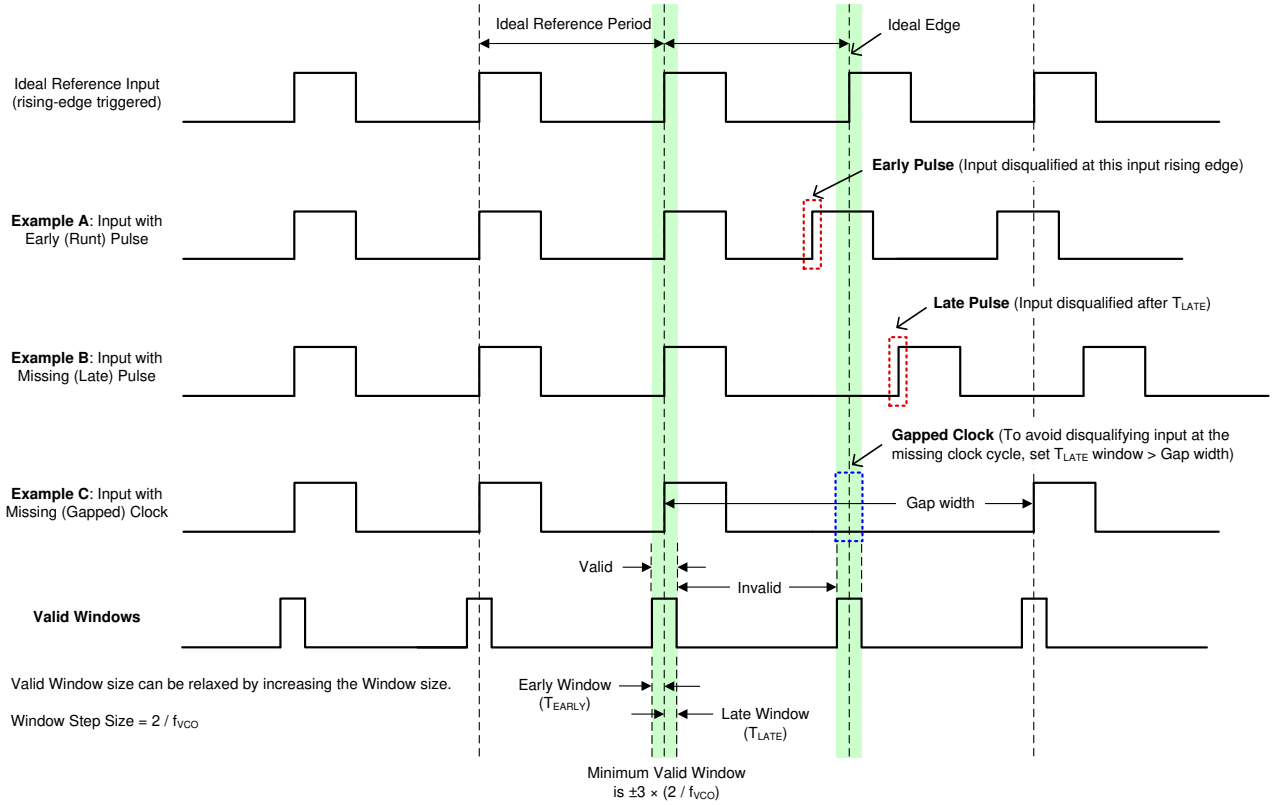

Figure 8-18. Early and Late Window Detector Examples

8.3.7.2.5 Phase Valid Monitor for 1PPS Inputs

The phase valid monitor is designed specifically for 1PPS input validation because the frequency and window detectors do not support this low frequency. The phase valid monitor uses a window detector to validate 1PPS input pulses that arrive within the nominal clock period (T_{IN}) plus a programmable jitter threshold (T_{JIT}). When the input pulse arrives within the counter window (T_V), the pulse is considered valid and the phase valid flag is cleared. When the input pulse does not arrive before T_V (due to a missing or late pulse), the flag is set immediately to disqualify the input. T_{JIT} must be set higher than the worst-case input cycle-to-cycle jitter.

The phase valid register settings also are valid for 1PPS ppm error threshold detect. Notice the T_{JIT} also impacts the worst case ppm error allowed. For example: High_Jitter_Freq = 1/(T_{IN} - T_{JIT}), then Max input allowable ppm error = (High_Jitter_Freq - Expected_Freq) / Expected_Freq × 1e6.

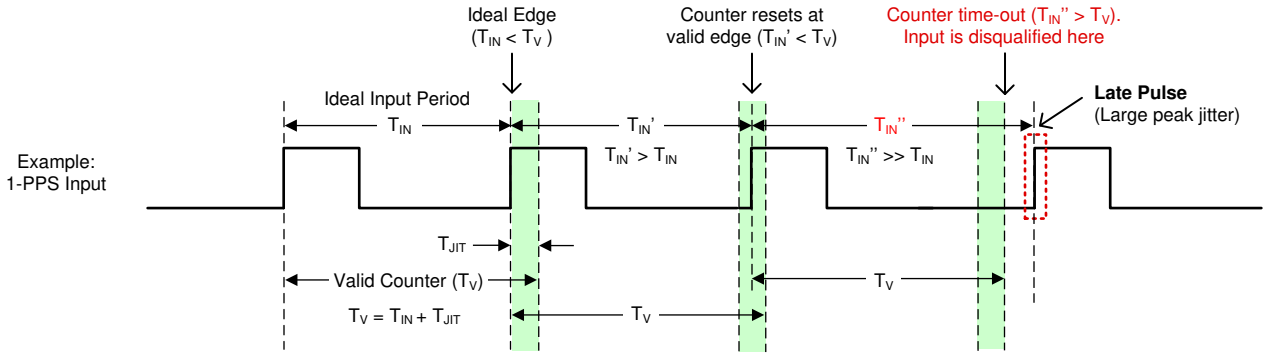

Figure 8-19. 1PPS Input Window Detector Example

8.3.7.3 PLL Lock Detectors

The loss-of-lock (LOL) status is available for each APLL and DPLL. The APLLs are monitored for loss-of-frequency lock only. The DPLL can be monitored for both loss-of-frequency lock (LOFL) and loss-of-phase lock (LOPL). The DPLL lock threshold and loss-of-lock threshold are programmable for both LOPL and LOFL detectors. If the BAW APLL loss-of-frequency lock is selected, then paired DPLL is monitored for LOPL only. The paired DPLL must be enabled for the digital monitoring of the BAW APLL VCBO lock detect.

The DPLL frequency lock detector clears the LOFL flag when the DPLL frequency error relative to the selected reference input is less than the lock ppm threshold. Otherwise, the lock detector sets the LOFL flag when the DPLL frequency error is greater than the unlock ppm threshold. The ppm delta between the lock and unlock thresholds provides hysteresis to prevent the LOFL flag from toggling when the DPLL frequency error is crossing these thresholds.

The BAW APLL frequency digital lock detector clears the LOFL flag when the VCBO frequency error relative to the XO reference input is less than the lock ppm threshold. Otherwise, the lock detector sets the LOFL flag when the VCBO frequency error is greater than the unlock ppm threshold. Make sure to take the ppm frequency tolerance of the XO input reference into account when setting the VCBO frequency lock and unlock thresholds. The ppm delta between the lock and unlock thresholds provides hysteresis to prevent the LOFL flag from toggling when the VCBO frequency error is crossing these thresholds.

A measurement accuracy (ppm) and averaging factor are used in computing the frequency lock detector register settings. A higher measurement accuracy (smaller ppm) or higher averaging factor increases the measurement delay to set or clear the LOFL flag. Higher averaging can be useful when locking to an input with high wander or when the PLL is configured with a narrow loop bandwidth. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

The DPLL phase lock detector clears the LOPL flag when the phase error of the DPLL is less than the phase lock threshold. Otherwise, the lock detector sets the LOPL flag when the phase error is greater than the phase unlock threshold.

Users can observe the APLL and DPLL lock detector flags through the status pins and the status bits.

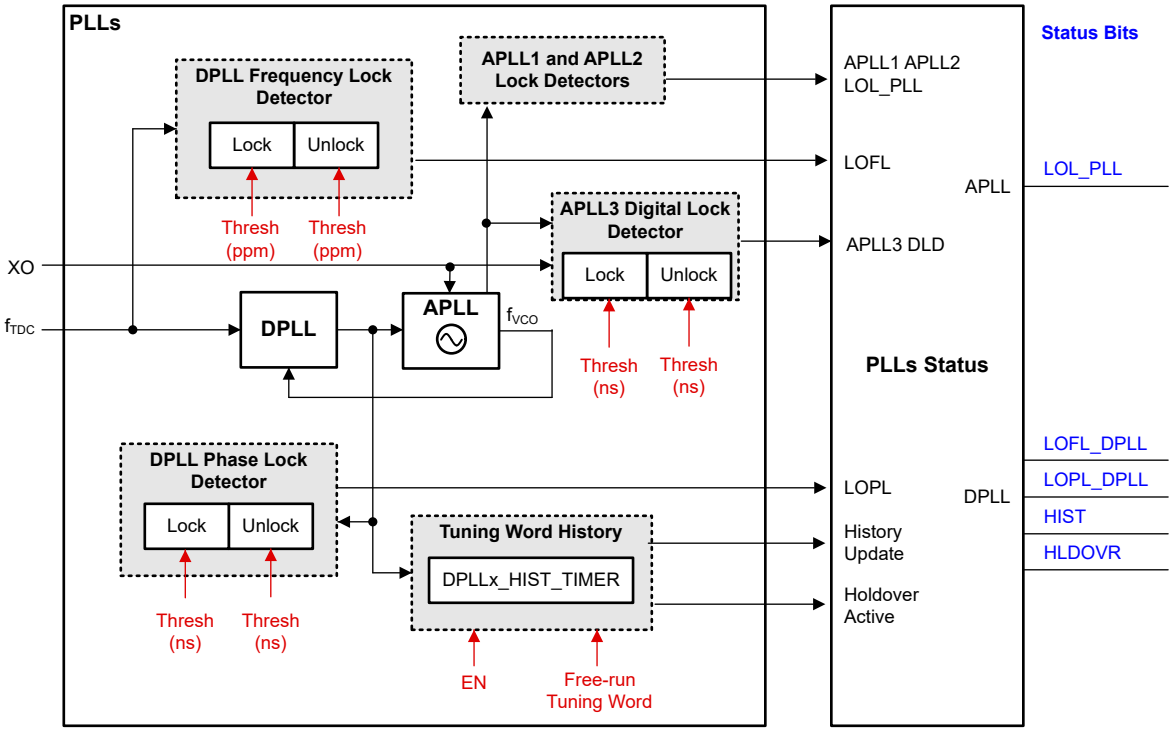

Figure 8-20. PLL Lock Detectors and History Monitor

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8.3.7.4 Tuning Word History

The DPLL domain has a tuning word history monitor block that determines the initial output frequency accuracy upon entry into holdover. When in holdover, the stability of the reference clock (on XO input) determines the long-term stability and accuracy of the output frequency. The tuning word can be updated from one of three sources depending on the DPLL operating mode:

1. Locked Mode: from the output of the digital loop filter when locked
2. Holdover Mode: from the final output of the history monitor
3. Free Run Mode: from the free-run tuning word register (user defined)

When the history monitor is enabled and the DPLL is locked, the device averages the reference input frequency by accumulating history from the digital loop filter output during a programmable averaging time (T_{AVG}) set by DPLLx_HIST_TIMER. When a valid reference input becomes invalid, the final tuning word value is stored to determine the initial holdover frequency accuracy. Generally, a longer T_{AVG} time produces a more accurate initial holdover frequency.

If the input reference clock fails and becomes invalid, the history data can be corrupted if the tuning word continues to update before the fail state is indicated by one of the reference input validation monitors. To avoid this scenario, any in progress accumulation is ignored and the recent history data is ignored. The most recent collected average data is discarded such that the actual history used is greater than T_{AVG} but less than 2 × T_{AVG}.

The tuning word history is initially cleared after a device hard reset or soft reset. After the DPLL locks to a new reference, the history monitor waits for the first T_{AVG} timer to expire before storing the first tuning word value and begins to accumulate history. The history monitor does not clear the previous history value during reference switchover or holdover exit. The history can be manually cleared or reset by toggling the history enable bit (DPLLx_HIST_EN = 1 → 0 → 1), if needed.

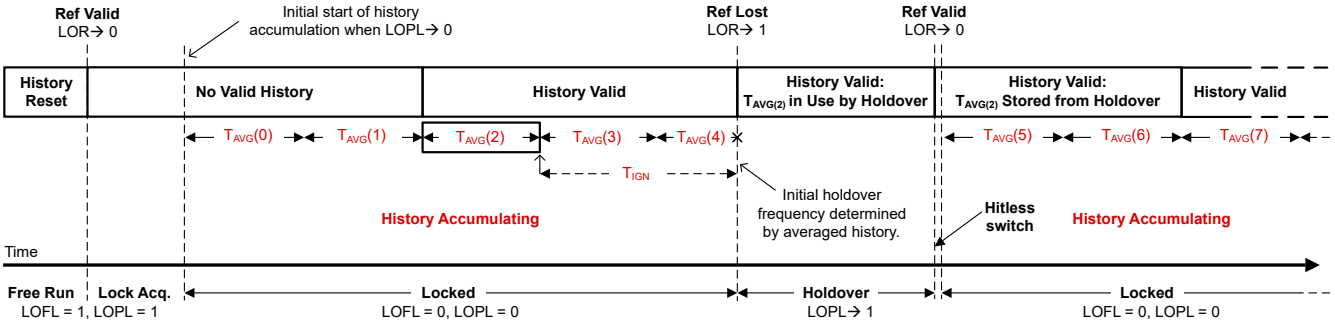

Figure 8-21. Tuning Word History Windows

When no tuning word history exists, the free-run tuning word value (DPLLx_FREE_RUN) is used and determines the initial holdover output frequency accuracy.

8.3.7.5 Status Outputs

The GPIO pins can be configured to output various status signals and interrupt flags for device diagnostic and debug purposes. The status signal, output driver type, and output polarity settings are programmable.

8.3.7.6 Interrupt

Any GPIO pin can be configured as a device interrupt output pin. The interrupt logic configuration is set through registers. When the interrupt logic is enabled, the interrupt output can be triggered from any combination of interrupt status indicators, including LOS for the XO, LOR for the selected DPLL input, LOL for APLL1, APLL2, and the DPLLs, and holdover and switchover events for the DPLLs. When the interrupt polarity is set high, a rising edge on the live status bit asserts the interrupt flag (sticky bit). Otherwise, when the polarity is set low, a falling edge on the live status bit asserts the interrupt flag. Any individual interrupt flag can be masked so the flag does not trigger the interrupt output. The unmasked interrupt flags are combined by the AND/OR gate to generate the interrupt output, which can be selected on either status pin.

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When a system host detects an interrupt from the device, the host can read the interrupt flag or *sticky* registers to identify which bits are asserted to resolve the fault conditions in the system. After the system faults have been resolved, the host can clear the interrupt output by writing 1 to the self-clearing INT_CLR field.

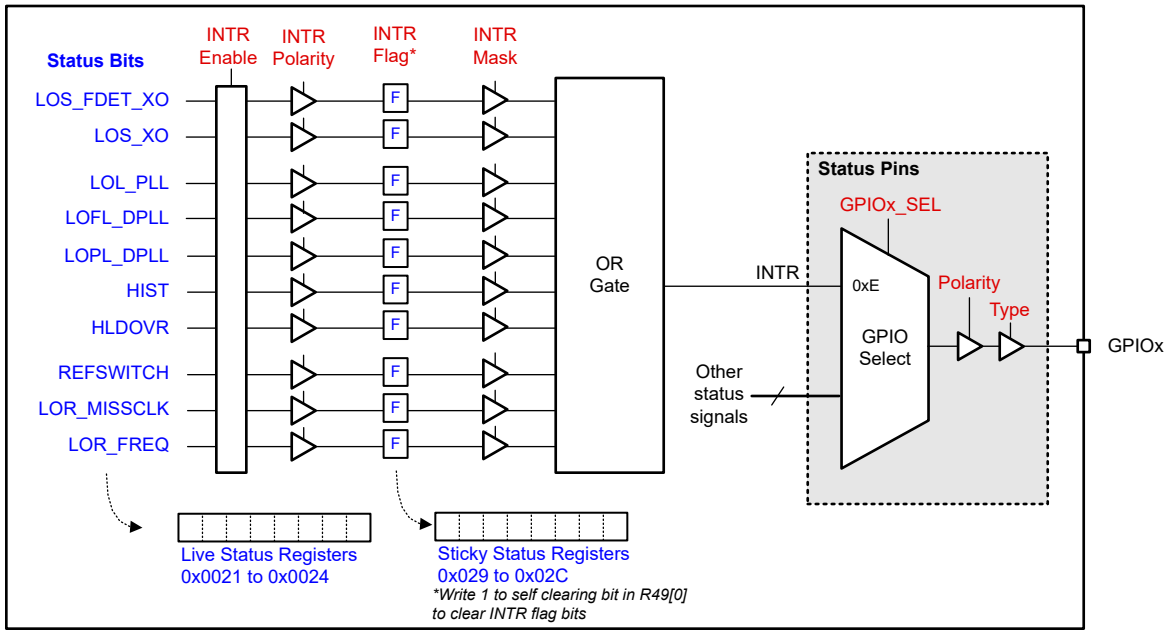

Figure 8-22. Status and Interrupt

8.3.8 PLL Relationships

Figure 8-23 shows the PLL architecture implemented in the LMK5C33414AS1. The PLLs can be configured in cascaded or independent modes as described in PLL Architecture Overview.

When a DPLL combines with an APLL in a feedback loop, the APLL must use the fixed 40-bit denominator. Select the 24-bit programmable denominator when the APLL is configured in an independent loop, like APLL1 and APLL2 in Figure 8-6 or all APLLs in Figure 8-7.

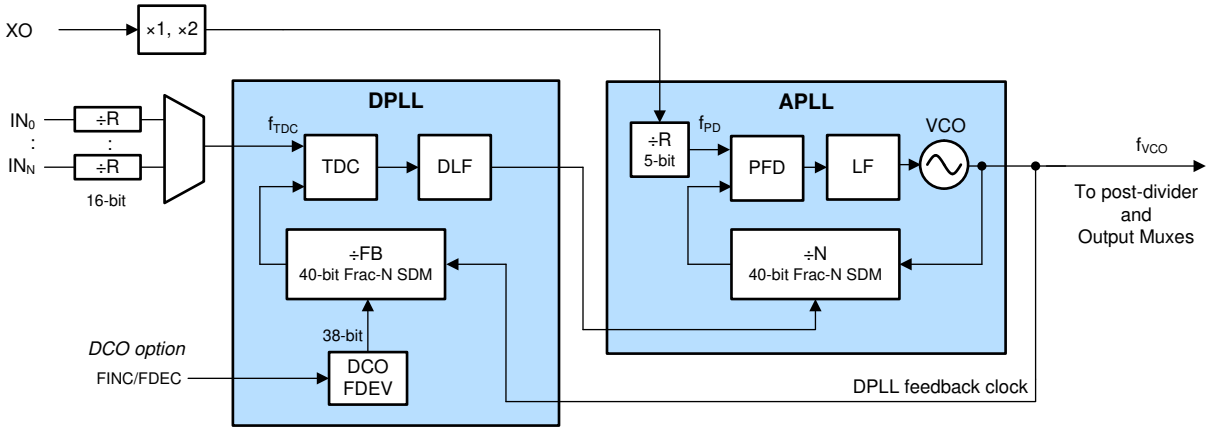

Figure 8-23. PLL Architecture

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8.3.8.1 PLL Frequency Relationships

The following equations provide the APLL and DLL frequency relationships required to achieve closed-loop operation. The TICS Pro programming software can be used to generate valid divider settings based on the desired frequency plan.

Note that any divider in the following equations refers to the actual divide value (or range) and not the programmable register value.

When DPLL operation is enabled, the calculated DPLL frequency and APLL frequency must be nominally the same. The DPLL adjustments to the paired APLL N divider 40-bit fixed denominator tracks the selected input reference source to synthesize the actual clock output desired frequency and phase.

When the APLL operates independently from the paired DPLL, TI recommends the programmable 24-bit denominator for hybrid synchronization or cascading between frequency domains to maintain 0ppm frequency error without DPLL control. In this scenario, the APLL tracks the cascade feedback divider reference from another APLL output.

When using ZDM for a PLL, the clock output divider must be accounted for in the VCO frequency calculations.

8.3.8.1.1 APLL Phase Frequency Detector (PFD) and Charge Pump

Equation 1 calculates the phase detector frequency which is used to find the VCO frequency in the APLL VCO Frequency calculation in Equation 2.

$$f_{PD} = f_{XO} \times D_{XO} / R_{XO} \quad (1)$$

where

- f_{PD} = APLL phase detector frequency
- f_{XO}: APLL reference is XO frequency or cascaded reference frequency from another APLL.
- D_{XO}: XO input doubler (1 = disabled, 2 = enabled)
- R_{XO}: APLL XO Input R divider value (1 to 32)

APLL2 or the BAW APLL has programmable charge pump settings from 0mA to 5.8mA in 0.4mA steps. Best performance from the BAW APLL is achieved with a charge pump currents of 0.8mA or higher. APLL1 has programmable charge pump settings of 1.6, 3.2, 4.8, or 6.4mA.

8.3.8.1.2 APLL VCO Frequency

The APLL phase locks the APLL VCO to the APLL reference using the applied APLL numerator. Use Equation 2 to calculate the VCO frequency.

$$f_{VCO} = f_{PD} \times (INT_{APLL} + NUM_{APLL} / DEN_{APLL}) \quad (2)$$

- f_{VCO}: VCO frequency
- f_{PD} = APLL phase detector frequency
- INT_{APLL}: APLL N divider integer value (12 bits, 1 to $2^{12} – 1$)
- NUM_{APLL}: APLL N divider numerator value (40 bits, 0 to $2^{40} – 1$, or 24 bits, 0 to $2^{24} – 1$)
- DEN_{APLL}: APLL N divider denominator value (fixed 2^{40}, or programmable 1 to 2^{24})
  - Avoid integer boundary spurs by keeping the NUM/DEN ratio away from an integer value.
  - $0.125 < NUM_{APLL} / DEN_{APLL} < 0.875$ (In DPLL Mode, avoid 0.5)

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8.3.8.1.3 DPLL TDC Frequency

Equation 3 calculates the TDC frequency which is used to find the VCO frequency in the DPLL VCO Frequency calculation in Equation 5. Two different TDC frequencies are possible for each DPLL to enable switching between non-integer related frequencies while keeping the TDC rate high.

$$f_{TDC} = f_{INx} \times D_{INx} / R_{INx} \quad (3)$$

$$f_{TDC} = f_{INy} \times D_{INy} / R_{INy} \quad (4)$$

where

- f_{TDC}: DPLL TDC input frequency (see Equation 3)
- f_{INx} or f_{INy}: INx or INy input frequency or cascaded reference frequency from another APLL.
- R_{INx} or R_{INy}: INx or INy R divider value (16 bits, 1 to $2^{16} – 1$)
- D_{INx} or D_{INy}: INx or INy input doubler (2 = disabled and 1 = enabled)

8.3.8.1.4 DPLL VCO Frequency

The DPLL phase locks the APLL VCO to the DPLL VCO frequency by updating the actual APLL numerator value. Use Equation 5 to calculate the VCO frequency. Each DPLL can have two different values for DPLL N to allow locking to the same VCO frequency using two different TDC frequencies. DPLLx_REF#_FB_SEL register selects which DPLL N value is used.

$$f_{VCO} = f_{TDC} \times (INT_{DPLL} + NUM_{DPLL} / DEN_{DPLL}) \quad (5)$$

where

- INT_{DPLL}: DPLL FB divider integer value (33 bits, 1 to $2^{33} – 1$)
- NUM_{DPLL}: DPLL FB divider numerator value (40 bits, 0 to $2^{40} – 1$)
- DEN_{DPLL}: DPLL FB divider denominator value (40 bits, 1 to 2^{40})
- N: $INT_{DPLL} + NUM_{DPLL} / DEN_{DPLL}$

8.3.8.1.5 Clock Output Frequency

Each APLL has a post divider which provides a VCO post divider frequency calculated in Equation 6, Equation 7, or Equation 8. The final output frequency is calculated by dividing from the VCO post divider frequency and the output divide (see Equation 9). For each output, the output frequency depends on the selected APLL clock source and output divider value.

APLL1 selected: $f_{POST_DIV} = f_{VCO1} / Pn_{APLL1}$ (6)

APLL2 selected: $f_{POST_DIV} = f_{VCO2} / P1_{APLL2}$ (7)

BAW APLL selected: $f_{POST_DIV} = f_{VCBO} / P1_{APLL3}$ (8)

OUTx: $f_{OUTx} = f_{POST_DIV} / OD_{OUTx}$ (9)

where

- f_{POST_DIV}: Output mux source frequency (APLL1, APLL2 or BAW APLL post-divider clock)
- Pn_{APLL1}: APLL1 primary P1 or secondary P2 post-divide value (2 to 7)
- $P1_{APLL2}$: APLL2 primary P1 post-divide value (2 to 13)
- $P1_{APLL3}$: APLL3 (BAW) post-divide value = div8 (2 to 8) , div8 times 2 (10, 12, 14, 16) , or bypass (1)
- f_{OUTx}: Output clock frequency (x = 0 to 15)
- OD_{OUTx}: OUTx output bypass or divider value. All outputs have a 12-bit divider with values 1 to $(2^{12} – 1)$. All outputs (except OUT2 and OUT3) have the option to follow the 12-bit divider with a 20-bit SYSREF divider that can be used to produce 1PPS or other frequencies below 1Hz when the SYSREF output is set for continuous output.

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8.3.8.2 Analog PLLs (APLL1, APLL2, APLL3)

Each APLL has a 40-bit fractional-N divider to support high-resolution frequency synthesis and very low phase noise and jitter. Each APLL also has the ability to tune the VCO frequency through sigma-delta modulator (SDM) control in DPLL mode. In cascaded mode, each APLL has the ability to lock the VCO frequency to another VCO frequency.

In free-run mode, the BAW APLL uses the XO input as an initial reference clock to the VCBO. The PFD of the BAW APLL compares the fractional-N divided clock with the reference clock and generates a control signal. The control signal is filtered by the BAW APLL loop filter to generate a control voltage to set the VCBO output frequency. The SDM modulates the N divider ratio to get the desired fractional ratio between the PFD input and the VCBO output. The other conventional APLL with the LC VCO operates similar to the VCBO. User can select the reference from either the VCBO clock or the XO clock.

In DPLL mode, the APLL fractional SDM is controlled by the DPLL loop to pull the VCO frequency into lock with the DPLL reference input. For example, Figure 8-6 shows how the APLL1 or APLL2 can derive the references from the VCBO if the respective DPLL1 or DPLL2 are disabled. The VCO1 or VCO2 is then effectively locked to the DPLL3 reference input, assuming there is no synthesis error introduced by the fractional N divide ratio of APLL1 or APLL2.

8.3.8.3 APLL Reference Paths

8.3.8.3.1 APLL XO Doubler

The APLL XO doubler can be enabled to double the PFD frequency for the APLL reference. Enabling the XO doubler adds minimal noise and can be useful to increase the PFD frequency to optimize phase noise, jitter, and fractional spurs. The flat portion of the APLL phase noise can improve when the PFD frequency is increased.

8.3.8.3.2 APLL XO Reference (R) Divider

Each APLL has a 5-bit XO reference (R) divider that can be used to meet the maximum APLL PFD frequency specification. The divider can also be used to verify the APLL fractional-N divide ratio (NUM/DEN) is between 0.125 to 0.875 (avoid 0.5), which is recommended to support the DPLL frequency tuning range. Otherwise, the R divider can be bypassed (divide by 1).

8.3.8.4 APLL Feedback Divider Paths

The VCO output of each APLL is fed back to the PFD block through the fractional feedback (N) divider. The VCO output is also fed back to the DPLL feedback path in DPLL mode. For hybrid synchronization or cascaded frequency domain architectures each VCO output also can source to the DPLL input reference selection muxes or as an XO input for other APLLs or through fixed feedback dividers.

8.3.8.4.1 APLL N Divider With Sigma-Delta Modulator (SDM)

The APLL fractional N divider includes a 12-bit integer portion (INT), a 40-b numerator portion (NUM), a fixed 40-bit or a programmable 24-bit denominator portion (DEN), and an SDM. The INT and NUM are programmable. When an APLL works with a DPLL in a loop, the APLL uses a fixed 40-bit denominator for very high frequency resolution on the VCO clock. When the APLL works in an independent loop (the paired DPLL is disabled), TI recommends a 24-bit programmable denominator. The total APLL N divider value is: N = INT + NUM / 2^{40} or INT + NUM / 2^{24} .

In APLL free-run mode, the PFD frequency and total N divider for the APLL determine the VCO frequency, which can be computed with 24-bit denominator by Equation 2.

8.3.8.5 APLL Loop Filters (LF1, LF2, LF3)

The APLL loop filter components can be programmed to optimize the APLL LBW depending on the phase noise of the XO input. The BAW APLL supports a programmable LBW from 100Hz to 10kHz (typical range) and the conventional LC APLL supports a programmable LBW from 100kHz to 1MHz (typical range). Figure 8-24 shows the APLL loop filter structure between the PFD/charge pump output and VCO control input.

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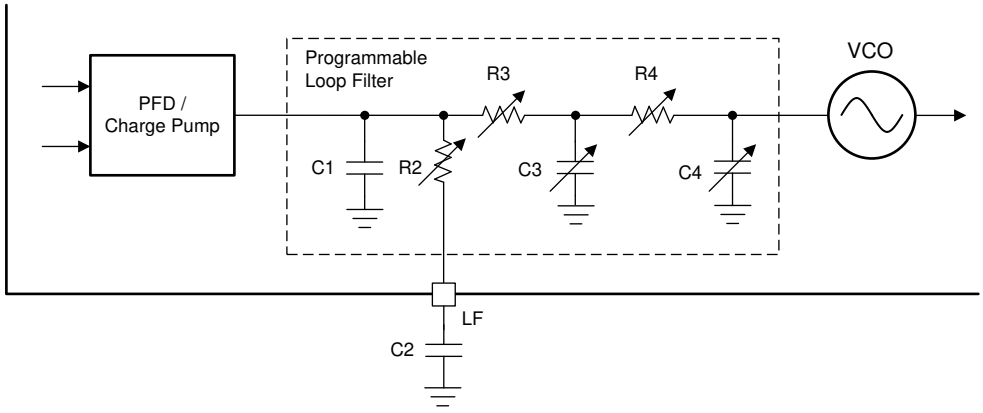

Figure 8-24. Loop Filter Structure of Each APLL

The BAW APLL is configured with a narrow LBW by default in TICSPRO and the ROM pages. As a result, the low jitter VCBO dominates the clock output phase noise in the carrier offset range from 8kHz to around 400kHz.

Using the default APLL loop filter settings listed in Table 8-3, the LBW for each APLL is summarized in Table 8-4.

Table 8-3. Default APLL Charge Pump and Loop Filter Components

COMPONENT	LOCATION	TYPE	DEFAULT VALUES FOR APLL1	DEFAULT VALUES FOR APLL2	DEFAULT VALUES FOR APLL3
Charge pump	Internal	Programmable	6.4mA	3.4mA	2.0mA
C1	Internal	Fixed	100pF	100pF	100pF
C2	External(1)	Fixed	100nF	100nF	470nF
C3	Internal	Programmable	70pF	70pF	70pF
C4	Internal	Programmable	70pF	70pF	70pF
R2	Internal	Programmable	0.222kΩ	0.183kΩ	0.301kΩ
R3	Internal	Programmable	0.657kΩ	0.657kΩ	5.5kΩ
R4	Internal	Programmable	0.657kΩ	0.657kΩ	5.5kΩ

(1) The external capacitor is connected to the LFx pin of the corresponding APLLx.

Table 8-4. Default APLL LBW (PFD = 96MHz)

APLL	VCO RANGE [MHz]	LBW [kHz](1)
1	4800 to 5350	282.5 to 291.8
2	5600 to 5950	152.8 to 137.8
3	2500	4.9

(1) The APLL LBW range corresponds to the VCO range, respectively.

8.3.8.6 APLL Voltage-Controlled Oscillators (VCO1, VCO2, VCO3)

Each APLL contains a fully-integrated VCO, which takes the voltage from the loop filter and converts the voltage into a frequency.

The VCBO (VCO3) uses proprietary BAW resonator technology with a very high quality factor to deliver the lowest phase jitter and has a tuning range of 2457.6MHz ± 100ppm. VCO2 uses a high-performance LC VCO with a wider tuning range of 5595MHz to 5950MHz to cover other additional unrelated clock frequencies, if needed. VCO1 uses a standard-performance LC VCO with a wider tuning range of 4800MHz to 5350MHz.

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8.3.8.6.1 VCO Calibration

Each APLL VCO must be calibrated to verify that the PLL can achieve lock and deliver optimal phase noise performance. VCO calibration establishes an optimal operating point within the VCO tuning range. VCO calibration is executed automatically during initial PLL start-up after device power-on, hard-reset, or soft-reset when the XO input is detected by the input monitor. To provide successful calibration and APLL lock, the XO clock must be stable in amplitude and frequency before the start of calibration; otherwise, the calibration can fail and prevent PLL lock and output clock start-up. Before VCO calibration and APLL lock, the output drivers are typically held in the mute state (configurable per output) to prevent spurious output clocks.

A VCO calibration can be triggered manually for a single APLL by toggling a PLL enable cycle (APLLx_EN bit = 0 → 1) through host programming. This can be needed after the APLL N divider value (VCO frequency) is changed dynamically through programming.

8.3.8.7 APLL VCO Clock Distribution Paths

Each APLL VCO post-divider supports an independently programmable divider.

The BAW APLL has one primary VCBO post-divider that is paired with an optional divide by 2. The VCBO post-divider clock div8 (÷2 to ÷8) or paired div8 and div2 (÷10, ÷12,÷14, ÷16) can be distributed to four of five output banks. If the system use case requires sourcing all five output banks and 16 outputs from the BAW APLL, then bypass the VCBO post-divider by setting VCBO post-divider = 1 and program the individual channel dividers to obtain the desired output frequencies.

APLL2 has one VCO post-divider clock (P1: ÷2 to ÷13) available for distribution to all outputs.

APLL1 has two VCO post-dividers. The primary VCO post-divider clock (P1: ÷2 to ÷7) is distributed for OUT0, OUT1, OUT2 and OUT3. The secondary APLL1 VCO post-divider clock (P2: ÷2 to ÷7) is distributed for OUT0 and OUT1.

8.3.8.8 DPLL Reference (R) Divider Paths

Each reference input clock has a dedicated 16-bit reference divider to the DPLL TDC block. The R divider output of the selected reference sets the TDC input frequency. To support hitless switching between inputs with different frequencies, the R dividers can be used to divide the clocks to a single common frequency to the DPLL TDC input.

8.3.8.9 DPLL Time-to-Digital Converter (TDC)

The TDC input compares the phase of the R divider clock of the selected reference input and the DPLL feedback divider clock from VCO. The TDC output generates a digital correction word corresponding to the phase error which is processed by the DPLL loop filter.

8.3.8.10 DPLL Loop Filter (DLF)

The DPLL supports a programmable loop bandwidth from 10mHz to 4kHz and can achieve jitter peaking below 0.1dB (typical). The low-pass jitter transfer characteristic of the DPLL attenuates the reference input noise with up to 60dB/decade roll-off above the loop bandwidth.

The DPLL loop filter output controls the fractional numerator of APLL to steer the VCO frequency into lock with the selected DPLL reference input.

8.3.8.11 DPLL Feedback (FB) Divider Path

The DPLL feedback path has a programmable prescaler (33 bits, 1 to $2^{33} – 1$) and a fractional feedback (FB) divider. The programmable DPLL FB divider includes a 33-bit integer portion (INT), 40-bit numerator portion (NUM), and 40-bit denominator portion (DEN). The total DPLL FB divider value is: FB_{DPLL} = INT + NUM / DEN.

In DPLL mode, the TDC frequency and total DPLL feedback divider and prescalers determine the VCO frequency. Refer to DPLL VCO Frequency for how to calculate the VCO frequency.

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8.3.9 Output Clock Distribution

The output clock distribution blocks include five output muxes, nine output dividers, and fourteen programmable differential output drivers in the LMK5C33414AS1.

The output dividers support output synchronization (SYNC) to allow phase synchronization between two or more output channels. OUT0, OUT4, and OUT10 have an optional internal ZDM synchronization feature to support deterministic input-to-output phase alignment (typically for 1PPS clocks) with programmable offset. See Section 8.3.20.

8.3.10 Output Source Muxes

The LMK5C33414AS1 employs 6 output source multiplexers or muxes (mux) to distribute frequency sources to the respective output banks. The 6:1 mux on OUT0 and OUT1 is the most flexible and provides selection among each APLL post divider, a buffered XO, or a buffered reference input as an output frequency source. The 3:1 muxes feeding the OUT2 and OUT3 bank can select a frequency source from the BAW APLL post divider, APLL2 post divider, and APLL1 primary post divider. The 2:1 muxes feeding the OUT4 to OUT13 bank can each select a frequency source from the BAW APLL post divider or the APLL2 post divider.

- OUT0 and OUT1 each have a separate 6:1 mux to individually select an output source. Select the same output source mux option for OUT0 and OUT1 to reduce crosstalk.
- OUT2 and OUT3 each have a separate 3:1 mux to individually select an output source. Select the same output source mux option for OUT2 and OUT3 to reduce crosstalk.
- OUT4 and OUT5 share a 2:1 mux to select an output source. Select the same output source mux option for OUT4, OUT5, OUT6, and OUT7 to reduce crosstalk.
- OUT6 and OUT7 share a 2:1 mux to select an output source. Select the same output source mux option for OUT4, OUT5, OUT6, and OUT7 to reduce crosstalk.
- OUT8 and OUT9 share a 2:1 mux to select an output source. Select the same output source mux option for OUT8, OUT9, OUT10, OUT11, OUT12, and OUT13 to reduce crosstalk.
- OUT10 and OUT11 share a 2:1 mux to select an output source. Select the same output source mux option for OUT8, OUT9, OUT10, OUT11, OUT12, and OUT13 to reduce crosstalk.
- OUT12 and OUT13 share a 2:1 mux to select an output source. Select the same output source mux option for OUT8, OUT9, OUT10, OUT11, OUT12, and OUT13 to reduce crosstalk.

Table 8-5 lists the available options for the output source mux.

Table 8-5. Output Source Mux Options

OUTPUT SOURCE MUX OPTION	OUTPUTS WITH OPTION	DESCRIPTION
REFx	OUT0, OUT1	Output channel mux is sourced from the selected reference input when R48[4:0] is configured and R78[5] is set. R48[4:0] = 0x0 for none, 0x1 for REF0, 0x2 for REF1, 0x4 for REF2, 0x8 for REF3
XO	OUT0, OUT1	Output channel mux is sourced from the XO input.
APLL1 PRI	OUT0, OUT1, OUT2, OUT3	Output channel mux is sourced from the APLL1 primary post-divider output.
APLL1 SEC	OUT0, OUT1	Output channel mux is sourced from the APLL1 secondary post-divider output.
APLL2	All OUTx	Output channel mux is sourced from the APLL2 post-divider output.
APLL3 (BAW)	All OUTx	Output channel mux is sourced from the BAW APLL post-divider output.

8.3.11 Output Channel Muxes

Each output clock is sourced from the output channel mux which stem from the output source muxes. Table 8-6 lists the available options for the output channel mux.

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Table 8-6. Output Channel Mux Options

OUTPUT CHANNEL MUX OPTION	DESCRIPTION
Bypass	Output clock is sourced directly from the APLL post-divider; the output channel divider is bypassed.
CHDIV	Output clock is sourced from the output channel divider.
CH / 2	Output clock is sourced from a divide by 2 channel.
SYSREF	Output clock is sourced from the SYSREF divider.
SYSREF + ADLY	Output clock is sourced from the SYSREF divider with analog delay.
Static DC	Output clock is static: OUTP is LOW and OUTN is HIGH. **Note**: The Static DC mux setting is different from the output enable bit (OUTx_EN) setting. When the output is disabled (OUTx_EN = 0), the output channel is tristated, high impedance, or Hi-Z.

8.3.12 Output Dividers (OD)

There are one or more output dividers after each output source mux.

Each channel in OUT[2:3] has an individual 12-bit channel divider. The OUT[4:5], OUT[6:7], OUT[8:9], OUT[10:11], and OUT[12:13] channels each have an individual 12-bit output divider cascaded with an optional 20-bit SYSREF divider. The output dividers are used to generate the final clock output frequency from the source selected by the output mux.

The OUT0 or OUT1 channel combines a 12-bit output channel divider (CD) and a 20-bit SYSREF divider to support output frequencies from 1Hz (1PPS) to 1250MHz. From VCO to output, the total divide value is the product of the PLL post-divider (P), output channel divider (CD)and SYSREF divider (SD) values (P × CD × SD).

For example, with the BAW APLL post-divider bypassed each 12-bit channel divider (CD) supports output frequencies from 100kHz to 1250MHz (or up to the maximum frequency supported by the configured output driver type). The SYSREF divider (SD) can be cascaded down to achieve lower clock frequencies down to 1Hz (1PPS).

Each output divider is powered from the same VDDO_x supply used for the clock output drivers. The output divider can be powered down if not used to save power. For each output group, the output divider is automatically powered down when both output drivers are disabled. For the OUT0 or OUT1 channels, the output divider is automatically powered down when the output driver is disabled.

8.3.13 SYSREF/1PPS Output

The LMK5C33414AS1 can support system reference clocks from 1PPS to 25MHz including JEDEC JESD204B or JESD204C SYSREF clocks. Any 12-bit output channel divider (except OUT2 and OUT3) can be cascaded with an individual 20-bit SYSREF divider. Set flexible SYSREF divider values to generate the same SYSREF/1PPS frequency on multiple outputs or different frequency multiples of SYSREF/1PPS based on application requirements. When aligning multiple SYSREF outputs, set SYSREF_REQ_MODE 0x1A[5:4] = 11 for resampling of the SYSREF request. The SYSREF/1PPS can also be replicated on GPIO1 or GPIO2 if additional single ended outputs are needed. The SYSREF request sample source SYSREF_REQ_SEL 0x1A[3:2] must be set to the same source as desired for SYSREF/1PPS output replication.

The SYSREF divider output signals can be replicated on either GPIO1 and GPIO2 to provide additional single ended 3.3V CMOS clocks after start-up if desired. To configure the SYSREF/1PPS output replication the GPIO must be enabled as an output (GPIOx_OUTEN = 1) and one of the SYSREF output to GPIO replication sources must be active. The SYSREF replication source comes from any one of the enabled SYSREF dividers used by or OUT12/13 by register programming (OUT_x_y_SR_GPIO_EN = 1). The GPIOx replicated SYSREF output is after static digital delay but before the analog and digital delay and pulser. The output is a continuous frequency as pulsed SYSREF mode is not supported for the GPIOx replica.

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There is some small fixed delay skew between the normal SYSREF and GPIO replicated SYSREF. An LVCMOS output clock is an unbalanced signal with large voltage swing; therefore, the signal can strongly interfere and couple noise onto other jitter-sensitive differential output clocks.

8.3.14 Output Delay

The LMK5C33414AS1 has the ability to tune output clock phase with delay function. In each channel divider path, there is a programmable static offset digital delay. With the SYSREF divider selected, the output clock can have additional programmable static offset digital delay, SYSREF digital delay and analog delay.

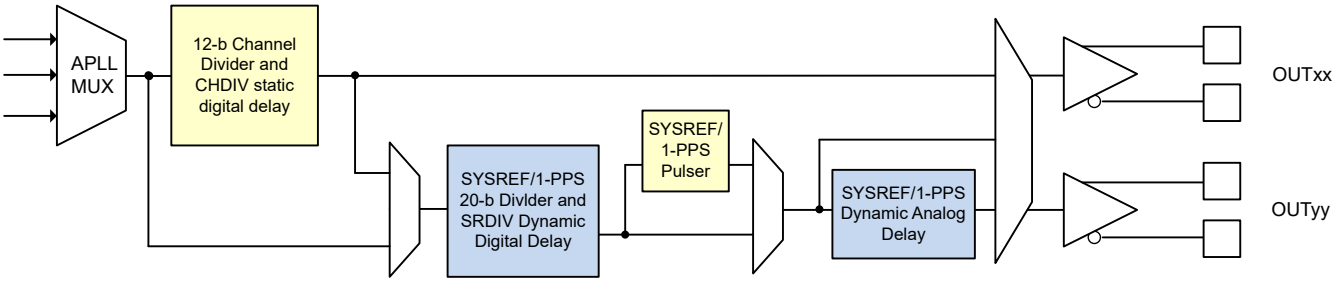

Figure 8-25. Programmable Static and Dynamic Output Delay

8.3.15 Clock Output Drivers

Each clock output (OUTx_P and OUTx_N) can be individually configured as a Differential Output driver. OUT0 or OUT1 has the additional capability for two 1.8V or 2.65V LVCMOS Output drivers per output pair. For additional low frequency single-ended clock outputs, GPIO1 and GPIO2 can be configured to replicate any SYSREF/1PPS Output divider output from another differential output pair.

Each output channel has a dedicated internal LDO regulator to provide excellent PSNR and minimize jitter and spurs induced by supply noise. For differential modes, the output clock specifications (such as output swing, phase noise, and jitter) are not sensitive to the VDDO_x voltage because of the internal LDO regulator of the channel.

The OUT0 and OUT1 channels (mux, divider, and drivers) are powered through a single output supply pin (VDDO_0_1). Similarly, OUT2 and OUT3 channels are powered by VDDO_2_3, OUT4 to OUT7 channels by VDDO_4_TO_7, and OUT8 to OUT13 channels by VDDO_8_TO_13. Each output supply pin must always be powered by 3.3V even if the respective outputs are not used.

Unused clock outputs can be disabled to save power.

8.3.15.1 Differential Output

The differential HSDS driver has programmable single-ended peak-to-peak amplitude (V_{OD}) and common-mode voltage (V_{CM}) settings. The V_{OD} ranges from 0.4V to 1V with a step size of roughly 100mV. There are three V_{CM} options available: S1, S2, S3, and S2 + S3. The HSDS driver can be AC-coupled for AC-LVPECL output clocks or other differential outputs. If there is an available V_{CM} setting that meets the receiver requirements, then the HSDS driver can be DC-coupled, such as for LVDS outputs.

The traditional HCSL output driver is PCIe compliant and requires 50Ω external termination. TI recommends placing the termination close to the receiver side.

Refer to Table 8-7 for the recommended differential output options and the Electrical Characteristics for the voltage variation of the V_{OD} and V_{CM}.

Table 8-7. Differential Output Options

DIFFERENTIAL DRIVER TYPE	V_{OD}, TYP [mV] REGISTER SETTING	V_{CM}, TYP [mV]	V_{CM} REGISTER SETTING
HSDS	400	350	S1
HSDS	400	700	S2
HSDS (LVDS)	400	1250	S3

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Table 8-7. Differential Output Options (continued)

DIFFERENTIAL DRIVER TYPE	V_{OD}, TYP [mV] REGISTER SETTING	V_{CM}, TYP [mV]	V_{CM} REGISTER SETTING
HSDS	500	400	S1
HSDS	600	450	S1
HSDS	600	800	S2 + S3
HSDS	700	500	S1
HSDS	700	900	S2 + S3
HSDS (AC-LVPECL)	800	550	S1
HSDS (AC-LVPECL)	800	1000	S2 + S3
HSDS (AC-LVPECL)	900	600	S1
HSDS (AC-LVPECL)	1000	650	S1
HCSL	750	350	N/A

8.3.15.2 LVCMOS Output

OUT0 and OUT1 have the additional capability for two 1.8V or 2.65V LVCMOS drivers per P and N output pair. Each LVCMOS output can be configured for normal polarity, inverted polarity, or disabled as Hi-Z or static low level. The LVCMOS output high level (V_{OH}) is determined by the internal programmable LDO regulator voltage of 1.8V or 2.65V for rail-to-rail LVCMOS output voltage swing.

LVCMOS mode is recommended for ASIC or processor clocks which do not have stringent phase noise or jitter requirements. An LVCMOS output clock is an unbalanced signal with large voltage swing, therefore the clock can be a strong aggressor and couple noise onto other jitter-sensitive differential output clocks. If an LVCMOS clock is required from an output pair, configure the pair with both outputs enabled but with opposite polarity (+/– or –/+) and leave the unused output floating with no trace connected.

8.3.16 Clock Output Interfacing and Termination

This section shows the recommended output termination. Unused clock outputs can be left floating and powered down by programming.

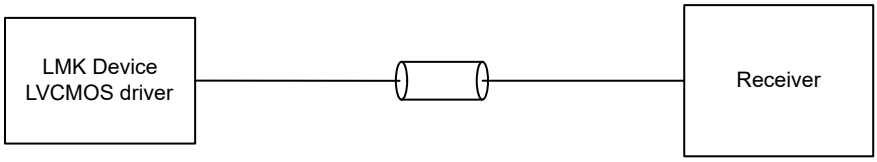

Figure 8-26. LVCMOS Output Termination

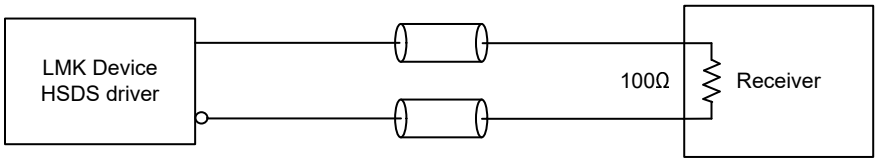

Figure 8-27. DC-Coupled HSDS/LVDS Output Termination

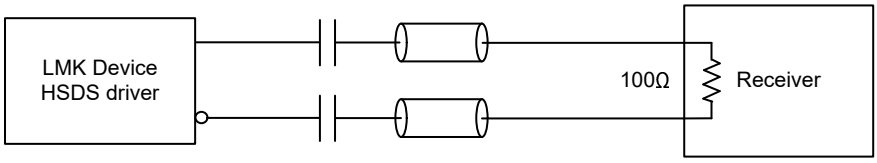

Figure 8-28. AC-Coupled HSDS Output Termination Method 1

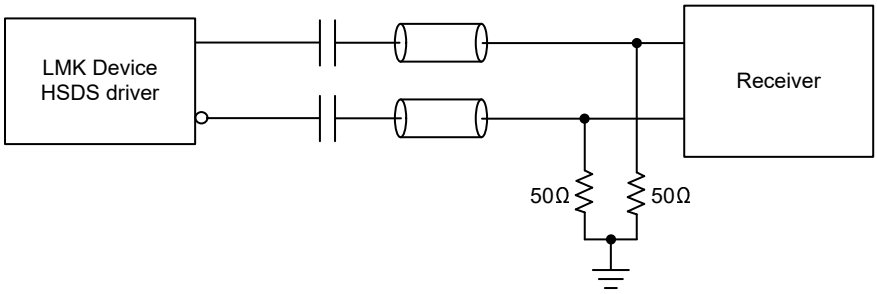

Figure 8-29. AC-Coupled HSDS Output Termination Method 2

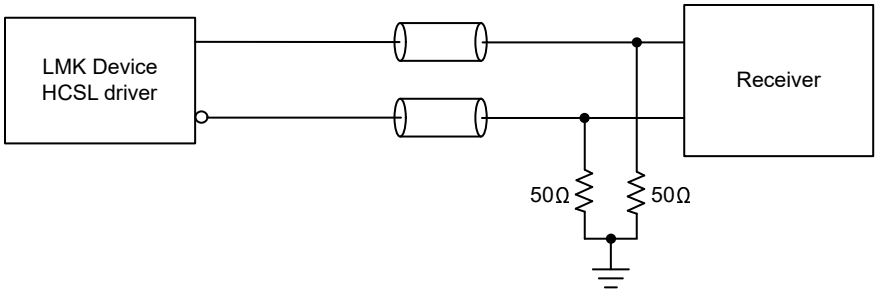

Figure 8-30. DC-Coupled HCSL Output Termination

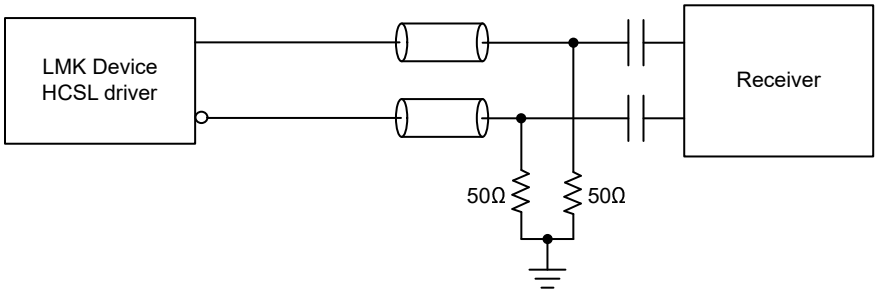

Figure 8-31. AC-Coupled HCSL Output Termination

8.3.17 Glitchless Output Clock Start-Up

When APLL auto-mute is enabled, the outputs starts up in synchronous fashion without clock glitches once APLL lock is achieved after any the following events: device power-on, exiting hard-reset, exiting soft-reset, or deasserting output SYNC.

8.3.18 Output Auto-Mute During LOL

Each output driver can automatically mute the clock when the selected output mux clock source is invalid, as configured by the MUTE enable field. The source can be invalid based on the LOL status of each PLL by configuring the APLL and DPLL mute control bits (MUTE_APLLx_LOCK, MUTE_DPLLx_LOCK, MUTE_DPLLx_PHLOCK). When auto-mute is disabled or bypassed (OUT_x_y_MUTE_EN = 0), the output clock can have incorrect frequency or be unstable before and during the VCO calibration.

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8.3.19 Output Synchronization (SYNC)

Output SYNC can be used to phase-align two or more output clocks with a common rising edge by allowing the output dividers to exit reset on the same PLL output clock cycle. Any output dividers selecting the same PLL output can be synchronized together as a SYNC group by triggering a SYNC event through the hardware pin or software bit.

The following requirements must be met to establish a SYNC group for two or more output channels:

- Output dividers have the respective sync enable bit set (OUT_x_y_DIV_SYNC_EN = 1)
- SYSREF dividers have the additional respective sync enable bit set (OUT_x_y_SR_DIV_SYNC_EN = 1), work with above set (OUT_x_y_DIV_SYNC_EN = 1)
- Output dividers have the output mux selecting the same PLL output
- The PLL (post-divider) output has the sync enable bit set (for example, PLL1_PRI_DIV_SYNC_EN = 1)
- SYNC_EN = 1

A SYNC event can be asserted by either a GPIOx pin programmed for SYNC input with GPIOx_MODE = 31 or the SYNC_SW register bit (active high). When SYNC is asserted, the SYNC-enabled dividers are held in reset and clock outputs are low. When SYNC is deasserted, the outputs from a common PLL starts with the initial clock phases synchronized or aligned. SYNC can also be used to set a low state on any SYNC-enabled outputs to prevent output clocks from being distributed to downstream devices until the receiver inputs are configured and ready to accept the incoming clock.

Output channels with the sync disabled (OUT_x_y_DIV_SYNC_EN = 0) is not affected by a SYNC event and continues normal output operation as configured. VCO post-divider clocks must be enabled for synchronization to verify that the driven dividers are synchronized accurately. However, any output deriving a clock from a reset VCO post-divider is not valid during SYNC, even if the channel divider is not selected for SYNC. VCO post-dividers not selected for synchronization do not stop running during the SYNC so the post-dividers can continue to source output channels that do not require synchronization. Output dividers with divide-by-1 (divider bypass mode) are not gated during the SYNC event.

Table 8-8. Output Synchronization

GPIOx as SYNC PIN GPIOx_MODE = 31		SYNC_SW R21[6]	OUTPUT DIVIDER AND DRIVER STATE
GPIOx_POL = 0	GPIOx_POL = 1		
1	0	1	Output drivers muted and output dividers reset
1 → 0	0 → 1	1 → 0	SYNCed outputs are released with synchronized phase
0	1	0	Normal output driver/divider operation as configured

8.3.20 Zero-Delay Mode (ZDM)

The DPLL supports an internal ZDM synchronization option to achieve a known and deterministic phase relationship between the selected DPLL reference input and OUT0, OUT4, or OUT10 clock depending on configuration and selected DPLL for ZDM.

With ZDM enabled, users can attain *zero* phase delay between the selected DPLL reference input clock and the selected zero-delay feedback clock. Figure 8-32 shows how the OUT0 clock can internally feedback to any DPLL as the zero-delay output clock. ZDM is primarily implemented to achieve deterministic phase relationship between an input and selected outputs such as 1PPS input to 1PPS outputs or 156.25MHz input to 156.25MHz outputs.

There is no need to route external clock signals from output to input as the zero-delay feedback clock from OUT0 is routed internally to the device ; OUT4 can also be used for DPLL2 internal ZDM feedback and OUT10 can be used for DPLL3 internal ZDM feedback.

1PPS phase alignment is able to re-establish with the phase slew control and ZDM. The phase slew control can reduce the phase build-out back to 0 at a controlled rate. To lock to a 1PPS signal using ZDM mode, the output static delay or DPLLx_PH_OFFSET can be programmed to zero out the phase error between the 1PPS input and 1PPS feedback clock. Hitless switching must be disabled when ZDM is used for 1PPS.

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See DPLL Programmable Phase Delay for an example of how input to output phase error in the DPLLx_PH_OFFSET field is calculated to apply fine adjustments less than 1ps.

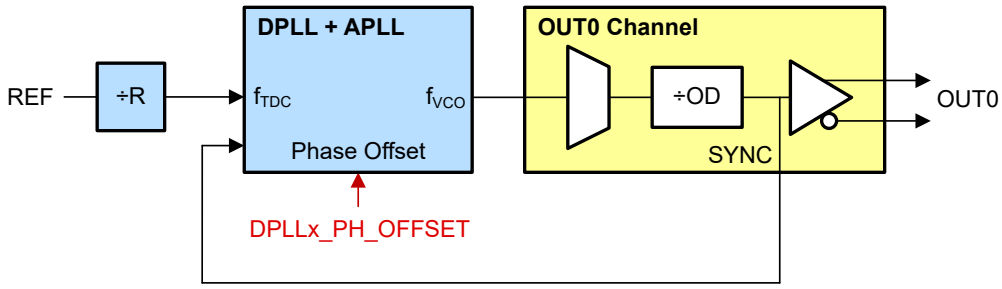

Figure 8-32. DPLL ZDM Synchronization Between Reference Input and OUT0

8.3.21 DPLL Programmable Phase Delay

Users can write to the DPLLx_PH_OFFSET[44:0] register fields to adjust the DPLL phase offset. The phase offset is a signed 2's complement value with a default setting of 0 and offsets the phase relationship of the feedback clock to reference clock at the TDC. The phase adjustment is common to all outputs derived from the DPLLx synchronization domain. DPLLx_PH_OFFSET adjustments occur in one direction. To shift in the negative direction, subtract the desired time offset from the period of the output clock to get the new phase offset.

Equation 10 and Equation 11 show the formulas to compute the DPLLx_PH_OFFSET field value to vary the output phase in fine adjustment steps. DPLLx_PH_OFFSET is related to the APLLx VCO period with a scaling factor for decimation and digital gain.

$$DPLLx_PH_OFFSET = 2 \times DESIRED_TIME_OFFSET \times f_{VCOx} \times SCALING_{DEC} \quad (10)$$

$$SCALING_{DEC} = DPLLx_PARAM_B \times (DPLLx_PARAM_C + 1) \times 2^{32 - DPLLx_PARAM_A} \quad (11)$$

where

- DPLLx_PH_OFFSET: Programmable register value adjusting DPLL output phase
- DESIRED_TIME_OFFSET: Desired DPLL phase adjustment (in seconds)
- f_{VCOx}: VCOx frequency
- $SCALING_{DEC}$: Scaling factor accounting for decimation and digital gain parameters
- DPLLx_PARAM_A/B/C: DPLL decimation and gain parameters. For DPLLx_PARAM_A, use a value of 32 in the equation if the register readback value is 0.

For example, if the user wants to introduce a phase offset of +1ns into a DPLL/APLL with a 2500MHz VCO, then use the following settings:

- DESIRED_TIME_OFFSET = +1ns
- f_{VCOx}: = 2500MHz
- $SCALING_{DEC} = 584 \times (7 + 1) \times 2^{32 - 32} = 4672$
- DPLLx_PH_OFFSET = 2 × 1e-9 × 2500e6 × 4672 = 23360

Alternatively, to apply a phase shift in the other direction, such as −1ns to a 25MHz output clock, use the following settings:

- DESIRED_TIME_OFFSET = 40ns - 1ns = 39ns
  - 40ns is the period of the output clock (25MHz).
- f_{VCOx}: = 2500MHz
- $SCALING_{DEC}$ = 4672
- DPLLx_PH_OFFSET = 2 × 39e-9 × 2500e6 × 4672 = 911040

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The DPLL parameters of a given configuration can be readback by accessing the registers listed in Table 8-9.

Table 8-9. DPLL Phase Offset Registers

FIELD NAME	REGISTER ADDRESS (HIGH BYTE TO LOW BYTE)
DPLL3_PH_OFFSET	R550, R551, R552, R553, R554, R555
DPLL3_PARAM_A	R567
DPLL3_PARAM_B	R548, R549
DPLL3_PARAM_C	R566
DPLL2_PH_OFFSET	R400, R401, R402, R403, R404, R405
DPLL2_PARAM_A	R417
DPLL2_PARAM_B	R398, R399
DPLL2_PARAM_C	R416
DPLL1_PH_OFFSET	R250, R251, R252, R253, R254, R255
DPLL1_PARAM_A	R267
DPLL1_PARAM_B	R248, R249
DPLL1_PARAM_C	R266

8.3.22 Time Elapsed Counter (TEC)

The Time Elapsed Counter (TEC) allows the user to make a precise time measurement between two (or more) events. The events can be either a rising or falling edge of a GPIO pin or a falling edge of the SPI SCS pin. Any GPIO pin can be programmed for TEC input. Rising or falling polarity can be selected using the GPIO polarity invert register. After each TEC event, the counter values is captured and the application can read back a 40-bit value. The elapsed time is calculated based on the difference in the read back values. The accuracy of the measurement is better than 7.5ns with a total measurement time over 59 minutes depending on exact configuration. Reading back at least the LSB of the TEC_CNTR to re-arm the TEC counter capture.

The TEC counter is clocked at a frequency based on PLL3 VCO frequency ÷8 or PLL2 VCO frequency ÷ 20. A time measurement is made by below steps.

1. Reset the TEC counter value. Recommended to reduce chance of counter roll-over between TEC capture events, but optional. If the reset is not done the user needs to detect roll-over of counter register which complicates Equation 12 for elapsed time calculation.
2. Trigger TEC capture event and read back the TEC registers containing the stored counter value.
3. Trigger the TEC capture event a second time and read back the TEC registers containing the stored counter value.
4. Use Equation 12 to calculate the elapsed time. The worst-case error is twice the TEC counter clock period. Table 8-10 lists some common TEC clock frequencies/periods and roll-over times.

$$\text{Elapsed Time} = (\text{2nd captured TEC value} - \text{1st captured TEC value}) / \text{TEC Clock Rate} \quad (12)$$

The TEC_CNTR register is split across five registers.

Table 8-10. Common TEC Clock Frequencies and Roll-Over Times

PLL SOURCE	VCO FREQUENCY	TEC CLOCK FREQUENCY	TEC CLOCK PERIOD (t)	ROLL-OVER TIME
PLL3	2457.6MHz	307.2MHz	Approximately 3.225ns	Approximately 59.6 minutes
PLL2	5950MHz	297.5MHz	Approximately 3.361ns	Approximately 61.6 minutes
PLL2	5898.24MHz	294.912MHz	Approximately 3.391ns	Approximately 62.1 minutes
PLL2	5625MHz	281.25MHz	Approximately 3.556ns	Approximately 65.1 minutes

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Table 8-10. Common TEC Clock Frequencies and Roll-Over Times (continued)

PLL SOURCE	VCO FREQUENCY	TEC CLOCK FREQUENCY	TEC CLOCK PERIOD (t)	ROLL-OVER TIME
PLL2	5600MHz	280MHz	Approximately 3.571ns	Approximately 65.4 minutes

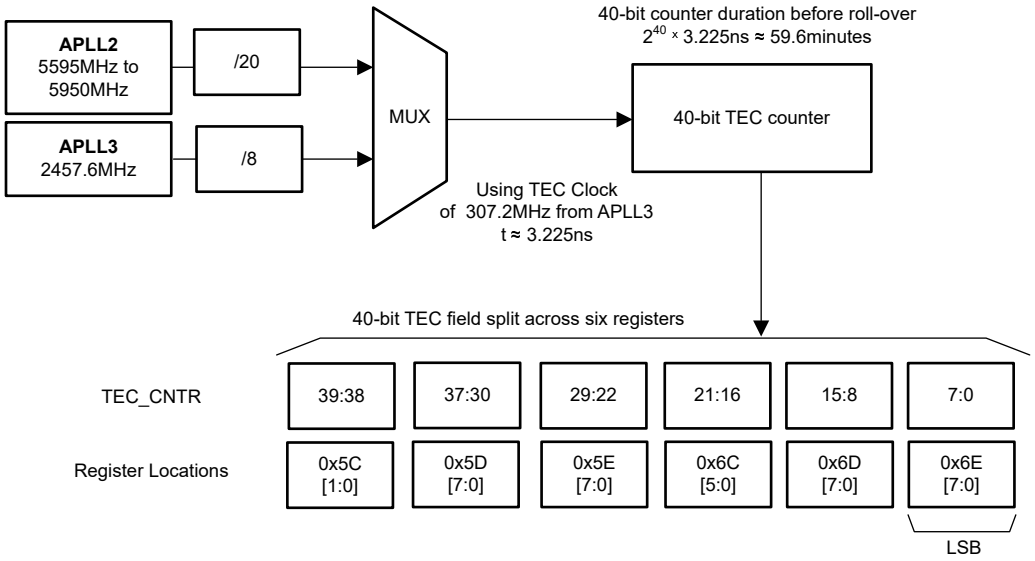

Figure 8-33. TEC Clock and Counter

Figure 8-34 illustrates the states of the Time Elapsed Counter function.

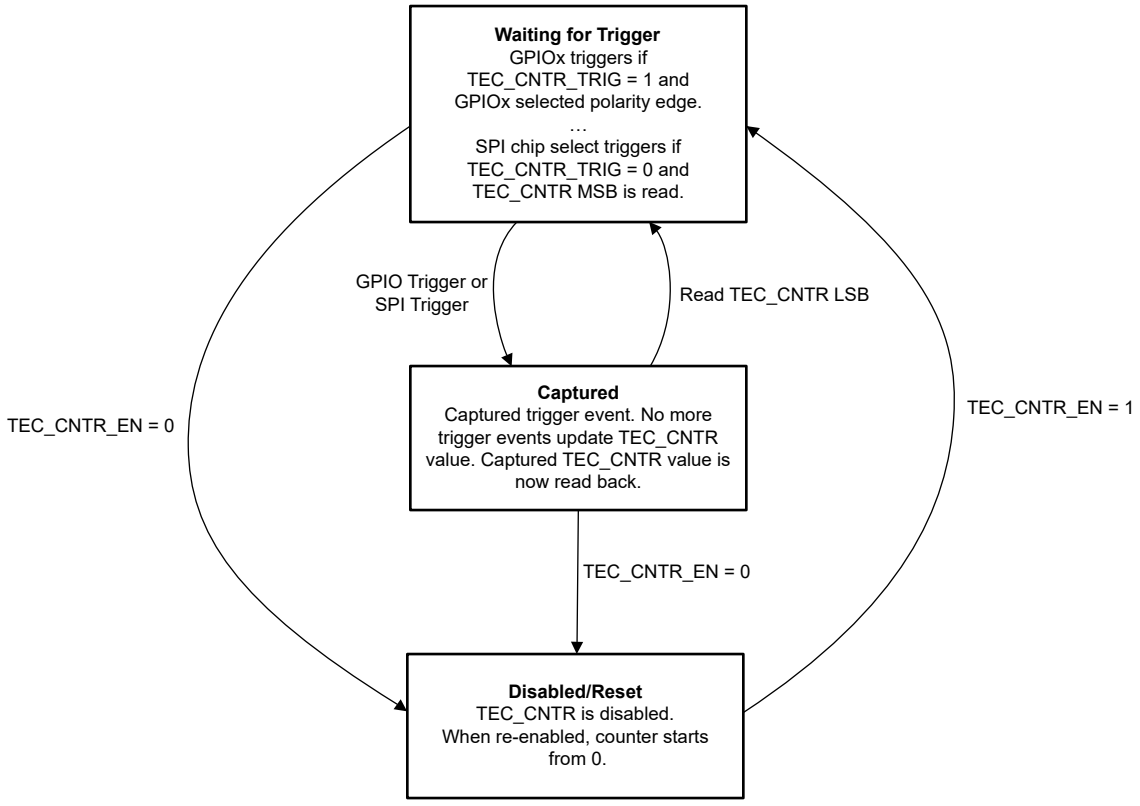

Figure 8-34. State Diagram of TEC

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8.3.22.1 Configuring TEC Functionality

1. Select the PLL to drive the Time Elapsed Counter (TEC). The BAW APLL offers the highest accuracy time measurement due to the highest TEC clock frequency, however, the conventional APLL (LC VCO) provides slightly longer roll-over times.
   - The BAW APLL source is selected by setting REF0_MISSCLK_VCOSEL to 0.
   - The conventional APLL source is selected by setting REF0_MISSCLK_VCOSEL to 1.
2. Select GPIO or SPI chip select as a trigger to capture the TEC counter value to TEC_CNTR field. Using a GPIO does not require any special timing for the SPI SCS pin. Using the GPIO pin for other purposes is possible, enable the TEC functionality when required.
   - GPIO trigger is selected by setting TEC_CNTR_TRIG to 1.
   - SPI chip select trigger is selected by setting TEC_CNTR_TRIG to 0.
3. Enable the TEC counter by setting TEC_CNTR_EN to 1.

8.3.22.2 SPI as a Trigger Source

When TEC_CNTR_EN = 1, each SCS falling edge the TEC counter is captured to the TEC_CNTR field. Subsequent to a SPI transaction which reads from the MSB of the TEC_CNTR field, no falling edge of SCS captures the TEC counter to the TEC_CNTR field until the LSB of the TEC_CNTR field is read.

Figure 8-35 shows when the TEC is latched during single register reads and Figure 8-36 for a multibyte read.

Figure 8-35 shows that the TEC counter is captured every falling SCS edge until TEC_CNTR MSB is read.

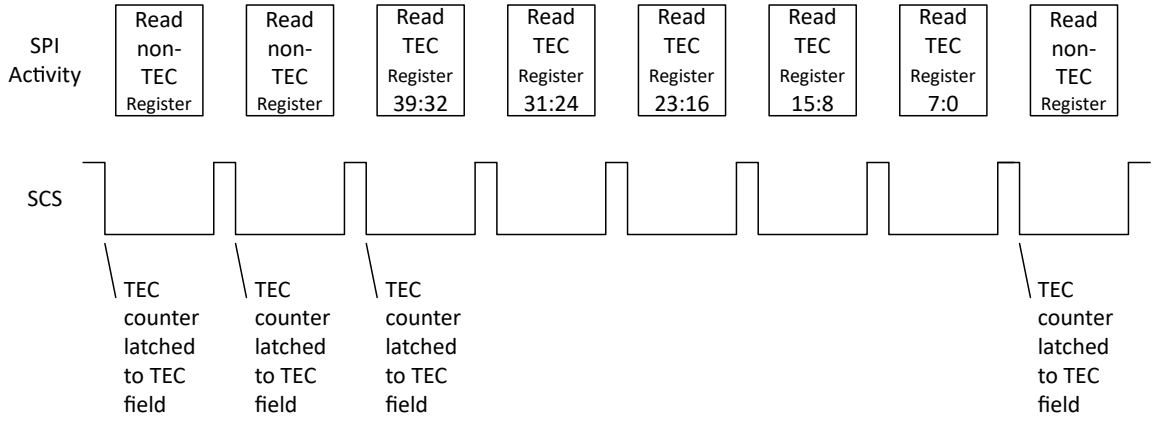

Figure 8-35. TEC Single Byte Read

Figure 8-36 shows that the TEC counter value can be captured and re-armed for capture during a single multibyte read, even if the first register read is not the TEC_CNTR registers.

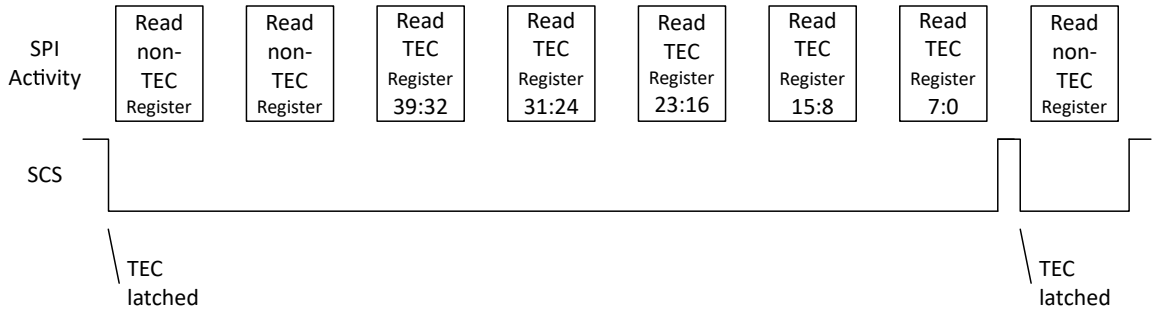

Figure 8-36. TEC Multibyte Read

8.3.22.3 GPIO Pin as a TEC Trigger Source

A rising edge of a GPIO pin selected for TEC functionality with GPIOx_MODE = 0x27 (TEC_TRIG_SEL) captures the TEC value to the TEC_CNTR field upon an edge of the selected polarity (GPIOx_POL). No further updates to the TEC_CNTR field is made by subsequent GPIOx pin edges until the LSB of the TEC_CNTR field is read. Figure 8-37 shows the timing of using a GPIO to capture TEC values.

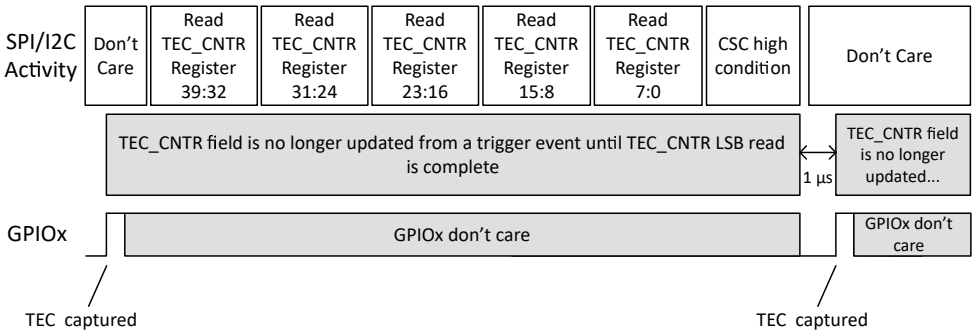

Figure 8-37. TEC Captured Using GPIO

8.3.22.3.1 An Example: Making a Time Elapsed Measurement Using TEC and GPIO1 as Trigger

1. Configure TEC registers as desired. In this example:
   - REF0_MISSCLK_VCOSEL is 0 so that VCBO frequency / 8 is used for TEC clock rate
   - TEC_CNTR_TRIG = 1 for GPIO1 trigger
   - TEC_CNTR_CLR = 0 for normal operation
2. Set GPIO1_MODE = 0x27 (TEC_TRIG_SEL) and GPIO1_POL as desired, 0 in this example for active high input.
3. Provide rising edge on GPIO1 to capture current TEC counter value into the TEC_CNTR field.
4. Read and store the TEC_CNTR field for the first time.
   - Example: 1st_captured_TEC_value = 204 354.
5. Provide rising edge on GPIO1.
6. Read and store the TEC_CNTR field for the second time.
   - Example: 2nd_captured_TEC_value = 76 516 568
7. Calculate time delta using equation #1 with TEC clock rate of 307.2MHz.
   - 248.412 155ms = (76 516 568 - 204 354) / 307.2MHz
   - Because the TEC clock rate is 307.2MHz, the accuracy of the measurement is ±3.26ns.

8.3.22.4 TEC Timing

When TEC_CNTR_TRIG is 1 (GPIO pin):

- Timing accuracy of 1 TEC cycle + 2ns requires a 20% to 80% rise time of less than or equal to 1ns.
- GPIOx rising edge must not occur within 10ns of rising SCS which sets TEC_CNTR_EN from 0 to 1.
- GPIOx must remain high for 10ns.
- A new GPIOx trigger must not arrive within 1µs of the rising edge of the SPI SCS after reading the LSB of the TEC_CNTR.

When TEC_CNTR_TRIG is 0 (SPI):

- Timing accuracy of 1 TEC cycle + 2ns requires an 80% to 20% fall time of less than or equal to 1ns.
- The TEC counter is captured to the TEC_CNTR registers at the falling edge of SPI SCS. No additional time to read back or pre-latching of register is required.

8.3.22.5 Other TEC Behavior

The TEC counter continually counts up and periodically rolls over from 2^{40} – 1 to 0.

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- The user software must determine if the counter has rolled over in between TEC reads. TI recommends resetting the TEC counter accordingly by toggling the TEC_CNTR_EN bit before a prospective starting trigger event, if known.

The REF0_MISSCLK_VCOSEL field also selects which VCO is used by all inputs for the early and missing reference clock validation, therefore the early and missing input validation registers can need to be re-calculated if REF0_MISSCLK_VCOSEL is changed. Changing REF0_MISSCLK_VCOSEL or validation calculations during operation can result in references using the missing pulse or both missing and runt pulse detectors to be momentarily disqualified and send the DPLL into holdover.

While TEC_CNTR_EN = 0, the TEC counter is held in reset, which is counter value 0. Performing an absolute time measurement from the moment that TEC_CNTR_EN transitions from 0 to 1 to a future trigger event is also possible. However the accuracy of this measurement is less than performing a relative measurement caused by two GPIO or two SPI CSC triggers.

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8.4 Device Functional Modes

8.4.1 DPLL Operating States

The following sections describe the DPLL states of operation shown in Figure 8-38. The diagram assumes that holdover is enabled.

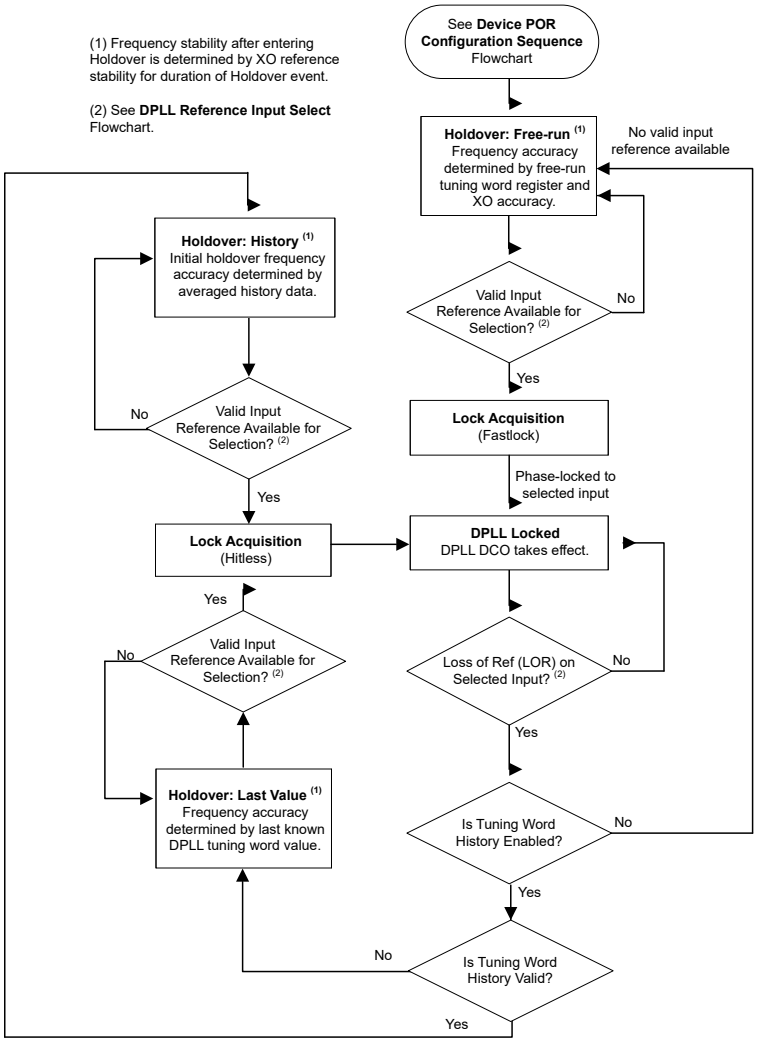

Figure 8-38. DPLL Operating States

8.4.1.1 Free-Run

After device POR configuration and initialization, APLL automatically locks to the XO clock when the XO input signal is valid. The output clock frequency accuracy and stability in free-run mode track the frequency accuracy and stability of the XO input. The reference inputs remain invalid (unqualified) during free-run mode. If the DPLL has locked, but not yet accumulated a valid history word and the reference is lost, then Free-Run is entered.

8.4.1.2 Lock Acquisition

The DPLL constantly monitors the reference inputs for a valid input clock. When at least one valid input clock is detected, the PLL channel exits free-run mode or holdover mode and initiate lock acquisition through the DPLL. The LMK5C33414AS1 supports the Fastlock feature where the DPLL temporarily engages a wider loop bandwidth to reduce the lock time. When the lock acquisition is done, the loop bandwidth is set to the normal configured loop bandwidth setting (BW_{DPLL}).

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8.4.1.3 DPLL Locked

When the DPLL locks, the APLL output clocks are frequency and phase locked to the selected DPLL reference input clock. While the DPLL is locked, the APLL output clocks is not affected by frequency drift on the XO input. The DPLL has a programmable frequency lock detector and phase lock detectors to indicate loss-of-frequency lock (LOFL) and loss-of-phase lock (LOPL) status flags, which can be observed through the status pins or status bits. When the frequency lock is detected (LOFL → 0), the tuning word history monitor (if enabled) begins to accumulate historical averaging data used to determine the initial output frequency accuracy upon entry into holdover mode.

8.4.1.4 Holdover

When a loss-of-reference (LOR) condition is detected and no valid input is available the DPLL enters holdover.

If history is disabled (DPLLx_HIST_EN = 0) the DPLL uses the 2's complement DPLLx_FREE_RUN[39:0] field which sets holdover frequency relative to the DPLL numerator. Short-term frequency accuracy is based on the accuracy of the DPLLx_FREE_RUN field.

If history is enabled (DPLLx_HIST_EN = 1) but the tuning history is not yet valid, then the DPLLx_FREE_RUN field is used as if DPLLx_HIST_EN is disabled. If the tuning history is valid, the DPLL enters holdover using historical data to minimize holdover frequency error. See *Tuning Word History*. In general, the longer the historical average time, the more accurate the initial holdover frequency assuming the 0ppm reference clock (XO input) is drift-free. The stability of the XO reference clock determines the long-term stability and accuracy of the holdover output frequency.

Upon entry into holdover, the LOPL flag is asserted (LOPL → 1). The LOFL flag reports DPLL frequency versus reference frequency is in tolerance. In holdover LOFL remains unchanged in holdover and not update until a valid reference is once again selected.

When a valid input becomes available for selection, the DPLL exits holdover mode and automatically phase lock with the new input clock without any output glitches.

8.4.2 Digitally-Controlled Oscillator (DCO) Frequency and Phase Adjustment

To support IEEE 1588 and other clock steering applications, the DPLL supports DCO mode to allow precise output clock frequency adjustment of less than 0.001 ppb/step. DCO can be implemented using DPLL DCO control or APLL DCO control. While the DPLL is operating in closed-loop mode, DPLL DCO modifies the effective DPLL numerator. While the DPLL is in holdover or not used, APLL DCO adjusts the effective APLL numerator.

8.4.2.1 DPLL DCO Control

DCO mode can be enabled (DPLLx_FB_FDEV_EN = 1) when the DPLL is locked.

There are three methods to steer frequency when using the DPLL DCO.

- Register relative adjustment
  - Preset the deviation amount in DPLL_FDEV
  - Write an 8-bit register to enable increment/decrement by the deviation amount
- GPIO relative adjustment
  - Step/Direction GPIOx trigger
  - Adjust DPLLx_FB_NUM by programming a deviation amount for each step in pin set direction.
- Register absolute adjustment
  - Write the DPLLx_FB_NUM [39:0] based on the frequency control word (FCW)

The DCO frequency step size can be programmed through a 38-bit frequency deviation word register (DPLL_FDEV bits). The DPLL_FDEV value is an offset added to or subtracted from the current numerator value of the DPLL fractional feedback divider and determines the DCO frequency offset at the VCO output.

The DCO frequency increment (FINC) or frequency decrement (FDEC) updates can be controlled through software control (DPLLx_FB_FDEV_UPDATE) or user selectable pin control (GPIOx). DCO updates through

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software control are always available through I2C or SPI by writing to the DPLLx_FB_FDEV_UPDATE register bit. Writing a 0 increments the DCO frequency by the programmed step size, and writing a 1 decrements the DCO frequency by the step size. SPI can achieve faster DCO update rates than I2C because the SPI has faster write speed.

When DPLL pin control is selected (FDEV_TRIG_DPLLx and FDEV_DIR_DPLLx on GPIOs), a rising edge on the GPIO pin defined in FDEV_TRIG_DPLLx applies a corresponding DCO update to the DPLL, another GPIO defined in FDEV_DIR_DPLLx determines the direction of the FDEV trigger. FDEV_DIR_DPLLx = 0 means positive, FDEV_DIR_DPLLx = 1 means negative. In this way, the GPIO pins functions as the FINC or FDEC input. The minimum positive pulse width applied to the trigger pins must be greater than 100ns to be captured by the internal sampling clock. The DCO update rate must be limited to less than 5MHz when using pin control.

When DCO control is disabled (DPLLx_FB_FDEV_EN = 0), the DCO frequency offset is cleared and the VCO output frequency is determined by the original numerator value of the DPLL fractional feedback divider.

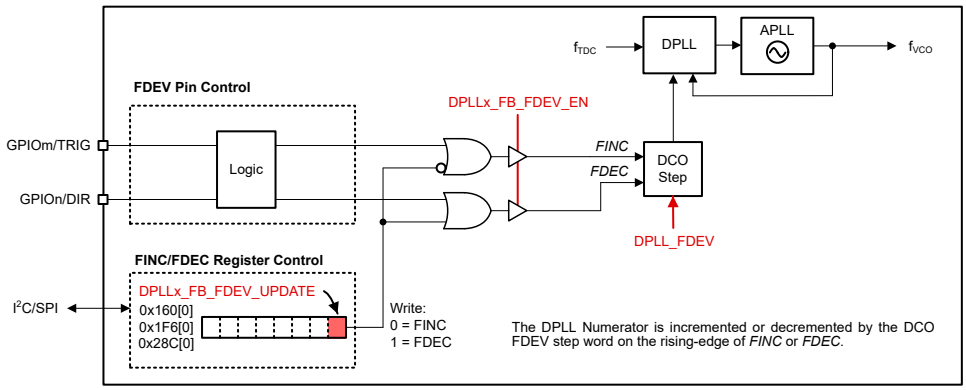

Figure 8-39. DCO Mode Control Options

8.4.2.2 DPLL DCO Relative Adjustment Frequency Step Size

Equation 13 shows the formula to compute the DPLLx_FB_FDEV register value required to meet the specified DCO frequency step size in ppb (part-per-billion) when DCO mode is enabled for the DPLL.

$$DPLLx_FB_FDEV = (Reqd_ppb / 10^9) \times DPLL_{DEN} \times f_{VCOx} / f_{TDCx} \quad (13)$$

where

- DPLLx_FB_FDEV: Frequency deviation value (0 to 2^{38}– 1)
- Reqd_ppb: Required DCO frequency step size (in ppb)
- $DPLL_{DEN}$: DPLL FB divider denominator value (1 to 2^{40}, register value of 0 = 2^{40})
- f_{VCOx}: VCOx frequency
- f_{TDCx}: TDCx frequency

8.4.2.3 APLL DCO Frequency Step Size

Users must write to the DPLLx_FREE_RUN register field to adjust the APLL DCO. When DPLLx_HIST_EN = 1, the relative adjustments are performed. When DPLLx_HIST_EN = 0 the DPLLx_FREE_RUN value is used for the APLLx DCO numerator. The effective APLLx numerator can be read back from APLLx_NUM_STAT.

Equation 14 shows the formula to compute the DPLLx_FREE_RUN field value required to meet the specified DCO frequency step size in ppb (part-per-billion) when relative APLL DCO mode is enabled. DPLLx_FREE_RUN is a signed value and the actual programmed value for a negative number can be calculated as the 2s complement.

$$DPLLx_FREE_RUN = (Reqd_ppb / 10^9) \times APLLx_{DEN} \times f_{VCOx} / f_{PDFx} \quad (14)$$

where

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- DPLLx_FREE_RUN: Frequency deviation value (-2^{39} to $2^{39}-1$)
- Reqd_ppb: Required DCO frequency step size (in ppb)
- $APLLx_{DEN}$: APLL FB divider denominator value (2^{40})
- f_{VCOx}: VCOx frequency
- f_{PDFx}: PLLx phase detector frequency

8.4.3 APLL Frequency Control

The device can also support APLL frequency and phase control through writing the 40-bit register DPLLx_FREE_RUN[39:0] while the DPLL is in holdover or not used. If the reference clock in a free-run mode or disabled, the DPLL disconnects with the APLL, but users can still adjust frequency and phase accuracy.

To enable APLL DCO control, set DPLLx_LOOP_EN = 1, and PLLx_MODE = 1 for 40-bit fractional denominator. DPLLx_EN can be set = 0.

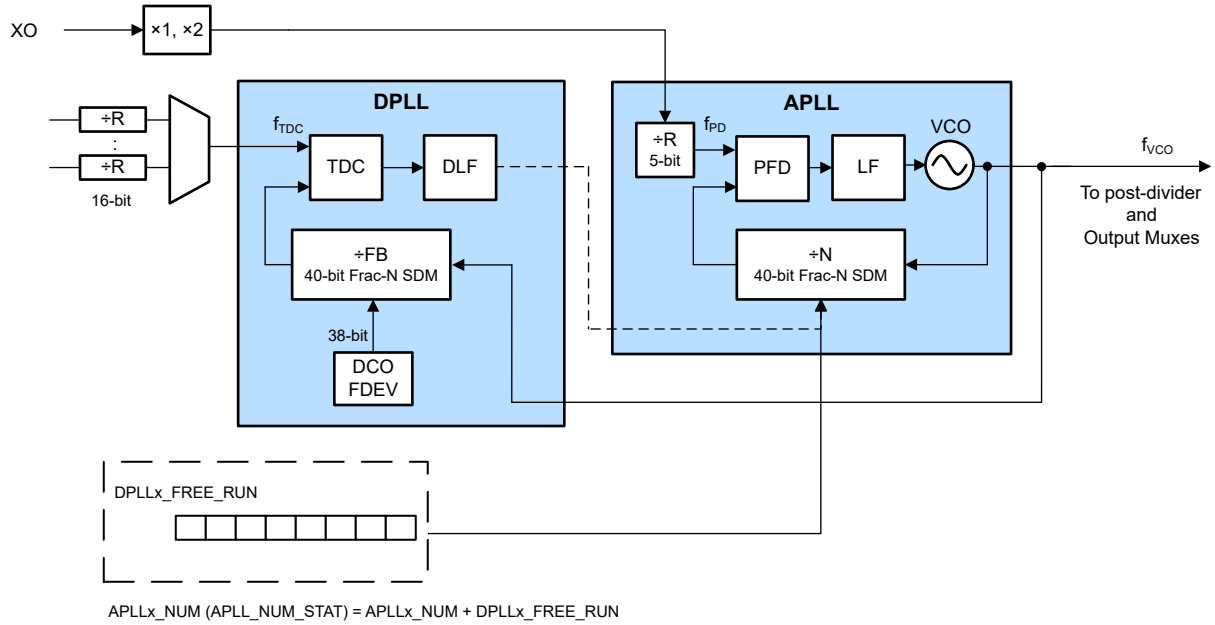

Figure 8-40. APLL DCO Mode

There are two alternative methods in adjusting the APLL DCO.

- Absolute frequency adjustment
  - Set DPLLx_HIST_EN = 0
  - Effective APLLx_NUM (APLLx_NUM_STAT) = APLLx_NUM + DPLLx_FREE_RUN
    - The APLLx_NUM_STAT is a read-only register and can be read back.
    - The DPLL loop filter block modifies the APLLx_NUM_STAT based on DPLLx_FREE_RUN value.
  - DPLLx_FREE_RUN is a 40-bit 2's complement number
- Relative frequency adjustment
  - Set DPLLx_HIST_EN = 1
  - DPLLx_FREE_RUN value is fed into the APLLx_NUM at a controlled rate defined by a step size register and step period register.
  - If another DPLLx_FREE_RUN write occurs before the LMK is complete in making the last adjustment, any remaining steps are lost and the new value begins to feed the APLL numerator.
  - A flag is set when the DPLLx_FREE_RUN word is fully fed into the effective APLLx_NUM (APLL_NUM_STAT).

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8.4.4 Device Start-Up

8.4.4.1 Device Power-On Reset (POR)

Figure 8-41 shows the device power-on reset (POR) configuration sequence. POR occurs when the PD# pin is deasserted and reaches a logic high state. After POR, the serial control interface of choice (I^2C or SPI) is selected. The LMK5C33414AS1 supports preconfigured device settings from the factory preprogrammed internal ROM Detailed Description. A programmable EEPROM Overlay provides a flexible start-up of output clocks. Refer to Programming for after start-up programming details.

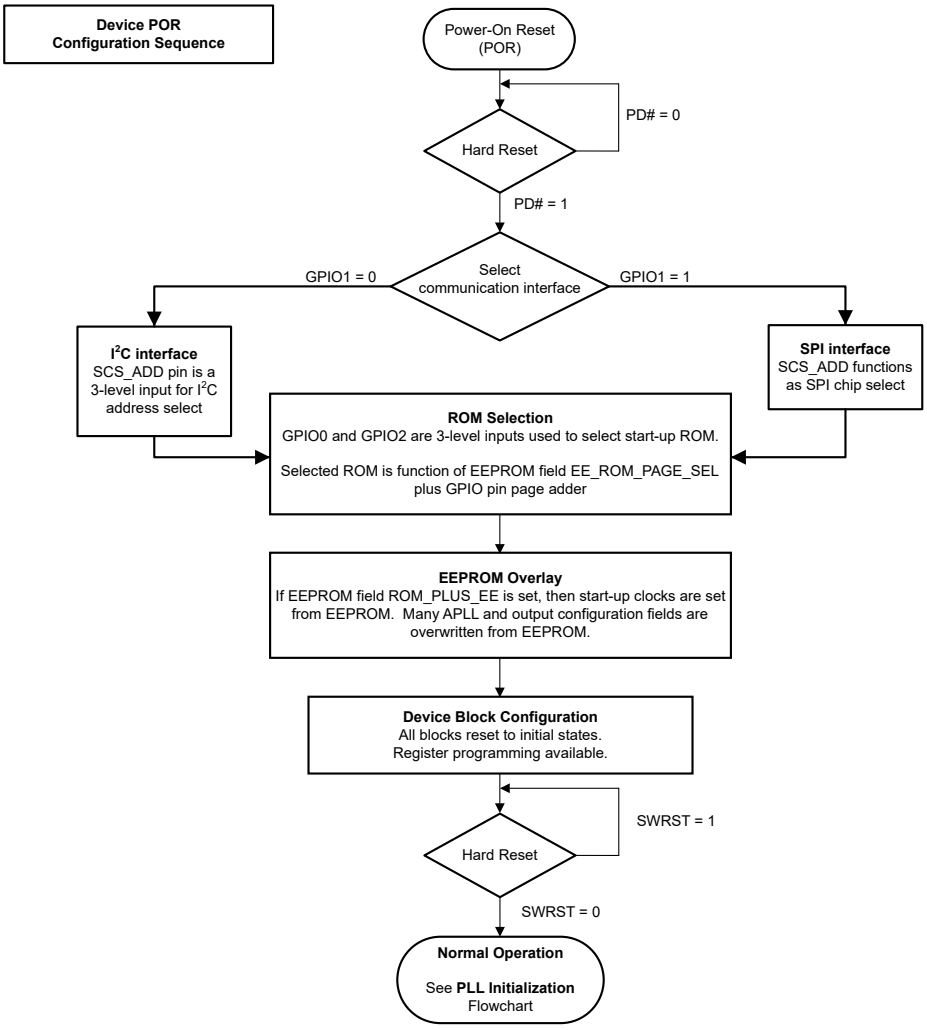

Figure 8-41. Device POR Sequence

After start-up, a global SWRST (R23[6]) restarts the device initialization sequence and APLL calibration state machine (see Figure 8-42). Issuing the global SWRST is recommended when modifying the APLL registers after POR to recalibrate all of the APLLs and re-align the output and SYSREF channel dividers.

When toggling the global SWRST, a disruption on the APLL output clocks can occur until the APLLs acquire lock again. An individual APLLx software reset (APLLx_SWRST) can be issued to avoid disturbing other APLL clocks. Use the APLLx_SWRST after bring-up when modifying the registers of the individual APLLx. For example, if only APLL1 registers are changed, then issue an APLL1_SWRST and only APLL1 outputs are briefly disrupted while APLL3 and APLL2 outputs remain undisturbed.

Issuing a SWRST is **not required** for the following cases:

- When no register writes are performed after boot-up.

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- When only the XO input termination type, INx input termination type, output drivers (such as swing level or channel divider), GPIO pin, status, or DCO registers are modified after boot-up.
- When programming the EEPROM.

Issuing a SWRST is **recommended** for the following cases:

- When most of the register writes are modified through I2C or SPI (such as during device configuration after boot-up).
- When the ZDM and SYSREF registers are configured. Not required if only changing the SYSREF divider value.
- When the APLLx registers are modified and a brief interruption on all of the APLLx clocks is not an issue.

Issuing an individual APLLx_SWRST is **recommended** for the following cases:

- When the device has been configured with the desired registers and only APLLx registers need to be modified without disturbing the other APLL output clocks.

8.4.4.2 PLL Start-Up Sequence

Figure 8-42 shows the general sequence for APLL start-up after POR. This sequence also applies after a global SWRST or APLLx_SWRST. To provide proper VCO calibration, the APLL reference clock must be stable in amplitude and frequency prior to the start of VCO calibration. Otherwise, the VCO calibration can fail and prevent start-up of the APLL and the output clocks.

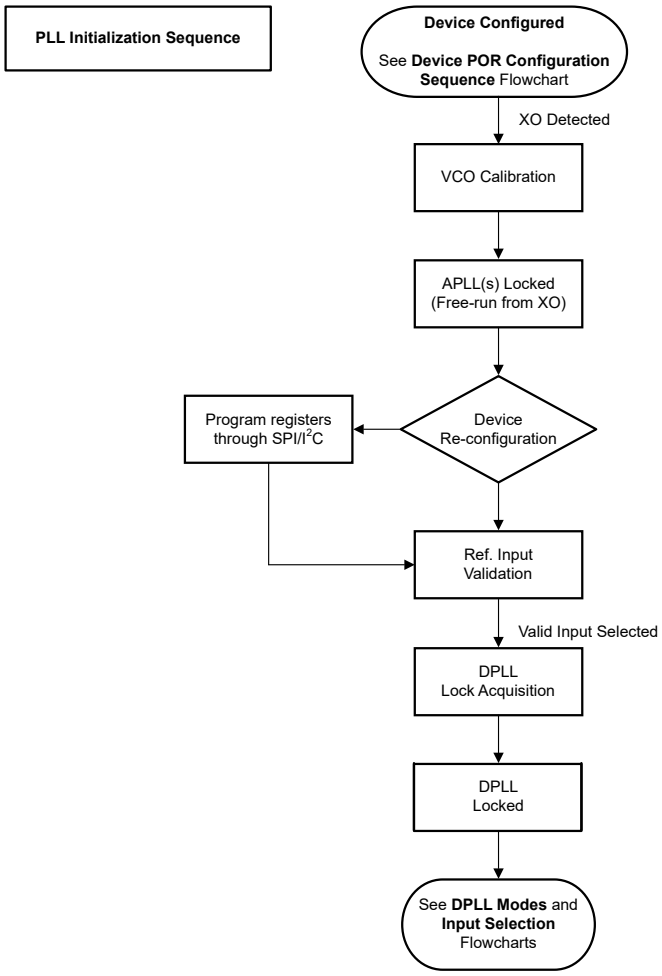

Figure 8-42. APLL Initialization Sequence

8.4.4.3 Start-Up Options for Register Configuration

The device can boot-up from either of the four listed options. The option selected depends on the system use case.

1. **Option 1: ROM**
   a. The device boots up from one of the ROM pages, the EEPROM overlay is bypassed, and no I2C transactions are performed after start-up.
   b. Use this option when both DPLL and APLL settings match a ROM page.
2. **Option 2: ROM → EEPROM**
   a. The device boots up from one of the ROM pages, then the EEPROM settings are loaded to the device and overwrite the XO, APLL, and output driver configuration.
   b. Use this option when the desired DPLL settings match a ROM page but the APLL settings do not. Also, use for free-run mode (APLL only, DPLL disabled) configurations.
3. **Option 3: ROM → EEPROM → in-system programming**
   a. The device boots up from one of the ROM pages, then the EEPROM settings are loaded to the device and overwrite the XO, APLL, and output driver configuration. I2C transactions are performed after start-up to update the remaining registers that are not stored in EEPROM (DPLL, SYSREF, and GPIO).
   b. Use this option when the desired DPLL and APLL settings do not match a ROM page.
4. **Option 4: ROM → in-system programming**
   a. The device boots up from one of the ROM pages, the EEPROM overlay is bypassed, and I2C transactions are performed to overwrite any undesired register value initialized by the ROM selection (DPLL, SYSREF, GPIO, XO, APLL, and output driver).
   b. Use this option when the EEPROM can not be preprogrammed to reduce start-up time or when the majority of the registers must be configured in-system.

8.4.4.4 GPIO1 and SCS_ADD Functionalities

The device can start-up as either I^2C or SPI depending on the 2-level input level sampled on the GPIO1 pin during POR.

- **GPIO1 = 0:** I^2C Serial Interface is selected and the SCS_ADD pin functions as a 3-level input for the I^2C address select.
- **GPIO1 = 1:** SPI Serial Interface is selected and the SCS_ADD functions as a SPI chip select.

8.4.4.5 ROM Page Selection

At POR, the sum of the GPIO2, GPIO0, and EE_ROM_PAGE_SEL (R20[6:3]) logic states determine which ROM page is used.

The EE_ROM_PAGE_SEL field is stored in EEPROM and has a factory default setting of EE_ROM_PAGE_SEL = 0. All register pages in the ROM are factory-set in hardware (mask ROM) and are not software programmable by the user.

Refer to ROM Detailed Description for the configuration of each ROM page and the required XO, INx, and OUTx frequency setting.

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8.4.4.6 ROM Detailed Description

Table 8-11. ROM Page Selection by GPIO2 and GPIO0

GPIO2 AT POR	GPIO0 AT POR	ROM PAGE WITH EE_ROM_PAGE_SEL = 0
L	L	ROM page 0. XO= 48MHz, REFCLK = 156.25MHz and 10MHz, outputs = 100MHz, 122.88MHz, 245.76MHz, 312.5MHz, 491.52MHz.
L	H	ROM page 1. XO= 48MHz, REFCLK = 10MHz, outputs = 100MHz, 312.5MHz, 491.52MHz.
H	L	ROM page 2. XO= 48MHz, REFCLK = 10MHz, outputs = 100MHz, 125MHz, 312.5MHz, 491.52MHz.
H	H	ROM page 3. Low power mode. All PLLs off, all outputs off.
L	M	ROM page 4. XO = 54MHz, REFCLK = 30.72MHz, outputs = 30.72MHz, 125MHz, 161.1328125MHz, 122.88MHz, 245.76MHz, 491.52MHz.
M	L	ROM page 5. XO= 20MHz, REFCLK = 156.25MHz, outputs = 100MHz, 125MHz, 156.25MHz, 245.76MHz, 491.52MHz
M	M	ROM page 6. XO= 48MHz, REFCLK = 156.25MHz, outputs = 1Hz (1-PPS), 25MHz, 100MHz, 122.88MHz, 125MHz, 156.25MHz, 245.76MHz, 491.52MHz
M	H	ROM page 7. XO= 48MHz, REFCLK = 156.25MHz, outputs = 1Hz (1-PPS), 20.48MHz, 25MHz, 100MHz, 122.88MHz, 125MHz, 156.25MHz, 245.76MHz, 491.52MHz
H	M	ROM page 8. XO= 48MHz, REFCLK = 491.52MHz and 156.25MHz, outputs = 25MHz, 122.88MHz, 125MHz, 156.25MHz, 491.52MHz

Table 8-12. ROM Detailed Description

ROM	XO	IN0	IN1	IN2	IN3	OUT0	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8	OUT9	OUT10	OUT11	OUT12	OUT13
0	48	156.25	10	–(1)	–(1)	100	100	122.88	245.76	312.5	312.5	312.5	312.5	491.52	1.92(2)	491.52	1.92(2)	491.52	1.92(2)
1	48	10	10	–(1)	–(1)	1.92(2) (4)	491.52 (4)	100(4)	100	491.52 (4)	491.52 (4)	491.52	1.92(2) (4)	122.88 (4)	122.88 (4)	491.52 (4)	1.92(2) (4)	491.52 (4)	1.92(2) (4)
2	48	10	10	–(1)	–(1)	1.92(2) (4)	491.52	100	100	1.92(2) (4)	491.52	491.52	1.92(2) (4)	122.88	1.92(2) (4)	491.52	1.92(2) (4)	491.52	1.92(2)
3	38.88	156.25	10	–(1)	–(1)	1.92(2) (4)	25(4)	100(4)	100(4)	156.25 (4)	156.25 (4)	156.25 (4)	156.25 (4)	1.92(2) (4)	122.88 (4)	1.92(2) (4)	122.88 (4)	1.92(2) (4)	122.88 (4)
4	54	30.72	30.72	–(1)	–(1)	125	125	30.72	30.72	161.1x (3)	161.1x (3)	161.1x (3)	161.1x (3)	122.88	122.88	245.76	245.76	491.52	491.52
5	20	156.25	156.25	–(1)	–(1)	100	125	156.25	156.25	245.76	491.52	245.76	7.68(2)	491.52	7.68(2)	491.52	7.68(2)	491.52	7.68(2)
6	48	156.25	156.25	–(1)	–(1)	1E-6(2) (4)	125	100	100	25	125(4)	156.25	156.25 (4)	245.76 (4)	7.68(2) (4)	491.52 (4)	7.68(2) (4)	122.88 (4)	20.48(2)
7	48	156.25	156.25	–(1)	–(1)	1E-6(2)	125	100	100	25	125	156.25	156.25	245.76	7.68(2)	491.52	7.68(2)	122.88 (4)	20.48(2)
8	48	491.52	156.25	–(1)	–(1)	125	25	312.5	156.25	491.52	7.68(2)	491.52	7.68(2)	491.52	7.68(2)	491.52	7.68(2)	491.52	7.68(2)

(1) The input or output clock frequency is not configured and the input or output channel is disabled.
(2) The output clock is sourced from the SYSREF channel divider.
(3) The exact output clock frequency is 161.1328125MHz.
(4) The output clock frequency is configured but the output channel is disabled.

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8.4.4.7 EEPROM Overlay

An integrated EEPROM supports user-customized output clocks on start-up when the ROM pages do not meet the start-up clocking requirements. The DPLL, SYSREF, and GPIO registers are not set by the EEPROM values and are instead initialized by the ROM Detailed Description. If the loaded DPLL settings from the ROM page are not valid for a system, the APLLs lock to the XO input instead. The DPLL reference inputs are considered valid and can lock to the DPLL once the DPLL registers are properly configured.

The device EEPROM overlay can be set by the ROM_PLUS_EE bit (R20[7]), which is stored in EEPROM. The factory default EEPROM setting for the ROM_PLUS_EE bit is 0.

- **ROM_PLUS_EE = 0:** The device is started with just the ROM settings.
- **ROM_PLUS_EE = 1:** The EEPROM overlay overwrites the XO, APLL, and output driver settings initialized from the ROM page selection.

8.5 Programming

8.5.1 Memory Overview

The LMK5C33414AS1 has four memory spaces.

1. **Registers** – Contains the active register settings currently used by the device.
2. **ROM** – Contains all register settings (DPLL, SYSREF, GPIO, XO, APLL, and output driver). Has default ROM pages that are not user programmable. See ROM Detailed Description.
3. **EEPROM** – Contains partial register settings (APLL and output). Can be programmed numerous times through I2C or SPI (refer to the Absolute Maximum Ratings for the maximum number of programming cycles). See EEPROM Overlay.
4. **SRAM** – Contains the same address and data mapping as the EEPROM. Use only for programming the EEPROM.

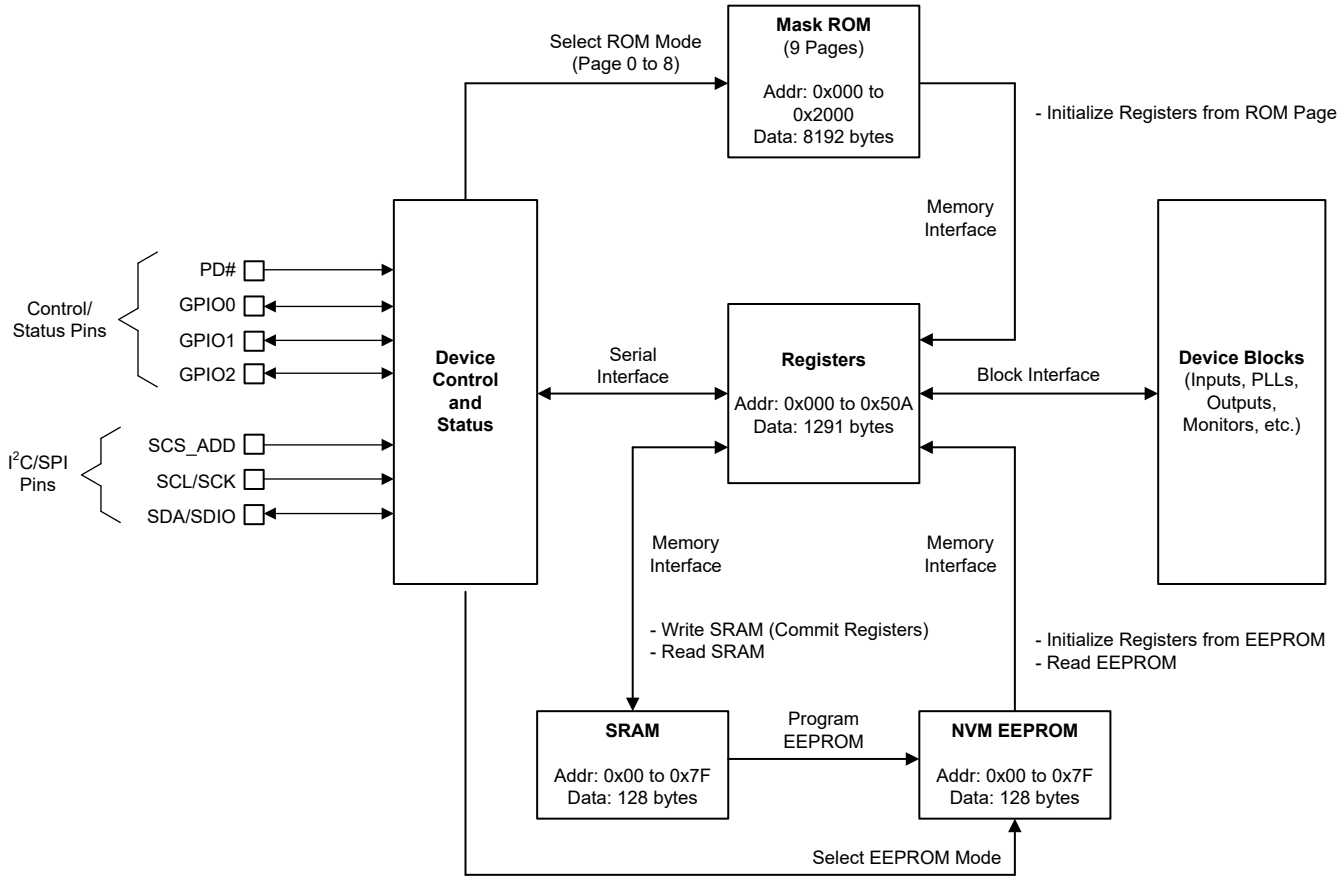

Figure 8-43. Device Control, Register, and Memory Interfaces

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8.5.2 Interface and Control

After start-up, a system host device (MCU or FPGA) can use either I2C or SPI to initialize, control, or monitor the registers and to access the SRAM and EEPROM maps. Some device features can also be controlled and monitored through the external logic control (GPIOx) and status pins. A 2-byte address and 1-byte data interface is used for the LMK5C33414AS1.

In the absence of a host, the LMK5C33414AS1 can self-start from one of the on-chip ROM pages and EEPROM overlay to initialize the registers upon device POR, see Device Start-Up.

8.5.2.1 Programming Through TICS Pro

The TICS Pro software tool for EVM programming has a step-by-step design flow to enter the user-selected clock design parameters, calculate the frequency plan, and generate the device register settings for the desired configuration. The register map data file (hex dump in text format) and EEPROM programming sequence can be exported to enable host programming of the device on start-up.

If desired, customers can post a TICS Pro setup file (.tcs) to the TI E2E public forum for TI to review and optimize the configuration settings.

8.5.2.2 SPI Serial Interface

When SPI control interface is selected, the device uses a 3-wire SPI with SDIO, SCK, and SCS signals (SPI_3WIRE_DIS = 0). When using SPI SCS_ADD also can act as a Time Elapsed Counter (TEC) trigger. When set SPI_3WIRE_DIS = 1, any GPIO can be selected as SDO to support readback with 4-wire SPI.

SPI and GPIO I/O are referenced to the 3.3V power supply and the output drivers are 3.3V LVCMOS compatible. The inputs are 1.8V, 2.5V, or 3.3V LVCMOS compatible. When the SPI host is 3.3V I/O, either 3-wire or 4-wire can be used without any voltage conversion. When the SPI host is not 3.3V I/O complaint, the SDO signal from LMK5C33414AS1 device must be divided to be compatible with the SPI host voltage level. The SDO pin can also be configured for open drain so the pullup resistors set the read back voltage as desired.

The host device must present data to the device MSB first. A message includes a transfer direction bit ($\overline{W}$/R), a 15-bit address field (A14 to A0), and a 8-bit data field (D7 to D0) as shown in Figure 8-44. The $\overline{W}$/R bit is 0 for a SPI write and 1 for a SPI read.

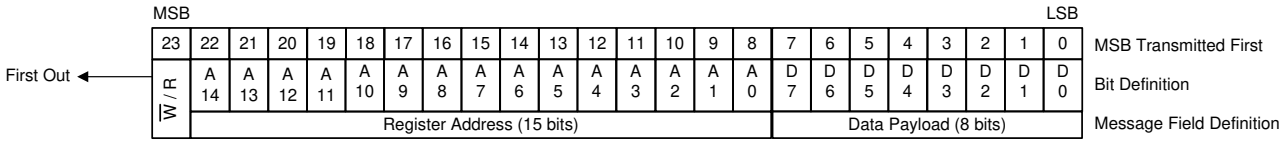

Figure 8-44. SPI Message Format

A message frame is initiated by asserting SCS low. The frame ends when SCS is deasserted high. The first bit transferred is the $\overline{W}$/R bit. The next 15 bits are the register address, and the remaining eight bits are data. On write transfers, data is committed in bytes as the final data bit (D0) is clocked in on the rising edge of SCK. If the write access is not an even multiple of eight clocks, the trailing data bits are not committed. On read transfers, data bits are clocked out from the SDO pin on the falling edges of SCK.

8.5.2.2.1 SPI Block Register Transfer

The LMK5C33414AS1 supports a SPI block write and block read transfers. A SPI block transfer is exactly (2 + N) bytes long, where N is the number of data bytes to write or read. The host device (SPI host) is only required to specify the lowest address of the sequence of addresses to be accessed. The device automatically increments the internal register address pointer if the SCS pin remains low after the host finishes the initial 24-bit transmission sequence. Each transfer of eight bits (a data payload width) results in the device automatically incrementing the address pointer (provided the SCS pin remains active low for all sequences).

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8.5.2.3 I²C Serial Interface

When GPIO1 = 0, the device operates as an I²C client and supports bus rates of 100kHz (standard mode) and 400kHz (fast mode). Slower bus rates can work as long as the other I²C specifications are met.

The five MSBs of the 7-bit I²C address are initialized from the EEPROM at start-up, see EEPROM Programming With the Direct Writes Method or Mixed Method as well as Five MSBs of the I2C Address and the EEPROM Revision Number.

The two LSBs of the I²C address are defined by the SCS_ADD pin state at start-up.

Table 8-13 shows the I²C address options based on the EEPROM default for the five MSBs of the I²C address and the SCS_ADD state.

Table 8-13. I²C Address Options

5 MSBs of I²C ADDRESS (FACTORY DEFAULT)	SCS_ADD PIN STATE	2 LSBs of I²C ADDRESS	I²C ADDRESS
0x19	Low	0	0x64
0x19	Vmid	2	0x66
0x19	High	1	0x65

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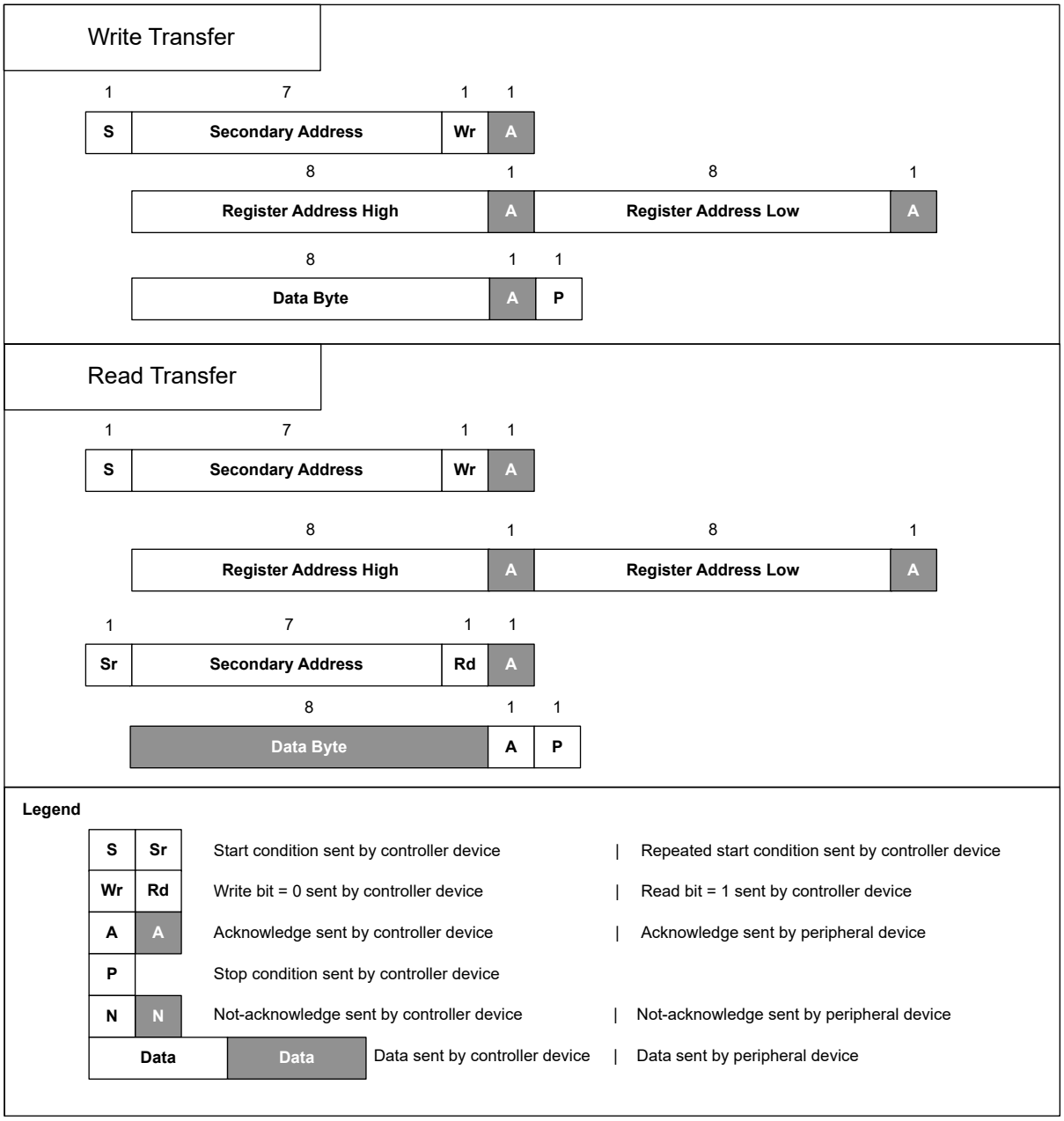

Figure 8-45. I²C Byte Write and Read Transfers

I²C Block Register Transfers

Figure 8-46 shows that the device supports I²C block write and block read register transfers.

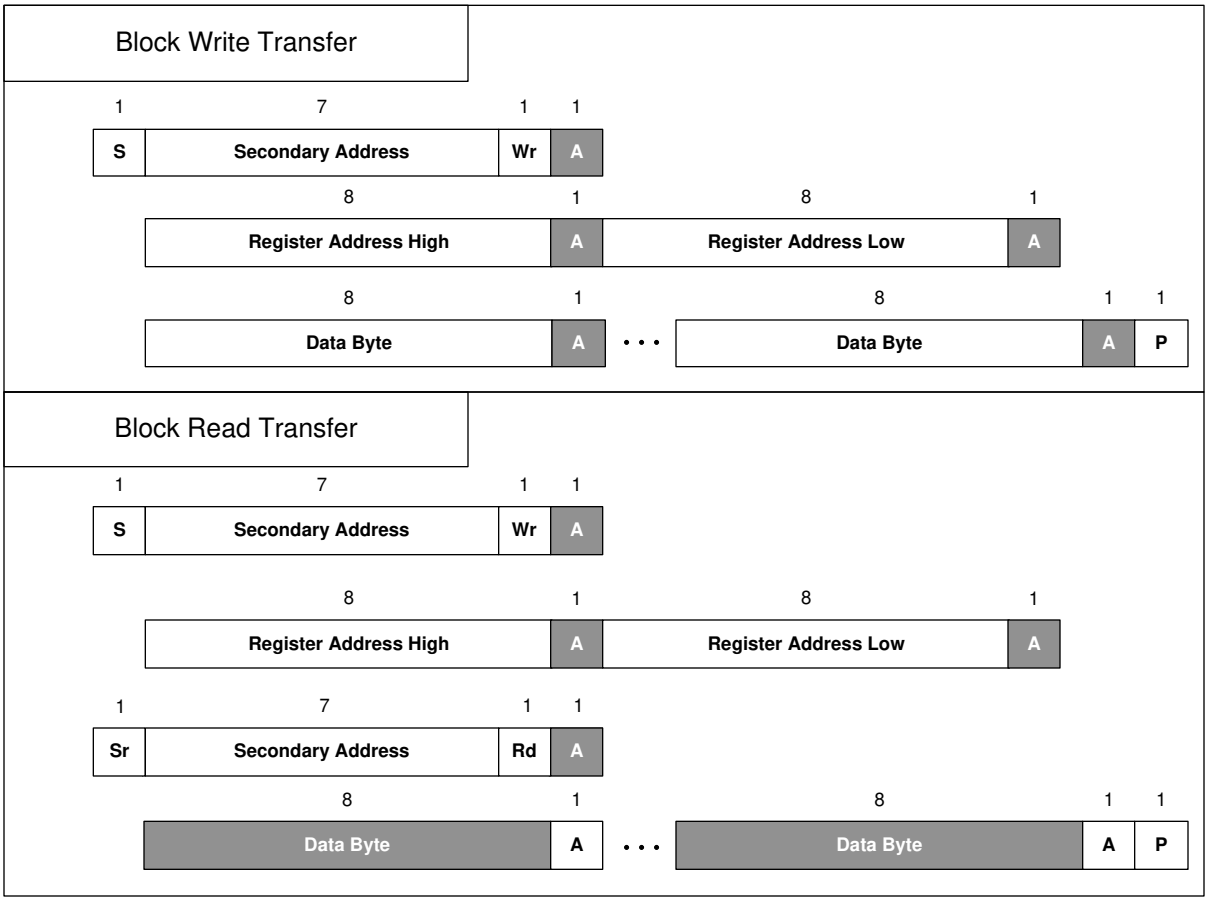

Figure 8-46. I²C Block Register Transfers

8.5.3 General Register Programming Sequence

For applications that use a system host to program the initial configuration through I²C or SPI after power up, this general procedure can be followed:

1. Apply power to the device to start in I²C or SPI mode (see Device Start-Up).
2. Set all outputs to static low to verify that there are no glitches at startup.
   a. For all outputs, configure the OUT_x_CONFIGURATION registers.
   b. For only OUT0 and OUT1, configure the OUT_x_CONFIGURATION and the OUT_x_STATIC_LOW registers.
3. Write to all of the registers EXCEPT the following registers:
   a. The registers listed in Step 2.
   b. R25[0] (SYNC_EN)
   c. R21[6] (SYNC_SW)
   d. R23[6] (SWRST)
   e. R23[5:3] (DPLLx_SWRST)
   f. R23[2:0] (APLLx_SWRST)
4. Perform global, DPLL, and APLL software resets by writing:
   a. SWRST = 1
   b. APLLx_SWRST = 1
   c. DPLLx_SWRST = 1

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d. SWRST = 0
e. **Note:** The DPLLx_SWRST and APLLx_SWRST are self-clearing bits.

5. Wait for the APLL or APLLs to lock by polling the PLL loss of lock status registers, LOL_PLLx, before asserting SYNC_EN and SYNC_SW.
6. Assert SYNC by writing:
   a. SYNC_EN = 1
   b. SYNC_SW = 1
7. Modify the output registers listed in Step 2: change from static low to the desired output states.
8. Dessert SYNC by writing:
   a. SYNC_SW = 0
   b. SYNC_EN = 0 (optional and not required)
9. Optional, but recommended: Clear the interrupt (INTR) status flags. These bits are not self-clearing (sticky) and can get set during start-up while the DPLL and APLL registers are not yet properly configured.

Alternatively, use the part-specific TICS Pro profile to export a customized register programming sequence for the currently loaded .tcs file as shown in Figure 8-47.

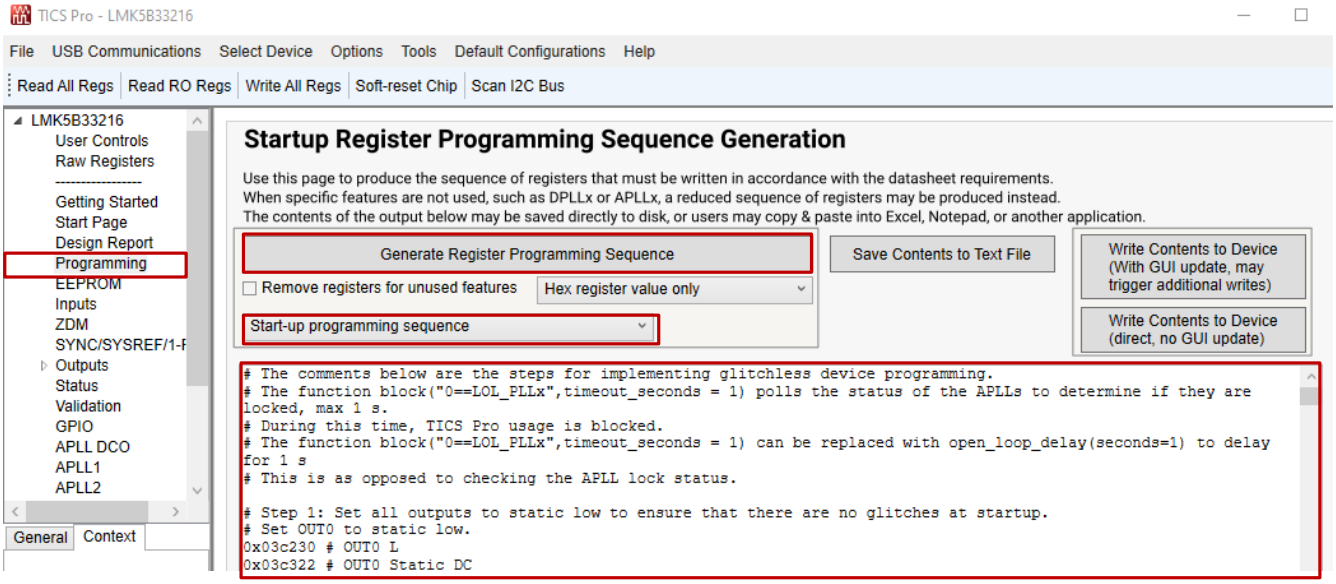

Figure 8-47. LMK5xxxxxx TICS Pro Programming Page (Screenshot From v1.7.7.4.)

8.5.4 Steps to Program the EEPROM

The first step is to program the SRAM with the desired register settings. The next step is to program the EEPROM through an automatic SRAM to EEPROM transfer. For more details on each step, refer to the listed sections:

1. Overview of the SRAM Programming Methods
2. EEPROM Programming With the Register Commit Method and
   EEPROM Programming With the Direct Writes Method or Mixed Method

8.5.4.1 Overview of the SRAM Programming Methods

The register data can be written to the SRAM by any of three methods:

1. Register Commit Method
   a. Uses the REGCOMMIT bit to enable the **automatic** transfer (mapping) of the active registers to SRAM.
   b. Modifies the SRAM and EEPROM by using the contents of the active registers.
   c. Does not require knowledge of the SRAM and EEPROM mapping.
   d. Cannot be used to modify the following EEPROM fields: TARGET_ADR_MSB and EEREV.

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e. Recommended for most applications and when pre-programming the device.
2. Direct Writes Method
   a. Requires direct and **manual** writes to each SRAM address.
   b. Modifies the SRAM and EEPROM without writing to the active register space, which allows the device to continue normal operation without disruption.
   c. Requires knowledge of the SRAM and EEPROM mapping.
   d. Can be used to modify the following EEPROM fields: TARGET_ADR_MSB and EEREV.
   e. Recommended when programming the EEPROM in-system (such as for a version update) to avoid output interruption.
   f. Recommended when overwriting all of the SRAM.
3. Mixed Method (Register Commit and Direct Writes)
   a. Recommended when only modifying **select** fields in SRAM, such as the TARGET_ADR_MSB and EEREV.
   b. Not recommended when overwriting all of the SRAM through the Direct Writes method.

8.5.4.2 EEPROM Programming With the Register Commit Method

1. Power cycle (toggle PD#).
2. Write to the active registers with the desired configuration and confirm the output clocks behave as expected.
3. Commit active registers to SRAM by setting R171[6] (REGCOMMIT) to 1.
   a. **Note:** REGCOMMIT is auto-cleared to 0 when the transfer is completed.
4. Enable EEPROM overlay by setting R20[7] (ROM_PLUS_EE) to 1.
5. Unlock EEPROM by setting to R180 (NVMUNLK) to 234.
6. In one transaction:
   a. Erase the contents of the EEPROM by setting R171[1] (NVMERASE) to 1.
   b. Initiate EEPROM programming to transfer the SRAM contents to EEPROM by setting R171[0] (NVMPROG) to 1.
   c. **Note:** Step 5 & 6 must be atomic (back-to-back) writes without any other register transactions in-between. Serial communication interruptions (such as access to other devices on the same bus) is also not allowed for successful EEPROM programming.
7. Wait for EEPROM programming to finish by polling R171[2] (NVMBUSY) until cleared or wait about 500ms.
   a. **Note:** Do not power down, PD# toggle, or continue to the next step until NVMBUSY is cleared to have a successful EEPROM programming.
8. Lock the EEPROM by setting NVMUNLK to 0.
9. At the next POR, if the EEPROM programming is successful, the EEPROM program count, R16 (NVMCNT), increments by 1. Also, if the EEPROM overlay bit is set, the active registers are loaded from EEPROM.

Hex instruction list:

```
R171    0x00AB40              # Set REGCOMMIT
R20     0x001480              # Enable EEPROM OVERLAY
R180    0x00B4EA              # UNLOCK EEPROM
R171    0x00AB03              # ERASE and PROGRAM SRAM contents to EEPROM
while(READ_REG(NVMBUSY) != 0) # NVMBUSY is located in 0xAB, bit 2
R180    0x00B400              # LOCK EEPROM
```

8.5.4.3 EEPROM Programming With the Direct Writes Method or Mixed Method

1. Attain the SRAM mapping of your desired configuration. The SRAM map is generated in TICS Pro. For the TARGET_ADR_MSB and EEREV mapping, see Five MSBs of the I2C Address and the EEPROM Revision Number.
2. **Mixed method only**: Commit active registers to SRAM by setting REGCOMMIT (R171[6]) to 1.
   a. **Note:** REGCOMMIT is auto-cleared to 0 when the transfer is completed.
3. Enable EEPROM overlay by setting R20[7] (ROM_PLUS_EE) to 1.
4. Configure the SRAM address pointer by setting R173[4:0] (MEMADR_12:8) to the 5 MSBs of the SRAM address.

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5. Configure the SRAM address pointer by R174 (MEMADR) to the 8 LSBs of the SRAM address.
6. Store the desired data at the specified SRAM address by setting R176 (RAMDAT) to the SRAM data from the SRAM map.
7. Repeat steps 4-6 for all desired SRAM addresses.
8. Unlock EEPROM by setting to R180 (NVMUNLK) to 234.
9. In one transaction:
   a. Erase the contents of the EEPROM by setting NVMERASE (R171[1]) to 1.
   b. Initiate EEPROM programming to transfer the SRAM contents to EEPROM by setting NVMPROG (R171[0]) to 1.
   c. **Note:** Step 5 & 6 must be atomic (back-to-back) writes without any other register transactions in-between. Serial communication interruptions (such as access to other devices on the same bus) is also not allowed for successful EEPROM programming.
10. Wait for EEPROM programming to finish by polling R171[2] (NVMBUSY) until cleared or wait about 500ms.
    a. **Note:** Do not power down, PD# toggle, or continue to the next step until NVMBUSY is cleared to have a successful EEPROM programming.
11. Lock the EEPROM by setting NVMUNLK to 0.
12. At the next POR, if the EEPROM programming is successful, the EEPROM program count, R16 (NVMCNT), increments by 1. Also, if the EEPROM overlay bit is set, the active registers are loaded from EEPROM.

Hex instruction example for changing the TARGET_ADR_MSB:

```
R171        0x00AB40          # Set REGCOMMIT (Mixed Method only)
R20         0x001480          # Enable EEPROM OVERLAY
R173        0x00AD00          # Set 5 MSBs of SRAM address
R174        0x00AE0C          # Set 8 LSBs of SRAM address
R176        0x00B019          # Set 5 MSBs of desired I2C address

R180        0x00B4EA          # UNLOCK EEPROM
R171        0x00AB03          # ERASE and PROGRAM SRAM contents to EEPROM
while(READ_REG(NVMBUSY) != 0) # NVMBUSY is located in 0xAB, bit 2
R180        0x00B400          # Lock EEPROM
```

Hex instruction example for changing the EEREV:

8.5.4.4 Five MSBs of the I2C Address and the EEPROM Revision Number

Table 8-14 summarizes the SRAM and EEPROM addresses of the TARGET_ADR_MSB and EEREV fields. These bytes can **only** be written by EEPROM Programming With the Direct Writes Method or Mixed Method. Modifying these bytes from the factory default settings is optional.

Table 8-14. User-Programmable Fields in EEPROM

SRAM/EEPROM ADDRESS BYTE # (DECIMAL)	SRAM/EEPROM ADDRESS BYTE # (HEX)	SRAM/EEPROM FIELD NAME	DESCRIPTION
12	0x0C	TARGET_ADR_MSB	**I²C Target Address MSB Bits** TARGET_ADR_MSB[7:3] can be written to set the five MSBs of the 7-bit peripheral address. TARGET_ADR_MSB[2:0] must be written with zeros. TARGET_ADR_MSB can only be modified by programming the SRAM and EEPROM. The TARGET_ADR_MSB value that is currently used by the device can be readback by the read-only register, R18. For more I²C address details, refer to GPIO1 and SCS_ADD Functionalities and I²C Serial Interface.

Table 8-14. User-Programmable Fields in EEPROM (continued)

SRAM/EEPROM ADDRESS BYTE # (DECIMAL)	SRAM/EEPROM ADDRESS BYTE # (HEX)	SRAM/EEPROM FIELD NAME	DESCRIPTION
13	0x0D	EEREV	**EEPROM Image Revision Number.** EEREV can be written to set the EEPROM image revision number or any customer-specific data for part traceability. EEREV can only be modified by programming the SRAM and EEPROM. The EEREV value that is currently used by the device can be readback by the read-only register, R19.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Device Start-Up Sequence

Device Power-On Reset (POR) shows the device start-up sequence.

9.1.2 Power Down (PD#) Pin

The PD# pin (active low) can be used for device power down and used to initialize the POR sequence. When PD# is pulled low, the entire device is powered down and the serial interface is disabled. When PD# is pulled high, the device POR sequence is triggered to begin the device start-up sequence and normal operation as depicted in Table 9-1. If the PD# pin is toggled to issue a momentary hard-reset, the negative pulse applied to the PD# pin must be greater than 200ns to be captured by the internal digital system clock.

Table 9-1. PD# Control

PD# PIN STATE	DEVICE OPERATION
0	Device is disabled
1	Normal operation

9.1.3 Strap Pins for Start-Up

At start-up, voltage level on GPIOs determine the operation mode of the device. GPIO1 selects SPI or I^2C mode. GPIO2 and GPIO0 select ROM page.

9.1.4 Pin States

Table 9-2 shows the different pin states of the device.

Table 9-2. Pin States in Different Stages

PIN NAME	POWER DOWN	STATES	POR (SPI)	STATES	POR (I^2C)	STATES	NORMAL OPERATION	STATES	SOFT RESET	STATES
PD#	LOW	2-level input	PD# transitions LOW to HIGH		PD# transitions LOW to HIGH		HIGH	2-level input	HIGH	2-level input
GPIO0	Ready for POR	3-level input	EEPROM/ ROM select	3-level input	EEPROM/ ROM select	3-level input	See table	GPIO	N/A	
GPIO1	Ready for POR	2-level input	VDD	2-level input	GND	2-level input	See table	GPIO	N/A	

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Table 9-2. Pin States in Different Stages (continued)

PIN NAME	POWER DOWN	STATES	POR (SPI)	STATES	POR (I^2C)	STATES	NORMAL OPERATION	STATES	SOFT RESET	STATES
GPIO2	Ready for POR	3-level input	EEPROM/ ROM select	3-level input	EEPROM/ ROM select	3-level input	See table	GPIO	N/A	
SCS_A DD	Ready for POR	3-level input	SCS	2-level input	I^2C address select	3-level input	2-level or 3-level input based on POR		N/A	
SDIO	N/A		SDIO	Data I/O	SDA	Data I/O	SDIO or SDA control interface serial data input/ output based on POR			
SCK	N/A		SCK	Clock input	SCL	Clock input	SCK or SCL control interface serial clock input based on POR			

9.1.5 ROM and EEPROM

Some applications require start-up clocks to operate the entire system at power on. Other applications can only require a valid clock for the logic device (CPU, ASIC, or FPGA) at power on which can then program the LMK5C33414AS1 with custom settings if the default ROM configuration does not meet the application requirements. The LMK5C33414AS1 provides ROM pages to support default output clocks on start-up and an EEPROM to allow customization of the start-up clocks if the ROM pages do not meet the application requirements. See *ROM Detailed Description* and *EEPROM Overlay* for more information.

9.1.6 Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains

9.1.6.1 Power-On Reset (POR) Circuit

The LMK5C33414AS1 integrates a built-in power-on reset (POR) circuit that holds the device in reset until all of the following conditions have been met:

- All V_{DD} core supplies have ramped above 2.72V
- PD# pin has ramped above 1.2V (minimum V_{IH})

9.1.6.2 Power Up From a Single-Supply Rail

As long as all VDD and VDDO supplies are driven by the same 3.3V supply rail that ramp in a monotonic manner from 0V to 3.135V, and the time between decision point 2 and stabilized supply voltage is less than 1ms, then there is no requirement to add a capacitor on the PD# pin to externally delay the device power-up sequence. Figure 9-1 shows that the PD# pin can be left floating or otherwise driven by a system host to meet the clock sequencing requirements in the system.

If time between decision point 2 and stabilized supply voltage is greater than 1ms, then the PD# pin must be delayed. Refer to *Power Up From Split-Supply Rails*.

As described in *Slow or Delayed XO Start-Up*, validating the XO reference after PD# decision point 1 is necessary to provide a successful calibration of the VCOs and to capture a valid DPLL reference reading.

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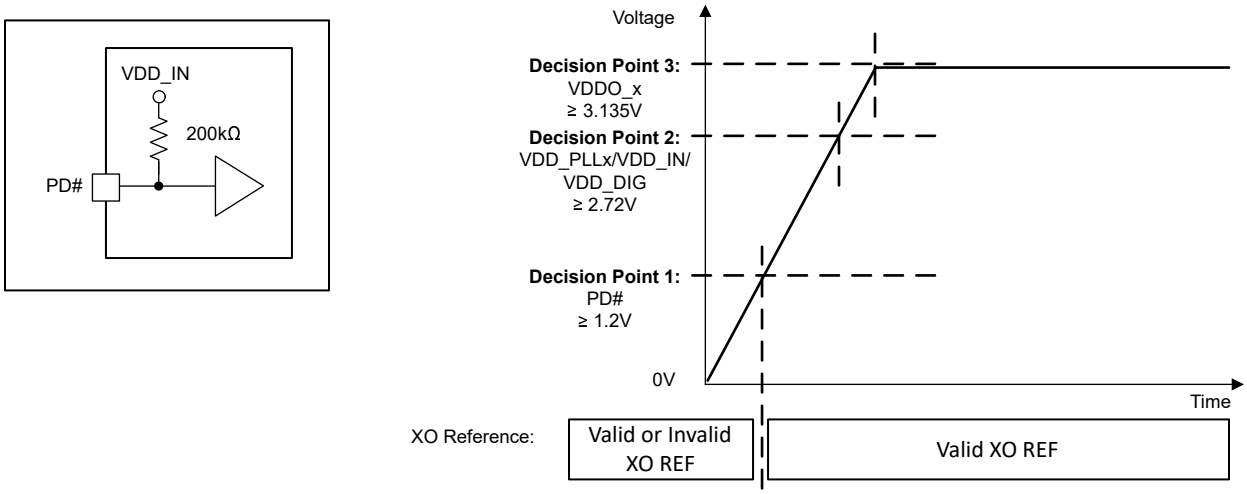

Figure 9-1. Recommendation for Power Up From a Single-Supply Rail

9.1.6.3 Power Up From Split-Supply Rails

If VDD or VDDO supplies are driven from different supply sources, TI recommends to start the PLL calibration after all of the supplies have ramped above 3.135V. This can be realized by delaying the PD# low-to-high transition. The PD# input incorporates a 200kΩ resistor to VDD_IN and as shown in Figure 9-2. A capacitor from the PD# pin to GND can be used to form an RC time constant with the internal pullup resistor. This RC time constant can be designed to delay the low-to-high transition of PD# until all the core supplies have ramped above 3.135V. Ramping the VDDO supply pins before the VDD supply pins is recommended.

Alternatively, the PD# pin can be driven high by a system host or power management device to delay the device power-up sequence until all supplies have ramped.

As described in *Slow or Delayed XO Start-Up*, the XO reference must be valid after PD# decision point 3 to provide a successful calibration of the VCOs and to capture a valid DPLL reference reading.

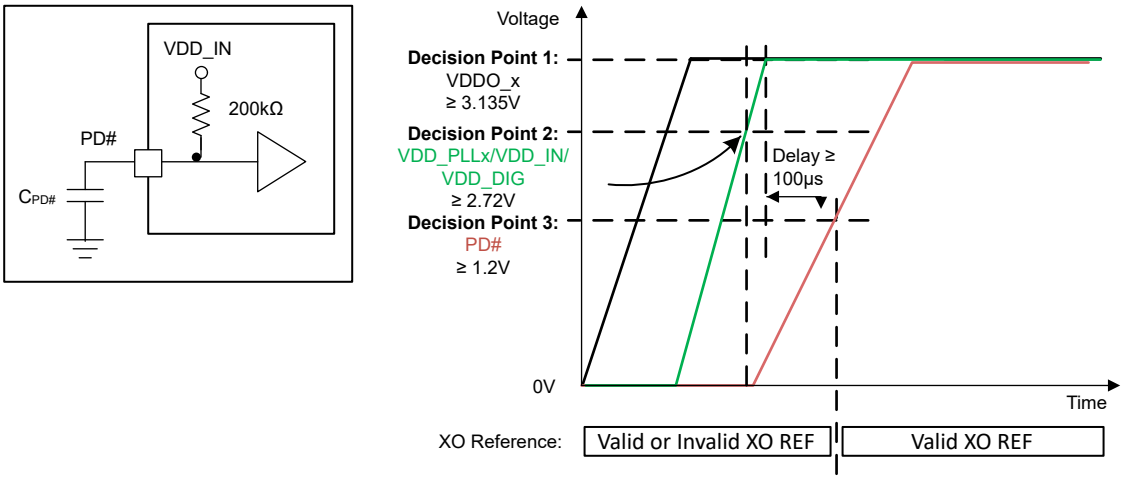

Figure 9-2. Recommendation for Power Up From Split-Supply Rails

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9.1.6.4 Non-Monotonic or Slow Power-Up Supply Ramp

In case the VDD core supplies ramp with a non-monotonic manner or with a slow ramp time from 0V to 3.135V of over 100ms, TI recommends to delay the VCO calibration until after all of the core supplies have ramped above 3.135V. This cam be achieved by delaying the PD# low-to-high transition with one of the methods described in *Power Up From Split-Supply Rails*.

If any core supply cannot ramp above 3.135V before the PD# low-to-high transition, issuing a device soft-reset after all core supplies have ramped is acceptable to manually trigger the VCO calibration and PLL start-up sequence.

9.1.7 Slow or Delayed XO Start-Up

Because the external XO clock input is used as the reference input for the BAW APLL and conventional APLL calibration, the XO input amplitude and frequency must be stable before the start of VCO calibration to provide successful PLL lock and output start-up. If the XO clock is not stable prior to VCO calibration, the VCO calibration can fail and prevent PLL lock and output clock start-up.

If the XO clock has a slow start-up time or has glitches on power-up (due to a slow or non-monotonic power supply ramp, for example), TI recommends to delay the start of VCO calibration until after the XO is stable. This can be achieved by delaying the PD# low-to-high transition until after the XO clock has stabilized using one of the methods described in *Power Up From Split-Supply Rails*. Issuing a device soft-reset is also possible after the XO clock has stabilized to manually trigger the VCO calibration and PLL start-up sequence.

The BAW APLL and VCBO is factory calibrated and is not sensitive to an invalid XO reference start-up. Upon a valid XO reference, the BAW APLL can acquire lock. When the BAW APLL is used in conjunction with the paired DPLL, the XO must be valid before the paired DPLL reference is validated.

9.2 Typical Application

Figure 9-3 shows a reference schematic to help implement the LMK5C33414AS1 and the peripheral circuitry. Power filtering examples are given for the core supply pins and independent output supply pins. Single-ended LVCMOS and differential LVDS, HSDS, AC-LVPECL, and HCSL clock interfacing examples are shown for the clock input and output pins. An external LVCMOS oscillator drives an AC-coupled voltage divider network as an example to interface the 3.3V LVCMOS output to meet the input voltage swing specified for the XO input. The XO pin of the LMK5C33414AS1 can accept 3.3V LVCMOS input. The required external capacitors are placed close to the network synchronizer and are shown with the suggested values. External pullup and pulldown resistor options at the logic I/O pins set the default input states. The I^2C or SPI pins and other logic I/O pins can be connected to a host device (not shown) to program and control the network synchronizer and monitor the status.

Figure 9-3. Typical Application Example

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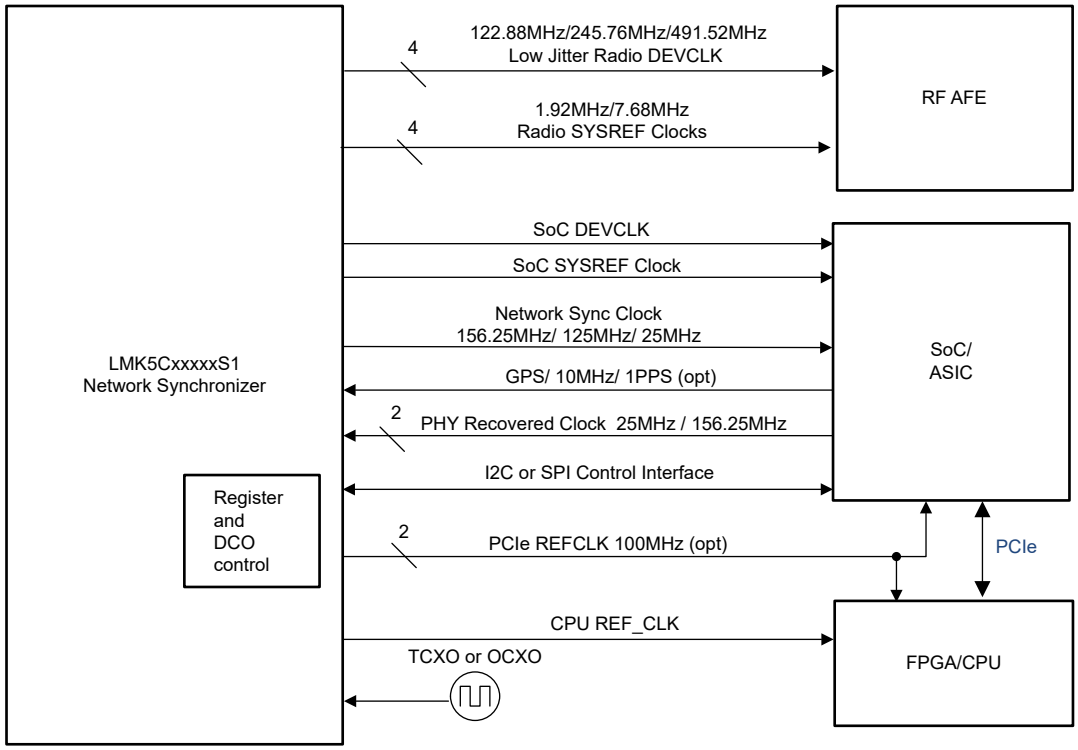

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9.2.1 Design Requirements

In a typical application, consider the following design requirements or parameters to implement the overall clock design:

1. Device initial configuration. The device must be configured as either host programmed (MCU or FPGA) or factory preprogrammed.
2. Device interface, set GPIO1 as desired for I^2C or SPI communications interface.
3. XO frequency, signal type, and frequency accuracy and stability. Consider a high-stability TCXO or OCXO for the XO input if any of the following is required:
   a. Standard-compliant frequency stability (such as SyncE, SONET/SDH, IEEE 1588)
   b. Lowest possible close-in phase noise at offsets ≤ 100Hz
   c. Narrow DPLL bandwidth ≤ 10Hz
4. For each DPLL/APLL domain, determine the following:
   a. Input clocks: frequency, buffer mode, priority, and input selection mode
   b. APLL reference: another VCO with Cascaded mode, or XO for Non-cascaded mode
   c. Output clocks: frequency, buffer mode
   d. DPLL loop bandwidth and maximum TDC frequency
   e. If the DCO Mode or ZDM is required
5. Input clock and PLL monitoring options
6. Status outputs and interrupt flag
7. Power supply rails

9.2.2 Detailed Design Procedure

In a typical application, the following steps are recommended:

1. Use the device GUI in the TICS Pro programming software for a step-by-step design flow to enter the design parameters, calculate the frequency plan for each PLL domain, and generate the register settings for the desired configuration. The register settings can be exported (registers hex dump in .txt format) to enable host programming.
   - A host device can program the register settings through the serial interface after power-up and issue a soft-reset (by SWRST bit) to start the device. Set SW_SYNC before, and clear after SWRST.
2. Tie the GPIO1 pin to ground to select the I^2C communications interface, or pull up GPIO1 high to VDD_DIG through an external resistor to select the SPI communications interface. Determine the logic I/O pin assignments for control and status functions. See GPIO1 and SCS_ADD Functionalities.
   - Connect I^2C/SPI and logic I/O pins (1.8V compatible levels) to the host device pins with the proper I/O direction and voltage levels.
3. Select an XO frequency by following *Oscillator Input (XO)*.
   - Choose an XO with target phase jitter performance that meets the frequency stability and accuracy requirements required for the output clocks during free-run or holdover.
   - The LMK5C33414AS1 can directly accept a 3.3V LVCMOS input into the XO pin.
   - Power the XO from a low-noise LDO regulator or optimize the power filtering to avoid supply noise-induced jitter on the XO clock.
   - **TICS Pro:** Configure the XO frequency to match the XO input.

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4. Wire the clock I/O for each APLL domain in the schematic and use TICS Pro to configure the device settings as follows:
   - Reference inputs: Follow the LVCMOS or differential clock input interface guidelines in *Clock Input Interfacing and Termination*.
     - **TICS Pro:** For DPLL mode, configure the reference input buffer modes to match the reference clock driver interface requirements. See *Reference Inputs*.
   - **TICS Pro:** For DPLL mode, configure the DPLL input selection modes and input priorities. See *Reference Input Mux Selection*.
   - **TICS Pro:** Configure each APLL reference from other VCO domain (Cascaded mode) or XO clock (Non-cascaded mode).
   - **TICS Pro:** Configure each output with the required clock frequency and APLL domain. TICS Pro can calculate the VCO frequencies and divider settings for the APLL and outputs. Consider the following output clock assignment guidelines to minimize crosstalk and spurs:
     - Group identical output frequencies (or harmonic frequencies) on adjacent channels and use the output pairs with a single divider (for example, OUT2/OUT3) when possible to minimize power.
     - Separate clock outputs when the difference of the two frequencies, $|f_{OUTx} – f_{OUTy}|$, falls within the jitter integration bandwidth (for example, 12kHz to 20MHz). Any outputs that are potential aggressors must be separated by at least four static pins (power pin, logic pin, or disabled output pins) to minimize potential coupling. If possible, separate these clocks by the placing them on opposite output banks, which are on opposite sides of the chip for best isolation.
     - Avoid or isolate any LVCMOS output (strong aggressor) from other jitter-sensitive differential output clocks. If an LVCMOS output is required, use dual complementary LVCMOS mode (+/- or -/+) with the unused LVCMOS output left floating with no trace.
     - If not all outputs pairs are used in the application, consider connecting an unused output to a pair of RF coaxial test structures for testing purposes (such as SMA, SMP ports).
   - **TICS Pro:** Configure the output drivers.
     - Configure the output driver modes to match the receiver clock input interface requirements. See *Clock Output Drivers*.
     - Configure any output SYNC groups that need the output phases synchronized. See *Output Synchronization (SYNC)*.
     - Configure the output auto-mute modes, and APLL and DPLL mute options. See *Output Auto-Mute During LOL*.
   - Clock output Interfacing: Follow the single-ended or differential clock output interface guidelines in *Clock Output Interfacing and Termination*.
     - Differential outputs can be AC-coupled and terminated and biased at the receiver inputs, or DC-coupled with proper receivers
     - LVCMOS outputs have internal source termination to drive 50Ω traces directly. LVCMOS V_{OH} level is determined by internal LDO programmed voltage (1.8V or 2.65V).
   - **TICS Pro:** Configure the DPLL loop bandwidth.
     - Below the loop bandwidth, the reference noise is added to the TDC noise floor and the XO/TCXO/OCXO noise. Above the loop bandwidth, the reference noise is attenuated with roll-off up to 60dB/decade. The optimal bandwidth depends on the relative phase noise between the reference input and the XO. The APLL loop bandwidth can be configured to provide additional attenuation of the reference input, TDC, and XO phase noise above the APLL bandwidth.
   - **TICS Pro:** Configure the maximum TDC frequency to optimize the DPLL TDC noise contribution for the desired use case.
     - *Wired*: A 400kHz maximum TDC rate is commonly specified. This supports SyncE and other use cases using a narrow loop bandwidth (≤10Hz) with a TCXO/OCXO/XO to set the frequency stability and wander performance.
     - *Wireless*: A 26MHz maximum TDC rate is commonly specified for lowest in-band TDC noise contribution. This supports wireless and other use cases where close-in phase noise is critical.
   - **TICS Pro:** If clock steering is needed (such as for IEEE-1588 PTP), enable DCO mode for the DPLL loop and enter the frequency step size (in ppb). The FDEV step register is computed according to *APLL DCO Frequency Step Size*. Enable the FDEV_TRIG and FDEV_DIR pin control on the GPIO pins if needed.

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- **TICS Pro:** If deterministic input-to-output clock phase is needed, configure ZDM for the corresponding OUTx. See *Section 8.3.20*.

5. **TICS Pro:** Configure the reference input monitoring options for each reference input. Disable the monitor when not required or when the input operates beyond the monitor's supported frequency range. See *Reference Input Monitoring*.
   - *Frequency monitor*: Set the valid and invalid thresholds (in ppm).
   - *Missing pulse monitor*: Set the late window threshold (T_{LATE}) to allow for the longest expected input clock period, including worst-case cycle-to-cycle jitter. For a gapped clock input, set T_{LATE} based on the number of allowable missing clock pulses.
   - *Runt pulse monitor*: Set the early window threshold (T_{EARLY}) to allow for the shortest expected input clock period, including worst-case cycle-to-cycle jitter.
   - *1PPS Phase validation monitor*: Set the phase validation jitter threshold, including worst-case input cycle-to-cycle jitter.
   - *Validation timer*: Set the amount of time the reference input must be qualified by all enabled input monitors before the input is valid for selection.
6. **TICS Pro:** Configure the DPLL lock detect and tuning word history monitoring options for each channel. See *PLL Lock Detectors* and *Tuning Word History*.
   - *DPLL frequency lock and phase lock detectors*: Set the lock and unlock thresholds for each detector.
7. **TICS Pro:** Configure each status output pin and interrupt flag as needed. See *Status Outputs* and *Interrupt*.
   - Select the desired status signal selection, status polarity, and driver mode (3.3V LVCMOS or open-drain). Open-drain requires an external pullup resistor.
   - If the Interrupt is enabled and selected as a status output, configure the flag polarity and the mask bits for any interrupt source, and the combinational OR gate, as needed.
8. Consider the following guidelines for designing the power supply:
   - Outputs with identical frequency or integer-related (harmonic) frequencies can share a common filtered power supply.
     - Example: 156.25MHz and 312.5MHz outputs on OUT5 and OUT6 can share a filtered VDDO supply, while 100MHz and 122.88MHz outputs on OUT0 and OUT3 can share a separate VDDO supply.
   - See *Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains*.

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9.2.3 Application Curves

Refer to the Typical Characteristics section for phase noise plots as outlined in the Table 9-3.

Table 9-3. Output Clock Phase Noise Plot Summary

Output Frequency [MHz]	Output Format	APLL Source	Link to Graph
491.52MHz	HSDS	BAW	Go
245.76MHz	HSDS	BAW	Go
122.88MHz	HSDS	BAW	Go
312.5MHz	HSDS	Conventional LC (APLL2)	Go
322.265625MHz	HSDS	Conventional LC (APLL2)	Go
212.5MHz	HSDS	Conventional LC (APLL2)	Go
161.1328125MHz	HSDS	Conventional LC (APLL2)	Go
155.52MHz	HSDS	Conventional LC (APLL2)	Go
153.6MHz	HSDS	Conventional LC (APLL2)	Go
312.5MHz	HSDS	Conventional LC (APLL1)	Go
100MHz	HSDS	Conventional LC (APLL1)	Go
50MHz	HSDS	Conventional LC (APLL1)	Go

9.3 Best Design Practices

- Power down unused blocks through registers to minimize power consumption.
- Use proper source or load terminations to match the impedance of input and output clock traces for any active signals to/from the device.
- Leave unused clock outputs floating and powered down through register control.
- Leave unused clock inputs floating.
- If needed, external biasing resistors (10kΩ pullup to 3.3V or 10kΩ pulldown) can be connected on each GPIO pin to select device operation mode during POR.
- Consider routing each GPIO pin to a test point or high-impedance input of a host device to monitor device status outputs.
- Consider using a LDO regulator to power the external XO/TCXO/OCXO source.
  - High jitter and spurious on the oscillator clock are often caused by high spectral noise and ripple on the power supply.
- Include dedicated header to access the I^2C or SPI of the device, as well as a header pin for ground.
  - This can enabled off-board programming for device bring-up, prototyping, and diagnostics using the TI USB2ANY interface and TICS Pro software tools.

9.4 Power Supply Recommendations

9.4.1 Power Supply Bypassing

Figure 9-4 shows two general placements of power supply bypass capacitors on either the back side or the component side of the PCB. If the capacitors are mounted on the back side, 0402 components can be employed. For component side mounting, use 0201 body size capacitors to facilitate signal routing. A combination of component side and back side placement can be used. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

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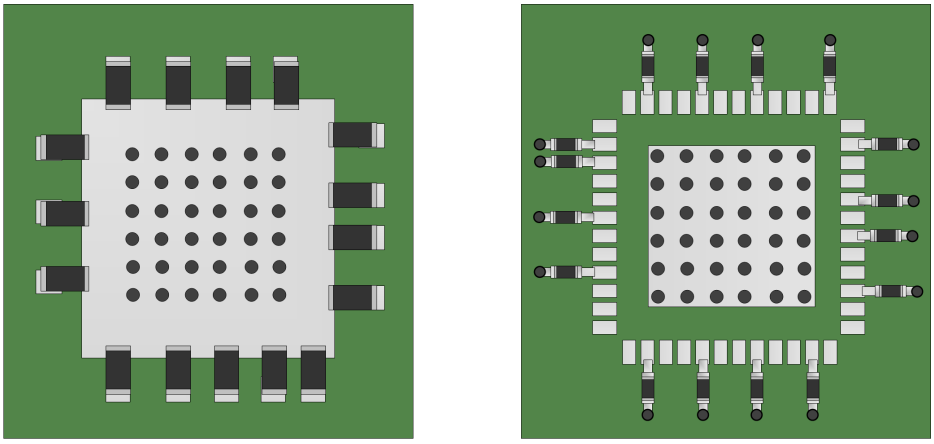

(**Does not** indicate actual location of the device supply pins)

Figure 9-4. Generalized Placement of Power Supply Bypass Capacitors

9.5 Layout

9.5.1 Layout Guidelines

- Isolate input, XO/OCXO/TCXO and output clocks from adjacent clocks with different frequencies and other nearby dynamic signals.
- Consider the XO/OCXO/TCXO placement and layout in terms of the supply/ground noise and thermal gradients from nearby circuitry (for example, power supplies, FPGA, ASIC) as well as system-level vibration and shock. These factors can affect the frequency stability/accuracy and transient performance of the oscillator.
- Avoid impedance discontinuities on controlled-impedance 50Ω single-ended (or 100Ω differential) traces for clock and dynamic logic signals.
- Place bypass capacitors close to the VDD and VDDO pins on the same side as the IC, or directly below the IC pins on the opposite side of the PCB. Larger decoupling capacitor values can be placed further away.
- Place external capacitors close to the CAP_x and LFx pins.
- Use multiple vias to connect wide supply traces to the respective power islands or planes if possible.
- Use at least a 6×6 through-hole via pattern to connect the IC ground/thermal pad to the PCB ground planes.
- See the Land Pattern Example, Solder Mask Details, and Solder Paste Example in *Mechanical, Packaging, and Orderable Information* section.

9.5.2 Layout Example

Below are printed circuit board (PCB) layout examples that show the application of thermal design practices and a low-inductance ground connection between the device DAP and the PCB. Place the ground return path for the supply decoupling capacitors close to the DAP. All OUTx pairs configured as differential signals must be routed differentially and meet the trace impedance requirements (typically 100 ohm differential).

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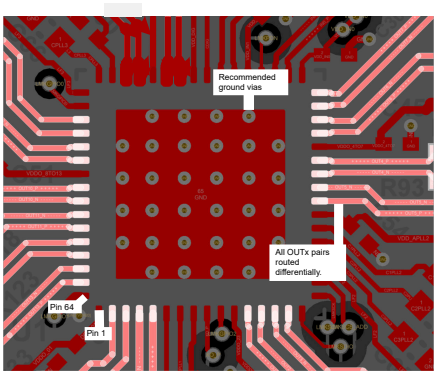

Figure 9-5. PCB Layout Example for LMK5C33414AS1, Top Layer

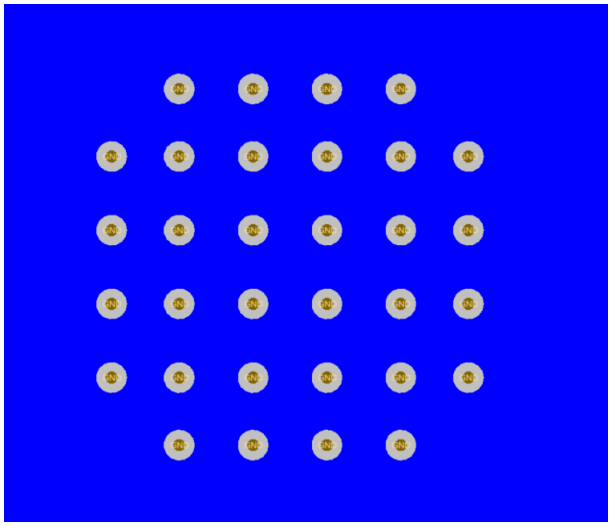

Figure 9-6. PCB Layout Example for LMK5C33414AS1, Bottom Layer

9.5.3 Thermal Reliability

The LMK5C33414AS1 is a high-performance device. To provide good electrical and thermal performance, TI recommends to design a thermally-enhanced interface between the IC ground or thermal pad and the PCB ground using at least a 6×6 through-hole through pattern connected to multiple PCB ground layers (see Figure 9-7).

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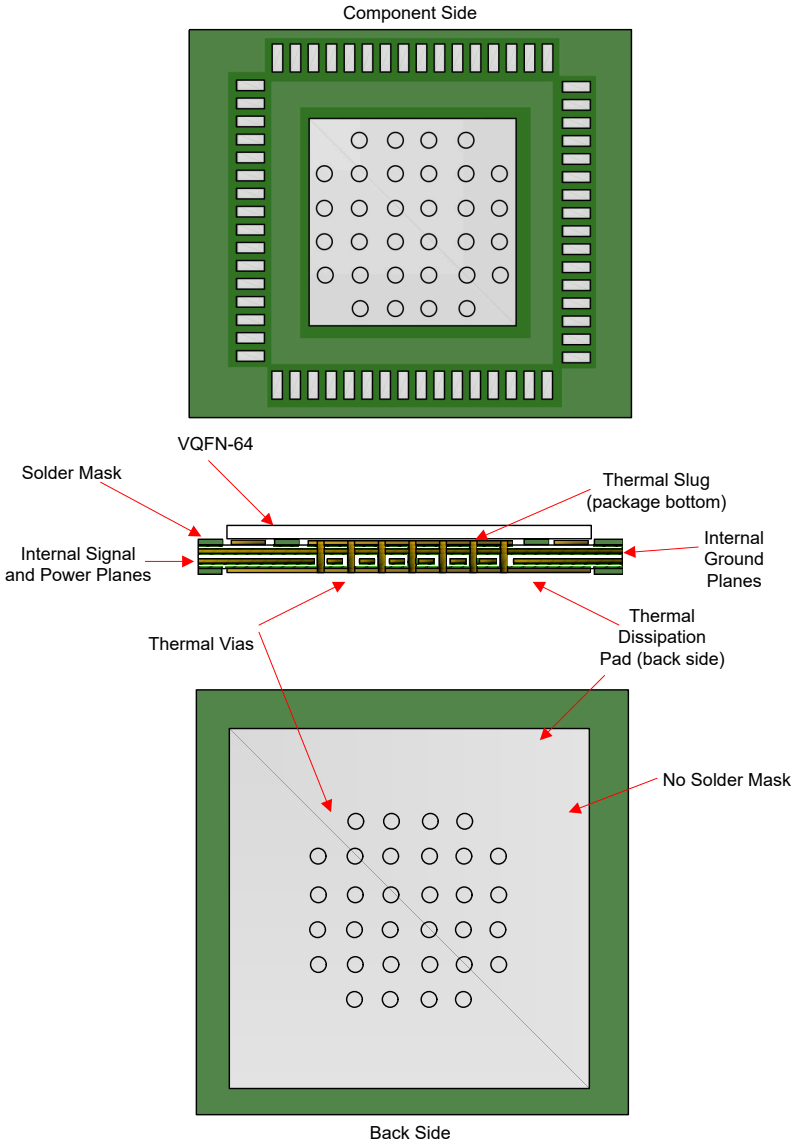

Figure 9-7. General PCB Ground Layout for Thermal Reliability (8+ Layers Recommended)

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 Clock Tree Architect Programming Software

The Clock Tree Architect is a clock tree synthesis tool that streamlines your design process by generating clock tree solutions based on your system requirements. The tool pulls data from an extensive database of clocking products to generate a system-level multi-chip clocking solution.

10.1.1.2 Texas Instruments Clocks and Synthesizers (TICS) Pro Software

The Texas Instruments clocks and synthesizers (TICS) Pro software is used to program the evaluation modules (EVMs) for product numbers with these prefixes: CDC, LMK and LMX. These products include phase-locked loops and voltage-controlled oscillators (PLL+VCO), synthesizers and clocking devices.

10.1.1.3 PLLatinum™ Simulation Tool

PLLATINUMSIM-SW PLLatinum™ simulation tool that allows users to create detailed designs and simulations of our PLLatinum™ integrated circuits, which include the LMK and LMX series of phase-locked loops (PLLs) and synthesizers.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, LMK5C33414AEVM User's Guide
- Texas Instruments, *LMK5B33216 Programmer's Guide*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2022) to Revision A (February 2025) **Page**

- Updated the number formatting for tables, figures, and cross-references throughout the document. 1
- Corrected output format type from LVPECL to AC-LVPECL throughout the document. 1
- Added typical RMS jitter with 4MHz HPF to *Features* section. 1
- Updated the numbering and formatting for tables, figures, and cross-references throughout the document. 1
- Clarified the *Description* section. 1
- Added the *Device Comparison* section. 4
- Clarified the VDD and VDDO supply pin requirements. 5
- Changed the recommended CAP_DIG capacitor value from 100nF to 10µF. 5
- Renamed "APLL3" to "BAW APLL" throughout the document. 5
- Clarified footnote 1 of the *Absolute Maximum Ratings* table. 8
- Changed from "JEDEC" to "AINSI/ESDA/JEDEC" for CDM parameter in the *ESD Ratings* table. 8
- Added the operating ambient temperature to the *Recommended Operating Conditions* . 8
- Corrected hyperlink in the *Thermal Information* table. 8
- Clarified test conditions in the *Electrical Characteristics* table. 8
- Updated the *Overview* section. 27
- Updated the *Functional Block Diagram* . 28
- Updated the *PLL Architecture Overview* section. 29
- Updated the *DPLL* section. 30
- Updated the *Independent DPLL Operation* section. 31
- Updated the *Cascaded DPLL Operation* section. 33
- Updated the *APLL Cascaded With DPLL* section. 35
- Added hysteresis and register information to the *Reference Input Buffer Modes* table. 40
- Added AC-coupled differential to reference diagram to the *Clock Input Interfacing and Termination* section. 41
- Updated the LVCMOS diagram in the *Clock Input Interfacing and Termination* section. 41
- Updated the *XO Input Monitoring* section. 45
- Updated the *APLL XO Reference (R) Divider* section. 53
- Added default APLL loop filter and loop bandwidth table to the *Analog Loop Filters* section. 53
- Added the *Output Source Muxes* section. 56
- Updated the *Output Channel Muxes* section. 56
- Updated by combining *SYSREF/1PPS Output Replication* into the *SYSREF/1PPS Output* section. 57
- Changed *Clock Outputs (OUTx_P/ N)* title to *Clock Output Drivers* and rearranged text. 58
- Clarified the differential output formats and added table to the *Differential Output* section. 58
- Clarified the *LVCMOS Output* section. 59
- Updated the *Zero-Delay Mode (ZDM)* section. 61
- Added the *DPLL Programmable Phase Delay* section. 62
- Updated the *Device Power-On Reset (POR)* section. 72
- Updated the *PLL Start-Up Sequence* section. 73
- Added the *Start-Up Options for Register Configuration* section. 74
- Added the *GPIO1 and SCS_ADD Functionalities* section. 74
- Added the ROM detailed description table to the *ROM Page Selection* section. 74
- Added the *ROM Detailed Description* section. 75
- Added the *Memory Overview* section. 76
- Added the *Programming Through TICS Pro* section. 77
- Updated the *General Register Programming Sequence* section. 80
- Added the *Steps to Program the EEPROM* section. 81
- Added the *Overview of the SRAM Programming Methods* section. 81
- Added the *EEPROM Programming With the Register Commit Method* section. 82
- Added the *EEPROM Programming With the Direct Writes Method or Mixed Method* section. 82

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- Added the *Five MSBs of the I2C Address and the EEPROM Revision Number* section..... 83
- Added the output phase noise plot summary table to the *Applications Curves* section..... 92

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK5C33414ARGCRS1	Active	Production	VQFN (RGC) | 64	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	LK5C33414A-S1
LMK5C33414ARGCRS1.A	Active	Production	VQFN (RGC) | 64	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	LK5C33414A-S1
LMK5C33414ARGCTS1	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	LK5C33414A-S1
LMK5C33414ARGCTS1.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	LK5C33414A-S1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

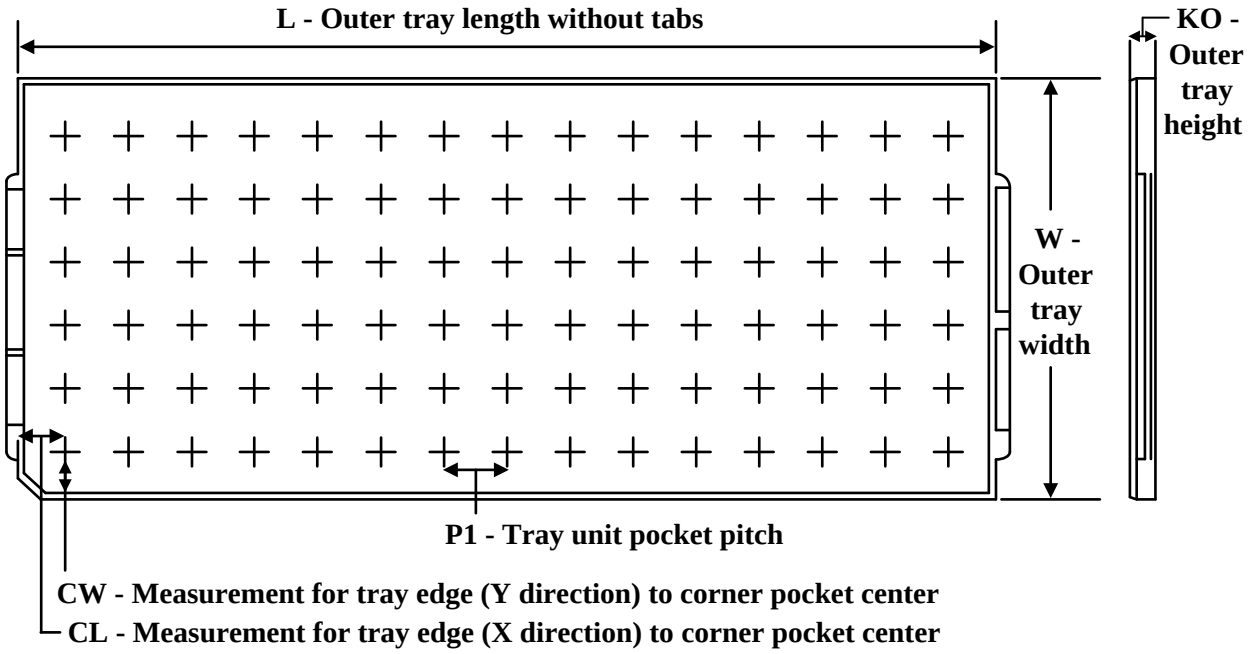
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LMK5C33414ARGCRS1	RGC	VQFN	64	2500	26 x 10	150	315	135.9	7620	11.8	10	10.35
LMK5C33414ARGCRS1.A	RGC	VQFN	64	2500	26 x 10	150	315	135.9	7620	11.8	10	10.35
LMK5C33414ARGCTS1	RGC	VQFN	64	250	26 x 10	150	315	135.9	7620	11.8	10	10.35
LMK5C33414ARGCTS1.A	RGC	VQFN	64	250	26 x 10	150	315	135.9	7620	11.8	10	10.35

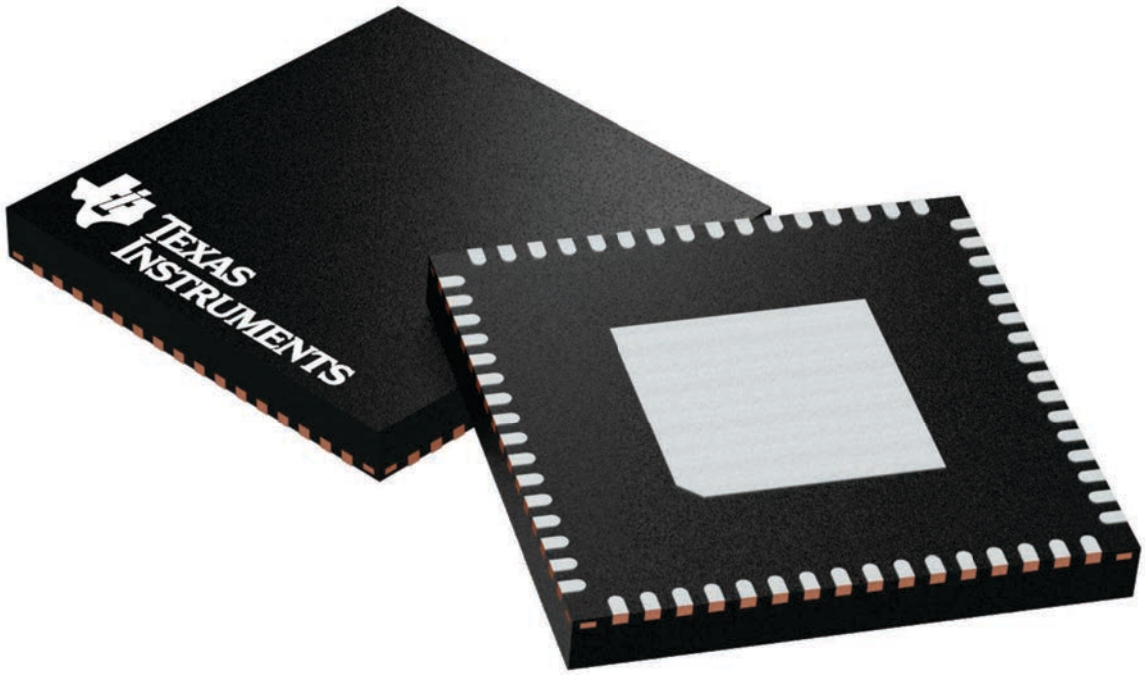
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

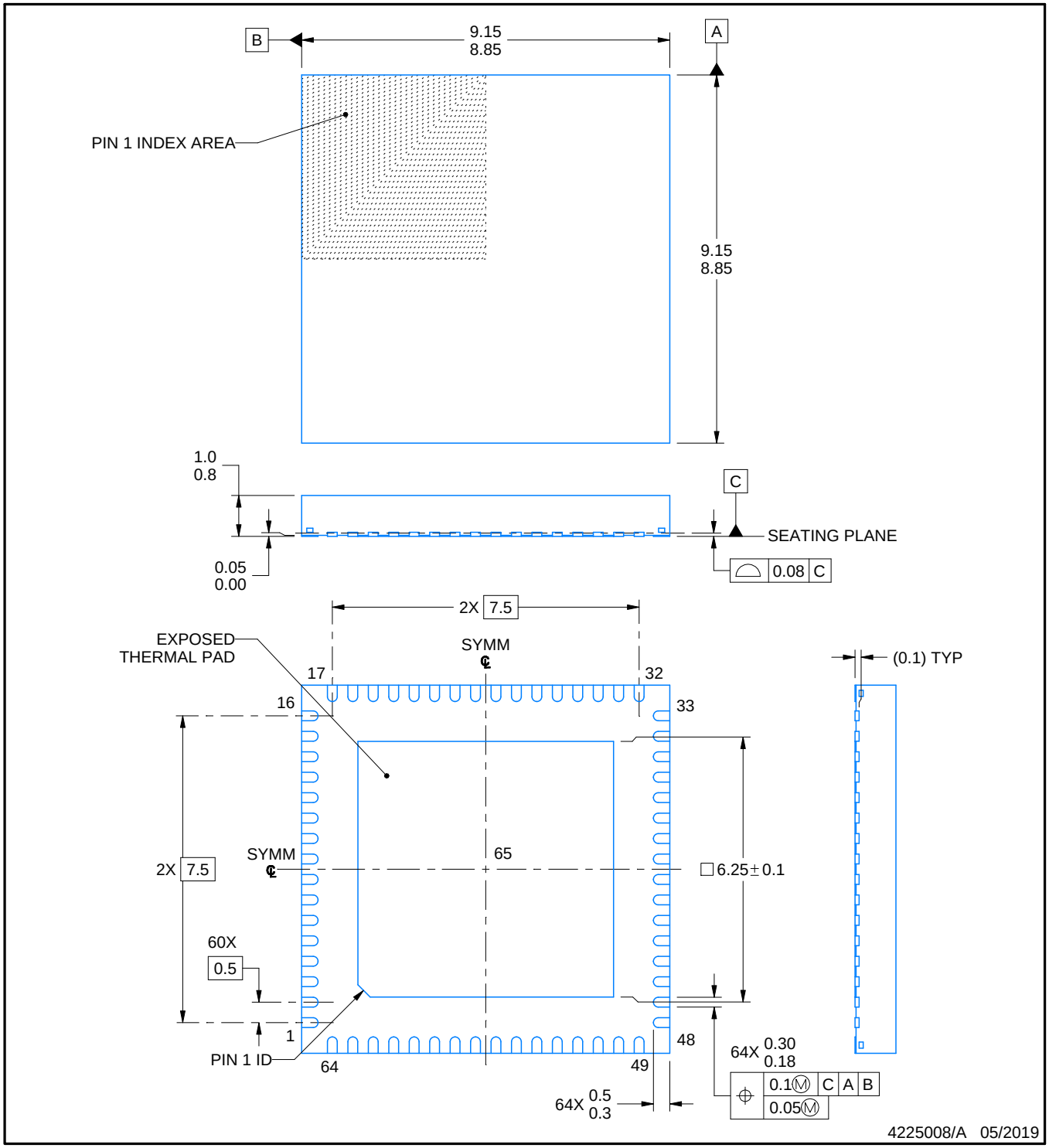
4224597/A

PACKAGE OUTLINE

RGC0064E

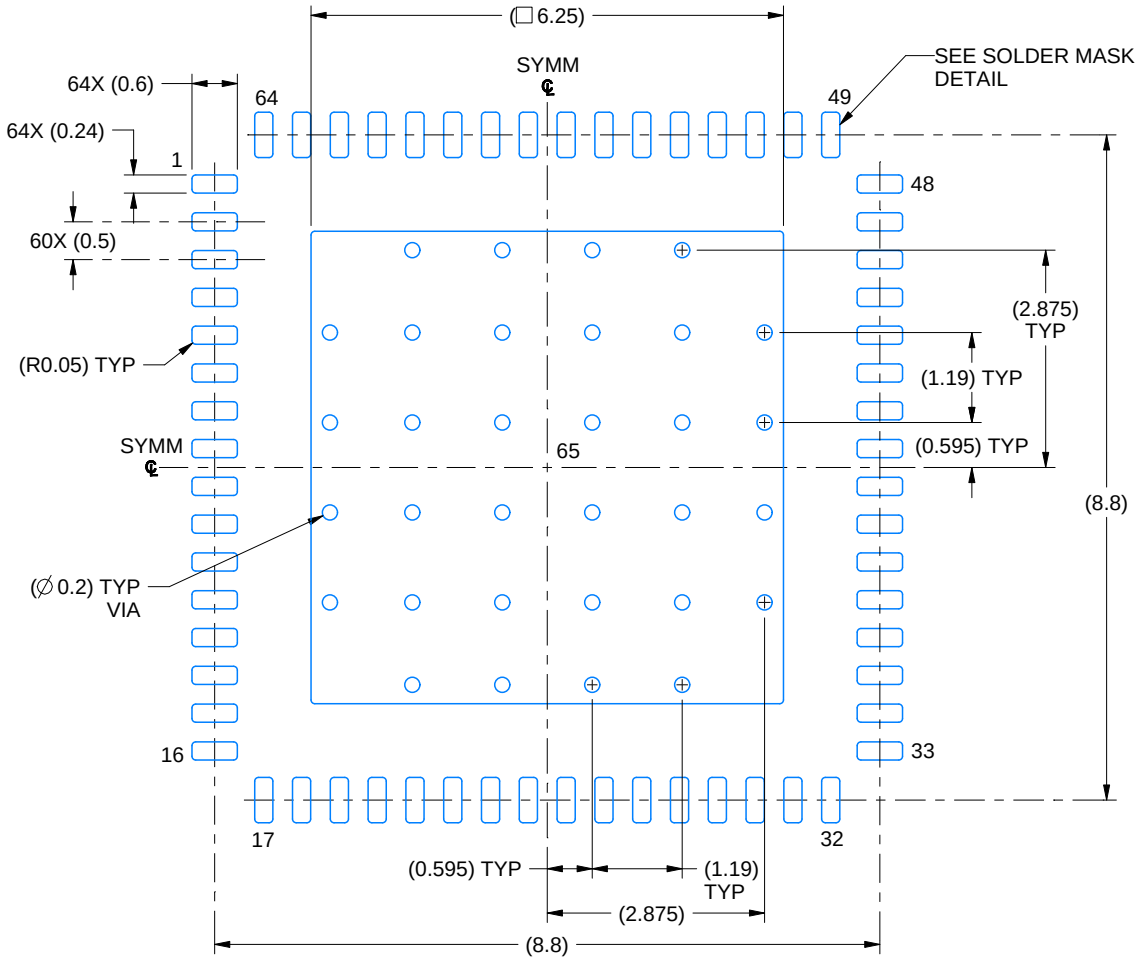
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

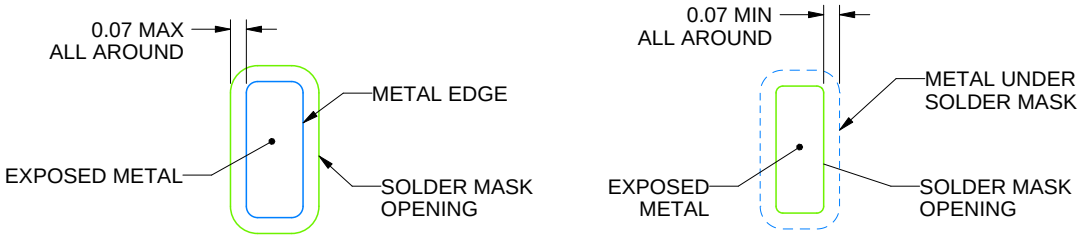


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

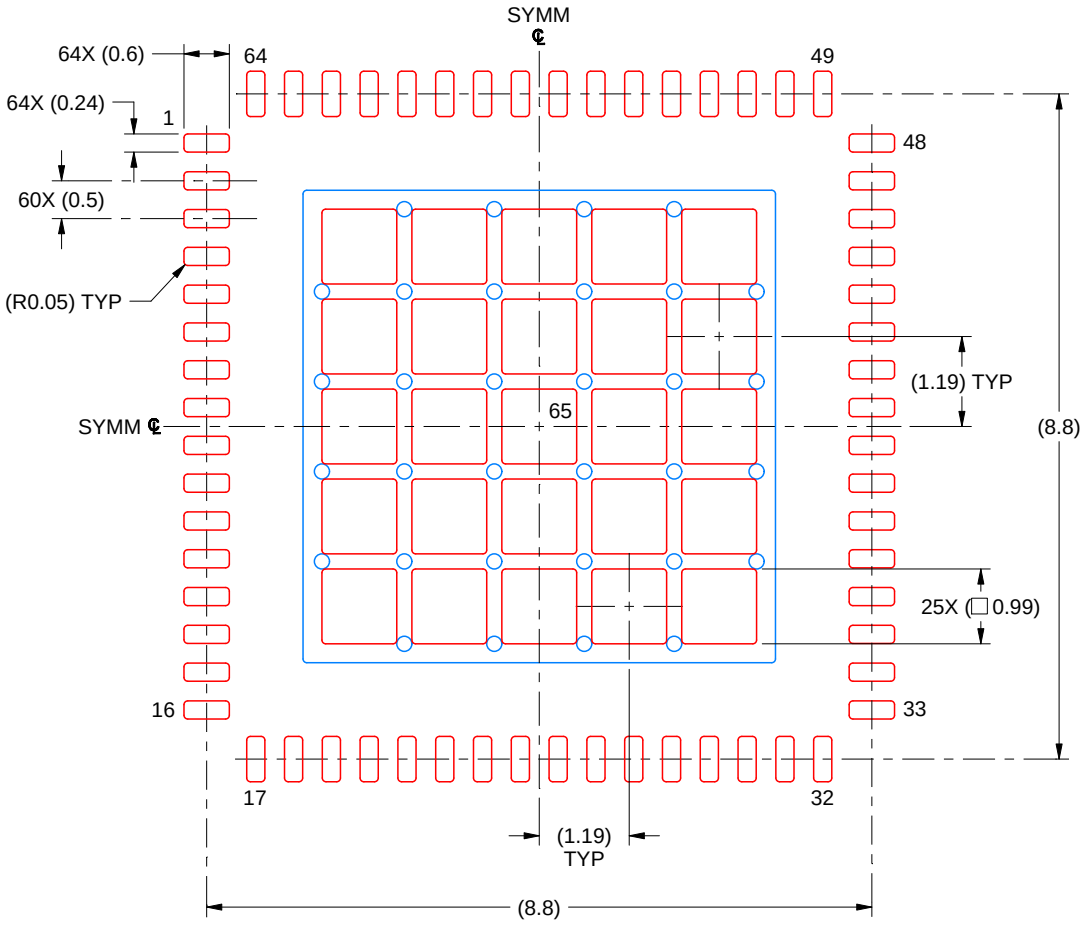


SOLDER MASK DETAILS

4225008/A 05/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225008/A 05/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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