LMX2485x 3-GHz Delta-Sigma Low-Power Dual PLLatinum™ Frequency Synthesizer

1 Features

- Quadruple Modulus Prescaler for Lower Divides
  - RF PLL: 8/9/12/13 or 16/17/20/21
  - IF PLL: 8/9 or 16/17
- Advanced Delta-Sigma Fractional Compensation
  - 12-Bit or 22-Bit Selectable Fractional Modulus
  - Up to 4th Order Programmable Delta-Sigma Modulator
- Features for Improved Lock Time
  - Fastlock / Cycle Slip Reduction With Integrated Time-Out Counter Which Requires Only a Single-Word Write
- Wide Operating Range
  - LMX2485 RF PLL: 500 MHz to 3.0 GHz
  - LMX2485E RF PLL: 50 MHz to 3.0 GHz
- Useful Features
  - Digital Lock Detect Output
  - Hardware and Software Power-Down Control
  - On-Chip Input Frequency Doubler.
  - RF Phase Detector Frequency up to 50 MHz
  - 2.5 to 3.6 V Operation With I_{CC} = 5.0 mA

2 Applications

- Cellular Phones and Base Stations
- Direct Digital Modulation Applications
- Satellite and Cable TV Tuners
- WLAN Standards

3 Description

The LMX2485 device is a low power, high performance delta-sigma fractional-N PLL with an auxiliary integer-N PLL. The device is fabricated using Texas Instruments' advanced process.

With delta-sigma architecture, fractional spurs at lower offset frequencies are pushed to higher frequencies outside the loop bandwidth. The ability to push close in spur and phase noise energy to higher frequencies is a direct function of the modulator order. Unlike analog compensation, the digital feedback technique used in the LMX2485 is highly resistant to changes in temperature and variations in wafer processing. The LMX2485 delta-sigma modulator is programmable up to fourth order, which allows the designer to select the optimum modulator order to fit the phase noise, spur, and lock time requirements of the system.

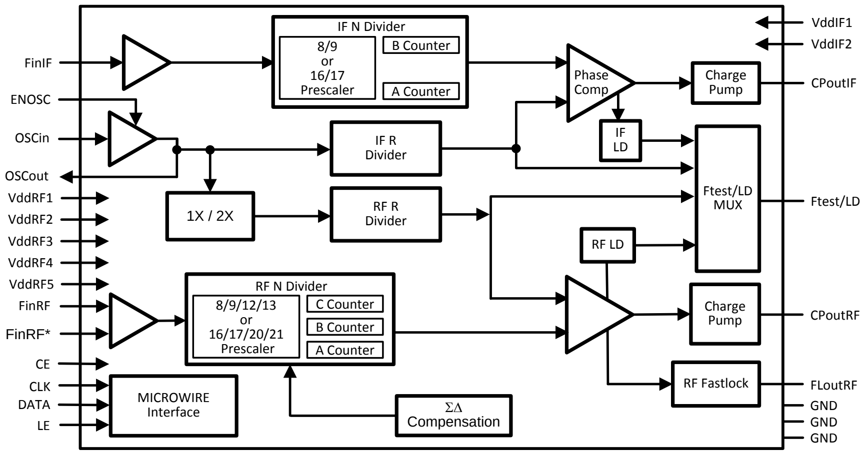
Serial data for programming the LMX2485 is transferred through a three-line, high-speed (20-MHz) MICROWIRE interface. The LMX2485 offers fine frequency resolution, low spurs, fast programming speed, and a single-word write to change the frequency. This makes it ideal for direct digital modulation applications, where the N-counter is directly modulated with information. The LMX2485 is available in a 24-lead 4.0 × 4.0 × 0.8 mm WQFN package.

Device Information(1)

PART NUMBER	RF PLL Frequency	IF PLL Frequency
LMX2485E	50 - 3000 MHz	75 - 800 MHz
LMX2485	500 - 3000 MHz	75 - 800 MHz

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

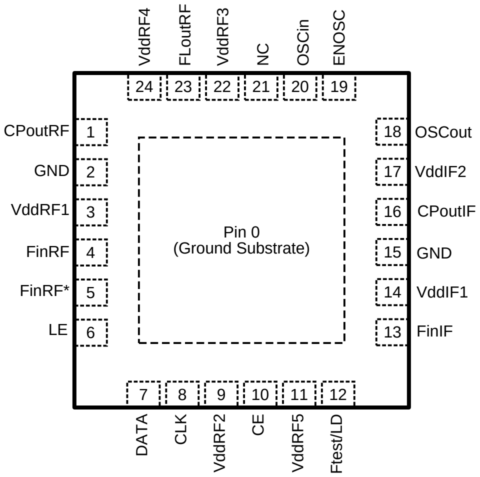
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (February 2013) to Revision G	Page
• Added *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision E (February 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	36

5 Pin Configuration and Functions

RTW Package
24-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
0	GND	—	Ground substrate; this is on the bottom of the package and must be grounded.
1	CPoutRF	O	RF PLL charge pump output
2	GND	—	RF PLL analog ground
3	VddRF1	—	RF PLL analog power supply
4	FinRF	I	RF PLL high-frequency input pin
5	FinRF*	I	RF PLL complementary high-frequency input pin; shunt to ground with a 100-pF capacitor.
6	LE	I	MICROWIRE load enable; high-impedance CMOS input. Data stored in the shift registers is loaded into the internal latches when LE goes HIGH.
7	DATA	I	MICROWIRE data; high-impedance binary serial data input.
8	CLK	I	MICROWIRE clock; high-impedance CMOS Clock input. Data for the various counters is clocked into the 24-bit shift register on the rising edge.
9	VddRF2	—	Power supply for RF PLL digital circuitry
10	CE	I	Chip Enable control pin; must be pulled high for normal operation.
11	VddRF5	I	Power supply for RF PLL circuitry
12	Ftest/LD	O	Test frequency output / lock detect
13	FinIF	I	IF PLL high-frequency input pin
14	VddIF1	—	IF PLL analog power supply
15	GND	—	IF PLL digital ground
16	CPoutIF	O	IF PLL charge pump output
17	VddIF2	—	IF PLL power supply
18	OSCout	O	Buffered output of the OSCin signal
19	ENOSC	I	Oscillator enable; when this is set to high, the OSCout pin is enabled regardless of the state of other pins or register bits.
20	OSCin	I	Input for TCXO signal
21	NC	I	This pin must be left open.
22	VddRF3	—	Power supply for RF PLL digital circuitry
23	FLoutRF	O	RF PLL fastlock output; also functions as programmable TRI-STATE CMOS output.
24	VddRF4	—	RF PLL analog power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2).

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	–0.3	4.25	V
V_i	Voltage on any pin with GND = 0 V	–0.3	V_{CC} + 0.3	V
T_L	Lead temperature (Solder 4 sec.)		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) For ensured specifications and test conditions, see the *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed. The voltage at all the power supply pins of VddRF1, VddRF2, VddRF3, VddRF4, VddRF5, VddIF1 and VddIF2 must be the same. V_{CC} will be used to refer to the voltage at these pins and I_{CC} will be used to refer to the sum of all currents through all these power pins.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1)	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±750	
		Machine model (MM)	±200	

(1) This is a high performance RF device is ESD-sensitive. Handling and assembly of this device should be done at an ESD free workstation.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage (1)	2.5	3	3.6	V
T_A	Operating temperature	–40	25	85	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed. The voltage at all the power supply pins of VddRF1, VddRF2, VddRF3, VddRF4, VddRF5, VddIF1 and VddIF2 must be the same. V_{CC} will be used to refer to the voltage at these pins and I_{CC} will be used to refer to the sum of all currents through all these power pins.

6.4 Thermal Information

THERMAL METRIC (1)		LMX2485, LMX2485E	UNIT
		RTW (WQFN)	
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

(V_{CC} = 3.0V; -40°C ≤ T_A ≤ +85°C unless otherwise specified)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC} PARAMETERS								
$I_{CC}RF$	Power supply current, RF synthesizer		IF PLL OFF RF PLL ON Charge Pump TRI-STATE			3.3		mA
$I_{CC}IF$	Power supply current, IF synthesizer		IF PLL ON RF PLL OFF Charge Pump TRI-STATE			1.7		mA
$I_{CC}TOTAL$	Power supply current, entire synthesizer		IF PLL ON RF PLL ON Charge Pump TRI-STATE			5		mA
$I_{CC}PD$	Powerdown current		CE = ENOSC = 0 V CLK, DATA, LE = 0 V			1	10	µA
RF SYNTHESIZER PARAMETERS								
f_{FinRF}	Operating frequency(1)	LMX2485	RF_P = 8		500		2000	MHz
			RF_P = 16		500		3000	
		LMX2485E	RF_P = 8		50		2000	
			RF_P = 16		50		3000	
p_{FinRF}	Input sensitivity		500 - 3000 MHz		-15		0	dBm
			50 - 500 MHz (LMX2485E only)		-8		8	
f_{COMP}	Phase detector frequency(2)						50	MHz
$I_{CPoutRF}SRCE$	RF charge pump source current(3)		RF_CPG = 0 $V_{CPoutRF}$ = V_{CC}/2			95		µA
			RF_CPG = 1 $V_{CPoutRF}$ = V_{CC}/2			190		µA
			RF_CPG = 15 $V_{CPoutRF}$ = V_{CC}/2			1520		µA
$I_{CPoutRF}SINK$	RF charge pump sink current(3)		RF_CPG = 0 $V_{CPoutRF}$ = V_{CC}/2			–95		µA
			RF_CPG = 1 $V_{CPoutRF}$ = V_{CC}/2			–190		µA
			RF_CPG = 15 $V_{CPoutRF}$ = V_{CC}/2			–1520		µA
$I_{CPoutRF}TRI$	RF charge pump TRI-STATE current magnitude		0.5 ≤ $V_{CPoutRF}$ ≤ V_{CC} -0.5			2	10	nA
| $I_{CPoutRF}$%MIS |	Magnitude of RF CP sink vs. CP source mismatch		$V_{CPoutRF}$ = V_{CC}/2 T_A = 25°C	RF_CPG > 2		3%	10%	
				RF_CPG ≤ 2		3%	13%	
| $I_{CPoutRF}$%V |	Magnitude of RF CP current vs. CP voltage		0.5 ≤ $V_{CPoutRF}$ ≤ V_{CC} -0.5 T_A = 25°C			2%	8%	
| $I_{CPoutRF}$%T |	Magnitude of RF CP current vs. temperature		$V_{CPoutRF}$ = V_{CC}/2			4%		
IF SYNTHESIZER PARAMETERS								
f_{FinIF}	Operating frequency				75		800	MHz
p_{FinIF}	IF input sensitivity				–10		5	dBm
f_{COMP}	Phase detector frequency						10	MHz
$I_{CPoutIF}SRCE$	IF charge pump source current		$V_{CPoutIF}$ = V_{CC}/2			3.5		mA
$I_{CPoutIF}SINK$	IF charge pump sink current		$V_{CPoutIF}$ = V_{CC}/2			–3.5		mA
$I_{CPoutIF}TRI$	IF charge pump TRI-STATE current magnitude		0.5 ≤ $V_{CPoutIF}$ ≤ V_{CC} RF -0.5			2	10	nA

(1) A slew rate of at least 100 V/uS is recommended for frequencies less than 500 MHz for optimal performance.
(2) For Phase Detector Frequencies greater than 20 MHz, Cycle Slip Reduction (CSR) may be required. Legal divide ratios are also required.
(3) Refer to table in *RF_CPG—RF PLL Charge Pump Gain* for complete listing of charge pump currents.

Electrical Characteristics (continued)

(V_{CC} = 3.0V; -40°C ≤ T_A ≤ +85°C unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\| I_{CPoutIF}\%MIS \|$	Magnitude of IF CP sink vs CP source mismatch	$V_{CPoutIF} = V_{CC}/2$ T_A = 25°C		1%	8%	
$\| I_{CPoutIF}\%V \|$	Magnitude of IF CP current vs CP voltage	$0.5 \leq V_{CPoutIF} \leq V_{CC} - 0.5$ T_A = 25°C		4%	10%	
$\| I_{CPoutIF}\%TEMP$	Magnitude of IF CP current vs temperature	$V_{CPoutIF} = V_{CC}/2$		4%		
OSCILLATOR PARAMETERS						
f_{OSCin}	Oscillator operating frequency	OSC2X = 0	5		110	MHz
		OSC2X = 1	5		20	MHz
v_{OSCin}	Oscillator input sensitivity		0.5		V_{CC}	V_{P-P}
I_{OSCin}	Oscillator input current		–100		100	µA
SPURS						
	Spurs in band	See (4)		–55		dBc
PHASE NOISE						
$L_{F1Hz}RF$	RF synthesizer normalized phase noise contribution(5)	RF_CPG = 0		–202		dBc/Hz
		RF_CPG = 1		–202		
		RF_CPG = 3		–206		
		RF_CPG = 7		–208		
		RF_CPG = 15		–210		
$L_{F1Hz}IF$	IF synthesizer normalized phase noise contribution			–209		dBc/Hz
DIGITAL INTERFACE (DATA, CLK, LE, ENOSC, CE, Ftest/LD, FLoutRF)						
V_{IH}	High-level input voltage		1.6		V_{CC}	V
V_{IL}	Low-level input voltage				0.4	V
I_{IH}	High-level input current	$V_{IH} = V_{CC}$	–1		1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V	–1		1	µA
V_{OH}	High-level output voltage	I_{OH} = –500 µA	V_{CC} - 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 500 µA			0.4	V

(4) To measure the in-band spur, the fractional word is chosen such that when reduced to lowest terms, the fractional numerator is one. The spur offset frequency is chosen to be the comparison frequency divided by the reduced fractional denominator. The loop bandwidth must be sufficiently wide to negate the impact of the loop filter. Measurement conditions are: Spur Offset Frequency = 10 kHz, Loop Bandwidth = 100 kHz, Fraction = 1/2000, Comparison Frequency = 20 MHz, RF_CPG = 7, DITH = 0, and a 4th Order Modulator (FM = 0). These are relatively consistent over tuning range.

(5) Normalized Phase Noise Contribution is defined as: $L_N(f) = L(f) – 20\log(N) – 10\log(f_{COMP})$ where L(f) is defined as the single side band phase noise measured at an offset frequency, f, in a 1 Hz Bandwidth. The offset frequency, f, must be chosen sufficiently smaller than the PLL loop bandwidth, yet large enough to avoid substantial phase noise contribution from the reference source. Measurement conditions are: Offset Frequency = 11 kHz, Loop Bandwidth = 100 kHz for RF_CPG = 7, Fraction = 1/2000, Comparison Frequency = 20 MHz, FM = 0, DITH = 0.

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
MICROWIRE INTERFACE TIMING						
t_{CS}	Data to clock set-up time	See Figure 1	25			ns
t_{CH}	Data to clock hold time	See Figure 1	8			ns
t_{CWH}	Clock pulse width high	See Figure 1	25			ns
t_{CWL}	Clock pulse width low	See Figure 1	25			ns
t_{ES}	Clock to load enable set-up time	See Figure 1	25			ns
t_{EW}	Load enable pulse width	See Figure 1	25			ns

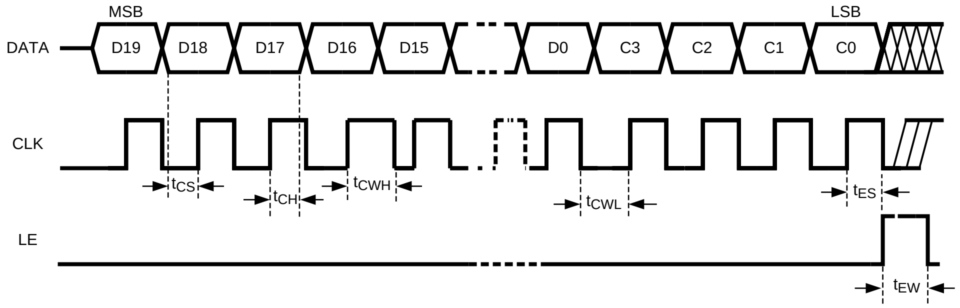
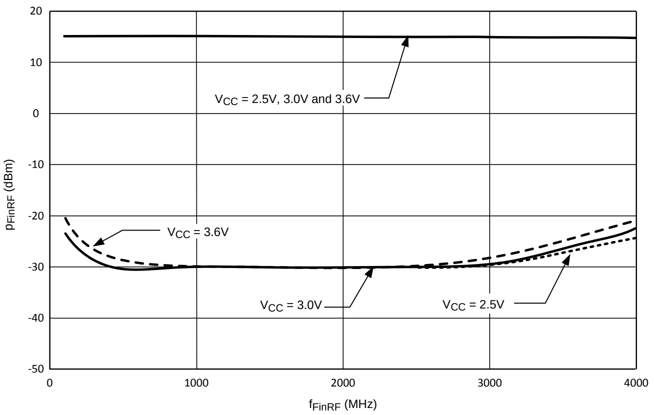


Figure 1. Microwire Input Timing Diagram

6.7 Typical Characteristics

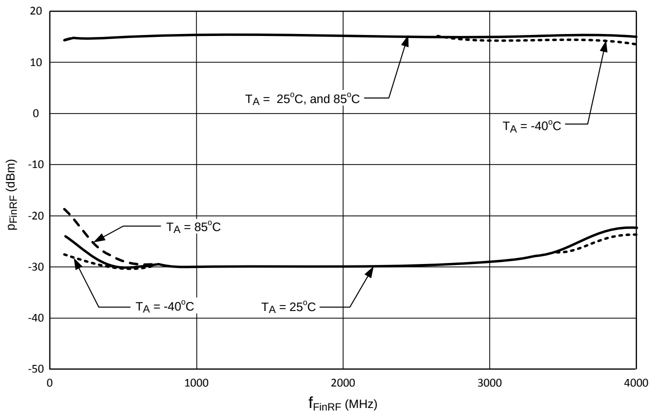
Typical characteristics do not imply any sort of ensured specification. Ensured specifications are in the *Electrical Characteristics* section.

6.7.1 Sensitivity



T_A = 25°C, RF_P = 16

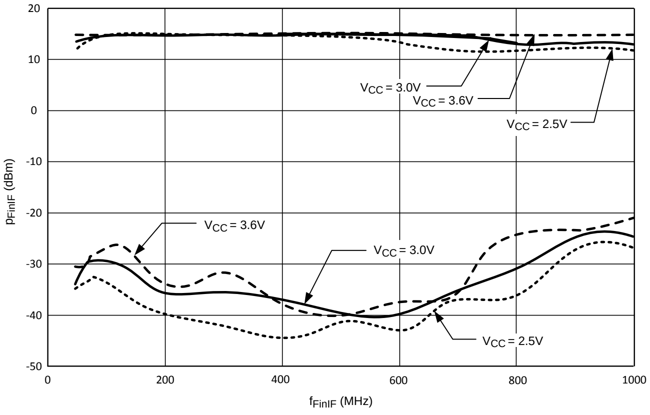
Figure 2. RF PLL Fin Sensitivity



V_{CC} = 3 V, RF_P = 16

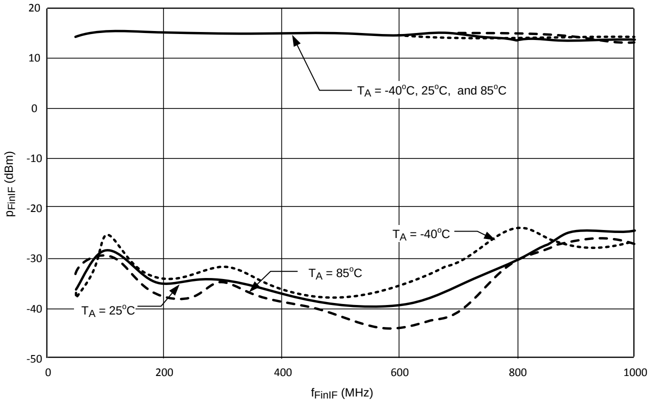
Figure 3. RF PLL Fin Sensitivity

Sensitivity (continued)



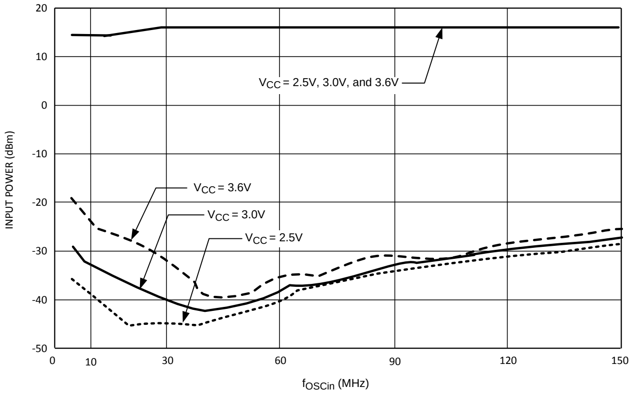
T_A = 25°C, IF_P = 16

Figure 4. IF PLL Fin Sensitivity



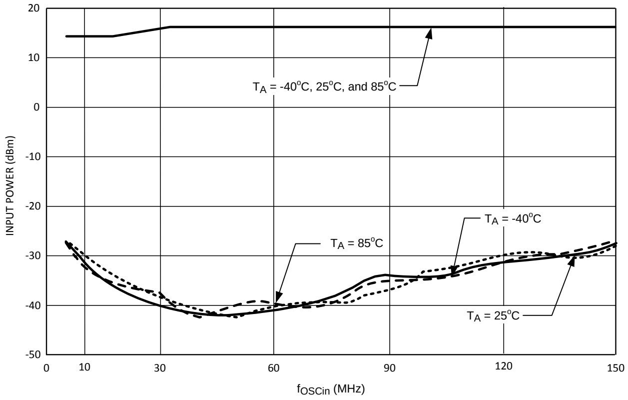
V_{CC} = 3 V, IF_P = 16

Figure 5. IF PLL Fin Sensitivity



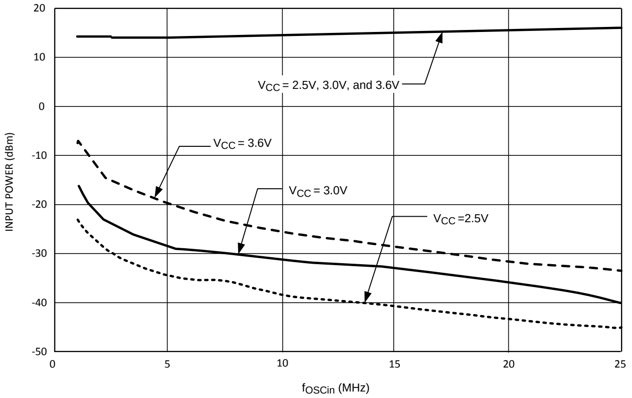
T_A = 25°C, OSC_2X = 0

Figure 6. OSCin Sensitivity



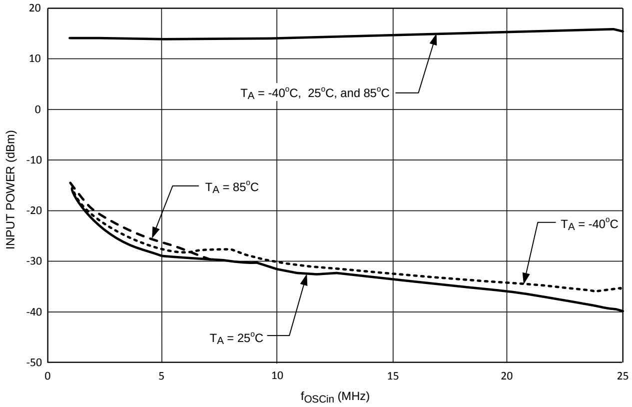
V_{CC} = 3 V, OSC_2X = 0

Figure 7. OSCin Sensitivity



T_A = 25°C, OSC_2X = 1

Figure 8. OSCin Sensitivity



V_{CC} = 3 V, OSC_2X = 1

Figure 9. OSCin Sensitivity

6.7.2 FinRF Input Impedance

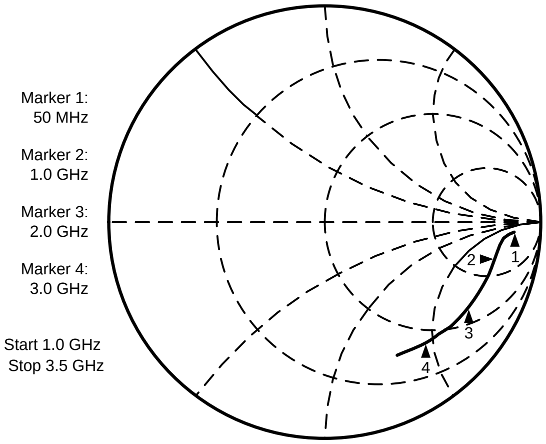


Figure 10. FinRF Input Impedance

Table 1. FinRF Input Impedance

FREQUENCY (MHz)	REAL (Ω)	IMAGINARY (Ω)
50	670	–276
100	531	–247
200	452	–209
300	408	–212
400	373	–222
500	337	–231
600	302	–237
700	270	–239
800	241	–236
900	215	–231
1000	192	–221
1100	172	–218
1200	154	–209
1300	139	–200
1400	127	–192
1500	114	–184
1600	104	–175
1700	96	–168
1800	88	–160
1900	80	–153
2000	74	–147
2200	64	–134
2400	56	–123
2600	50	–113
2800	45	–103
3000	39	–94
3200	37	–86
3400	33	–78
3600	30	–72
3800	28	–69
4000	26	–66

6.7.3 FinIF Input Impedance

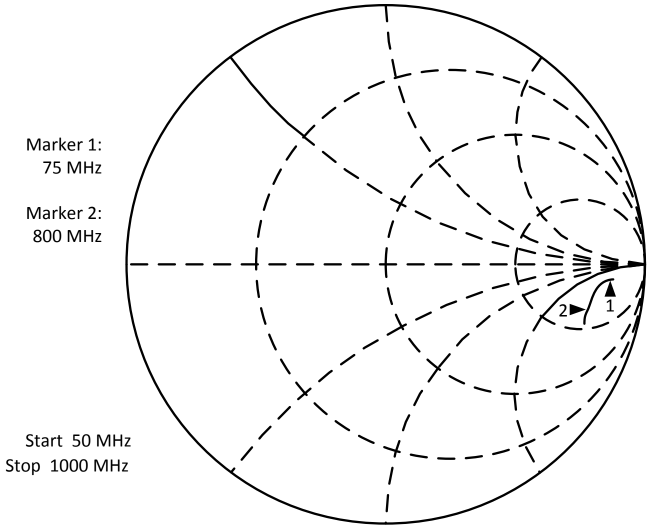


Figure 11. FinIF Input Impedance

Table 2. IF PLL Input Impedance

FinIF INPUT IMPEDANCE		
FREQUENCY (MHZ)	**REAL (Ω)**	**IMAGINARY (Ω)**
50	583	–286
75	530	–256
100	499	–241
200	426	–209
300	384	–209
400	347	–219
500	310	–224
600	276	–228
700	244	–228
800	216	–223
900	192	–218
1000	173	–208

6.7.4 OSCin Input Impedance

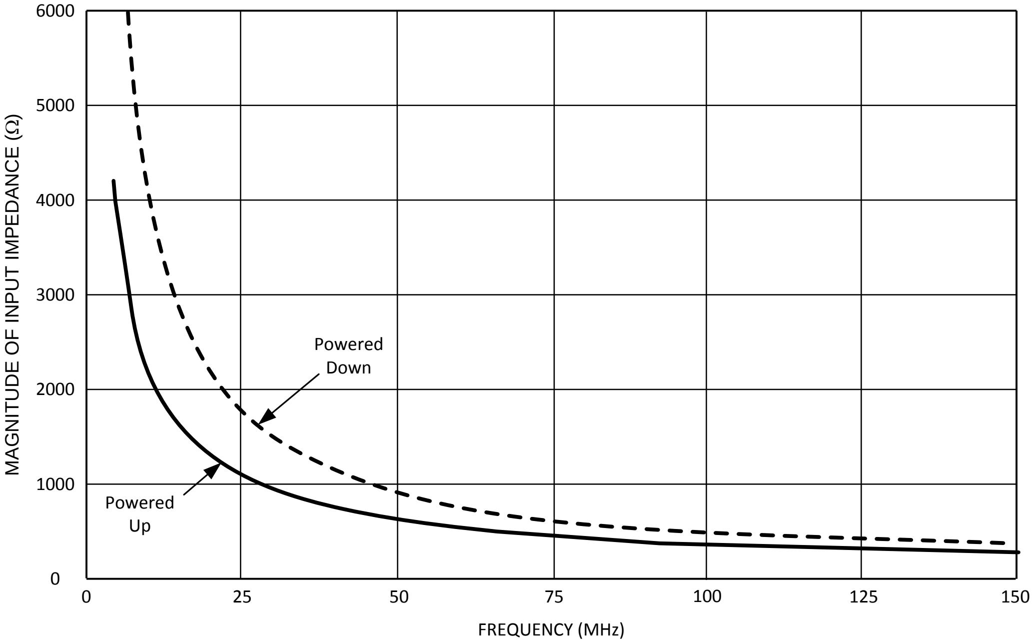
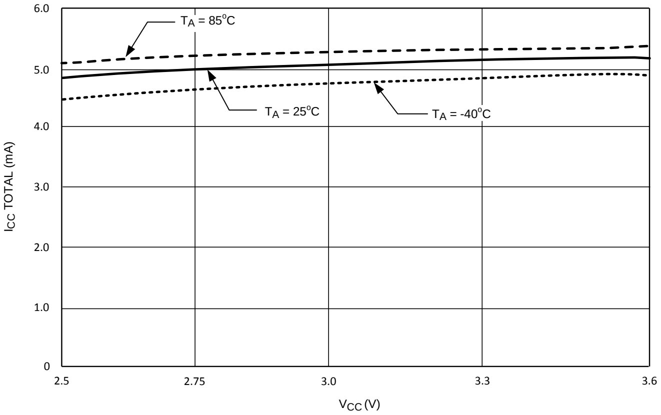


Figure 12. OSCin Input Impedance

Table 3. OSCin Input Impedance

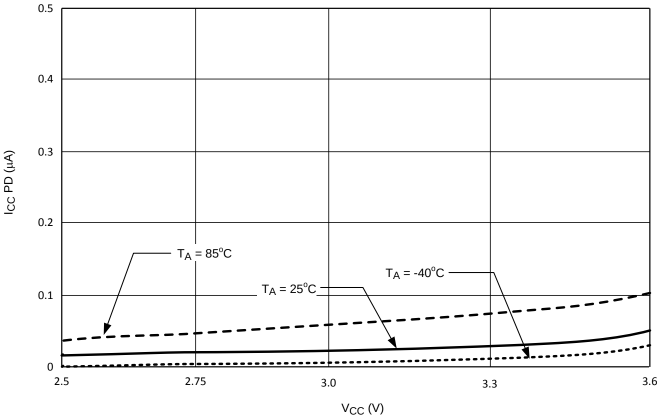
FREQUENCY (MHz)	POWERED-UP			POWERED-DOWN		
	REAL	IMAGINARY	MAGNITUDE	REAL	IMAGINARY	MAGNITUDE
5	1730	-3779	4157	392	-8137	8146
10	846	-2236	2391	155	-4487	4490
20	466	-1196	1284	107	-2215	2217
30	351	-863	932	166	-1495	-1504
40	316	-672	742	182	-1144	1158
50	278	-566	631	155	-912	925
60	261	-481	547	153	-758	774
70	252	-425	494	154	-652	669
80	239	-388	456	147	-576	595
90	234	-358	428	145	-518	538
100	230	-337	407	140	-471	492
110	225	-321	392	138	-436	458
120	219	-309	379	133	-402	123
130	214	-295	364	133	-374	397
140	208	-285	353	132	-349	373
150	207	-279	348	133	-329	355

6.7.5 Currents



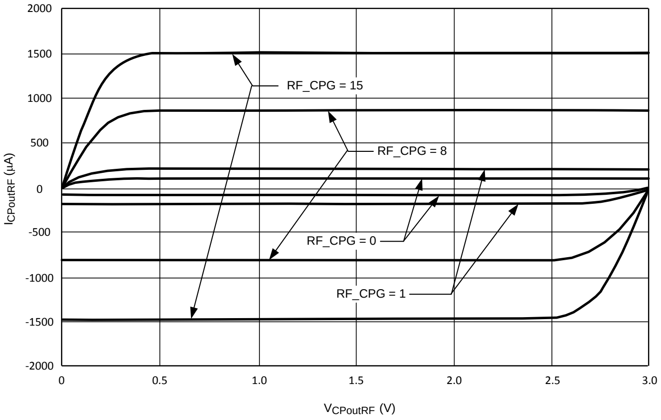
CE = High

Figure 13. Power Supply Current



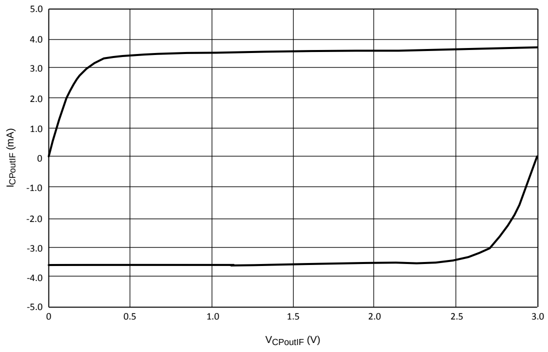
CE = LOW

Figure 14. Power Supply Current



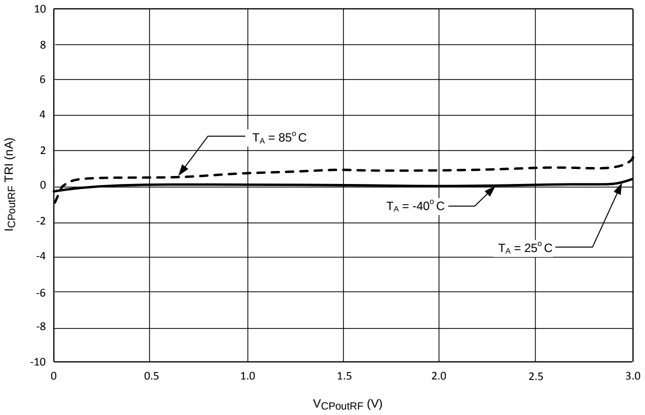
V_{CC} = 3 V

Figure 15. RF PLL Charge Pump Current



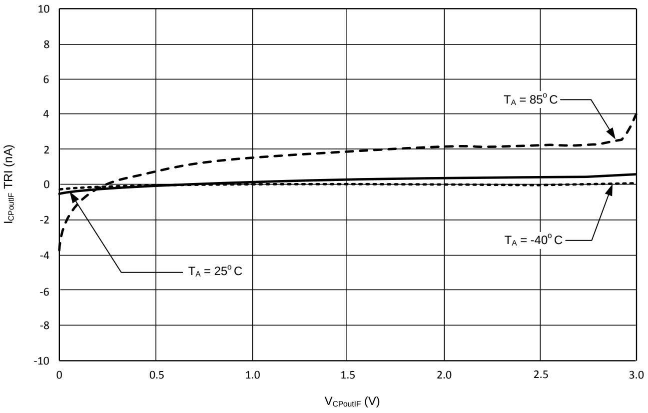
V_{CC} = 3 V

Figure 16. IF PLL Charge Pump Current



V_{CC} = 3 V

Figure 17. Charge Pump Leakage RF PLL



V_{CC} = 3 V

Figure 18. Charge Pump Leakage IF PLL

7 Parameter Measurement Information

7.1 Bench Test Set-Ups

7.1.1 Charge Pump Current Measurement

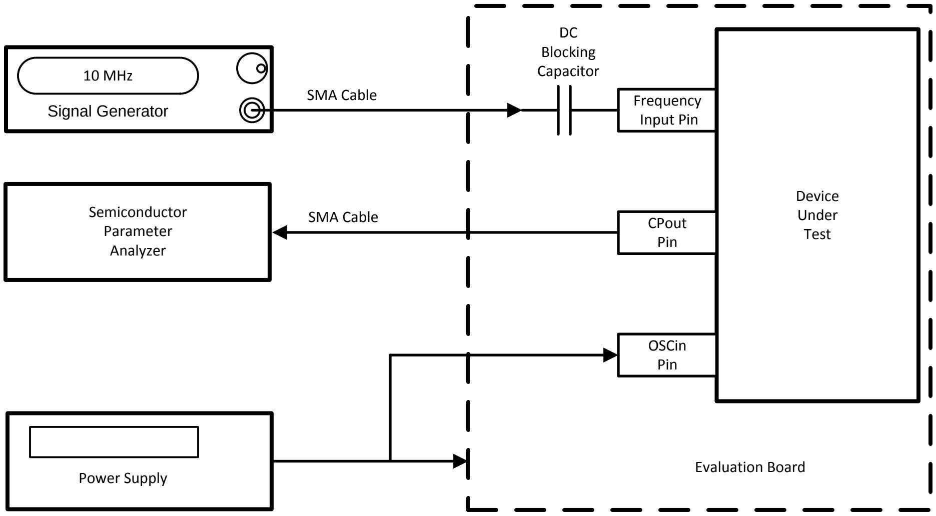


Figure 19. Charge Pump Current Measurement

Figure 19 shows the test procedure for testing the RF and IF charge pumps. These tests include absolute current level, mismatch, and leakage measurement. To measure the charge pump currents, a signal is applied to the high frequency input pins. The reason for this is to guarantee that the phase detector gets enough transitions to be able to change states. If no signal is applied, it is possible that the charge pump current reading will be low due to the fact that the duty cycle is not 100%. The OSCin Pin is tied to the supply. The charge pump currents can be measured by simply programming the phase detector to the necessary polarity. For instance, to measure the RF charge pump, a 10 MHz signal is applied to the FinRF pin. The source current can be measured by setting the RF PLL phase detector to a positive polarity, and the sink current can be measured by setting the phase detector to a negative polarity. The IF PLL currents can be measured in a similar way. The magnitude of the RF PLL charge pump current is controlled by the RF_CPG bit. Once the charge pump currents are known, the mismatch can be calculated as well. To measure leakage, the charge pump is set to a TRI-STATE mode by enabling the RF_CPT and IF_CPT bits. Table 4 shows a summary of the various charge pump tests.

Table 4. Programmable Settings for Charge Pump Current Tests

CURRENT TEST	RF_CPG	RF_CPP	RF_CPT	IF_CPP	IF_CPT
RF Source	0 to 15	0	0	X	X
RF Sink	0 to 15	1	0	X	X
RF TRI-STATE	X	X	1	X	X
IF Source	X	X	X	0	0
IF Sink	X	X	X	1	0
IF TRI-STATE	X	X	X	X	1

7.1.2 Charge Pump Current Specification Definitions

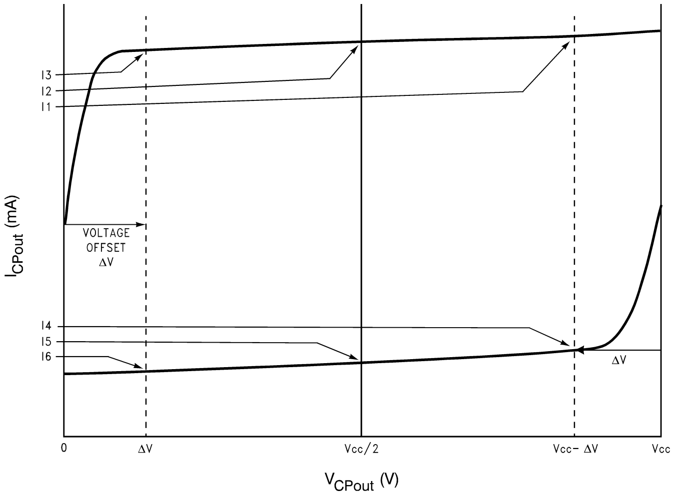


Figure 20. Charge Pump Current Specification Definitions

I1 = Charge Pump Sink Current at V_{CPout} = Vcc - ΔV

I2 = Charge Pump Sink Current at V_{CPout} = Vcc/2

I3 = Charge Pump Sink Current at V_{CPout} = ΔV

I4 = Charge Pump Source Current at V_{CPout} = Vcc - ΔV

I5 = Charge Pump Source Current at V_{CPout} = Vcc/2

I6 = Charge Pump Source Current at V_{CPout} = ΔV

ΔV = Voltage offset from the positive and negative supply rails. Defined to be 0.5 V for this part.

v_{CPout} refers to either $V_{CPoutRF}$ or $V_{CPoutIF}$

I_{CPout} refers to either $I_{CPoutRF}$ or $I_{CPoutIF}$

7.1.2.1 Charge Pump Output Current Magnitude Variation vs Charge Pump Output Voltage

Use Equation 1 to calculate the charge pump output current variation versus the charge pump output voltage.

$$I_{CPout} \text{ Vs } V_{CPout} = \frac{(|I1| - |I3|)}{(|I1| + |I3|)} \times 100\% = \frac{(|I4| - |I6|)}{(|I4| + |I6|)} \times 100\% \quad (1)$$

7.1.2.2 Charge Pump Sink Current vs Charge Pump Output Source Current Mismatch

Use Equation 2 to calculate the charge pump sink current versus the source current mismatch.

$$I_{CPout} \text{ Sink Vs } I_{CPout} \text{ Source} = \frac{|I2| - |I5|}{\frac{1}{2}(|I2| + |I5|)} \times 100\% \quad (2)$$

7.1.2.3 Charge Pump Output Current Magnitude Variation vs Temperature

Use Equation 3 to calculate the charge pump output current magnitude variation versus the temperature.

$$I_{CPout} \text{ Vs } T_A = \frac{|I_2|\big|_{T_A} - |I_2|\big|_{T_A = 25°C}}{|I_2|\big|_{T_A = 25°C}} \times 100\%$$

$$= \frac{|I_5|\big|_{T_A} - |I_5|\big|_{T_A = 25°C}}{|I_5|\big|_{T_A = 25°C}} \times 100\% \qquad (3)$$

7.1.3 Sensitivity Measurement Procedure

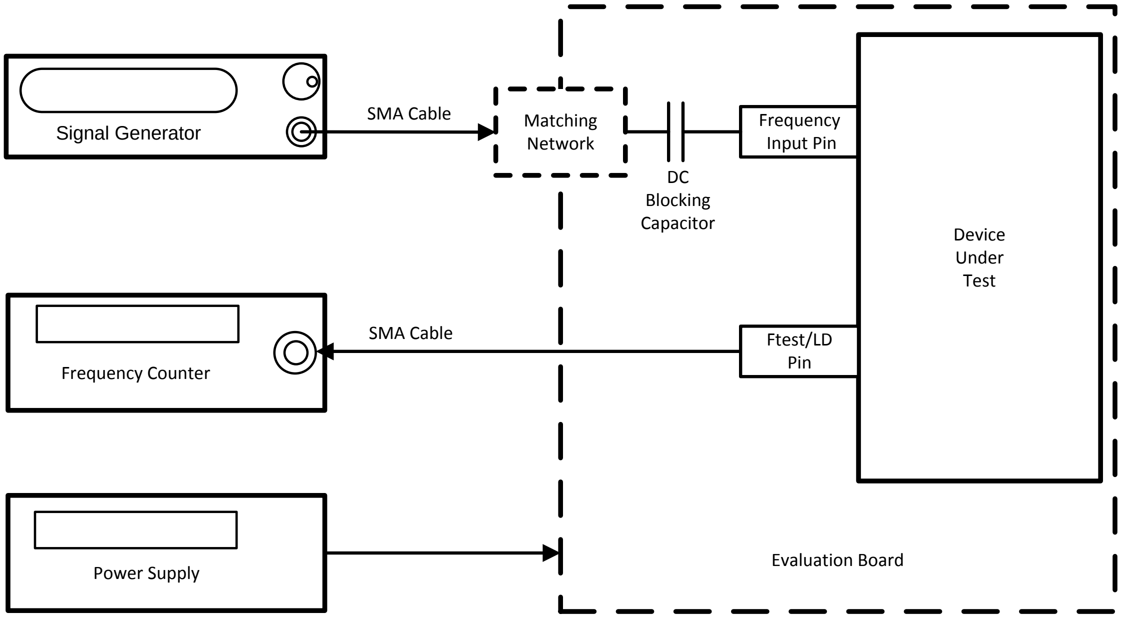


Figure 21. Setup for Sensitivity Measurement

Table 5. Sensitivity Set-Up Diagram

FREQUENCY INPUT PIN	DC-BLOCKING CAPACITOR	CORRESPONDING COUNTER	DEFAULT COUNTER VALUE	MUX VALUE
OSCin	1000 pF	RF_R / 2	50	14
FinRF	100 pF// 1000 pF	RF_N / 2	502 + 2097150 / 4194301	15
FinIF	100 pF	IF_N / 2	534	13
OSCin	1000 pF	IF_R / 2	50	12

Sensitivity is defined as the power level limits beyond which the output of the counter being tested is off by 1 Hz or more of its expected value. It is typically measured over frequency, voltage, and temperature. To test sensitivity, the MUX[3:0] word is programmed to the appropriate value. The counter value is then programmed to a fixed value and a frequency counter is set to monitor the frequency of this pin. The expected frequency at the Ftest/LD pin should be the signal generator frequency divided by twice the corresponding counter value. The factor of two comes in because the LMX2485 has a flip-flop which divides this frequency by two to make the duty cycle 50% to make it easier to read with the frequency counter. The frequency counter input impedance should be set to high impedance. To perform the measurement, the temperature, frequency, and voltage is set to a fixed value and the power level of the signal is varied. If the power level at the part is assumed to be 4 dB less than the signal generator power level. This accounts for 1 dB for cable losses and 3 dB for the pad. The power level range where the frequency is correct at the Ftest/LD pin to within 1 Hz accuracy is recorded for the sensitivity limits. The temperature, frequency, and voltage can be varied to produce a family of sensitivity curves. Because this is an open-loop test, the charge pump is set to TRI-STATE and the unused side of the PLL (RF or IF) is powered down when not being tested. For this part, there are actually four frequency input pins, although there is only one frequency test pin (Ftest/LD). The conditions specific to each pin are shown in Table 5.

NOTE

For the RF N counter, a fourth order fractional modulator is used in 22-bit mode with a fraction of 2097150 / 4194301 is used. The reason for this long fraction is to test the RF N counter and supporting fractional circuitry as completely as possible.

7.1.4 Input Impedance Measurement

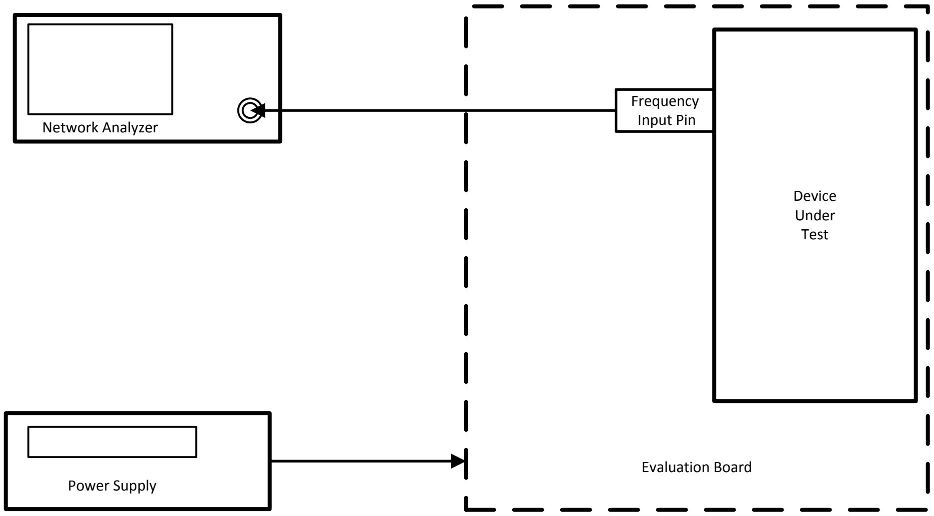


Figure 22. Input Impedance Measurement

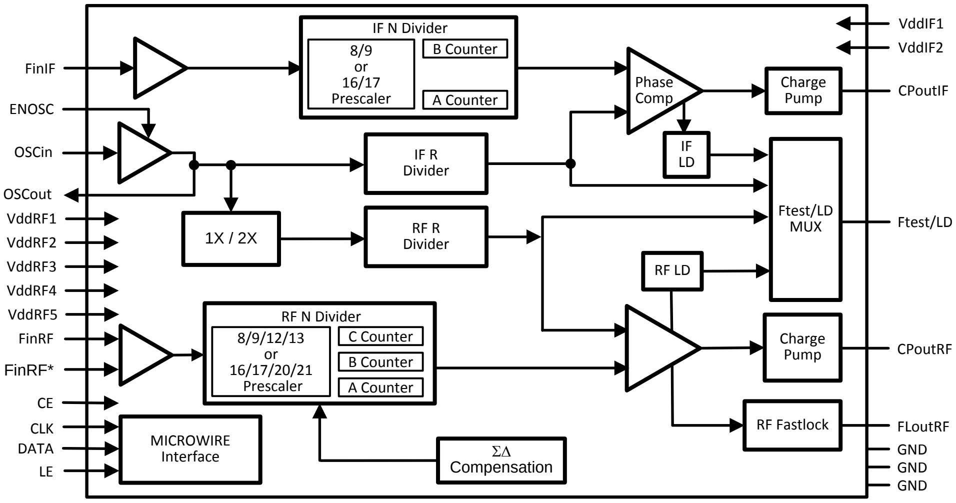
Figure 22 shows the test set-up used for measuring the input impedance for the LMX2485. The DC-blocking capacitor used between the input SMA connector and the pin being measured must be changed to a 0-Ω resistor. This procedure applies to the FinRF, FinIF, and OSCin pins. The basic test procedure is to calibrate the network analyzer, ensure that the part is powered up, and then measure the input impedance. The network analyzer can be calibrated by using either calibration standards or by soldering resistors directly to the evaluation board. An open can be implemented by putting no resistor, a short can be implemented by soldering a 0-Ω resistor as close as possible to the pin being measured, and a short can be implemented by soldering two 100-Ω resistors in parallel as close as possible to the pin being measured. Calibration is done with the PLL removed from the PCB. This requires the use of a clamp down fixture that may not always be generally available. If no clamp down fixture is available, then this procedure can be done by calibrating up to the point where the DC-blocking capacitor usually is, and then implementing port extensions with the network analyzer. The 0-Ω resistor is added back for the actual measurement. Once the set-up is calibrated, it is necessary to ensure that the PLL is powered up. This can be done by toggling the power down bits (RF_PD and IF_PD) and observing that the current consumption indeed increases when the bit is disabled. Sometimes it may be necessary to apply a signal to the OSCin pin to program the part. If this is necessary, disconnect the signal once it is established that the part is powered up. It is useful to know the input impedance of the PLL for the purposes of debugging RF problems and designing matching networks. Another use of knowing this parameter is make the trace width on the PCB such that the input impedance of this trace matches the real part of the input impedance of the PLL frequency of operation. In general, it is good practice to keep trace lengths short and make designs that are relatively resistant to variations in the input impedance of the PLL.

8 Detailed Description

8.1 Overview

The LMX2485 consists of integrated N counters, R counters, and charge pumps. The TCXO, VCO and loop filter are supplied external to the chip.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 TCXO, Oscillator Buffer, and R Counter

The oscillator buffer must be driven single-ended by a signal source, such as a TCXO. The OSCout pin is included to provide a buffered output of this input signal and is active when the OSC_OUT bit is set to one. The ENOSC pin can be also pulled high to ensure that the OSCout pin is active, regardless of the status of the registers in the LMX2485.

The R counter divides this TXCO frequency down to the comparison frequency.

8.3.2 Phase Detector

The maximum phase detector operating frequency for the IF PLL is straightforward, but it is a little more involved for the RF PLL because it is fractional. The maximum phase detector frequency for the LMX2485 RF PLL is 50 MHz. However, this is not possible in all circumstances due to illegal divide ratios of the N counter. The crystal reference frequency also limits the phase detector frequency, although the doubler helps with this limitation. There are trade-offs in choosing the phase detector frequency. If this frequency is run higher, then phase noise will be lower, but lock time may be increased due to cycle slipping and the capacitors in the loop filter may become rather large.

8.3.3 Charge Pump

For the majority of the time, the charge pump output is high impedance, and the only current through this pin is the Tri-State leakage. However, it does put out fast correction pulses that have a width that is proportional to the phase error presented at the phase detector.

The charge pump converts the phase error presented at the phase detector into a correction current. The magnitude of this current is theoretically constant, but the duty cycle is proportional to the phase error. For the IF PLL, this current is not programmable, but for the RF PLL it is programmable in 16 steps. Also, the RF PLL allows for a higher charge pump current to be used when the PLL is locking to reduce the lock time.

Feature Description (continued)

8.3.4 Loop Filter

The loop filter design can be rather involved. In addition to the regular constraints and design parameters, delta-sigma PLLs have the additional constraint that the order of the loop filter should be one greater than the order of the delta sigma modulator. This rule of thumb comes from the requirement that the loop filter must roll off the delta sigma noise at 20 dB/decade faster than it rises. However, because the noise can not have infinite power, it must eventually roll off. If the loop bandwidth is narrow, this requirement may not be necessary. For the purposes of discussion in this data sheet, the pole of the loop filter at 0 Hz is not counted. So a second order filter has 3 components, a 3rd order loop filter has 5 components, and the 4th order loop filter has 7 components. Although a 5th order loop filter is theoretically necessary for use with a 4th order modulator, typically a 4th order filter is used in this case. The loop filter design, especially for higher orders can be rather involved, but there are many simulation tools and references available, such as the one given at the end of the functional description block.

8.3.5 N Counters and High Frequency Input Pins

The N counter divides the VCO frequency down to the comparison frequency. Because prescalers are used, there are limitations on how small the N value can be. The N counters are discussed in greater depth in the programming section. Because the input pins to these counters (FinRF and FinIF) are high frequency, layout considerations are important.

8.3.5.1 High Frequency Input Pins, FinRF and FinIF

TI recommends that the VCO output go through a resistive pad and then through a DC-blocking capacitor before it gets to these high frequency input pins. If the trace length is sufficiently short (< 1/10th of a wavelength), then the pad may not be necessary, but a series resistor of about 39 Ω is still recommended to isolate the PLL from the VCO. The DC-blocking capacitor should be chosen at least to be 27 pF, depending on frequency. It may turn out that the frequency is above the self-resonant frequency of the capacitor, but because the input impedance of the PLL tends to be capacitive, it actually is a benefit to exceed the tune frequency. The pad and the DC-blocking capacitor should be placed as close to the PLL as possible

*8.3.5.2 Complementary High Frequency Pin, FinRF**

These inputs may be used to drive the PLL differentially, but it is very common to drive the PLL in a single ended fashion. A shunt capacitor should be placed at the FinRF* pin. The value of this capacitor should be chosen such that the impedance, including the ESR of the capacitor, is as close to an AC short as possible at the operating frequency of the PLL. 100 pF is a typical value, depending on frequency.

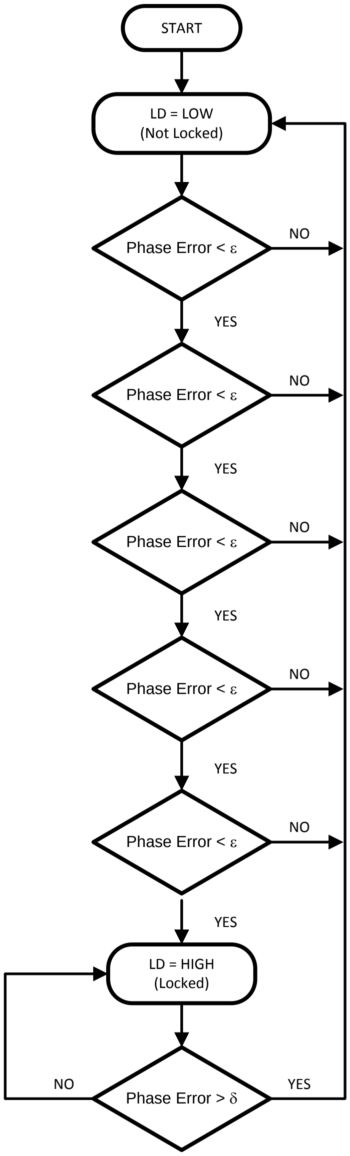
8.3.6 Digital Lock Detect Operation

The RF PLL digital lock detect circuitry compares the difference between the phase of the inputs of the phase detector to a RC generated delay of ε. To indicate a locked state (Lock = HIGH) the phase error must be less than the ε RC delay for 5 consecutive reference cycles. Once in lock (Lock = HIGH), the RC delay is changed to approximately δ. To indicate an out of lock state (Lock = LOW), the phase error must become greater δ. The values of ε and δ are dependent on which PLL is used and are shown in Table 6:

Table 6. Digital Lock Detection Tolerances

PLL	ε	δ
RF	10 ns	20 ns
IF	15 ns	30 ns

When the PLL is in the power-down mode and the Ftest/LD pin is programmed for the lock detect function, it is forced LOW. The accuracy of this circuit degrades at higher comparison frequencies. To compensate for this, the DIV4 word should be set to one if the comparison frequency exceeds 20 MHz. The function of this word is to divide the comparison frequency presented to the lock detect circuit by 4. If the MUX[3:0] word is set such as to view lock detect for both PLLs, an unlocked (LOW) condition is shown whenever either one of the PLLs is determined to be out of lock.



8.3.7 Cycle Slip Reduction and Fastlock

The LMX2485 offers both cycle slip reduction (CSR) and Fastlock with time-out counter support. This means that it requires no additional programming overhead to use them. TI recommends that the charge pump current in the steady-state be 8X or less to use cycle slip reduction, and 4X or less in steady-state to use Fastlock. The next step is to decide between using Fastlock or CSR. This determination can be made based on the ratio of the comparison frequency (f_{COMP}) to loop bandwidth (BW).

Table 7. Using Cycle Slip Reduction and Fastlock

COMPARISON FREQUENCY (f_{COMP})	FASTLOCK	CYCLE SLIP REDUCTION (CSR)
$f_{COMP} \leq 1.25$ MHz	Noticeable better than CSR	Likely to provide a benefit, provided that $f_{COMP} > 100$ X BW
1.25 MHz $< f_{COMP} \leq 2$ MHz	Marginally better than CSR	
$f_{COMP} > 2$ MHz	Same or worse than CSR	

8.3.7.1 Cycle Slip Reduction (CSR)

Cycle slip reduction works by reducing the comparison frequency during frequency acquisition while keeping the same loop bandwidth, thereby reducing the ratio of the comparison frequency to the loop bandwidth. In cases where the ratio of the comparison frequency exceeds about 100 times the loop bandwidth, cycle slipping can occur and significantly degrade lock times. The greater this ratio, the greater the benefit of CSR. This is typically the case of high comparison frequencies. In circumstances where there is not a problem with cycle slipping, CSR provides no benefit. There is a glitch when CSR is disengaged, but because CSR should be disengaged long before the PLL is actually in lock, this glitch is not an issue. A good rule of thumb for CSR disengagement is to do this at the peak time of the transient response. Because this time is typically much sooner than Fastlock should be disengaged, it does not make sense to use CSR and Fastlock in combination.

8.3.7.2 Fastlock

Fastlock works by increasing the loop bandwidth only during frequency acquisition. In circumstances where the comparison frequency is less than or equal to 2 MHz, Fastlock may provide a benefit beyond what CSR can offer. Because Fastlock also reduces the ratio of the comparison frequency to the loop bandwidth, it may provide a significant benefit in cases where the comparison frequency is greater than 2 MHz. However, CSR can usually provide an equal or larger benefit in these cases, and can be implemented without using an additional resistor. The reason for this restriction on frequency is that Fastlock has a glitch when it is disengaged. As the time of engagement for Fastlock decreases and becomes on the order of the fast lock time, this glitch grows and limits the benefits of Fastlock. This effect becomes worse at higher comparison frequencies. There is always the option of reducing the comparison frequency at the expense of phase noise to satisfy this constraint on comparison frequency. Despite this glitch, there is still a net improvement in lock time using Fastlock in these circumstances. When using Fastlock, TI also recommends that the steady-state charge pump state be 4X or less. Also, Fastlock was originally intended only for second order filters, so when implementing it with higher order filters, the third and fourth poles can not be too close in, or it will not be possible to keep the loop filter well optimized when the higher charge pump current and Fastlock resistor are engaged.

8.3.7.3 Using Cycle Slip Reduction (CSR) to Avoid Cycle Slipping

Once it is decided that CSR is to be used, the cycle slip reduction factor needs to be chosen. The available factors are 1/2, 1/4, and 1/16. To preserve the same loop characteristics, TI recommends that the following constraint be satisfied:

8.3.7.3.1 (Fastlock Charge Pump Current) / (Steady-State Charge Pump Current) = CSR

To satisfy this constraint, the maximum charge pump current in steady-state is 8X for a CSR of 1/2, 4X for a CSR of 1/4, and 1X for a CSR of 1/16. Because the PLL phase noise is better for higher charge pump currents, it makes sense to choose CSR only as large as necessary to prevent cycle slipping. Choosing it larger than this will not improve lock time, and will result in worse phase noise.

Consider an example where the desired loop bandwidth in steady-state is 100 kHz and the comparison frequency is 20 MHz. This yields a ratio of 200. Cycle slipping may be present, but would not be too severe if it was there. If a CSR factor of 1/2 is used, this would reduce the ratio to 100 during frequency acquisition, which is probably sufficient. A charge pump current of 8X could be used in steady-state, and a factor of 16X could be used during frequency acquisition. This yields a ratio of 1/2, which is equal to the CSR factor and this satisfies the above constraint. In this circumstance, it could also be decided to just use 16X charge pump current all the time, because it would probably have better phase noise, and the degradation in lock time would not be too severe.

8.3.7.4 Using Fastlock to Improve Lock Times

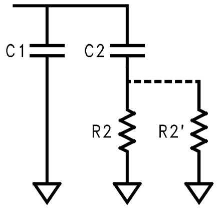


Figure 23. Loop Filter with Fastlock Resistor

Once it is decided that Fastlock is to be used, the loop bandwidth multiplier, K, is needed to determine the theoretical impact of Fastlock on the loop bandwidth and the resistor value, R2p, that is switched in parallel during Fastlock. This ratio is calculated as follows:

Table 8. K = (Fastlock Charge Pump Current) / (Steady-State Charge Pump Current)

K	LOOP BANDWIDTH	R2p VALUE	LOCK TIME
1	1.00 X	Open	100%
2	1.41 X	R2/0.41	71%
3	1.73 X	R2/0.73	58%
4	2.00 X	R2	50%
8	2.83 X	R2/1.83	35%
9	3.00 X	R2/2	33%
16	4.00 X	R2/3	25%

Table 8 shows how to calculate the Fastlock resistor and theoretical lock time improvement, once the ratio , K, is known. This all assumes a second order filter (not counting the pole at 0 Hz). However, TI generally recommends that the loop filter order be one greater than the order of the delta sigma modulator, which means that a second order filter is never recommended. In this case, the value for R2p is typically about 80% of what it would be for a second order filter. Because the Fastlock disengagement glitch gets larger and it is harder to keep the loop filter optimized as the K value becomes larger, designing for the largest possible value for K usually, but not always yields the best improvement in lock time. To get a more accurate estimate requires more simulation tools, or trial and error.

8.3.7.5 Capacitor Dielectric Considerations for Lock Time

The LMX2485 has a high fractional modulus and high charge pump gain for the lowest possible phase noise. One consideration is that the reduced N value and higher charge pump may cause the capacitors in the loop filter to become larger in value. For larger capacitor values, it is common to have a trade-off between capacitor dielectric quality and physical size. Using film capacitors or NPO/COG capacitors yields the best possible lock times, where as using X7R or Z5R capacitors can increase lock time by 0 – 500%. However, it is a general tendency that designs that use a higher compare frequency tend to be less sensitive to the effects of capacitor dielectrics. Although the use of lesser quality dielectric capacitors may be unavoidable in many circumstances, allowing a larger footprint for the loop filter capacitors, using a lower charge pump current, and reducing the fractional modulus are all ways to reduce capacitor values. Capacitor dielectrics have very little impact on phase noise and spurs.

8.3.8 Fractional Spur and Phase Noise Controls

Control of the fractional spurs is more of an art than an exact science. The first differentiation that needs to be made is between primary fractional and sub-fractional spurs. The primary fractional spurs are those that occur at increments of the channel spacing only. The sub-fractional spurs are those that occur at a smaller resolution than the channel spacing, usually one-half or one-fourth. There are trade-offs between fractional spurs, sub-fractional spurs, and phase noise. The rules of thumb presented in this section are just that. There will be exceptions. The bits that impact the fractional spurs are FM and DITH, and these bits should be set in this order.

The first step to do is choose FM, for the delta sigma modulator order. TI recommends to start with FM = 3 for a third order modulator and use strong dithering. In general, there is a trade-off between primary and sub-fractional spurs. Choosing the highest order modulator (FM = 0 for 4th order) typically provides the best primary fractional spurs, but the worst sub-fractional spurs. Choosing the lowest modulator order (FM = 2 for 2nd order), typically gives the worst primary fractional spurs, but the best sub-fractional spurs. Choosing FM = 3, for a 3rd order modulator is a compromise.

The second step is to choose DITH, for dithering. Dithering has a very small impact on primary fractional spurs, but a much larger impact on sub-fractional spurs. The only problem is that it can add a few dB of phase noise, or even more if the loop bandwidth is very wide. Disabling dithering (DITH = 0), provides the best phase noise, but the sub-fractional spurs are worst (except when the fractional numerator is 0, and in this case, they are the best). Choosing strong dithering (DITH = 2) significantly reduces sub-fractional spurs, if not eliminating them completely, but adds the most phase noise. Weak dithering (DITH = 1) is a compromise.

The third step is to tinker with the fractional word. Although 1/10 and 400/4000 are mathematically the same, expressing fractions with much larger fractional numerators often improve the fractional spurs. Increasing the fractional denominator only improves spurs to a point. A good practical limit could be to keep the fractional denominator as large as possible, but not to exceed 4095, so it is not necessary to use the extended fractional numerator or denominator.

This steps can be done in different orders and it might take a few iterations to find the optimum performance. Special considerations should be taken for lower frequencies that are less than 100 MHz. In addition squaring up the wave, it is often helpful to use lowest terms fractions instead of highest terms fractions. Also, dithering may turn out to not be so useful. All the things are to introduce a methodical way of thinking about optimizing spurs, not an exact method. There will be exceptions to all these rules.

NOTE

For more information concerning delta-sigma PLLs, loop filter design, cycle slip reduction, Fastlock, and many other topics, visit www.ti.com. Here there is the EasyPLL simulation tool and an online reference called *PLL Performance, Simulation, and Design*.

8.4 Device Functional Modes

8.4.1 Power Pins, Power-Down, and Power-Up Modes

TI recommends that all of the power pins be filtered with a series 18-Ω resistor and then placing two capacitors shunt to ground, thus creating a low pass filter. Although it makes sense to use large capacitor values in theory, the ESR (Equivalent Series Resistance) is greater for larger capacitors. For optimal filtering minimize the sum of the ESR and theoretical impedance of the capacitor. Therefore TI recommends to provide two capacitors of very different sizes for the best filtering. 1 µF and 100 pF are typical values. The small capacitor should be placed as close as possible to the pin.

The power down state of the LMX2485 is controlled by many factors. The one factor that overrides all other factors is the CE pin. If this pin is low, the part will be powered down. Asserting a high logic level on this pin is necessary to power up the chip, however, there are other bits in the programming registers that can override this and put the PLL back in a power-down state. Provided that the voltage on the CE pin is high, programming the RF_PD and IF_PD bits to zero ensures that the part will be powered up. Programming either one of these bits to one will power down the appropriate section of the synthesizer, provided that the ATPU bit does not override this.

Table 9. Power-Up and Down States

CE PIN	RF_PD	ATPU Bit Enabled + N Counter Write	PLL STATE
Low	X	X	Powered Down (Asynchronous)
High	X	Yes	Powered Up
High	0	No	Powered Up
High	1	No	Powered Down (Asynchronous)

8.5 Programming

8.5.1 General Programming Information

The 24-bit data registers are loaded through a MICROWIRE Interface. These data registers are used to program the R counter, the N counter, and the internal mode control latches. The data format of a typical 24-bit data register is shown in Table 10. The control bits CTL [3:0] decode the register address. On the rising edge of LE, data stored in the shift register is loaded into one of the appropriate latches (selected by address bits). Data is shifted in MSB first.

NOTE

It is best to program the N counter last, because doing so initializes the digital lock detector and Fastlock circuitry. *Initialize* means it resets the counters, but it does NOT program values into these registers. The exception is when 22-bit is not being used. In this case, it is not necessary to program the R7 register.

Table 10. Register Structure

MSB					**LSB**
DATA [21:0]		**CTL [3:0]**			
23	4	3	2	1	0

8.5.1.1 Register Location Truth Table

The control bits CTL [3:0] decode the internal register address. Table 11 shows how the control bits are mapped to the target control register.

Table 11. Programmable Registers

C3	C2	C1	C0	DATA LOCATION
x	x	x	0	R0
0	0	1	1	R1
0	1	0	1	R2
0	1	1	1	R3
1	0	0	1	R4
1	0	1	1	R5
1	1	0	1	R6
1	1	1	1	R7

8.5.1.2 Control Register Content Map

Because the LMX2485 registers are complicated, they are organized into two groups, basic and advanced. The first four registers are basic registers that contain critical information necessary for the PLL to achieve lock. The last 5 registers are for features that optimize spur, phase noise, and lock time performance. The next page shows these registers.

8.5.1.3 Quick Start Register Map

Although TI highly recommends that the user eventually take advantage of all the modes of the LMX2485, the quick start register map is shown in order for the user to get the part up and running quickly using only those bits critical for basic functionality. The following default conditions for this programming state are a third order delta-sigma modulator in 12-bit mode with no dithering and no Fastlock.

Table 12. Quick Start Register Map

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R0	RF_N[10:0]											RF_FN[11:0]												0
R1	RF_PD	RF_P	RF_R[5:0]						RF_FD[11:0]												0	0	1	1
R2	IF_PD	IF_N[18:0]																			0	1	0	1
R3	0001				RF_CPG[3:0]				IF_R[11:0]												0	1	1	1
R4	0	0	1	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	0	0	1	0	0	1

8.5.1.4 Complete Register Map

The complete register map shows all the functionality of all registers, including the last five.

Table 13. Complete Register Map

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0] (Except for the RF_N Register, which is [22:0])																				C3	C2	C1	C0
R0	RF_N[10:0]											RF_FN[11:0]												0
R1	RF_PD	RF_P	RF_R[5:0]						RF_FD[11:0]												0	0	1	1
R2	IF_PD	IF_N[18:0]																			0	1	0	1
R3	ACCESS[3:0]				RF_CPG[3:0]				IF_R[11:0]												0	1	1	1
R4	ATPU	0	1	0	0	0	DITH [1:0]		FM [1:0]		0	OSC _2X	OSC _OUT	IF_ CPP	RF_ CPP	IF_P	MUX [3:0]				1	0	0	1
R5	RF_FD[21:12]										RF_FN[21:12]										1	0	1	1
R6	CSR[1:0]		RF_CPF[3:0]				RF_TOC[13:0]														1	1	0	1
R7	0	0	0	0	0	0	0	0	0	0	DIV4	0	1	0	0	1	IF_ RST	RF_ RST	IF_ CPT	RF_ CPT	1	1	1	1

8.6 Register Maps

8.6.1 R0 Register

NOTE

This register has only one control bit, so the N counter value to be changed with a single write statement to the PLL.

Table 14. R0 Register

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[22:0]																							C0
R0	RF_N[10:0]											RF_FN[11:0]												0

8.6.1.1 RF_FN[11:0]—Fractional Numerator for RF PLL

Refer to *Fractional Numerator Determination { RF_FN[21:12], RF_FN[11:0], Access[1] }* for a more detailed description of this control word.

8.6.1.2 RF_N[10:0]—RF N Counter Value

The RF N counter contains an 8/9/12/13 and a 16/17/20/21 prescaler. The N counter value can be calculated as follows:

$N = RF\_P \cdot RF\_C + 4 \cdot RF\_B + RF\_A$

$RF\_C \geq Max\{RF\_A, RF\_B\}$, for $N-2^{FM}-1$ ... $N+2^{FM}$ is a necessary condition. This rule is slightly modified in the case where the RF_B counter has an unused bit, where this extra bit is used by the delta-sigma modulator for the purposes of modulation. Consult the tables below for valid operating ranges for each prescaler.

Table 15. Operation With the 8/9/12/13 Prescaler (RF_P=0)

RF_N	RF_N [10:0]										
	RF_C [6:0]							RF_B [1:0]		RF_A [1:0]	
<25	N values less than 25 are prohibited.										
25-26	Possible only with a second order delta-sigma engine.										
27-30	Possible only with a second or third order delta-sigma engine.										
31	0	0	0	0	0	1	1	0	1	1	1
...	.	.	.	.	.	.	.	0	.	.	.
1023	1	1	1	1	1	1	1	0	1	1	1
>1023	N values greater than 1023 are prohibited.										

Table 16. Operation With the 16/17/20/21 Prescaler (RF_P=1)

RF_N	RF_N [10:0]										
	RF_C [6:0]							RF_B [1:0]		RF_A [1:0]	
<49	N values less than 49 are prohibited.										
49-50	Possible only with a second order delta-sigma engine.										
51-54	Possible with a second or third order delta-sigma engine.										
55	0	0	0	0	0	1	1	0	1	1	1
...	.	.	.	.	.	.	.	.	.	.	.
2039	1	1	1	1	1	1	1	0	1	1	1
2040-2043	Possible with a second or third order delta-sigma engine.										
2044-2045	Possible only with a second order delta-sigma engine.										
>2045	N values greater than 2045 are prohibited.										

8.6.2 R1 Register

Table 17. R1 Register

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R1	RF_PD	RF_P	RF_R[5:0]						RF_FD[11:0]												0	0	1	1

8.6.2.1 RF_FD[11:0]—RF PLL Fractional Denominator

The function of these bits are described in *Fractional Denominator Determination { RF_FD[21:12], RF_FD[11:0], Access[1]}*.

8.6.2.2 RF_R [5:0]—RF R Divider Value

The RF R Counter value is determined by this control word.

NOTE

This counter does allow values down to one.

Table 18. RF_R [5:0]—RF R Divider Value

R VALUE	RF_R[5:0]					
1	0	0	0	0	0	1
...	.	.	.	.	.	.
63	1	1	1	1	1	1

8.6.2.3 RF_P—RF Prescaler Bit

The prescaler used is determined by this bit.

Table 19. RF_P—RF Prescaler Bit

RF_P	PRESCALER	MAXIMUM FREQUENCY
0	8/9/12/13	2000 MHz
1	16/17/20/21	3000 MHz

8.6.2.4 RF_PD—RF Power-Down Control Bit

When this bit is set to 0, the RF PLL operates normally. When it is set to one, the RF PLL is powered down and the RF Charge pump is set to a TRI-STATE mode. The CE pin and ATPU bit also control power down functions, and will override the RF_PD bit. The order of precedence is as follows. First, if the CE pin is LOW, then the PLL will be powered down. Provided this is not the case, the PLL will be powered up if the ATPU bit says to do so, regardless of the state of the RF_PD bit. After the CE pin and the ATPU bit are considered, then the RF_PD bit then takes control of the power-down function for the RF PLL.

8.6.3 R2 Register

Table 20. R2 Register

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R2	IF_PD	IF_N[18:0]																			0	1	0	1

8.6.3.1 IF_N[18:0]—IF N Divider Value

Table 21. IF_N Counter Programming With the 8/9 Prescaler (IF_P=0)

N VALUE	IF_N[18:0]																		
	IF_B															IF_A			
≤23	N values less than or equal to 23 are prohibited because IF_B ≥ 3 is required.																		
24-55	Legal divide ratios in this range are: 24-27, 32-36, 40-45, 48-54																		
56	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
57	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
262143	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1

Table 22. Operation With the 16/17 Prescaler (IF_P=1)

N VALUE	IF_B															IF_A			
≤47	N values less than or equal to 47 are prohibited because IF_B ≥ 3 is required.																		
48-239	Legal divide ratios in this range are: 48-51, 64-68, 80-85, 96-102, 112-119, 128-136, 144-153, 160-170, 176-187, 192-204, 208-221, 224-238																		
240	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
241	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
524287	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.6.3.2 IF_PD—IF Power Down Bit

When this bit is set to 0, the IF PLL operates normally. When it is set to 1, the IF PLL powers down and the output of the IF PLL charge pump is set to a TRI-STATE mode. If the ATPU bit is set and register R0 is written to, the IF_PD will be reset to 0 and the IF PLL will be powered up. If the CE pin is held low, the IF PLL will be powered down, overriding the IF_PD bit.

8.6.4 R3 Register

Table 23. R3 Register

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R3	ACCESS[3:0]				RF_CPG[3:0]				IF_R[11:0]												0	1	1	1

8.6.4.1 IF_R[11:0]—IF R Divider Value

For the IF R divider, the R value is determined by the IF_R[11:0] bits in the R3 register. The minimum value for IF_R is 3.

Table 24. IF_R[11:0]—IF R Divider Value

R VALUE	IF_R[11:0]											
3	0	0	0	0	0	0	0	0	0	0	1	1
...	.	.	.	.	.	.	.	.	.	.	.	.
4095	1	1	1	1	1	1	1	1	1	1	1	1

8.6.4.2 RF_CPG—RF PLL Charge Pump Gain

This is used to control the magnitude of the RF PLL charge pump in steady-state operation.

Table 25. RF_CPG—RF PLL Charge Pump Gain

RF_CPG	CHARGE PUMP STATE	TYPICAL RF CHARGE PUMP CURRENT AT 3 V (µA)
0	1X	95
1	2X	190
2	3X	285
3	4X	380
4	5X	475
5	6X	570
6	7X	665
7	8X	760
8	9X	855
9	10X	950
10	11X	1045
11	12X	1140
12	13X	1235
13	14X	1330
14	15X	1425
15	16X	1520

8.6.4.3 ACCESS—Register Access Word

It is mandatory that the first 5 registers R0-R4 be programmed. The programming of registers R5-R7 is optional. The ACCESS[3:0] bits determine which additional registers must be programmed. Any one of these registers can be individually programmed. According to Table 26, when the state of a register is in default mode, all the bits in that register are forced to a default state and it is not necessary to program this register. When the register is programmable, it needs to be programmed through the MICROWIRE. Using this register access technique, the programming required is reduced up to 37%.

Table 26. ACCESS—Register Access Word

ACCESS BIT	REGISTER LOCATION	REGISTER CONTROLLED
ACCESS[0]	R3[20]	Must be set to 1
ACCESS[1]	R3[21]	R5
ACCESS[2]	R3[22]	R6
ACCESS[3]	R3[23]	R7

The default conditions the registers is shown in Table 27:

Table 27. R4 – R7 Registers

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data[19:0]																				**C3**	**C2**	**C1**	**C0**
R4	R4 Must be programmed manually.																							
R5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
R6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
R7	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	1	1	1

This corresponds to the following bit settings.

Table 28. R4 – R7 Register Descriptions

REGISTER	BIT LOCATION	BIT NAME	BIT DESCRIPTION	BIT VALUE	BIT STATE
R4	R4[23]	ATPU	Autopowerup	0	Disabled
	R4[17:16]	DITH	Dithering	2	Strong
	R4[15:14]	FM	Modulation Order	3	3rd Order
	R4[12]	OSC_2X	Oscillator Doubler	0	Disabled
	R4[11]	OSC_OUT	OSCout Pin Enable	0	Disabled
	R4[10]	IF_CPP	IF Charge Pump Polarity	1	Positive
	R4[9]	RF_CPP	RF Charge Pump Polarity	1	Positive
	R4[8]	IF_P	IF PLL Prescaler	1	16/17
	R4[7:4]	MUX	Ftest/LD Output	0	Disabled
R5	R5[23:14]	RF_FD[21:12]	Extended Fractional Denominator	0	Disabled
	R5[13:4]	RF_FN[21:12]	Extended Fractional Numerator	0	Disabled
R6	R6[23:22]	CSR	Cycle Slip Reduction	0	Disabled
	R6[21:18]	RF_CPF	Fastlock Charge Pump Current	0	Disabled
	R6[17:4]	RF_TOC	RF Time-out Counter	0	Disabled
R7	R7[13]	DIV4	Lock Detect Adjustment	0	Disabled (Fcomp ≤ 20 MHz)
	R7[7]	IF_RST	IF PLL Counter Reset	0	Disabled
	R7[6]	RF_RST	RF PLL Counter Reset	0	Disabled
	R7[5]	IF_CPT	IF PLL Tri-State	0	Disabled
	R7[4]	RF_CPT	RF PLL Tri-State	0	Disabled

8.6.5 R4 Register

This register controls the conditions for the RF PLL in Fastlock.

Table 29. R4 Register

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R4	ATPU	0	1	0	0	0	DITH [1:0]		FM [1:0]		0	OSC_ 2X	OSC_ OUT	IF_ CPP	RF_ CPP	IF_P	MUX [3:0]				1	0	0	1

8.6.5.1 MUX[3:0] Frequency Out and Lock Detect MUX

These bits determine the output state of the Ftest/LD pin.

Table 30. MUX[3:0] Frequency Out and Lock Detect MUX

MUX[3:0]				OUTPUT TYPE	OUTPUT DESCRIPTION
0	0	0	0	High Impedance	Disabled
0	0	0	1	Push-Pull	General-purpose output, Logical “High” State
0	0	1	0	Push-Pull	General-purpose output, Logical “Low” State
0	0	1	1	Push-Pull	RF and IF Digital Lock Detect
0	1	0	0	Push-Pull	RF Digital Lock Detect
0	1	0	1	Push-Pull	IF Digital Lock Detect
0	1	1	0	Open-Drain	RF and IF Analog Lock Detect
0	1	1	1	Open-Drain	RF Analog Lock Detect
1	0	0	0	Open-Drain	IF Analog Lock Detect
1	0	0	1	Push-Pull	RF and IF Analog Lock Detect
1	0	1	0	Push-Pull	RF Analog Lock Detect
1	0	1	1	Push-Pull	IF Analog Lock Detect
1	1	0	0	Push-Pull	IF R Divider divided by 2
1	1	0	1	Push-Pull	IF N Divider divided by 2
1	1	1	0	Push-Pull	RF R Divider divided by 2
1	1	1	1	Push-Pull	RF N Divider divided by 2

8.6.5.2 IF_P—IF Prescaler

When this bit is set to 0, the 8/9 prescaler is used. Otherwise the 16/17 prescaler is used.

Table 31. IF_P—IF Prescaler

IF_P	IF Prescaler	MAXIMUM FREQUENCY
0	8/9	800 MHz
1	16/17	800 MHz

8.6.5.3 RF_CPP—RF PLL Charge Pump Polarity

Table 32. RF_CPP—RF PLL Charge Pump Polarity

RF_CPP	RF CHARGE PUMP POLARITY
0	Negative
1	Positive (Default)

8.6.5.4 IF_CPP—IF PLL Charge Pump Polarity

For a positive phase detector polarity, which is normally the case, set this bit to 1. Otherwise set this bit for a negative phase detector polarity.

Table 33. IF_CPP—IF PLL Charge Pump Polarity

IF_CPP	IF CHARGE PUMP POLARITY
0	Negative
1	Positive

8.6.5.5 OSC_OUT Oscillator Output Buffer Enable

Table 34. OSC_OUT Oscillator Output Buffer Enable

OSC_OUT	OSCout PIN
0	Disabled (High Impedance)
1	Buffered output of OSCin pin

8.6.5.6 OSC2X—Oscillator Doubler Enable

When this bit is set to 0, the oscillator doubler is disabled and the TCXO frequency presented to the IF R and RF R counters is equal to that of the input frequency of the OSCin pin. When this bit is set to 1, the TCXO frequency presented to the RF R counter is doubled. Phase noise added by the doubler is negligible.

Table 35. OSC2X—Oscillator Doubler Enable

OSC2X	FREQUENCY PRESENTED TO RF R COUNTER	FREQUENCY PRESENTED TO IF R COUNTER
0	f_{OSCin}	f_{OSCin}
1	2 x f_{OSCin}	

8.6.5.7 FM[1:0]—Fractional Mode

Determines the order of the delta-sigma modulator. Higher order delta-sigma modulators reduce the spur levels closer to the carrier by pushing this noise to higher frequency offsets from the carrier. In general, the order of the loop filter should be at least one greater than the order of the delta-sigma modulator to allow for sufficient roll-off.

Table 36. FM[1:0]—Fractional Mode

FM	FUNCTION
0	Fractional PLL mode with a 4th order delta-sigma modulator
1	Disable the delta-sigma modulator. Recommended for test use only.
2	Fractional PLL mode with a 2nd order delta-sigma modulator
3	Fractional PLL mode with a 3rd order delta-sigma modulator

8.6.5.8 DITH[1:0]—Dithering Control

Dithering is a technique used to spread out the spur energy. Enabling dithering can reduce the main fractional spurs, but can also give rise to a family of smaller spurs. Whether dithering helps or hurts is application specific. Enabling the dithering may also increase the phase noise. In most cases where the fractional numerator is zero, dithering usually degrades performance.

Dithering tends to be most beneficial in applications where there is insufficient filtering of the spurs. This often occurs when the loop bandwidth is very wide or a higher order delta-sigma modulator is used. Dithering tends not to impact the main fractional spurs much, but has a much larger impact on the sub-fractional spurs. If it is decided that dithering will be used, best results will be obtained when the fractional denominator is at least 1000.

Table 37. DITH[1:0]—Dithering Control

DITH	DITHERING MODE USED
0	Disabled
1	Weak Dithering
2	Strong Dithering
3	Reserved

8.6.5.9 ATPU—PLL Automatic Power Up

When this bit is set to 1, both the RF and IF PLL when the R0 register is written to. When the R0 register is written to, the PD_RF and PD_IF bits are changed to 0 in the PLL registers. The exception to this case is when the CE pin is low. In this case, the ATPU function is disabled.

8.6.6 R5 Register

Table 38. R5 Register

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R5	RF_FD[21:12]										RF_FN[21:12]										1	0	1	1

8.6.6.1 Fractional Numerator Determination { RF_FN[21:12], RF_FN[11:0], Access[1] }

In the case that the ACCESS[1] bit is 0, then the part operates in 12-bit fractional mode, and the RF_FN2[21:12] bits become do not care bits. When the ACCESS[1] bit is set to 1, the part operates in 22-bit mode and the fractional numerator is expanded from 12 to 22-bits.

Table 39. Fractional Numerator Determination { RF_FN[21:12], RF_FN[11:0], Access[1] }

FRACTIONAL	RF_FN[21:12]										RF_FN[11:0]											
NUMERATOR	(THESE BITS ONLY APPLY IN 22-BIT MODE)																					
0	In 12-bit mode, these are do not care. In 22-bit mode, for N <4096, these bits should be all set to 0.										0	0	0	0	0	0	0	0	0	0	0	0
1											0	0	0	0	0	0	0	0	0	0	0	1
...											.	.	.	.	.	.	.	.	.	.	.	.
4095											1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.6.6.2 Fractional Denominator Determination { RF_FD[21:12], RF_FD[11:0], Access[1]}

In the case that the ACCESS[1] bit is 0, then the part is operates in the 12-bit fractional mode, and the RF_FD[21:12] bits become do not care bits. When the ACCESS[1] is set to 1, the part operates in 22-bit mode and the fractional denominator is expanded from 12 to 22-bits.

Table 40. Fractional Denominator Determination { RF_FD[21:12], RF_FD[11:0], Access[1]}

FRACTIONAL	RF_FD[21:12]										RF_FD[11:0]											
DENOMINATOR	(These bits only apply in 22-bit mode)																					
0	In 12-bit mode, these are do not care. In 22-bit mode, for N <4096, these bits should be all set to 0.										0	0	0	0	0	0	0	0	0	0	0	0
1											0	0	0	0	0	0	0	0	0	0	0	1
...											.	.	.	.	.	.	.	.	.	.	.	.
4095											1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.6.7 R6 Register

Table 41. R6 Register

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R6	CSR[1:0]		RF_CPF[3:0]				RF_TOC[13:0]														1	1	0	1

8.6.7.1 RF_TOC—RF Time Out Counter and Control for FLoutRF Pin

The RF_TOC[13:0] word controls the operation of the RF Fastlock circuitry as well as the function of the FLoutRF output pin. When this word is set to a value between 0 and 3, the RF Fastlock circuitry is disabled and the FLoutRF pin operates as a general-purpose CMOS TRI-STATE I/O. When RF_TOC is set to a value between 4 and 16383, the RF Fastlock mode is enabled and the FLoutRF pin is used as the RF Fastlock output pin. The value programmed into the RF_TOC[13:0] word represents two times the number of phase detector comparison cycles the RF synthesizer will spend in the Fastlock state.

Table 42. RF_TOC—RF Time Out Counter and Control for FLoutRF Pin

RF_TOC	FASTLOCK MODE	FASTLOCK PERIOD [CP EVENTS]	FLoutRF PIN FUNCTIONALITY
0	Disabled	N/A	High Impedance
1	Manual	N/A	Logic “0” State. Forces all Fastlock conditions
2	Disabled	N/A	Logic “0” State
3	Disabled	N/A	Logic “1” State
4	Enabled	4X2 = 8	Fastlock
5	Enabled	5X2 = 10	Fastlock
…	Enabled	…	Fastlock
16383	Enabled	16383X2 = 32766	Fastlock

8.6.7.2 RF_CPF—RF PLL Fastlock Charge Pump Current

Specify the charge pump current for the Fastlock operation mode for the RF PLL.

NOTE

The Fastlock charge pump current, steady-state current, and CSR control are all interrelated.

Table 43. RF_CPF—RF PLL Fastlock Charge Pump Current

RF_CPF	RF CHARGE PUMP STATE	TYPICAL RF CHARGE PUMP CURRENT AT 3 V (µA)
0	1X	95
1	2X	190
2	3X	285
3	4X	380
4	5X	475
5	6X	570
6	7X	665
7	8X	760
8	9X	855
9	10X	950
10	11X	1045
11	12X	1140
12	13X	1235
13	14X	1330
14	15X	1425
15	16X	1520

8.6.7.3 CSR[1:0]—RF Cycle Slip Reduction

CSR controls the operation of the Cycle Slip Reduction Circuit. This circuit can be used to reduce the occurrence of phase detector cycle slips.

NOTE

The Fastlock charge pump current, steady-state current, and CSR control are all interrelated. Refer to *Cycle Slip Reduction and Fastlock* for information on how to use this.

Table 44. CSR[1:0]—RF Cycle Slip Reduction

CSR	CSR STATE	SAMPLE RATE REDUCTION FACTOR
0	Disabled	1
1	Enabled	1/2
2	Enabled	1/4
3	Enabled	1/16

8.6.8 R7 Register

Table 45. R7 Register

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data[19:0]																				C3	C2	C1	C0
R7	0	0	0	0	0	0	0	0	0	0	DIV4	0	1	0	0	1	IF_RST	RF_RST	IF_CPT	RF_CPT	1	1	1	1

8.6.8.1 DIV4—RF Digital Lock Detect Divide By 4

Because the digital lock detect function is based on a phase error, it becomes more difficult to detect a locked condition for larger comparison frequencies. When this bit is enabled, it subdivides the RF PLL comparison frequency (it does not apply to the IF comparison frequency) presented to the digital lock detect circuitry by 4. This enables this circuitry to work at higher comparison frequencies. TI recommends that this bit be enabled whenever the comparison frequency exceeds 20 MHz and RF digital lock detect is being used.

8.6.8.2 IF_RST—IF PLL Counter Reset

When this bit is enabled, the IF PLL N and R counters are reset, and the charge pump is put in a Tri-State condition. This feature should be disabled for normal operation.

NOTE

A counter reset is applied whenever the chip is powered up through software or CE pin.

Table 46. IF_RST—IF PLL Counter Reset

IF_RST	IF PLL N AND R COUNTERS	IF PLL CHARGE PUMP
0 (Default)	Normal Operation	Normal Operation
1	Counter Reset	Tri-State

8.6.8.3 RF_RST—RF PLL Counter Reset

When this bit is enabled, the RF PLL N and R counters are reset and the charge pump is put in a Tri-State condition. This feature should be disabled for normal operation. This feature should be disabled for normal operation.

NOTE

A counter reset is applied whenever the chip is powered up through software or CE pin.

Table 47. RF_RST—RF PLL Counter Reset

RF_RST	RF PLL N AND R COUNTERS	RF PLL CHARGE PUMP
0 (Default)	Normal Operation	Normal Operation
1	Counter Reset	Tri-State

8.6.8.4 RF_TRI—RF Charge Pump Tri-State

When this bit is enabled, the RF PLL charge pump is put in a Tri-State condition, but the counters are not reset. This feature is typically disabled for normal operation.

Table 48. RF_TRI—RF Charge Pump Tri-State

RF_TRI	RF PLL N AND R COUNTERS	RF PLL CHARGE PUMP
0 (Default)	Normal Operation	Normal Operation
1	Normal Operation	Tri-State

8.6.8.5 IF_TRI—IF Charge Pump Tri-State

When this bit is enabled, the IF PLL charge pump is put in a Tri-State condition, but the counters are not reset. This feature is typically disabled for normal operation.

Table 49. IF_TRI—IF Charge Pump Tri-State

IF_TRI	IF PLL N AND R COUNTERS	IF PLL CHARGE PUMP
0 (Default)	Normal Operation	Normal Operation
1	Normal Operation	Tri-State

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This device ideal for use in a broad class of applications, especially those requiring low current consumption and low fractional spurs. For applications that only need a single PLL, the unused PLL can be powered down and will not draw any extra current or generate any spurs or crosstalk.

9.2 Typical Application

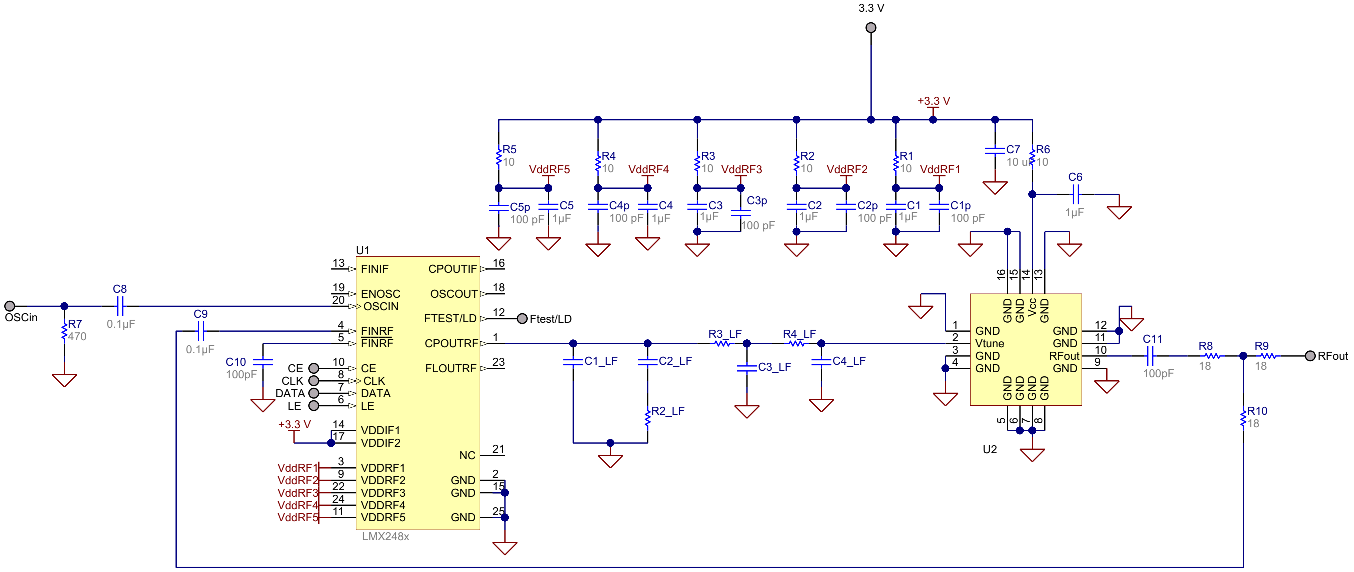


Figure 24. Typical Application With Just RF Side Used

Typical Application (continued)

9.2.1 Design Requirements

Table 50 lists the design parameters of the LMX2485x.

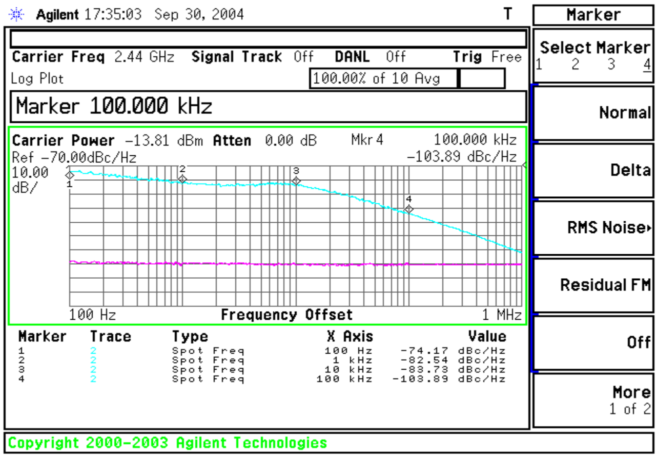
Table 50. Design Parameters

PARAMETER		VALUE
PM	Phase Margin	48.3 degrees
BW	Loop Bandwidth	11.3 kHz
T3/T1	Pole Ratios	40.20%
T4/T3		36.30%
K_{PD}	Phase Detector Gain	400 µA
f_{PD}	Phase Detector Frequency	10 MHz
f_{VCO}	Output Frequency	2400 – 2480 MHz
Vcc	Supply Voltage	3 V
K_{VCO}	VCO Gain	55 MHz/V
C_{VCO}	VCO Input Capacitance	22 pF
C1_LF	Loop Filter Components	2.7 nF
C2_LF		47 nF
C3_LF		270 pF
C4_LF		180 pF
R2_LF		820 Ω
R3_LF		3.9 kΩ
R4_LF		5.6 kΩ

9.2.2 Detailed Design Procedure

The design of the loop filter involves balancing requirements of lock time, spurs, and phase noise. This design is fairly involved, but the TI website has references, design tools, and simulation tools cover the loop filter design and simulation in depth.

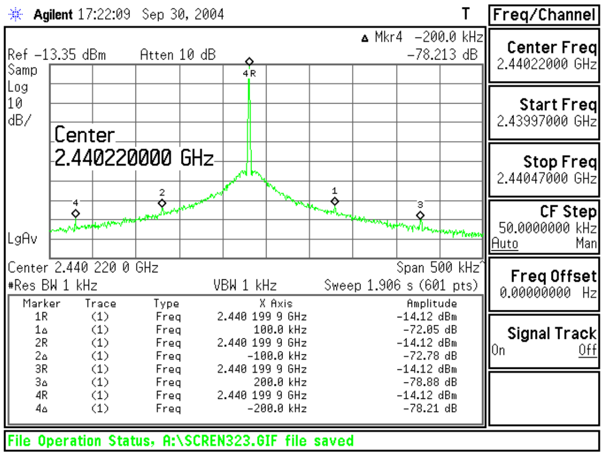
9.2.3 Application Curves



```
Carrier Freq 2.44 GHz   Signal Track Off   DANL  Off     Trig Free
Log Plot                          100.00% of 10 Avg
Marker 100.000 kHz
Carrier Power -13.81 dBm  Atten 0.00 dB   Mkr 4     100.000 kHz
Ref -70.00dBc/Hz                                  -103.89 dBc/Hz

Marker   Trace    Type          X Axis         Value
1        2        Spot Freq     100 Hz     -74.17 dBc/Hz
2        2        Spot Freq       1 kHz    -82.54 dBc/Hz
3        2        Spot Freq      10 kHz    -83.73 dBc/Hz
4        2        Spot Freq     100 kHz   -103.89 dBc/Hz
```

Figure 25. Phase Noise at 2440 MHz



```
                                      Δ Mkr4  -200.0 kHz
Ref -13.35 dBm     Atten 10 dB                -78.213 dB

Center 2.440 220 0 GHz                       Span 500 kHz
#Res BW 1 kHz           VBW 1 kHz    Sweep 1.906 s (601 pts)

Marker   Trace   Type     X Axis               Amplitude
 1R      (1)     Freq     2.440 199 9 GHz      -14.12 dBm
 1Δ      (1)     Freq         100.0 kHz        -72.05 dB
 2R      (1)     Freq     2.440 199 9 GHz      -14.12 dBm
 2Δ      (1)     Freq        -100.0 kHz        -72.78 dB
 3R      (1)     Freq     2.440 199 9 GHz      -14.12 dBm
 3Δ      (1)     Freq         200.0 kHz        -78.88 dB
 4R      (1)     Freq     2.440 199 9 GHz      -14.12 dBm
 4Δ      (1)     Freq        -200.0 kHz        -78.21 dB

File Operation Status, A:\SCREN323.GIF file saved
```

Figure 26. Spurs for Fractional Channel of 2440.2 MHz

10 Power Supply Recommendations

Low-noise regulators are generally recommended for the supply pins. It is OK to have one regulator supply the part, although it is best to put individual bypassing as shown in the *Layout Guidelines* for the best spur performance. If only using one PLL and not both DO NOT DISCONNECT OR GROUND power pins! For instance, the IF PLL supply pins also supply other blocks than just the IF PLL and they must be connected. However, if the IF PLL is disabled, then one can eliminate all bypass capacitors for these pins.

11 Layout

11.1 Layout Guidelines

The critical pin is the high frequency input pin that should be short. In general, try to keep the ground and power planes 20 mils or further from vias to supply pins to ensure that no spur energy can couple to them.

11.2 Layout Example

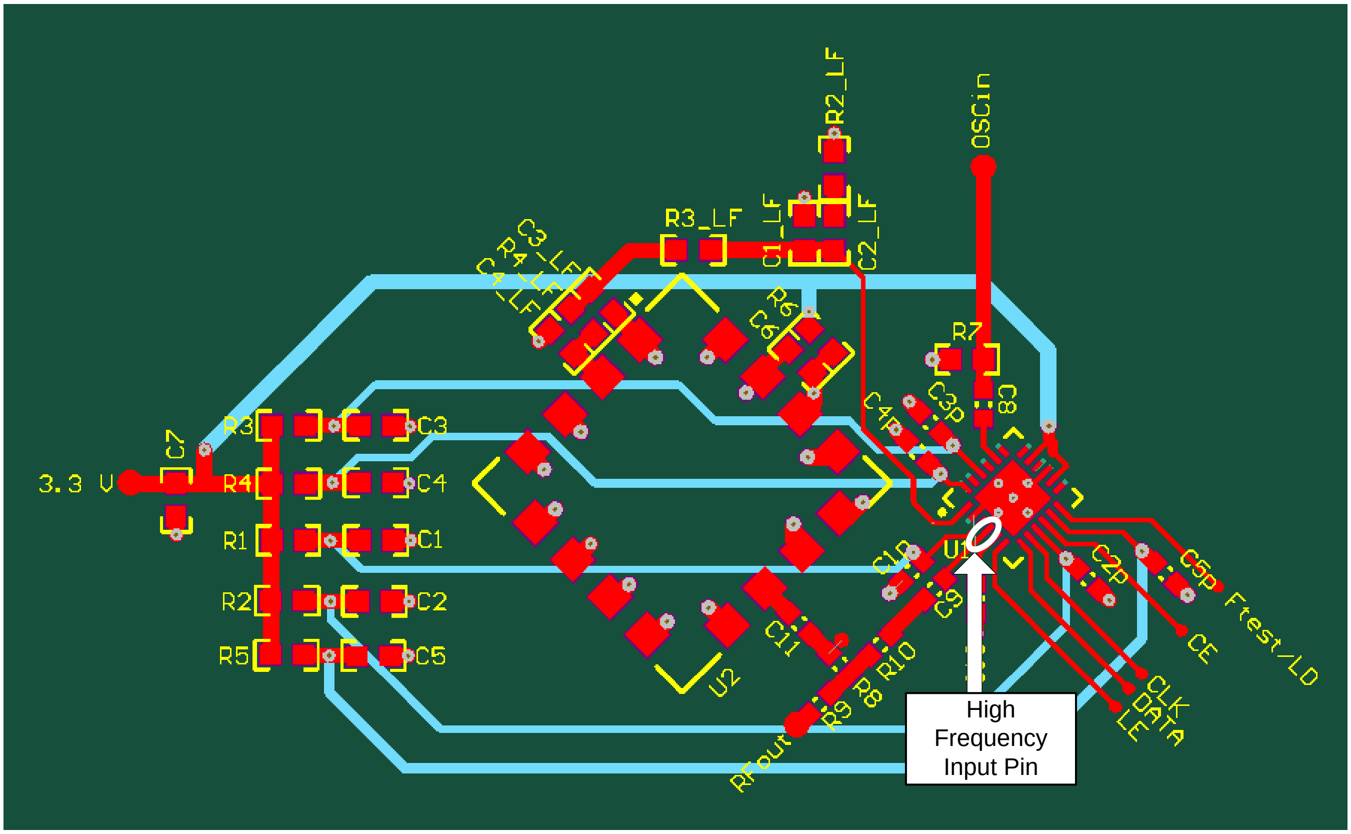


Figure 27. Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 51. Related Links

PARTS	PRODUCT FOLDER	SAMPLE AND BUY	TECHNICAL DOCUMENTS	TOOLS AND SOFTWARE	SUPPORT AND COMMUNITY
LMX2485	Click here	Click here	Click here	Click here	Click here
LMX2485E	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

PLLatinum, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMX2485ESQ/NOPB	Active	Production	WQFN (RTW) | 24	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	2485E>D
LMX2485ESQ/NOPB.A	Active	Production	WQFN (RTW) | 24	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	2485E>D
LMX2485ESQX/NOPB	Active	Production	WQFN (RTW) | 24	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	2485E>D
LMX2485ESQX/NOPB.A	Active	Production	WQFN (RTW) | 24	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	2485E>D
LMX2485SQ/NOPB	Active	Production	WQFN (RTW) | 24	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	X2485>D
LMX2485SQ/NOPB.A	Active	Production	WQFN (RTW) | 24	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	X2485>D
LMX2485SQX/NOPB	Active	Production	WQFN (RTW) | 24	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	X2485>D
LMX2485SQX/NOPB.A	Active	Production	WQFN (RTW) | 24	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	X2485>D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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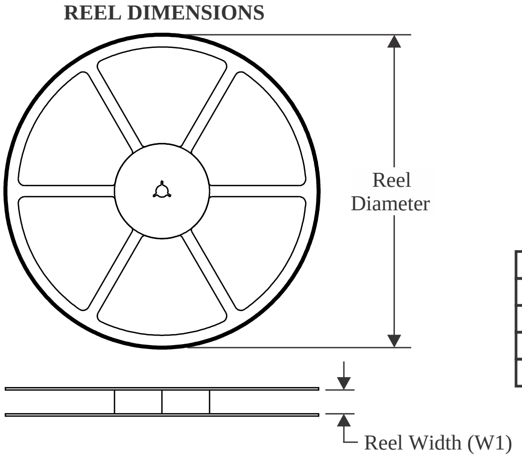
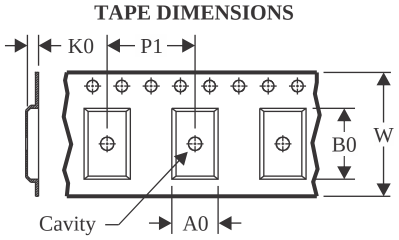
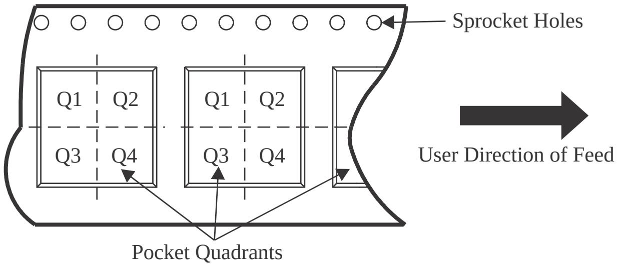
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

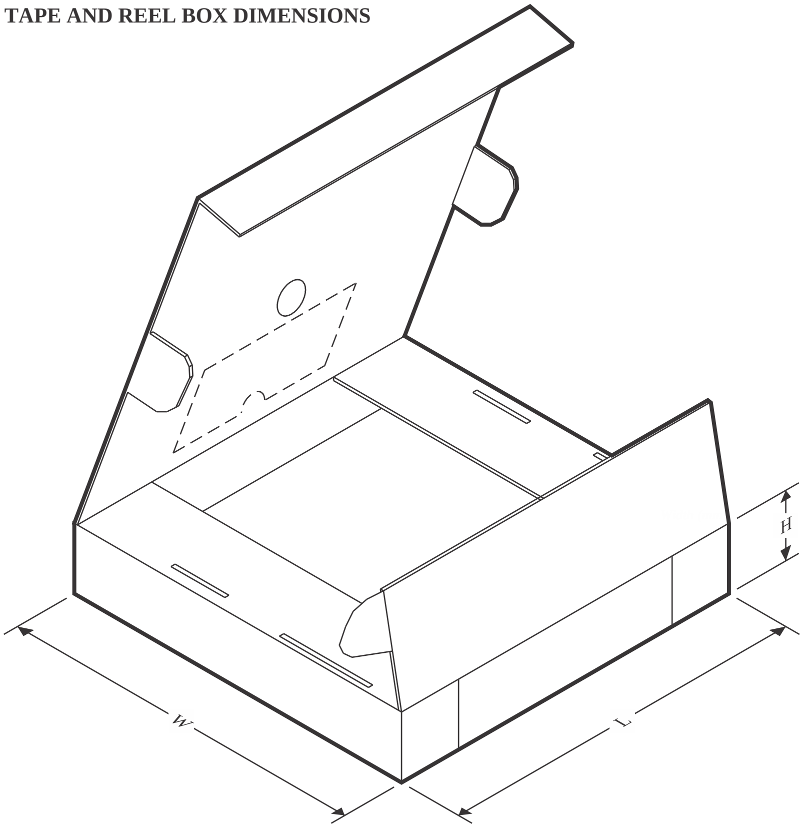
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

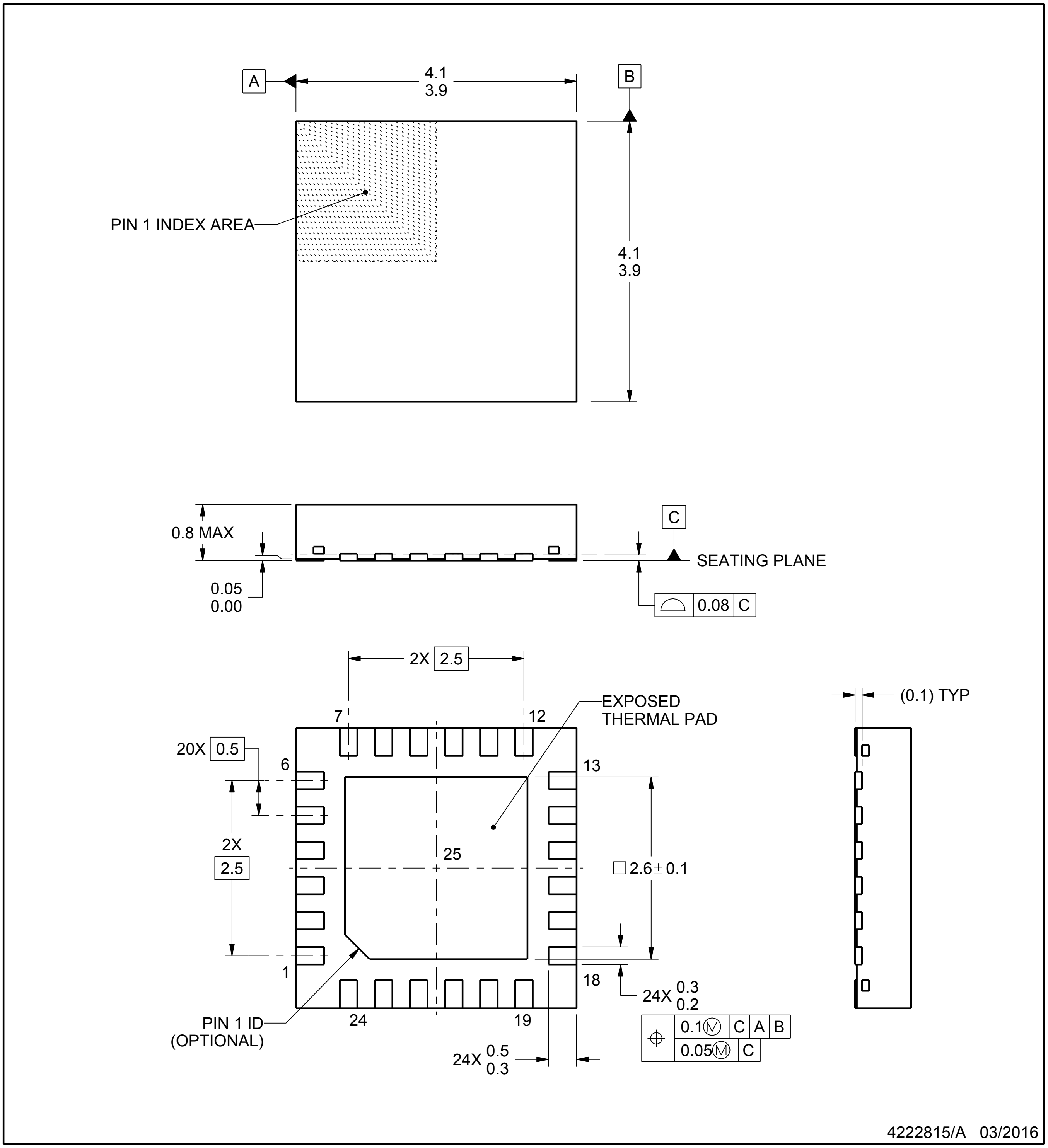
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2485ESQ/NOPB	WQFN	RTW	24	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMX2485ESQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMX2485SQ/NOPB	WQFN	RTW	24	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMX2485SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

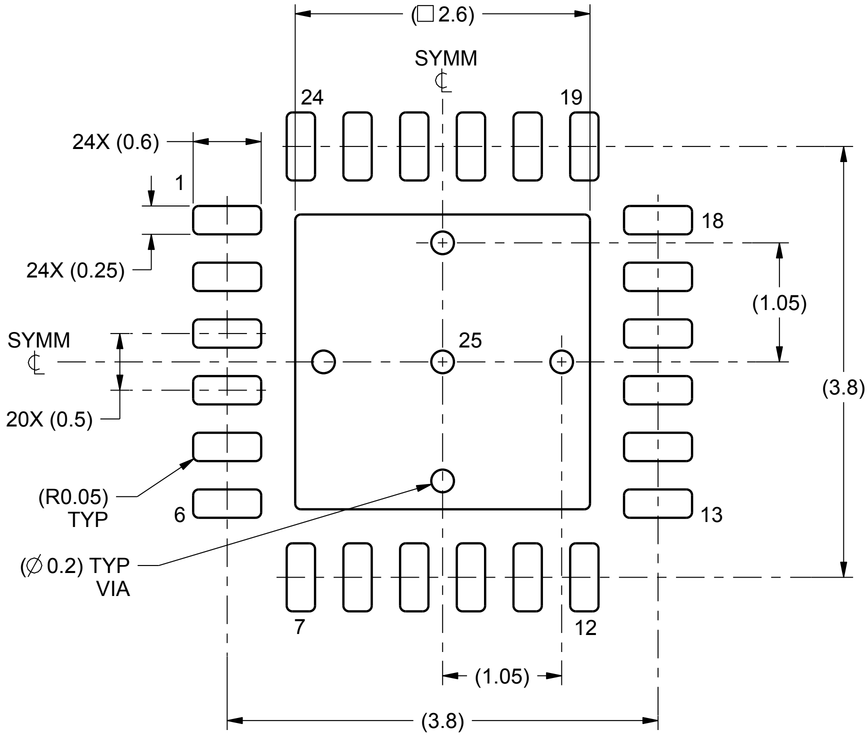
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2485ESQ/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LMX2485ESQX/NOPB	WQFN	RTW	24	4500	356.0	356.0	36.0
LMX2485SQ/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LMX2485SQX/NOPB	WQFN	RTW	24	4500	356.0	356.0	36.0



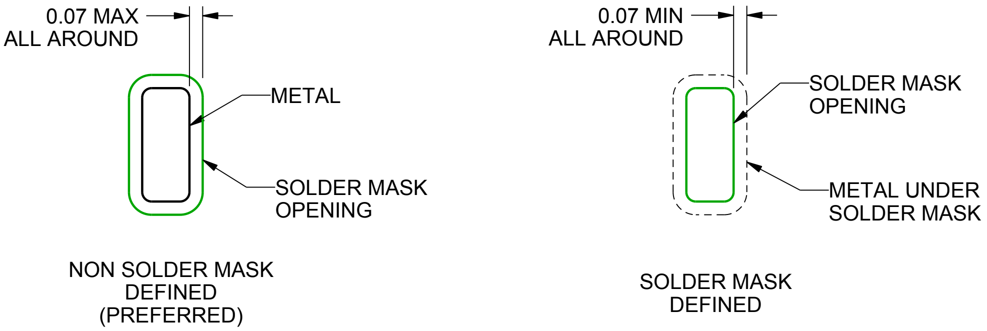
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

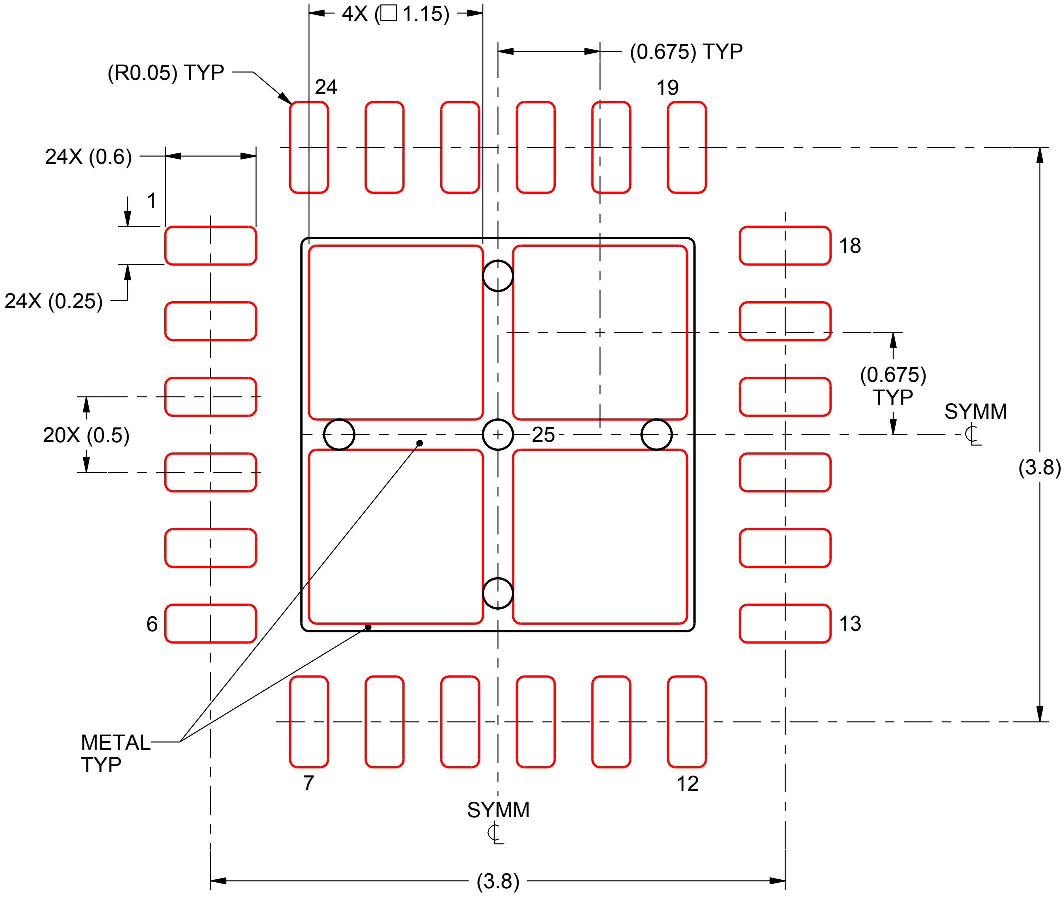


SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025