



## Single-Supply, 10MHz, Rail-to-Rail Output, Low-Noise, JFET Amplifier

 Check for Samples: [OPA141](#), [OPA2141](#), [OPA4141](#)

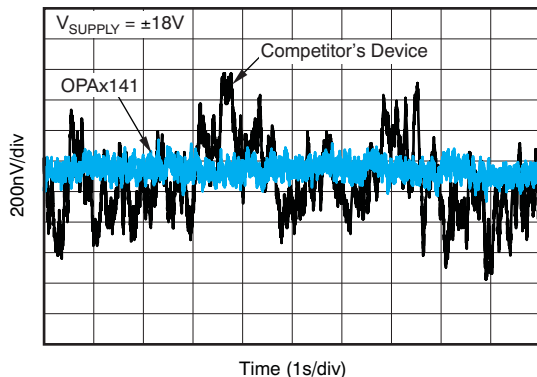
### FEATURES

- **Low Supply Current:** 2.3mA max
- **Low Offset Drift:** 10 $\mu$ V/ $^{\circ}$ C max
- **Low Input Bias Current:** 20pA max
- **Very Low 1/f Noise:** 250nV<sub>PP</sub>
- **Low Noise:** 6.5nV/ $\sqrt{\text{Hz}}$
- **Wide Bandwidth:** 10MHz
- **Slew Rate:** 20V/ $\mu$ s
- **Input Voltage Range Includes V<sub>-</sub>**
- **Rail-to-Rail Output**
- **Single-Supply Operation:** 4.5V to 36V
- **Dual-Supply Operation:**  $\pm$ 2.25V to  $\pm$ 18V
- **No Phase Reversal**
- **MSOP-8, TSSOP Packages**

### APPLICATIONS

- **Battery-Powered Instruments**
- **Industrial Controls**
- **Medical Instrumentation**
- **Photodiode Amplifiers**
- **Active Filters**
- **Data Acquisition Systems**
- **Portable Audio**
- **Automatic Test Systems**

#### 0.1Hz to 10Hz NOISE



### DESCRIPTION

The OPA141, OPA2141, and OPA4141 amplifier family is a series of low-power JFET input amplifiers that feature good drift and low input bias current. The rail-to-rail output swing and input range that includes V<sub>-</sub> allow designers to take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

The OPA141 achieves 10MHz unity-gain bandwidth and 20V/ $\mu$ s slew rate while consuming only 1.8mA (typ) of quiescent current. It runs on a single 4.5 to 36V supply or dual  $\pm$ 2.25V to  $\pm$ 18V supplies.

All versions are fully specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for use in the most challenging environments. The OPA141 (single) and OPA2141 (dual) versions are available in both MSOP-8 and SO-8 packages; the OPA4141 (quad) is available in the SO-14 and TSSOP-14 packages.

### RELATED PRODUCTS

FEATURES	PRODUCT
Precision, Low-Power, 10MHz FET Input Industrial Op Amp	OPA140 <sup>(1)</sup>
2.2nV/ $\sqrt{\text{Hz}}$ , Low-Power, 36V Operational Amplifier in SOT-23 Package	OPA209 <sup>(1)</sup>
Low-Noise, High-Precision, JFET-Input Operational Amplifier	<a href="#">OPA827</a>
Low-Noise, Low I <sub>Q</sub> Precision Operational Amplifier	<a href="#">OPA376</a>
High-Speed, FET-Input Operational Amplifier	<a href="#">OPA132</a>

1. Preview product; estimated availability in Q3 2010.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage		±20	V
Signal Input Terminals	Voltage <sup>(2)</sup>	(V–) –0.5 to (V+) +0.5	V
	Current <sup>(2)</sup>	±10	mA
Output Short-Circuit <sup>(3)</sup>		Continuous	
Operating Temperature, T <sub>A</sub>		–55 to +150	°C
Storage Temperature, T <sub>A</sub>		–65 to +150	°C
Junction Temperature, T <sub>J</sub>		+150	°C
ESD Ratings	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	500	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to V<sub>S</sub>/2 (ground in symmetrical dual-supply setups), one amplifier per package.

## PACKAGE INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA141	SO-8	D	O141A
	MSOP-8	DGK	141
OPA2141	SO-8	D	O2141A
	MSOP-8	DGK	2141
OPA4141	TSSOP-14	PW	O4141A
	SO-14	D	O4141AG4

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

**THERMAL INFORMATION**

THERMAL METRIC		OPA141, OPA2141	OPA141, OPA2141	UNITS
		D (SO)	DGK (MSOP) <sup>(1)</sup>	
		8	8	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	160	180	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance <sup>(3)</sup>	75	55	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	60	130	
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	9	n/a	
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	50	120	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance <sup>(7)</sup>	n/a	n/a	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

**THERMAL INFORMATION**

THERMAL METRIC		OPA4141	OPA4141	UNITS
		D (SO)	PW (TSSOP) <sup>(1)</sup>	
		14	14	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	97	135	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance <sup>(3)</sup>	56	45	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	53	66	
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	19	n/a	
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	46	60	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance <sup>(7)</sup>	n/a	n/a	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
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**ELECTRICAL CHARACTERISTICS:  $V_S = +4.5V$  to  $+36V$ ;  $\pm 2.25V$  to  $\pm 18V$**

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ C$  to  $+125^\circ C$ .

At  $T_A = +25^\circ C$ ,  $R_L = 2k\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

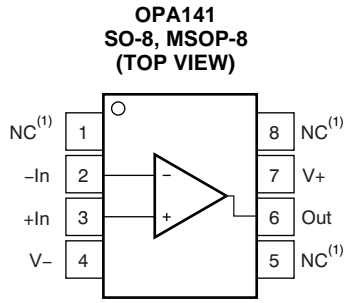
PARAMETER	CONDITIONS	OPA141, OPA2141, OPA4141			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Offset Voltage, RTI	$V_{OS}$	$V_S = \pm 18V$	$\pm 1$	$\pm 3.5$	mV
<b>Over Temperature</b>		<b><math>V_S = \pm 18V</math></b>		<b><math>\pm 4.3</math></b>	<b>mV</b>
<b>Drift</b>	$dV_{OS}/dT$	<b><math>V_S = \pm 18V</math></b>	<b><math>\pm 2</math></b>	<b><math>\pm 10</math></b>	$\mu V/^\circ C$
vs Power Supply	PSRR	$V_S = \pm 2.25V$ to $\pm 18V$	$\pm 0.14$	$\pm 2$	$\mu V/V$
<b>Over Temperature</b>		<b><math>V_S = \pm 2.25V</math> to <math>\pm 18V</math></b>		<b><math>\pm 4</math></b>	<b><math>\mu V/V</math></b>
<b>INPUT BIAS CURRENT</b>					
Input Bias Current	$I_B$		$\pm 2$	$\pm 20$	pA
<b>Over Temperature</b>				<b><math>\pm 5</math></b>	<b>nA</b>
Input Offset Current	$I_{OS}$		$\pm 2$	$\pm 20$	pA
<b>Over Temperature</b>				<b><math>\pm 1</math></b>	<b>nA</b>
<b>NOISE</b>					
Input Voltage Noise					
$f = 0.1Hz$ to $10Hz$			250		nV <sub>PP</sub>
$f = 0.1Hz$ to $10Hz$			42		nV <sub>RMS</sub>
Input Voltage Noise Density	$e_n$				
$f = 10Hz$			12		nV/ $\sqrt{Hz}$
$f = 100Hz$			6.5		nV/ $\sqrt{Hz}$
$f = 1kHz$			6.5		nV/ $\sqrt{Hz}$
Input Current Noise Density	$i_n$				
$f = 1kHz$			0.8		fA/ $\sqrt{Hz}$
<b>INPUT VOLTAGE RANGE</b>					
<b>Common-Mode Voltage Range</b>	$V_{CM}$		<b>(V-) -0.1</b>	<b>(V+) -3.5</b>	<b>V</b>
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 18V$ , $V_{CM} = (V-) -0.1V$ to $(V+) -3.5V$	120	126	dB
<b>Over Temperature</b>		<b><math>V_S = \pm 18V</math>, <math>V_{CM} = (V-) -0.1V</math> to <math>(V+) -3.5V</math></b>	<b>120</b>		<b>dB</b>
<b>INPUT IMPEDANCE</b>					
Differential					
				$10^{13} \parallel 8$	$\Omega \parallel pF$
Common-Mode					
		$V_{CM} = (V-) -0.1V$ to $(V+) -3.5V$		$10^{13} \parallel 6$	$\Omega \parallel pF$
<b>OPEN-LOOP GAIN</b>					
Open-Loop Voltage Gain	$A_{OL}$	$V_O = (V-) +0.35V$ to $(V+) -0.35V$ , $R_L = 2k\Omega$	114	126	dB
<b>Over Temperature</b>		<b><math>V_O = (V-) +0.35V</math> to <math>(V+) -0.35V</math>, <math>R_L = 2k\Omega</math></b>	<b>108</b>		<b>dB</b>
<b>FREQUENCY RESPONSE</b>					
Gain Bandwidth Product	BW		10		MHz
Slew Rate			20		V/ $\mu s$
Settling Time, 12-bit (0.024)			880		ns
THD+N		1kHz, $G = 1$ , $V_O = 3.5V_{RMS}$	0.00005		%
Overload Recovery Time			600		ns

**ELECTRICAL CHARACTERISTICS:  $V_S = +4.5V$  to  $+36V$ ;  $\pm 2.25V$  to  $\pm 18V$  (continued)**
**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ C$  to  $+125^\circ C$ .

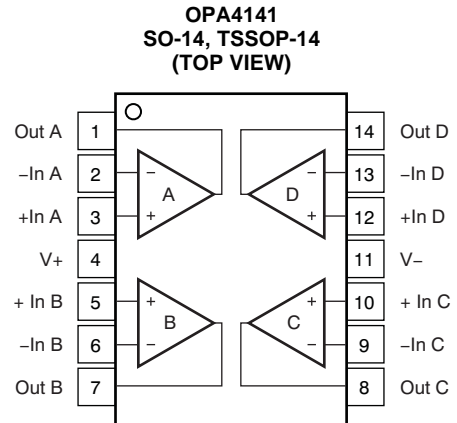
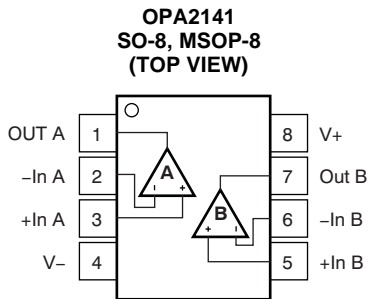
 At  $T_A = +25^\circ C$ ,  $R_L = 2k\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	OPA141, OPA2141, OPA4141			UNIT
		MIN	TYP	MAX	
<b>OUTPUT</b>					
Voltage Output $V_O$	$R_L = 10k\Omega$	$(V-)+0.2$		$(V+)-0.2$	V
	$R_L = 2k\Omega$	$(V-)+0.35$		$(V+)-0.35$	V
Short-Circuit Current $I_{SC}$	Source		+36		mA
	Sink		-30		mA
Capacitive Load Drive $C_{LOAD}$		See <a href="#">Figure 19</a> and <a href="#">Figure 20</a>			
Open-Loop Output Impedance $R_O$	$f = 1MHz, I_O = 0$ (See <a href="#">Figure 18</a> )		10		$\Omega$
<b>POWER SUPPLY</b>					
Specified Voltage Range $V_S$		$\pm 2.25$		$\pm 18$	V
Quiescent Current (per amplifier) $I_Q$	$I_O = 0mA$		1.8	2.3	mA
		<b>Over Temperature</b>		<b>3.1</b>	<b>mA</b>
<b>CHANNEL SEPARATION</b>					
Channel Separation	At dc		0.02		$\mu V/V$
	At 100kHz		10		$\mu V/V$
<b>TEMPERATURE RANGE</b>					
Specified Range		-40		+125	$^\circ C$
Operating Range		-55		+150	$^\circ C$

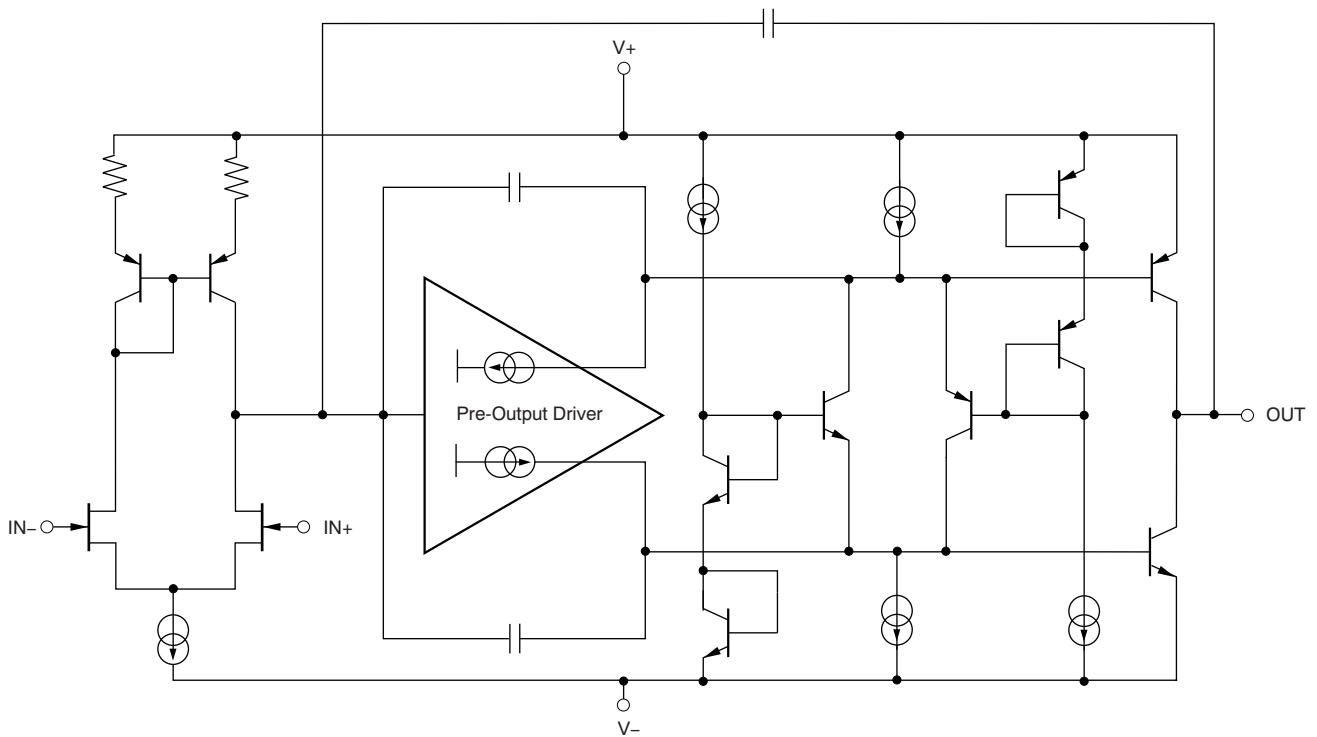
**PIN ASSIGNMENTS**



(1) NC denotes no internal connection.



**SIMPLIFIED BLOCK DIAGRAM**



**Figure 1.**

## TYPICAL CHARACTERISTICS SUMMARY

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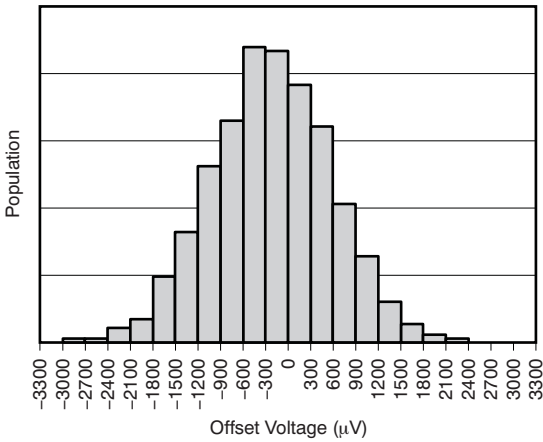
**Table 1. Characteristic Performance Measurements**

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**TYPICAL CHARACTERISTICS**

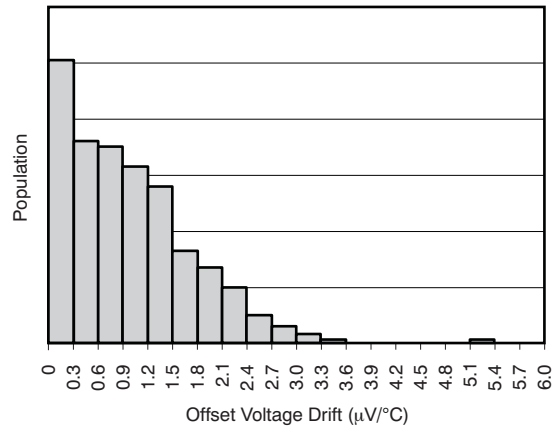
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ ,  $R_L = 2\text{k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

**OFFSET VOLTAGE PRODUCTION DISTRIBUTION**



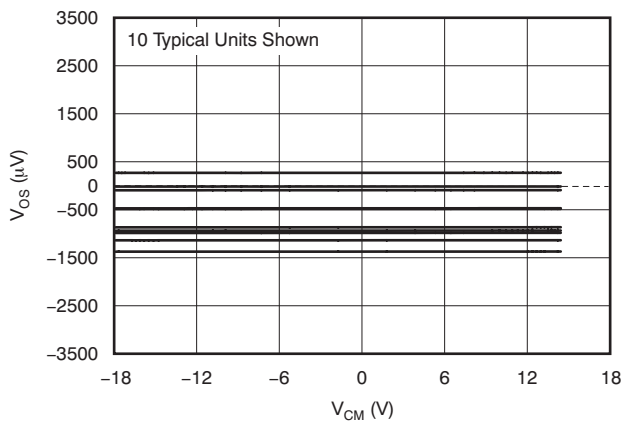
**Figure 2.**

**OFFSET VOLTAGE DRIFT DISTRIBUTION**



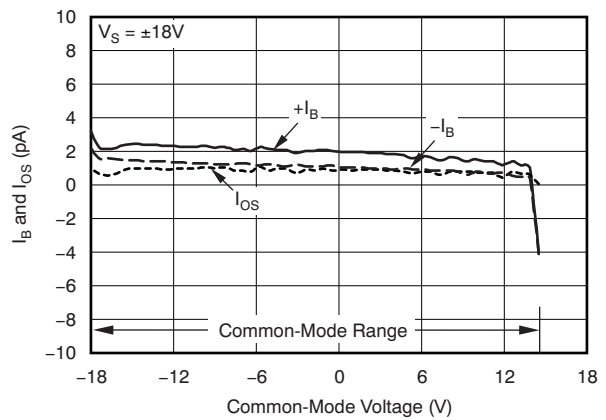
**Figure 3.**

**OFFSET VOLTAGE vs COMMON-MODE VOLTAGE**



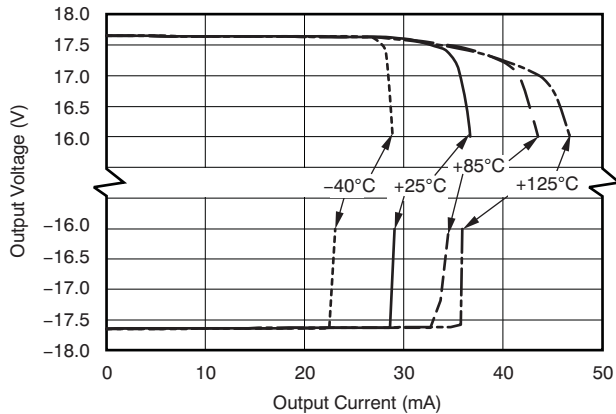
**Figure 4.**

**I<sub>B</sub> AND I<sub>OS</sub> vs COMMON-MODE VOLTAGE**



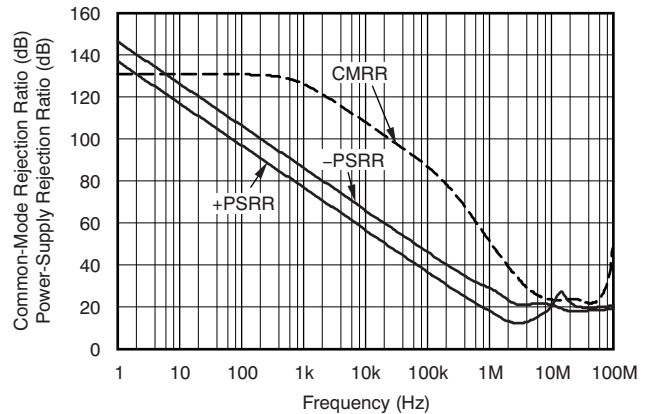
**Figure 5.**

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (MAX SUPPLY)**



**Figure 6.**

**CMRR AND PSRR vs FREQUENCY (Referred to Input)**

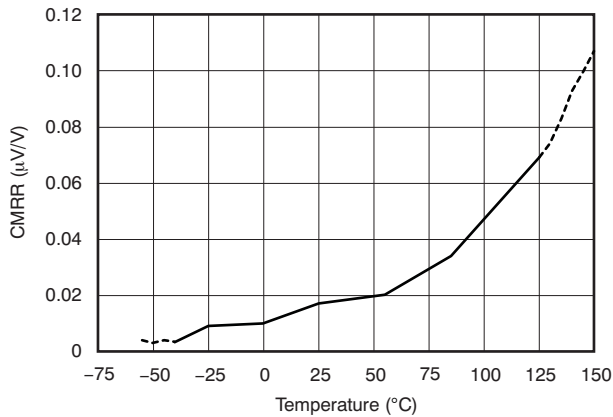


**Figure 7.**

**TYPICAL CHARACTERISTICS (continued)**

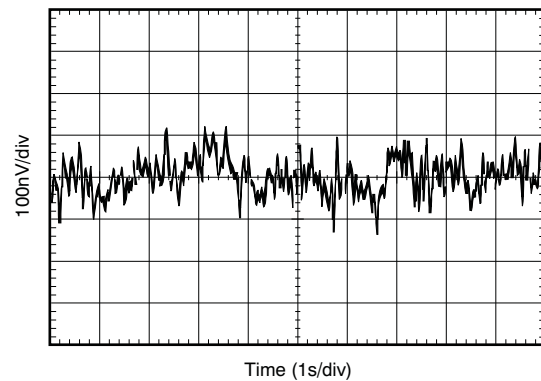
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ ,  $R_L = 2\text{k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

**COMMON-MODE REJECTION RATIO vs TEMPERATURE**



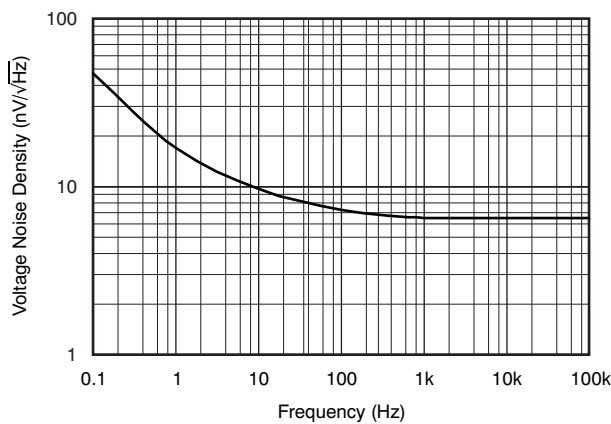
**Figure 8.**

**0.1Hz to 10Hz NOISE**



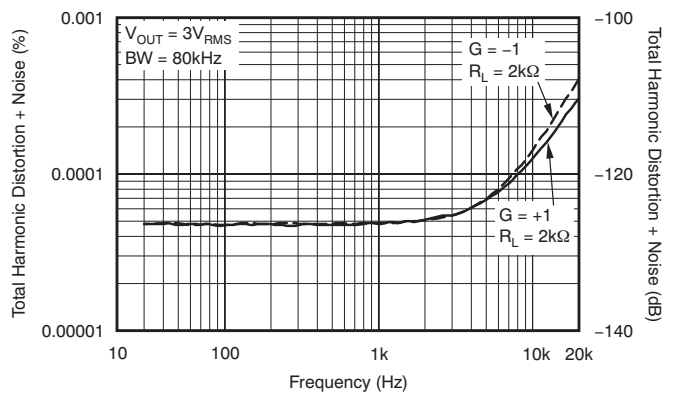
**Figure 9.**

**INPUT VOLTAGE NOISE DENSITY vs FREQUENCY**



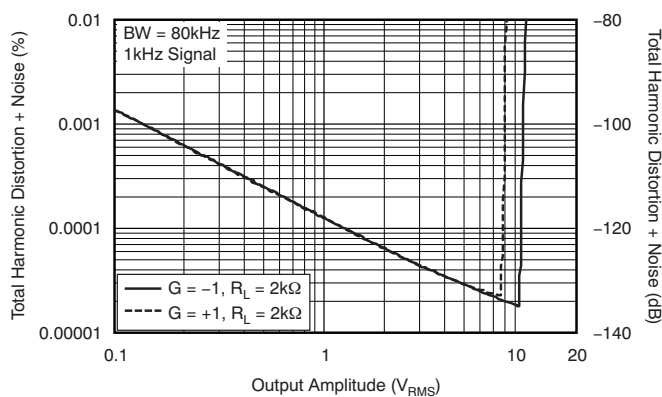
**Figure 10.**

**THD+N RATIO vs FREQUENCY**



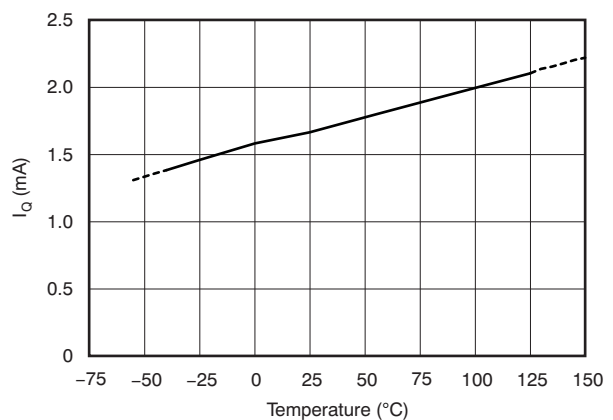
**Figure 11.**

**THD+N RATIO vs OUTPUT AMPLITUDE**



**Figure 12.**

**QUIESCENT CURRENT vs TEMPERATURE**



**Figure 13.**

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ ,  $R_L = 2\text{k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

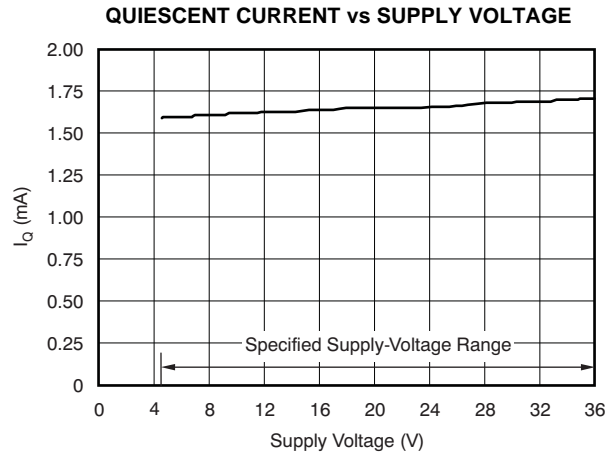


Figure 14.

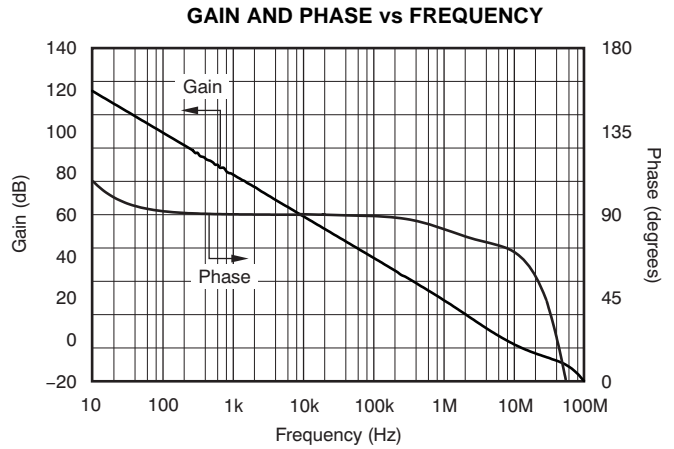


Figure 15.

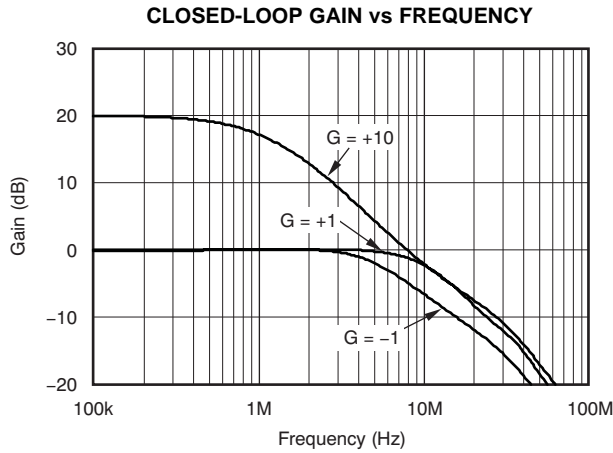


Figure 16.

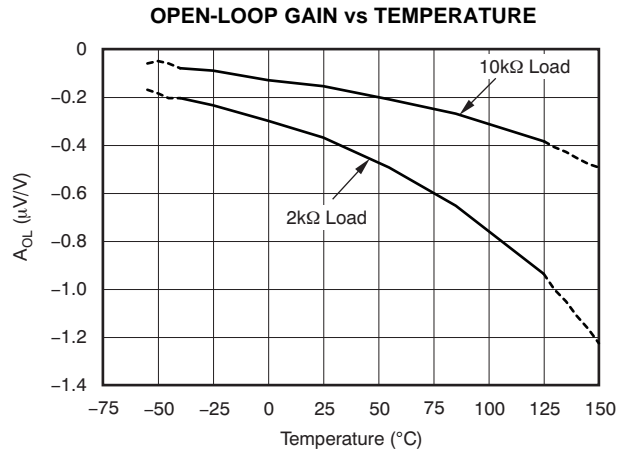


Figure 17.

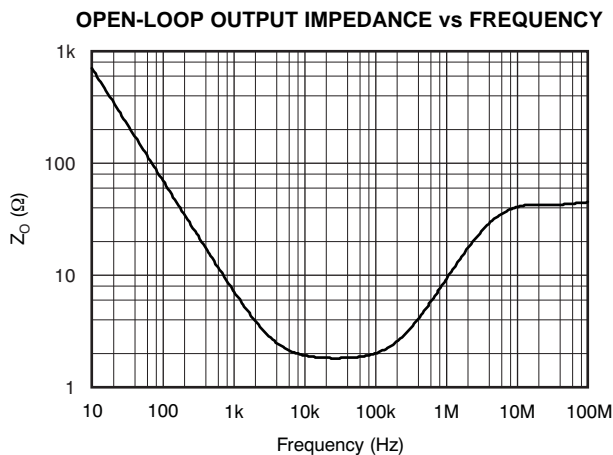


Figure 18.

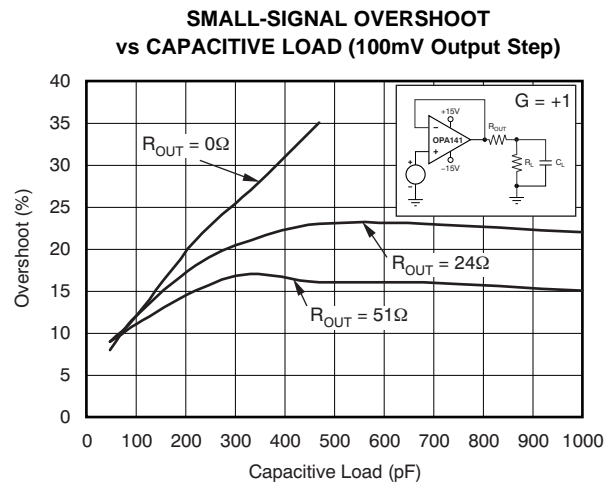


Figure 19.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ ,  $R_L = 2\text{k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

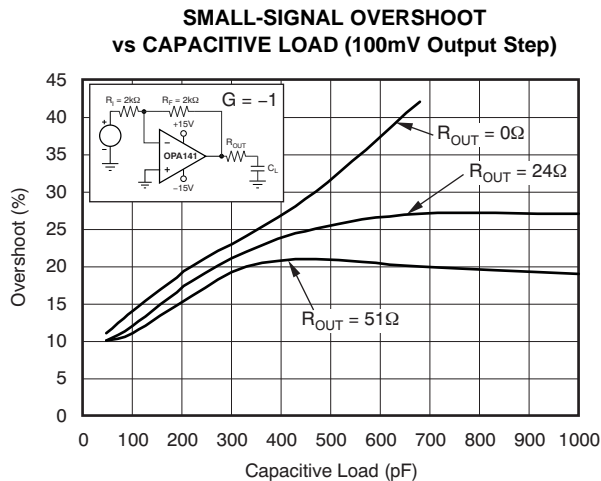


Figure 20.

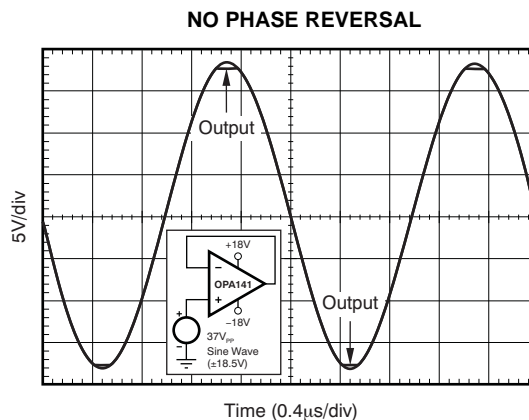


Figure 21.

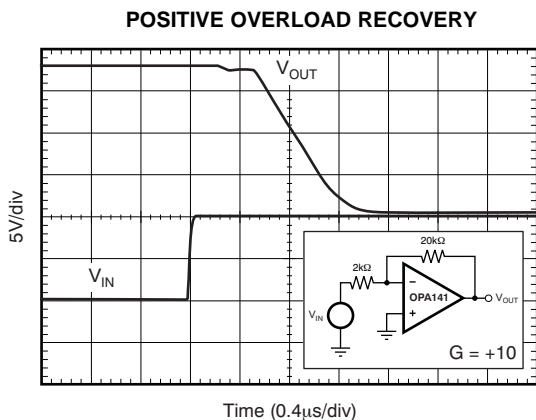


Figure 22.

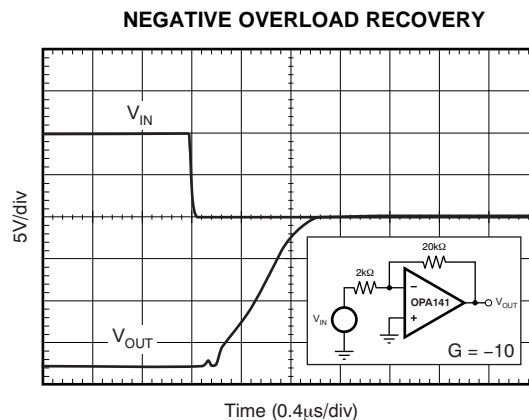


Figure 23.

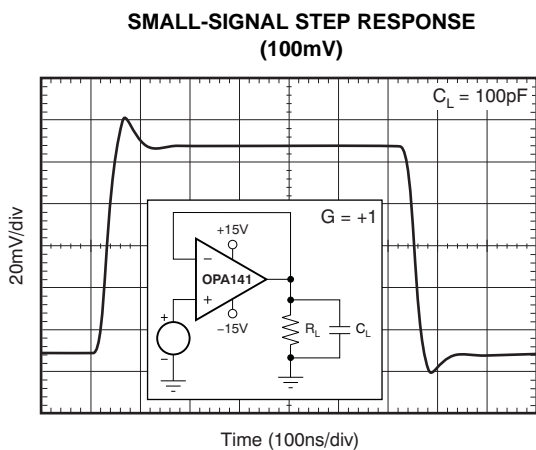


Figure 24.

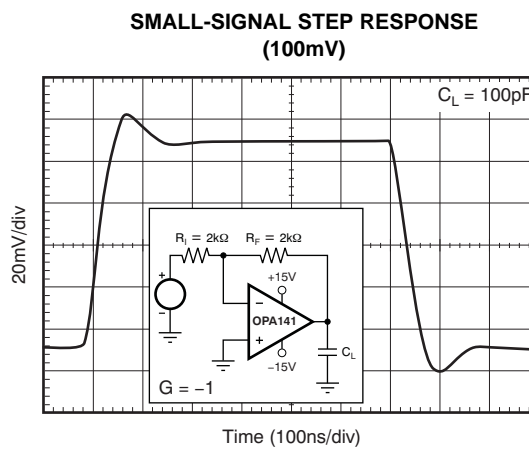


Figure 25.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ ,  $R_L = 2\text{k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

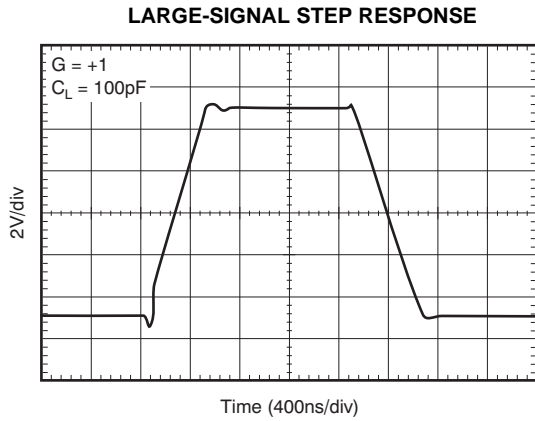


Figure 26.

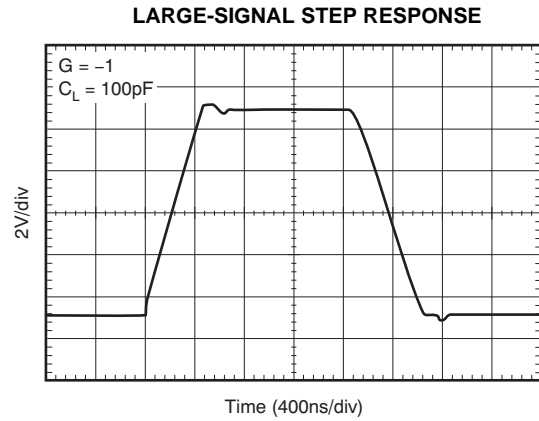


Figure 27.

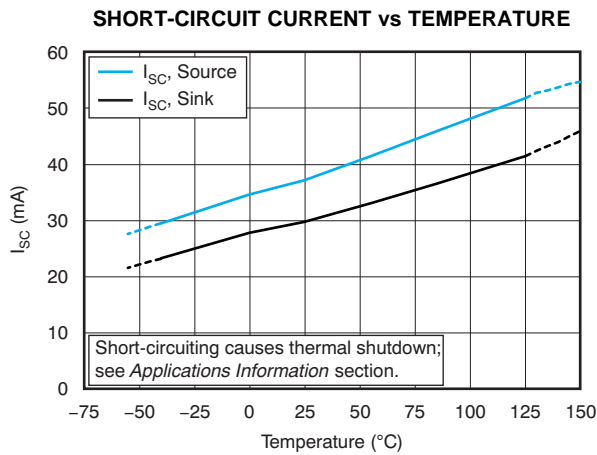


Figure 28.

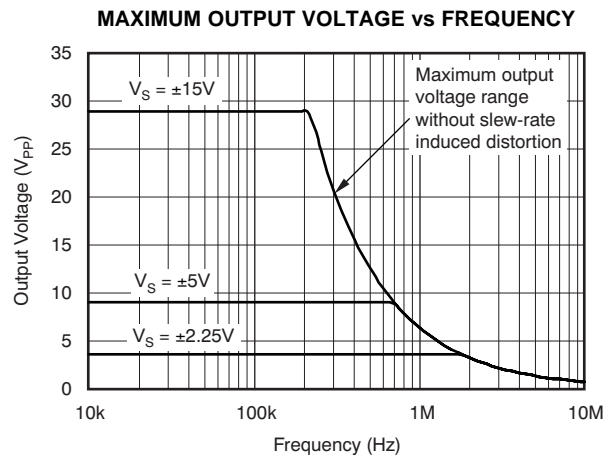


Figure 29.

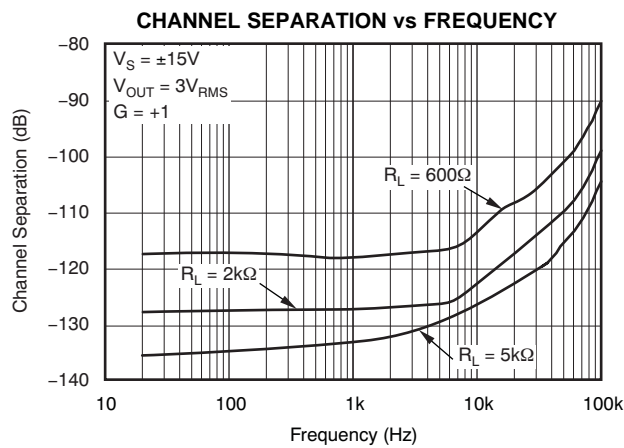


Figure 30.

## APPLICATION INFORMATION

The OPA141, OPA2141, and OPA4141 are unity-gain stable, operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1µF capacitors are adequate. [Figure 1](#) shows a simplified schematic of the OPA141.

### OPERATING VOLTAGE

The OPA141, OPA2141, and OPA4141 series of op amps can be used with single or dual supplies from an operating range of  $V_S = +4.5V (\pm 2.25V)$  and up to  $V_S = +36V (\pm 18V)$ . These devices do not require symmetrical supplies; they only require a minimum supply voltage of +4.5V ( $\pm 2.25V$ ). For  $V_S$  less than  $\pm 3.5V$ , the common-mode input range does not include midsupply. Supply voltages higher than +40V can permanently damage the device; see the [Absolute Maximum Ratings](#) table. Key parameters are specified over the operating temperature range,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Key parameters that vary over the supply voltage or temperature range are shown in the [Typical Characteristics](#) section of this data sheet.

### CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPAx141 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor ( $R_{OUT}$  equal to 50Ω, for example) in series with the output.

[Figure 19](#) and [Figure 20](#) illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of  $R_{OUT}$ . Also, refer to [Applications Bulletin AB-028](#) (literature number [SBOA015](#), available for download from the [TI web site](#)) for details of analysis techniques and application circuits.

### NOISE PERFORMANCE

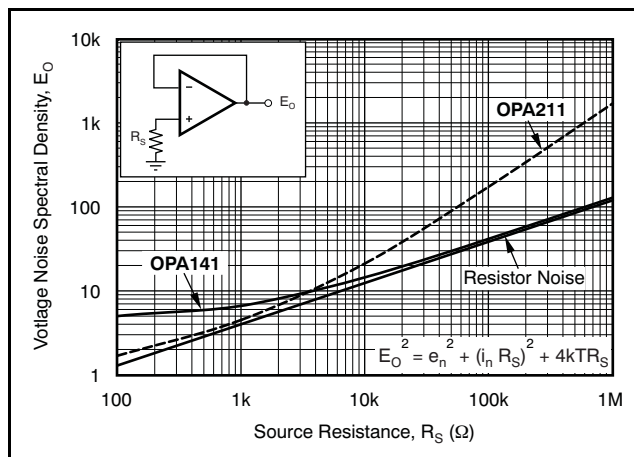
[Figure 31](#) shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA141 and OPA211 are shown

with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA141, OPA2141, and OPA4141 family has both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPAx141 series is negligible for any practical source impedance, which makes it the better choice for applications with high source impedance.

The equation in [Figure 31](#) shows the calculation of the total circuit noise, with these parameters:

- $e_n$  = voltage noise
- $I_n$  = current noise
- $R_S$  = source impedance
- $k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  J/K
- $T$  = temperature in degrees Kelvin (K)

For more details on calculating noise, see the section on [Basic Noise Calculations](#).



**Figure 31. Noise Performance of the OPA141 and OPA211 in Unity-Gain Buffer Configuration**

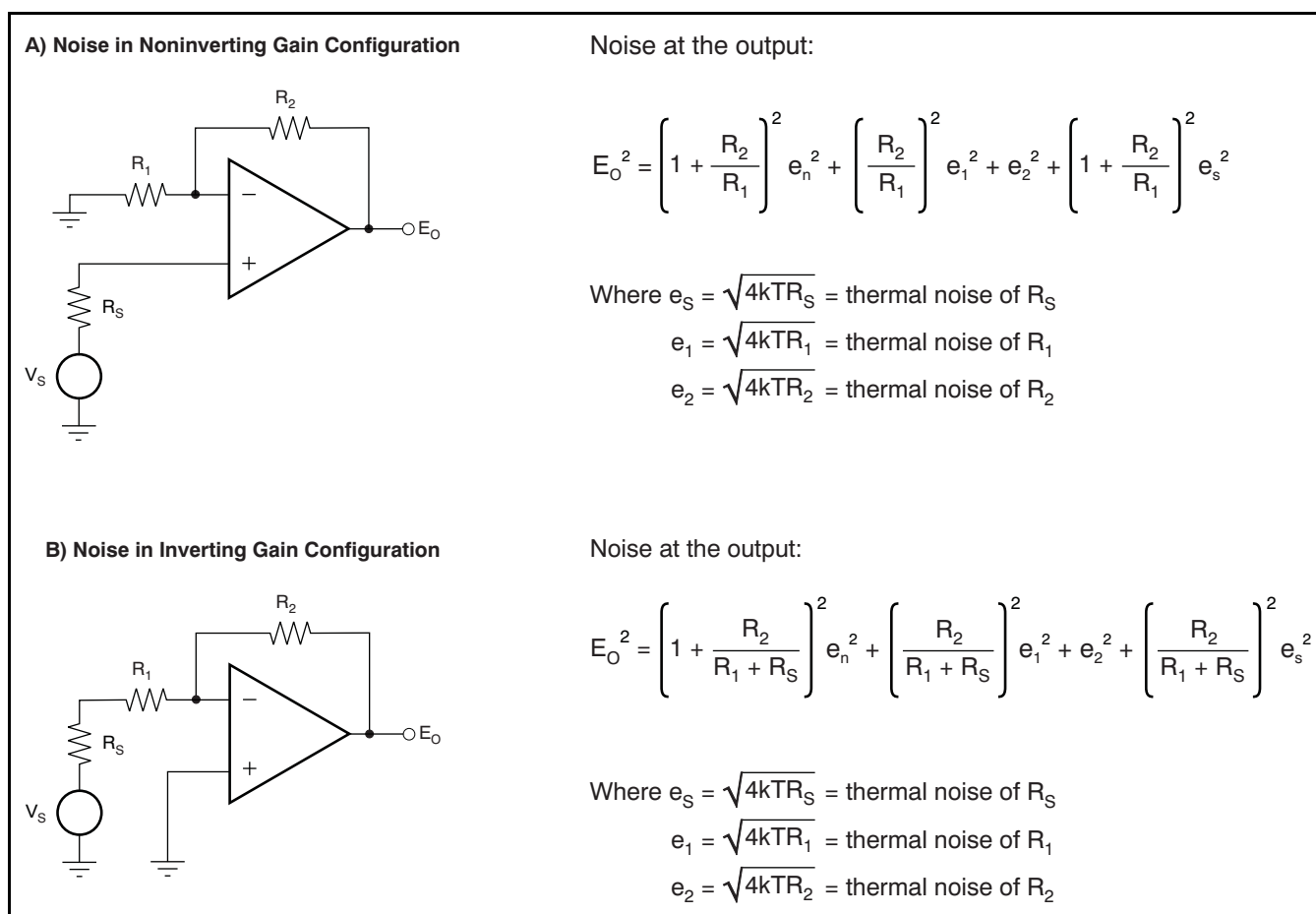
## BASIC NOISE CALCULATIONS

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 31. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 32 illustrates both noninverting (A) and inverting (B) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx141 means that its current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.



For the OPAx141 series of operational amplifiers at 1kHz,  $e_n = 6.5\text{nV}/\sqrt{\text{Hz}}$ .

**Figure 32. Noise Calculation in Gain Configurations**

## PHASE-REVERSAL PROTECTION

The OPA141, OPA2141, and OPA4141 family has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA141, OPA2141, and OPA4141 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see [Figure 21](#)).

## OUTPUT CURRENT LIMIT

The output current of the OPAx141 series is limited by internal circuitry to +36mA/–30mA (sourcing/sinking), to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature, as shown in [Figure 28](#).

## POWER DISSIPATION AND THERMAL PROTECTION

The OPAx141 series of op amps are capable of driving 2k $\Omega$  loads with power-supply voltages of up to  $\pm 18$ V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8k $\Omega$  at a supply voltage of +36V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance may be used, as long as the output current does not exceed 13mA; otherwise, the device short-circuit current protection circuit may activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA141, OPA2141, and OPA4141 series devices improves heat dissipation compared to conventional materials. Printed circuit board (PCB) layout can also help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by acting as an additional heatsink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

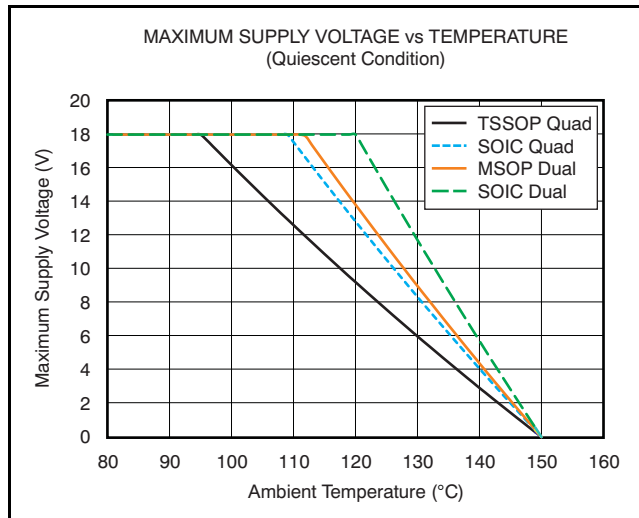
Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to mid-supply, the typical short-circuit current of 36mA leads to an internal power dissipation of over 600mW at a supply of  $\pm 18$ V.

In the case of a dual OPA2141 in an MSOP-8 package (thermal resistance  $\theta_{JA} = 180^{\circ}\text{C}/\text{W}$ ), such power dissipation would lead the die temperature to be 220 $^{\circ}\text{C}$  above ambient temperature, when both channels are shorted. This temperature increase significantly decreases the operating life of the device.

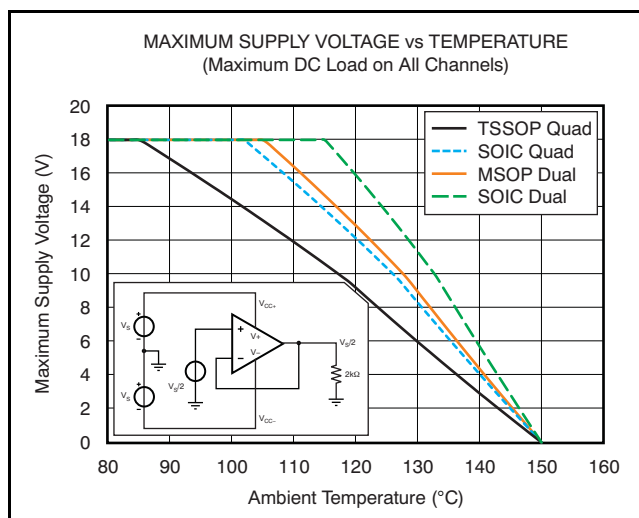
In order to prevent excessive heating, the OPAx141 series has an internal thermal shutdown circuit, which shuts down the device if the die temperature exceeds approximately +180 $^{\circ}\text{C}$ . Once this thermal shutdown circuit activates, a built-in hysteresis of 15 $^{\circ}\text{C}$  ensures that the die temperature must drop to approximately +165 $^{\circ}\text{C}$  before the device switches on again.

Additional consideration should be given to the combination of maximum operating voltage, maximum operating temperature, load, and package type. [Figure 33](#) and [Figure 34](#) show several practical considerations when evaluating the OPA2141 (dual version) and the OPA4141 (quad version).

As an example, the OPA4141 has a maximum total quiescent current of 12.4mA (3.1mA/channel) over temperature. The TSSOP-14 package has a typical thermal resistance of 135 $^{\circ}\text{C}/\text{W}$ . This parameter means that because the junction temperature should not exceed 150 $^{\circ}\text{C}$  in order to ensure reliable operation, either the supply voltage must be reduced, or the ambient temperature should remain low enough so that the junction temperature does not exceed 150 $^{\circ}\text{C}$ . This condition is illustrated in [Figure 33](#) for various package types. Moreover, resistive loading of the output causes additional power dissipation and thus self-heating, which also must be considered when establishing the maximum supply voltage or operating temperature. To this end, [Figure 34](#) shows the maximum supply voltage versus temperature for a worst-case dc load resistance of 2k $\Omega$ .



**Figure 33. Maximum Supply Voltage vs Temperature (OPA2141 and OPA4141), Quiescent Condition**



**Figure 34. Maximum Supply Voltage vs Temperature (OPA2141 and OPA4141), Maximum DC Load**

## ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin

functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See Figure 35 for an illustration of the ESD circuits contained in the OPAx141 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx141 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one Figure 35 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 35 depicts a specific example where the input voltage,  $V_{IN}$ , exceeds the positive supply voltage ( $+V_S$ ) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $+V_S$  can sink the current, one of the upper input steering diodes conducts and directs current to  $+V_S$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

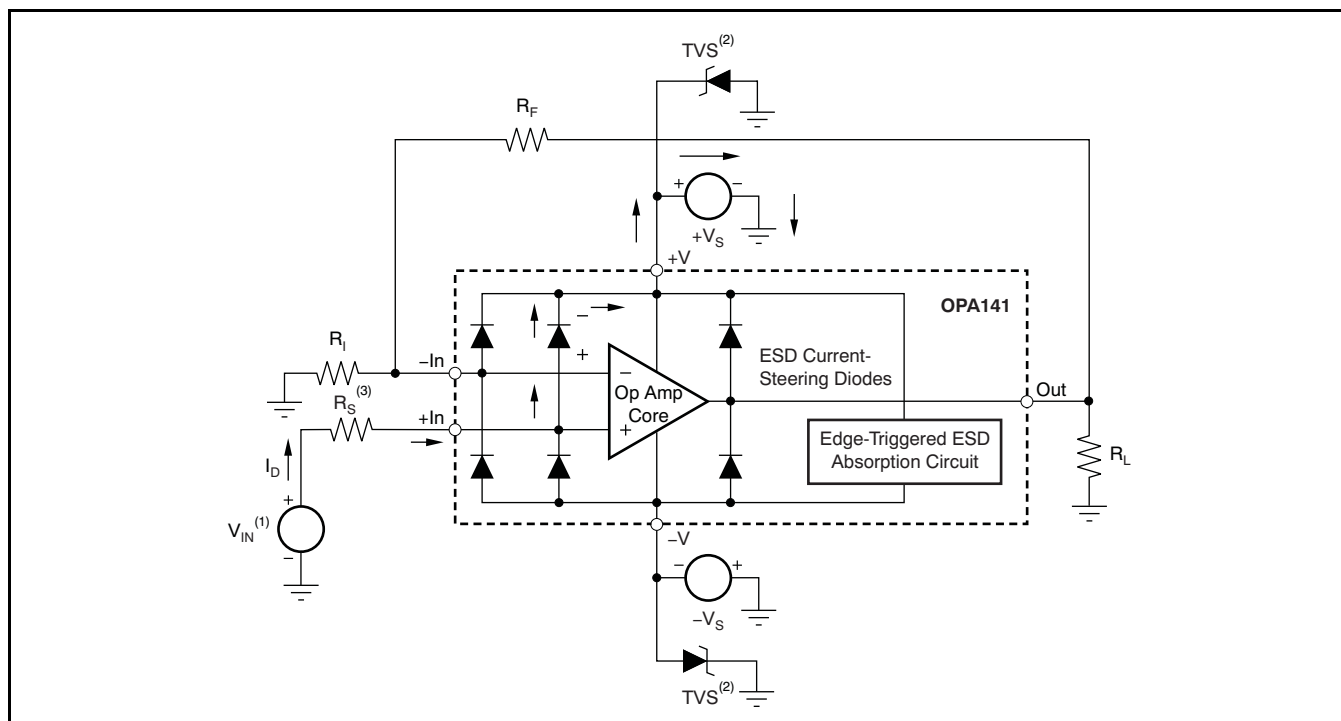
If the supply is not capable of sinking the current,  $V_{IN}$  may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies  $+V_S$  and/or  $-V_S$  are at 0V.

Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins as shown in Figure 35. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



- (1)  $V_{IN} = +V_S + 500\text{mV}$ .
- (2) TVS:  $+V_{S(\text{max})} > V_{\text{TVSBR}(\text{Min})} > +V_S$
- (3) Suggested value approximately 1k $\Omega$ .

Figure 35. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA141AID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O141A
OPA141AID.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O141A
<a href="#">OPA141AIDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	Call TI   Nipdauag   Nipdau	Level-2-260C-1 YEAR	-40 to 125	141
OPA141AIDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	141
OPA141AIDGKRG4	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	141
OPA141AIDGKRG4.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	141
<a href="#">OPA141AIDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	Call TI   Nipdauag   Nipdau	Level-2-260C-1 YEAR	-40 to 125	141
OPA141AIDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	141
<a href="#">OPA141AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O141A
OPA141AIDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O141A
OPA141AIDRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O141A
OPA141AIDRG4.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O141A
<a href="#">OPA2141AID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2141A
OPA2141AID.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2141A
<a href="#">OPA2141AIDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	Call TI   Nipdauag   Nipdau	Level-2-260C-1 YEAR	-40 to 125	2141
OPA2141AIDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2141
OPA2141AIDGKRG4	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2141
OPA2141AIDGKRG4.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2141
<a href="#">OPA2141AIDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	Call TI   Nipdauag   Nipdau	Level-2-260C-1 YEAR	-40 to 125	2141
OPA2141AIDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2141
<a href="#">OPA2141AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2141A
OPA2141AIDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2141A
<a href="#">OPA4141AID</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
OPA4141AID.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
OPA4141AIDG4	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
OPA4141AIDG4.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA4141AIDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
OPA4141AIDR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
<a href="#">OPA4141AIPW</a>	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
OPA4141AIPW.B	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
OPA4141AIPWG4	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
OPA4141AIPWG4.B	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
<a href="#">OPA4141AIPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A
OPA4141AIPWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA141AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA141AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA141AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA141AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA141AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2141AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2141AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2141AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2141AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4141AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4141AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

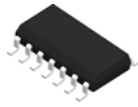

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA141AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA141AIDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA141AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA141AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA141AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA2141AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2141AIDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2141AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA2141AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA4141AIDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA4141AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA141AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA141AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2141AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2141AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4141AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4141AID.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4141AIDG4	D	SOIC	14	50	506.6	8	3940	4.32
OPA4141AIDG4.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4141AIPW	PW	TSSOP	14	90	508	8.5	3250	2.8
OPA4141AIPW.B	PW	TSSOP	14	90	508	8.5	3250	2.8
OPA4141AIPWG4	PW	TSSOP	14	90	508	8.5	3250	2.8
OPA4141AIPWG4.B	PW	TSSOP	14	90	508	8.5	3250	2.8



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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